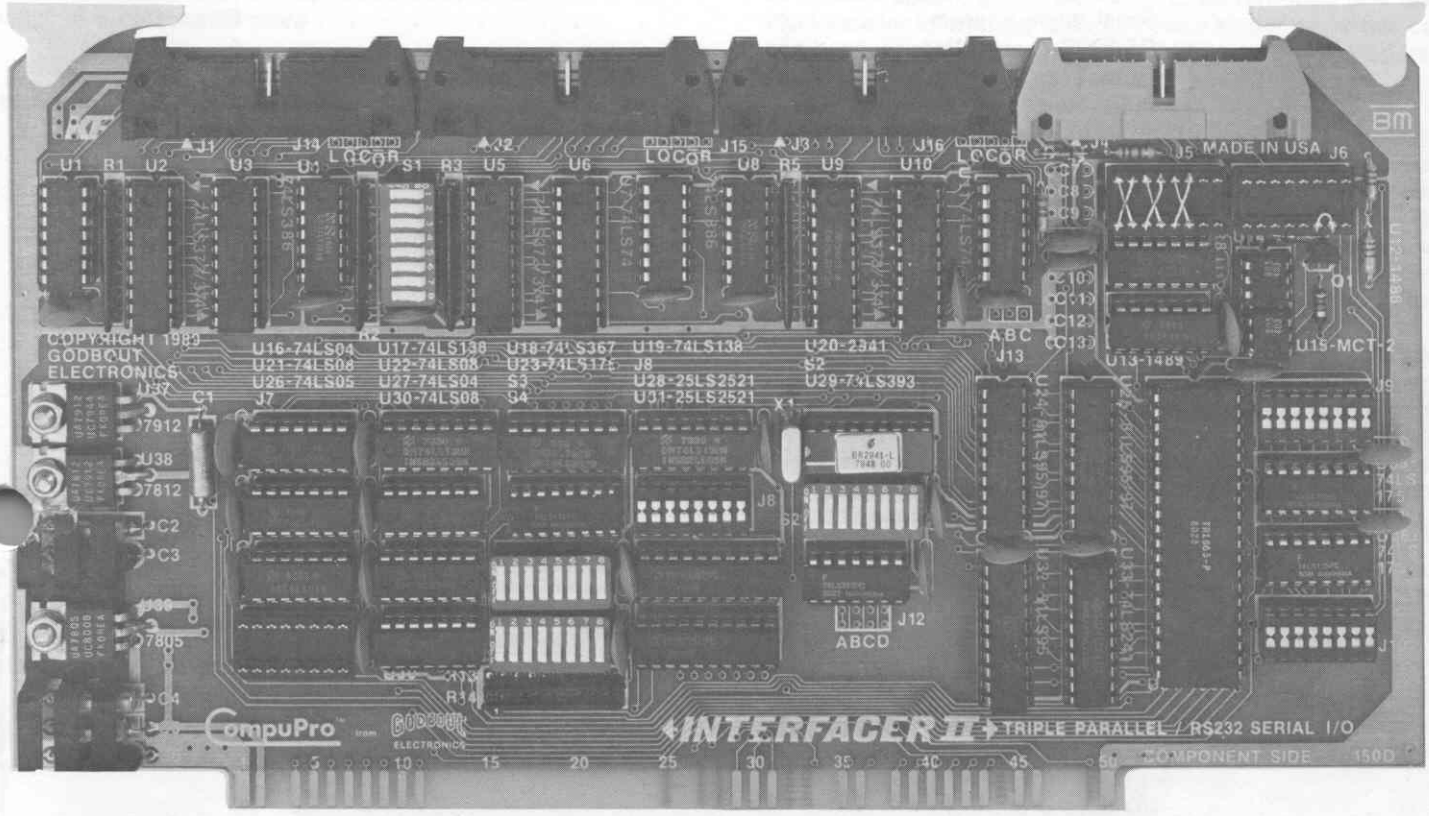
INTERFACER II T.M.

USER'S MANUAL



3 Parallal & 1 Serial I/O • S-100

RS232 • with full handshake

150D mac

CompuPro™ from GODBOUT

1/81

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ABOUT THE INTERFACER II

Congratulations on your decision to purchase the ERFACER II, a triple parallel/ single channel RS-232 serial board designed specifically for full electrical and mechanical compatibility with the IEEE 696/S100 standard. The S-100 bus is the professional level choice for commercial, industrial and scientific applications. We believe that this board with the rest of the S-100 portion of the CompuPro family, is one of the best boards available for that bus.

Features, such as full RS232 handshaking, crystal controlled baud rate generator, a reliable hardware UART, three full duplex parallel I/O ports with handshaking and interrupts and a selectable rate interrupt clock allow for maximum flexibility at a reasonable price.

Thank you for choosing a CompuPro product....welcome to the club.

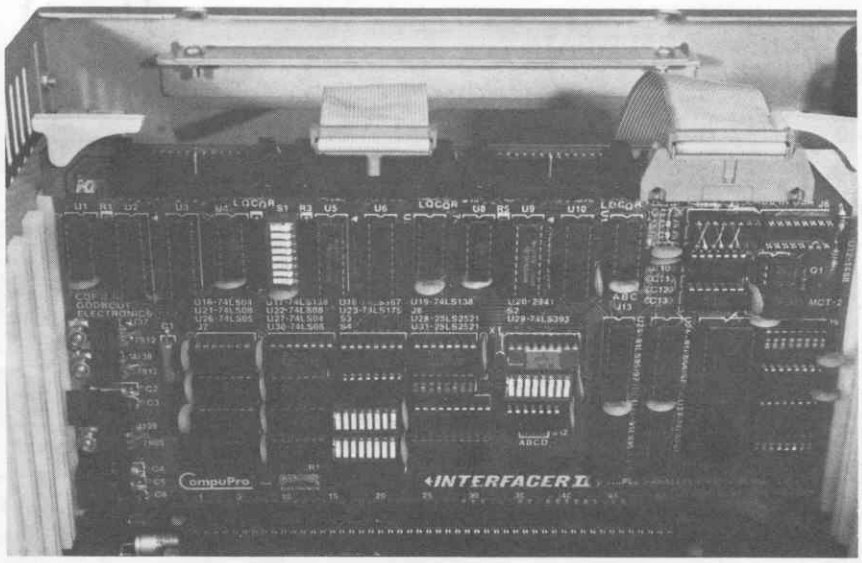
TECHNICAL OVERVIEW

The serial section of Interfacer II incorporates a reliable LSI technology UART chip to perform the basic serial-to-parallel and parallel-to-serial conversions necessary for serial communication. By using the UART, the CPU is freed of the time consuming drudgery of performing serial I/O operations by software techniques. Because of this, I/O operations are far more reliable and easier to implement.

In addition to the UART, several other features are included to make this board extremely flexible and easy to use. These features include an on board crystal controlled baud rate generator for reliable Baud rates independent of your CPU clock speed, conversion to TTL, current loop and RS-232 levels for interfacing to almost every kind of serial device, and hardware/software programmability for power-on operation and easy parameter modification.

The parallel section of the INTERFACER II consists of three full duplex latched parallel ports for I/O data and one port for status and interrupt control. The use of TTL latches rather than a MOS parallel interface chip negates the need for mode selection and initialization, and allows each port to have strobe, attention and enable bits, an input interrupt, and 16 true data lines for a three port total of 48 true data lines.

Other features standard to all CompuPro boards include thorough bypassing of all supply lines to suppress transients, on board regulators, and low power Schottky TTL and MOS technology integrated circuits for reliably cool operation. All this and sockets for all ICs go onto a double-sided, solder masked printed circuit board with a complete component layout legend.



Shown above is a typical installation using (2) optional Interfacer cable assemblies. These cables consist of an Ansley 609-25S 25-pin 'D' connector and an Ansley 609-2601M 26-pin female transistion connector.

Individual cable parts or assembled cables in 18 and 30 inch lengths are available from Godbout Electronics.

I/O ADDRESS ASSIGNMENT

The serial Channel on this board is addressable as a single 2 port block anywhere through the 256 port I/O space. In addition, this Channel can be disabled and electrically removed from the I/O space. DIP switch S3 addresses the two port block. The Channel will have the data port residing at the port address, and the status port residing at the port address + 1. The Channel is addressed as follows:

SWITCH POSITION	FUNCTION	
1	ADDRESS A1	
2	ADDRESS A2	
3	ADDRESS A3	'ON' = '0'
4	ADDRESS A4	
5	ADDRESS A5	'OFF' = '1'
6	ADDRESS A6	
7	ADDRESS A7	
8	CHANNEL DIS.	'ON' = DISABLED 'OFF'= ENABLED

EXAMPLE: To address the serial channel at the first I/O port address pair 00H and 01H, positions 1 through 7 of switch S3 would be ON and position 8 would be OFF so that the Channel is enabled. This configuration places the data port at 00H (even address) and the status port at 01H (odd address).

BAUD RATE SELECTION

Dip switch S2 is used to select the Baud rate for the serial Channel. Switch positions 1 - 4 set the Baud rate for both the receiver and transmitter sections of the serial Channel as shown below.

ON = '0'
OFF = '1'

SWITCH POSITION 1 2 3 4	BAUD RATE
0 0 0 0	50 BAUD
1 0 0 0	75 BAUD
0 1 0 0	110 BAUD
1 1 0 0	134.5 BAUD
0 0 1 0	150 BAUD
1 0 1 0	300 BAUD
0 1 1 0	600 BAUD
1 1 1 0	1200 BAUD
0 0 0 1	1800 BAUD
1 0 0 1	2000 BAUD
0 1 0 1	2400 BAUD
1 1 0 1	3600 BAUD
0 0 1 1	4800 BAUD
1 0 1 1	7200 BAUD
0 1 1 1	9600 BAUD
1 1 1 1	19200 BAUD

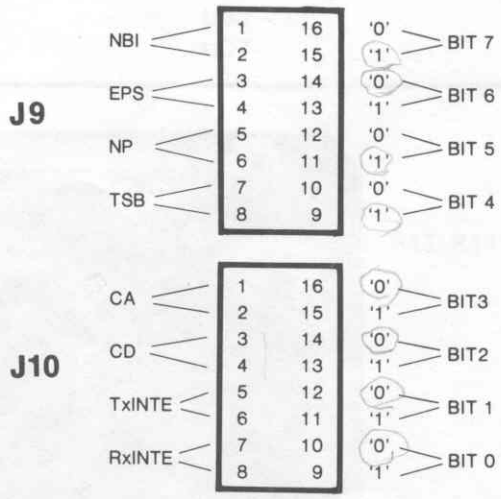
EXAMPLE: To set the serial Channel to 9600 baud, DIP switch S2 would have position 1 ON and positions 2, 3, and 4 would be OFF. To set the serial Channel to 110 baud, DIP switch S2 would have positions 1, 3, and 4 ON and position 2 would be OFF.

UART PROGRAMMING

On power-up the control latches are all reset to a defi state as shown below. If the UART parameters for your system configuration are set properly for the reset state, no software initialization is necessary for proper operation of this board. To set the power-up parameters, the proper logic level for the programming header should be chosen from the table and the corresponding header trace should be left intact while the trace with the opposite level should be cut (an X-ACTO knife works great). For example, if odd parity is desired, the table shows that EPS should be a logic '0' and the header diagram indicates that the trace between pins 3 and 14 should remain while the trace between pins 4 and 13 should be cut.*NOTE: never leave both traces to a signal line unbroken as this could lead to heating and possible damage to the 74LS175's.*

The state of this board may be altered at any time by outputting a new control word to the Control Port. To change the mask under software control, simply output a '1' to the proper data bit of the Control Port corresponding to the signal that you desire to change. This will flip the logic level of the particular signal to the opposite state (i.e. odd parity will become even parity). Outputting a '0' to a bit will return it to the power-up setting.

UART PROGRAMMING



SIGNAL	'0'	'1'
EPS	ODD PARITY	EVEN PARITY
NBI	7 BITS	8 BITS
TSB	1 STOP BIT	2 STOP BITS
NP	PARITY	NO PARITY
TxINT E	DISABLED	ENABLED
RxINT E	DISABLED	ENABLED
CA	"SPACING"	"MARKING"
CD	"SPACING"	"MARKING"

VECTORED INTERRUPTS

When enabled and jumpered to the appropriate interrupt pin on the S-100 bus, the serial Channel has both a transmit and receive interrupt line. The receive interrupt line (RxINT) is driven low when data is available from the UART and the RXINTE line has been enabled as described in the UART PROGRAMMING section. This line resets to a high impedance state after the data has been fetched from the UART. The transmit interrupt line (TxINT) is driven low when the UART is ready to accept a character from the CPU and the TXINTE line has been enabled as described in the UART PROGRAMMING section. This line resets to a high impedance state when the UART transmitter buffer is full and it cannot accept another character. Note that 'sINTA', S-100 bus pin 96, is not monitored by this board and is not needed to implement a useful interrupt scheme.

	S-100 BUS	PINS	J7			
VI0	4	—	1	16	—	INT J1
VI1	5	—	2	15	—	INT J2
VI2	6	—	3	14	—	INT J3
VI3	7	—	4	13	—	NC
VI4	8	—	5	12	—	TMRI
VI5	9	—	6	11	—	NC
VI6	10	—	7	10	—	RxINT
VI7	11	—	8	9	—	TxINT

To enable an interrupt which is initially disabled or disable an interrupt that is initially enabled by the UART programming dip shunt (see UART Programming), a logical '1' should be output to the Interrupt Enable Bit of the Control Port.

STATUS PORT BIT ASSIGNMENT

Inputs from the status port to the CPU are defined as follows:

DATA BIT	NAME	SIGNAL
D0	TBMT	Transmitter buffer empty
D1	DAV	Data available
D2	OPT	Optional status line
D3	PE	Parity error
D4	OR	Over run
D5	FE	Framing error
D6	CC	RS232 CC input
D7	CB	RS232 CB input

CONTROL PORT BIT ASSIGNMENT

Outputs to the control port from the CPU are defined as follows:

DATA BIT	NAME	SIGNAL
D0	RxINT E	Receiver interrupt enable
D1	TxINT E	Transmitter interrupt enable
D2	CD	RS232 CD output
D3	CA	RS232 CA output
D4	TSB	Number of stop bits
D5	NP	No parity
D6	EPS	Even parity select
D7	NBI	Number of bits/character

SERIAL MODE JUMPERS

The INTERFACER II board with its unique serial programming jumpers, allows the user to adapt his board to all standard RS-232 pin configurations and to non-standard current loop configurations. In current loop mode, this board may be set to use the on board current source or an external current source. For example, a teletype requires that the on board current source be used, so the serial mode jumpers (J5 and J6) should be set like the example shown on the following page. In RS-232 mode, these jumpers may be set so that this board operates in a 'master' mode where it behaves as the Data Terminal Equipment (DTE), or it may be set so that the board operates in a 'slave' mode where it behaves as the Data Communication Equipment (DCE). Since almost all CRT terminals and serial interface printers operate as the 'master' or as the Data Terminal Equipment, then the INTERFACER II board must operate as the 'slave' or Data Communication Equipment. For example, to connect the INTERFACER II to a terminal like an ADM 3A or a Hazeltine, the serial mode jumpers (J5 and J6) should be set in 'slave' mode as shown on the following page. To connect the INTERFACER II to a modem is a different set-up because modems are set to operate as 'slaves'. When connected to a Modem, the INTERFACER II should be set in the 'master' mode as shown on the following page.

RS-232C CONTROL LINES

The RS-232 control and data lines are defined as shown below.

PIN#	CIRCUIT	DIR.	DESCRIPTION
1	AA		PROTECTIVE GROUND
2	BA	TO DCE	TRANSMITTED DATA
3	BB	TO DTE	RECEIVED DATA
4	CA	TO DCE	REQUEST TO SEND
5	CB	TO DTE	CLEAR TO SEND
6	CC	TO DTE	DATA SET READY
7	AB		SIGNAL GROUND
8	CF	TO DTE	REC'D LINE SIGNAL DET.
20	CD	TO DCE	DATA TERMINAL READY

Four hardwired RS-232 handshaking signals are provided for interfacing to equipment needing these lines as shown below. These lines may be set to power-up either marking or spacing, and their state may be altered by software commands as described in the UART PROGRAMMING Section.

OUTPUT LINES

DATA BIT	RS-232 LINE	DB25 PIN CONNECTION
D2	CD	20 OR 6 *
D3	CA	4 OR 5 *

INPUT LINES

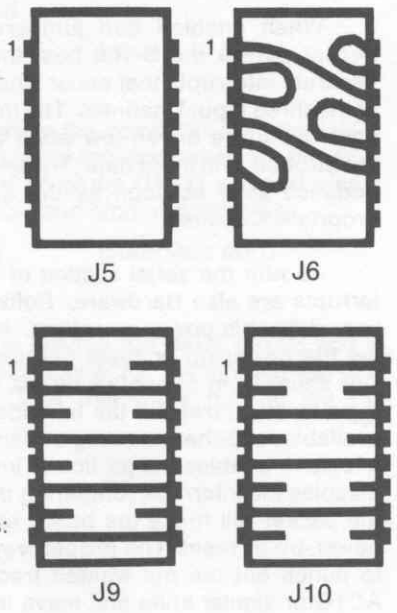
DATA BIT	RS-232 LINE	DB25 PIN CONNECTION
D2(OPT.)	CF	8*
D6	CC	6 OR 20 *
D7	CB	5 OR 4 *

NOTE: Non-starred pin numbers indicate the DB25 pin number when the Serial Mode Jumpers are set for 'master' mode. The starred pin numbers indicate the DB25 pin number when the Serial Mode Jumpers are set for 'slave' mode.

One optional input line (CF or Rec'd Line Signal Detect) is provided at locations J13. If point 'B' is jumpered to point 'A', this line will appear on Status Bit D2. By jumpering point 'B' to point 'C', the 'End of Character' output (EOC) from the UART will appear on Status Bit D2.

TYPICAL PROGRAMMING JUMPERS

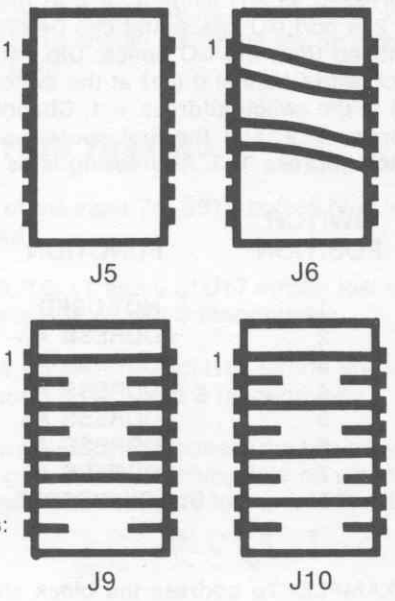
Current loop - on board current sources EXAMPLE: TTY



This configuration yields:

Even parity
8 data bits
2 stop bits
No parity
Interrupts disabled

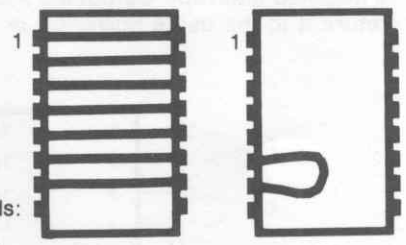
Current loop - external current sources



This configuration yields:

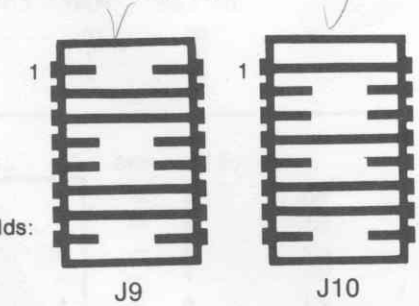
Odd parity
7 data bits
1 stop bit
No parity
Interrupts disabled

RS - 232C - Master mode EXAMPLE: Modem



This configuration yields:

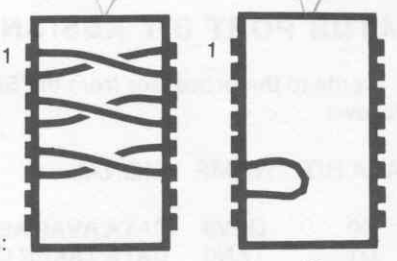
CA "spacing" on pin 4
CD "marking" on pin 20
BA (Tx data) on pin 2
BB (Rx data) on pin 3
CB Status to I/O board on pin 5
CC Status to I/O board on pin 6
CF (Received line signal detector on pin 8)



This configuration yields:

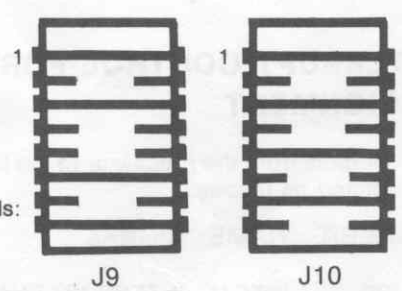
Odd parity
8 data bits
1 stop bit
No parity
Tx Inte enabled
Rx Inte disabled

RS - 232C - Slave mode EXAMPLE: CRT Terminal, printer



This configuration yields:

CA "spacing" on pin 5
CD "spacing" on pin 6
BA (Tx data) on pin 3
BB (Rx data) on pin 2
CB Status to I/O board on pin 4
CC Status to I/O board on pin 20



This configuration yields:

Odd parity
7 data bits
2 stop bit
No parity
Interrupts disabled

I/O ADDRESS ASSIGNMENT

The parallel Channels on the INTERFACER II board are addressed as any single four port block anywhere through the 256 port I/O space and can be disabled and electrically removed from the I/O space. Dip switch S4 addresses the block with Channel 0 (J1) at the switch address, Channel 1 (J2) at the switch address + 1, Channel 2 (J3) at the switch address + 2, and the Status/Interrupt Control Port at the switch address + 3. Addressing is as shown below.

SWITCH POSITION	FUNCTION	
1	NOT USED	
2	ADDRESS A2	
3	ADDRESS A3	ON = "0"
4	ADDRESS A4	OFF = "1"
5	ADDRESS A5	
6	ADDRESS A6	
7	ADDRESS A7	
8	BLOCK DISABLE -	ON = DISABLED
		OFF = ENABLED

SET to 32-35

EXAMPLE: To address the block starting at C8H, switch positions 3,6,7 & 8 would be OFF and 2,4 & 5 would be ON. In this configuration, Channel 0 (J1) would be at port C8H, Channel 1 (J2) would be at port C9H, Channel 2 (J3) would be at CAH, and the Status/Interrupt Control Port would be at CBH.

STATUS PORT BIT ASSIGNMENT

Inputs to the processor from the Status Port are defined as follows:

DATA BIT	NAME	SIGNAL
D0	DAV0	DATA AVAILABLE CHANNEL 0
D1	TKN0	DATA TAKEN CHANNEL 0
D2	DAV1	DATA AVAILABLE CHANNEL 1
D3	TKN1	DATA TAKEN CHANNEL 1
D4	DAV2	DATA AVAILABLE CHANNEL 2
D5	TKN2	DATA TAKEN CHANNEL 2
D6	NOT USED	
D7	NOT USED	

INTERRUPT CONTROL PORT BIT ASSIGNMENT

Outputs from the processor to the Interrupt Control Port are defined as follows:

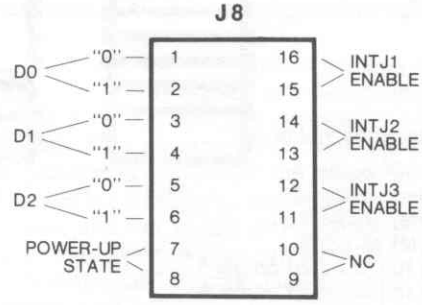
DATA BIT	NAME	SIGNAL
D0	INTEJ1	INTERRUPT ENABLE CHANNEL 0
D1	INTEJ2	INTERRUPT ENABLE CHANNEL 1
D2	INTEJ3	INTERRUPT ENABLE CHANNEL 2
D3	TMRIE	TIMER INTERRUPT ENABLE
D4-D7	NOT USED	

PARALLEL VECTORED INTERRUPTS

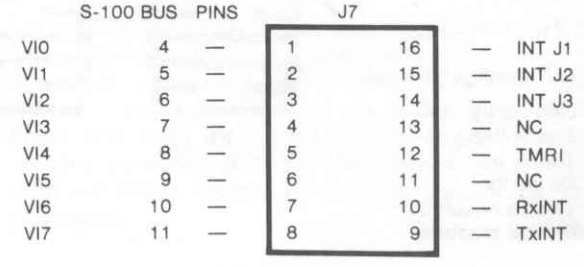
When enabled and jumpered to the appropriate interrupt pin on the S-100 bus, the parallel block has three separate interrupts that occur when data is strobed into each of the three input Channels. The interrupt lines, INTJ1, INTJ2, and INTJ3, are driven low when J1, J2, and J3 respectively are strobed with input data. These lines are reset to a high impedance state as soon as the data is taken from the appropriate Channel.

As with the serial section of this board, the parallel interrupts are also Hardware/ Software programmable with a user definable power on setting. Jumper socket J8 is used to set the power-up or reset parameters by programming the DIP shunt from the figure below. On power-up or reset, the logic levels shown on the left side of the jumper socket are available for either enabling or disabling the interrupts. Since a logic '1' enables the particular input interrupt and a logic '0' disables the interrupt, jumpering the appropriate level across the socket will make the board assume a known state after power-up or reset. The proper way to program this setting is to punch out the not wanted trace of the shunt with an X-ACTO or similar knife and leave the trace intact that has the proper level.

To alter the programmed setting under software control, the user should output a logic '1' to the proper bit of the Interrupt/ Control Port shown in the figure or the bit assignment table. This will disable an enabled interrupt and enable a disabled interrupt. Outputting a logic '0' to the same bit will return it to the users power-up or reset configuration.



DATA BIT	PORT	CONNECTOR
D0	0	J1
D1	1	J2
D2	2	J3



INPUT STROBE LINE

The strobe line on each input Channel is used to latch data from an external device into the input register when a 74LS374 or 74LS373 latch is used. This line also sets the status flag (DAVx) so that the processor can tell if data has been entered.

If a 74LS374 is used as the input register, a transition on the strobe line latches the data and sets the status flag (DAVx). The strobe polarity select switch should be set as described below so that the peripheral's data is valid during the strobe's transition. With the select switch (S1-2, S1-4, and S1-6) ON, a low to high transition on strobe will latch the data. With the select switch OFF, a high to low transition on strobe will latch the data.

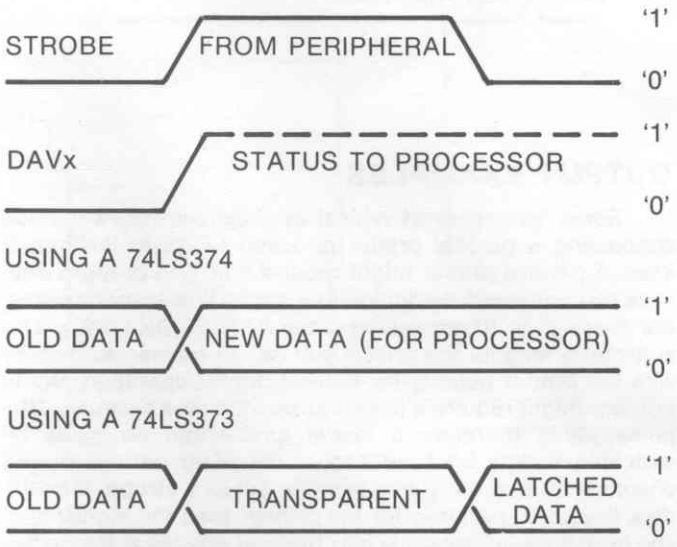
If a 74LS373 is used as the input register, the strobe line can assume two different modes. The first mode is similar to the latched mode of the 74LS374 described above except that during the strobe pulse the data is transparent through latch to the processor. At the end of the strobe pulse, the data will be latched and stable for the processor to access. With the strobe select switch (S1-2, S1-4, and S1-6) ON, a positive going strobe pulse will latch the data at the end of the pulse. With the select switch OFF, a negative going strobe pulse will latch the data at the end of the pulse. The second mode is the fully transparent mode where the data is never latched but is available for inputting at any time by the processor. This mode is useful whenever the data has no strobe bit associated with it. This mode is entered when the strobe line is left open with the strobe select switch ON. See the timing diagrams below for a visual representation of the input data and the strobe relationships.

NOTE: In the diagrams below, the strobe is provided by the external device and the incoming data is shown as what is available to the processor in relation to the strobe pulse.

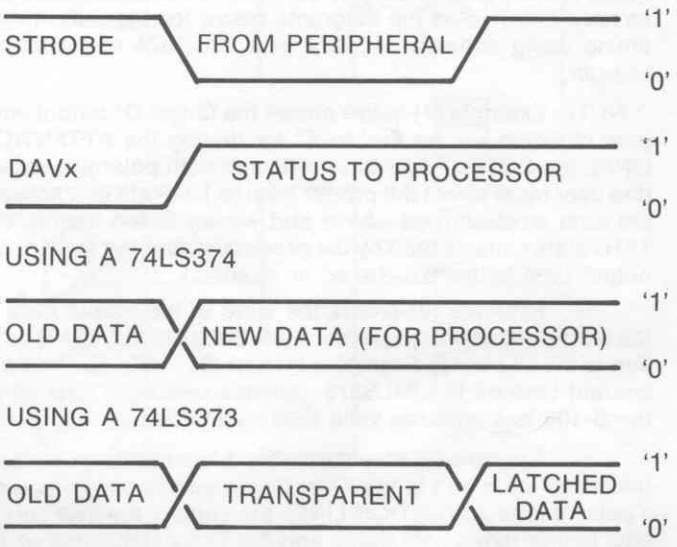
INPUT EXAMPLES

Some examples of typical applications might include connecting a ASCII keyboard or a set of sense switches to one of the input Channels of the INTERFACER II. A keyboard usually has a strobe line to indicate that it has current valid data on its data outputs therefore, using one of the 74LS374 latches would be best. The keyboard data lines would be connected accordingly to input data lines of the parallel Channel and the keyboard strobe line would be connected to the Channel STROBE input. The Strobe Select switch would be ON for a positive keyboard strobe, and OFF for a negative keyboard strobe. If connecting some sense switches to the input lines, a 74LS373 would be the best choice because there are usually no strobe lines associated with switches. The switches should be connected to the input lines so that they ground the inputs (no pullup resistors are needed since they are supplied on the board) and the STROBE LINE should be left floating with the Strobe Select switch ON. This allows the processor to input the data from the switches at any time. Another example of an input signal that usually does not have a strobe associated with it would be the Busy line and other status bits from a printer or other device.

WITH THE STROBE SELECT SWITCH 'ON':



WITH THE STROBE SELECT SWITCH 'OFF':



OUTPUT ENABLE LINE

The OUTPUT ENABLE LINE on each Channel is used to Tri-State the output register and enable the Q and Q* output flags as described below. By Tri-Stating the output register, the user may bus the output data from several different sources onto the same 8 data lines. In this mode, the TKNx status bit will stay high until the ouput register goes active, at which point the TKNx status bit will go low. If the output register is active at all times, (most applications will be this way) the TKNx status bit will stay low at all times.

When the Polarity Select Switch (S1-3, S1-5, and S1-7) is ON, the OUTPUT ENABLE LINE must be low to enable the output register. With the Select Switch OFF, the OUTPUT ENABLE LINE must be high or left open to enable the output register.

ATTENTION LINE

The ATTENTION LINE is used to inform an external device that new data is now available for it. This line may be jumpered (J14, J15, and J16) to provide any one of four different outputs. With the Common jumpered to either Q or Q*, and the OUTPUT ENABLE LINE set so that the output of the register is Tri-Stated, then the ATTENTION LINE will go high (Q) or low (Q*) when data is strobed into the output register and the TKNx status bit will go high. When the OUTPUT ENABLE LINE level is changed to enable the data, then the ATTENTION LINE will return to its original level and the TKNx status bit will go low. In this mode, the OUTPUT ENABLE LINE is used to transfer the data out of the register and reset the attention flag. Since the level of the ATTENTION LINE may be sampled by the processor through the status port (TKNx), a high speed handshaking data transfer can occur.

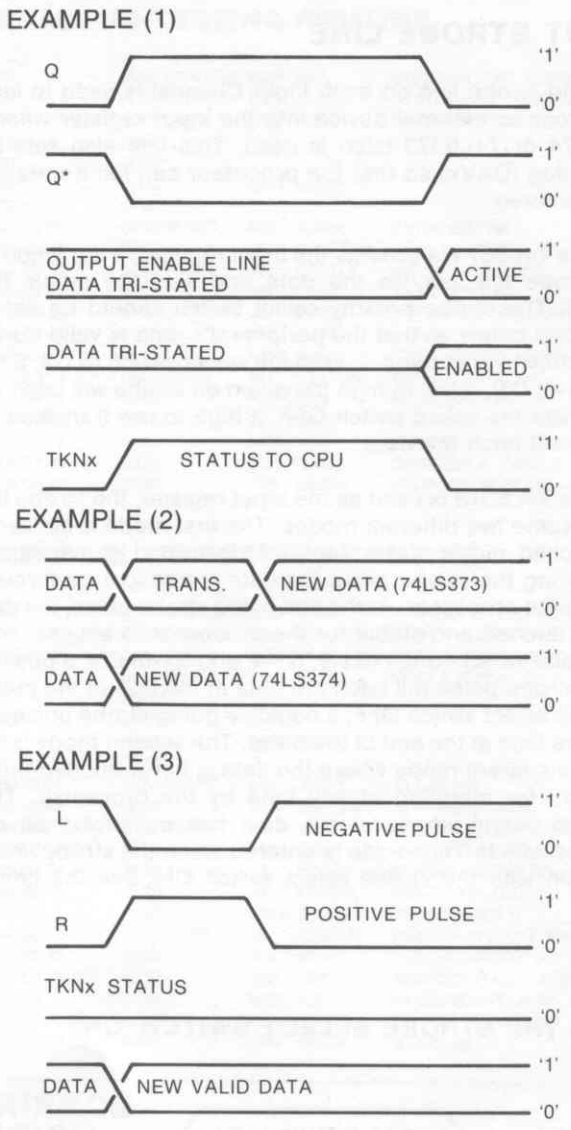
With the Common tied to either the 'L' or the 'R', the ATTENTION LINE becomes a positive (R) or negative (L) going strobe pulse with a width of the system PWR* strobe (between 150 and 1000ns). In this mode, the the OUTPUT ENABLE LINE should be set so that the data is active at all times, rendering the TKNx status bit low at all times. This mode is best used when the external device needs the data strobed into it. See the diagrams below for the output data timing using either a 74LS373 or a 74LS374 as an output register.

NOTE: Example (1) below shows the Q and Q* output lines (one of which will be tied to 'C' for driving the ATTENTION LINE), the OUTPUT ENABLE LINE with both polarities shown (the user must select the proper level to Tri-State and activate the data as described above and shown in the figure), the TKNx status line as read by the processor, and the state of the output data (either Tri-Stated or enabled).

Example (2) shows the state of the output data in the output register using either a 74LS373 or 74LS374 in relation to the strobes in Examples (1) and (3). NOTE: The transparent time on the 74LS373 contains new valid data since the S-100 bus supplies valid data during this time.

Example (3) shows both the 'L' and 'R' output pulses (one of which is tied to the 'C' or Common line for generating a pulse on the ATTENTION LINE), the state of the new output data (either new or old data), and the TKNx status line which is low to the proccessor at all times (assuming that the data is held active at all times with the OUTPUT ENABLE LINE).

OUTPUT DATA TIMING



OUTPUT EXAMPLES

Some examples of typical applications might include connecting a parallel printer or some LED's to the output lines. A parallel printer might require that 7, 8, or more data lines be connected in addition to a strobe line. In many cases, the strobe (L or R) connected to the ATTENTION LINE will be sufficiently long for the printer and can be connected directly with the proper polarity for correct printer operation. Some printers might require a longer strobe than the system PWR* pulse width, therefore a longer strobe can be made by switching a data bit from one of the other parallel output channels on and off via software to act as a strobe. If only 7 data lines are required for the printer, then the eighth data line from the same channel may be used with the software being tailored to provide a strobe pulse of almost any length.

PROGRAMMABLE TIMER INTERRUPT

The INTERFACER II is equipped with a simple programmable/fixed rate interrupt source for timing. By enabling the timer through the Interrupt Control Port and jumpering the interrupt to the appropriate vectored interrupt line on the bus, a fixed rate timer is established. The basic interrupt rate is set by positions 5 - 8 of Dip switch S2 as shown below. Further reductions in the basic rate are obtained by re-jumpering J12 as described below.

SWITCH POSITION 5 6 7 8	INTERRUPT RATE
0 0 0 0	50 INT/SEC.
1 0 0 0	75 INT/SEC.
0 1 0 0	110 INT/SEC.
1 1 0 0	134.5 INT/SEC.
0 0 1 0	150 INT/SEC.
1 0 1 0	300 INT/SEC.
0 1 1 0	600 INT/SEC.
1 1 1 0	1200 INT/SEC.
0 0 0 1	1800 INT/SEC.
1 0 0 1	2000 INT/SEC.
0 1 0 1	2400 INT/SEC.
1 1 0 1	3600 INT/SEC.
0 0 1 1	4800 INT/SEC.
1 0 1 1	7200 INT/SEC.
0 1 1 1	9600 INT/SEC.
1 1 1 1	19200 INT/SEC.

ON = '0' OFF = '1'

The above basic rate can be reduced by a factor of 2, 4, 8 by cutting the trace at J12 from 'A' to common on the solder side of the board, and installing a jumper between common and 'B', 'C', or 'D' for a reduction of 2, 4, or 8.

EXAMPLE: To set the interrupt rate to 9600 INT/SEC., DIP switch S2 would have position 5 ON and positions 6, 7, and 8 would be OFF.

EXAMPLE: To set the interrupt rate to 110 INT/SEC., DIP switch S2 would have positions 5, 7, and 8 ON and position 6 would be OFF.

EXAMPLE: To set the interrupt rate to 25 INT/SEC., (50 INT/SEC. divided by 2) DIP switch S2 would have positions 4-8 ON and a jumper installed between common and 'B' of J12 as described above.

The timer control bit is initially disabled after power-up or reset and must be initialized to be made operational. This is accomplished by outputting a logic '1' to the Interrupt/Control Port bit D3. The timer can be disabled by outputting a '0' to the control bit in the same fashion that it was enabled.

The proper response to a timer interrupt is to disable the timer as described above and then immediately re-enable it. This removes the interrupt from the bus in preparation for the next timer interrupt.

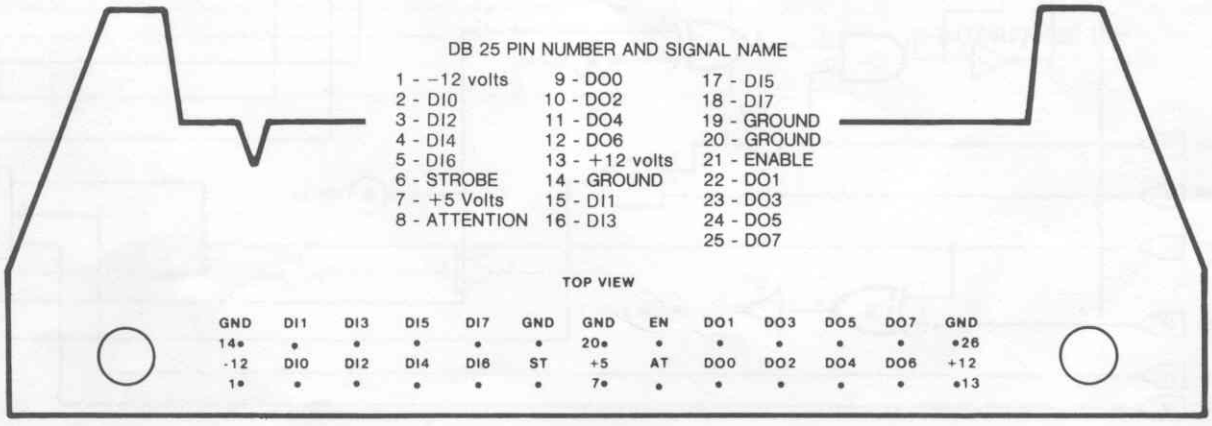
	S-100 BUS	PINS	J7			
VI0	4	—	1	16	—	INT J1
VI1	5	—	2	15	—	INT J2
VI2	6	—	3	14	—	INT J3
VI3	7	—	4	13	—	NC
VI4	8	—	5	12	—	TMRI
VI5	9	—	6	11	—	NC
VI6	10	—	7	10	—	RxINT
VI7	11	—	8	9	—	TxINT

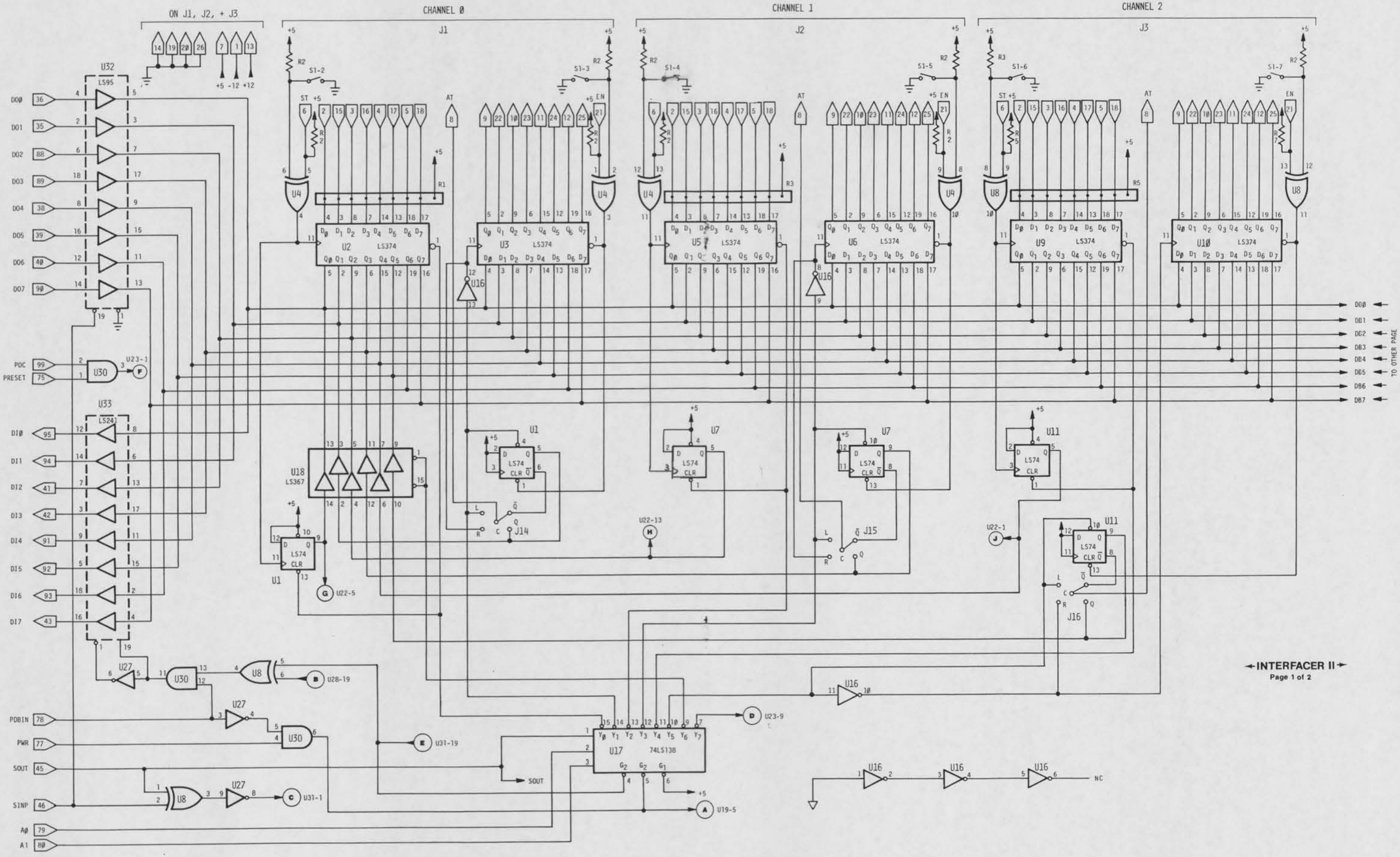
I/O CONNECTOR PINOUTS

A small amount of current is available for powering external devices such as a keyboard or A to D converter at each port connector. The total current available is shown below:

+ 5 volts @ 200 ma	TOTAL FOR
+12 volts @ 50 ma	ALL 3 PARALLEL
−12 volts @ 50 ma	CONNECTORS

CONNECTOR PINOUT - PARALLEL I/O PORT





INTERFACER II
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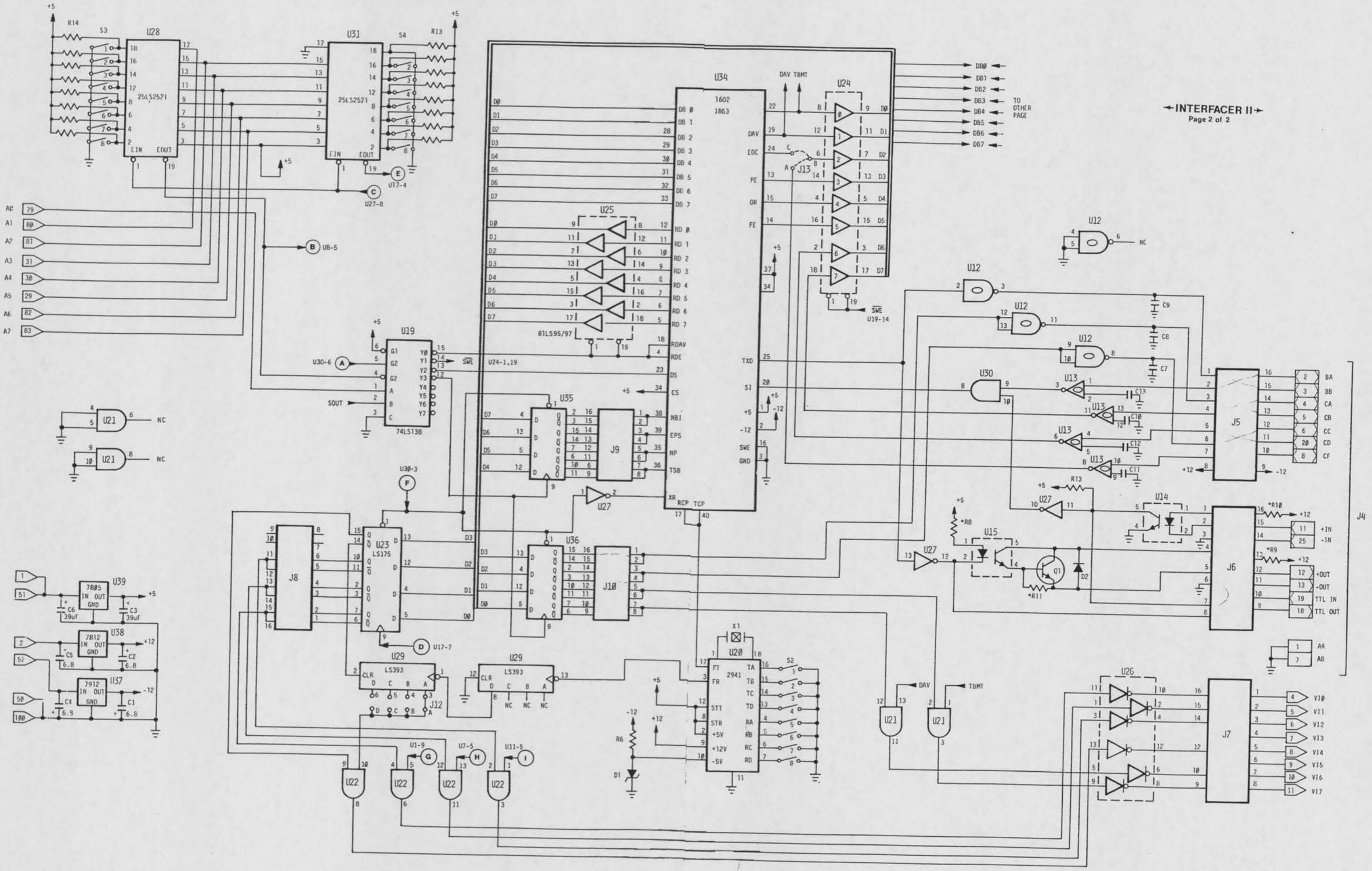
U28
25LS2521
U31
25LS2521
S3
S4
R14
R13
U34
1602
1863
U24
U25
81LS95/97
U19
74LS138
U35
J9
U27
U36
J10
U23
LS175
J8
U29
LS393
J12
U20
2941
X1
S2
U30
U12
U13
J5
J6
J7
J4
U14
U15
Q1
U26
U21
U22
U39
7805
U38
7812
U157
7912
TO OTHER PAGE
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BOARD POWER-UP AND TESTING

CHECKING-OUT YOUR BOARD

Now for the fun part . . . BEFORE you install the board in your system, take the time to check these few things over.

- ☐ 1. ARE ALL THE JUMPERS AND DIP SHUNTS PROPERLY INSERTED?
- ☐ 2. ARE THE BAUD RATE SWITCHES SET TO THE PROPER BAUD RATE FOR YOUR TERMINAL?
- ☐ 3. ARE THE PORTS YOU WANT TO USE PROPERLY ADDRESSED AND ENABLED?
- ☐ 4. IF YOU DON'T WANT TO USE A PORT, IS IT DISABLED?
- ☐ 5. ARE THE HARDWARE/SOFTWARE PROGRAMMING JUMPERS SET THE WAY YOU REALLY WANT THEM?
- ☐ 6. ARE YOU SURE YOU AREN'T TYING TWO OR MORE OF THE PROGRAMMING OUTPUTS TOGETHER?
- ☐ 7. ARE THE INTERRUPT JUMPERS SET TO THE PROPER INTERRUPT LINE, OR ARE THEY COMPLETELY REMOVED?
- ☐ 8. IF USING CURRENT LOOP, ARE THE PROGRAMMING LINES SET PROPERLY FOR USING EITHER ON-BOARD CURRENT SOURCE OR THE EXTERNAL SOURCE?
- ☐ 9. IF USING RS232, ARE THE PROGRAMMING LINES SET PROPERLY FOR MASTER OR SLAVE MODE?
- ☐ 10. ARE THE OPTION JUMPERS SET THE WAY YOU WANT?
- ☐ 11. ARE THE PARALLEL INTERRUPT MASK JUMPERS SET THE WAY YOU WANT?
- ☐ 12. ARE THE POLARITY SELECT SWITCHES SET PROPERLY?

If you have answered yes to all of the above, you are ready to install the board in your system. Enter the serial testing routine via either the front panel switches, editor assembler, or any means available.

SERIAL I/O TESTING ROUTINE

```
0000              0050 CONTROL EQU  01H      CONTROL PORT ADDRESS
0000              0060 STATUS  EQU  01H      STATUS PORT ADDRESS
0000              0070 DATA    EQU  00H      DATA PORT ADDRESS
0000              0080*
0000              0090*
0000              0100         ORG  0000H
0000              0110*
0000 3E 00        0120 START   MVI  A,00H    INITIALIZE THE
0002 D3 01        0130         OUT  CONTROL  CONTROL PORT
0004 DB 01        0140 BEGIN   IN   STATUS   INPUT STATUS AND
0006 E6 02        0150         ANI  02H      MASK FOR DAV
0008 CA OE        0160         JZ   BEGIN    IF NON/CHECK AGAIN
000B DB 00        0170         IN   DATA     IF DAV, 1 INPUT DATA &
000D 47           0180         MOV  B,A      MOVE TO REGISTER B
000E DB 01        0190 LOOP    IN   STATUS   INPUT STATUS AND
0010 E6 01        0200         ANI  01H      MASK FOR TBMT
0012 CA 0E        0210         JZ   LOOP     IF NOT READY, CHECK AGAIN
0015 78           0222         MOV  A,B      IF TBMT-1, MOVE DATA INTO
0016 D3 00        0230         OUT  DATA     REGISTER A, THEN OUTPUT
001B C3 04        0240         JMP  BEGIN    JUMP FOR NEXT CHARACTER
```

PARALLEL I/O TESTING ROUTINE

```
0000              0000 STATUS  EQU  0F3H     STATUS PORT ADDRESS
0000              0010 PORT0   EQU  0F0H     PORT 0 - CONN. J1
0000              0020 PORT1   EQU  0F1H     PORT 1 - CONN. J2
0000              0030 PORT2   EQU  0F2H     PORT 2 - CONN. J3
0000              0040*
0000              0050*
0000              0060         ORG  0000H
0000              0070
0000 3E 00        0080 START   MVI  A,00H    CLEAR THE
0002 D3 F3        0090         OUT  STATUS   INTERRUPT MASK
0004 DB F3        0100 BEGIN   IN   STATUS   INPUT STATUS AND MASK
0006 E6 01        0110         ANI  01H      FOR PORT 0 DATA AVL
0008 CA 04 00     0120         JZ   BEGIN    IF NONE / TRY AGAIN
000B DB F0        0130         IN   PORT0    INPUT DATA AND
000D 47           0140         MOV  B,A      STORE IN REG. B
000E DB F3        0150 LOOP    IN   STATUS   INPUT STATUS AND MASK
000E E6 02        0160         ANI  01H      FOR DATA ACCEPTED
0012 C2 OE 00     0170         JNZ  LOOP     RECHECK IF NOT ACCEPTED
0015 78           0180         MOV  A,B      RETRIEVE DATA AND
0016 D3 F0        0190         OUT  PORT0    OUTPUT TO PORT 0
0018 C3 04 00     0200         JMP  BEGIN    START AGAIN
```

IF YOU EXPERIENCE A MALFUNCTION

SERIAL SECTION TESTING

1. Verify that the Baud rate you want is being delivered to the UART. With a scope or frequency counter, measure the frequency at pins 40 and 17 of the UART. Remember that the UART needs a 16x clock, so the frequency will be 16 times the Baud rate.

   EXAMPLE: 1200 Baud x 16 = 19.2KHz
   for people with scopes:

   $$\text{Frequency (Hz)} = \frac{1}{\text{cycle period (seconds)}}$$

2. Verify with scope or logic probe that data reaches pin 20 of the UART when you type a character on your terminal. If not - trace back and see where it's being lost.

3. Verify that the status bit DAV (pin 19 of the UART) goes high after striking a character from the terminal. If it does not, and data is getting to the UART, you may have a bad UART.

4. Verify that your computer is getting the status of the board by running a simple program like the one below.

```
LOOP  IN   STATUS    (your status port)
      JMP  LOOP
```

   Verify that the line SWE pulses low while this program is running (pins 1 and 9 of the status gate U24) and that the data is getting on to the buss from the buss driver U33 as pin 1 and 19 pulse low and high, respectively.

5. Verify that the programming latches (U35, U36) and the UART are receiving their control strobes when the following program is run:

```
LOOP  OUT  CONTROL   (your control port)
      JMP  LOOP
```

   The line CS should strobe low while this program is running (check pin 9 of U35 and U36).

Verify that data is reaching the UART's from the host computer by running the following program and observing that pin 34 of the UART (DS) strobes low. NOTE: Only garbage will be transmitted.

```
LOOP   OUT  DATA        (your data port)
       JMP  LOOP
```

7. Verify that data is reaching the computer from the UART by running the following programs and observing that RDE strobes low (pins 4 and 18 of the UART) and that pins 1 and 19 of U33 strobe low and high, respectively.

```
LOOP   IN   DATA        (your data port)
       JMP  LOOP
```

8. Verify that serial data is leaving the UART pin 25 and is propagated to the output connector pin through the output level translators. Test this while running the I/O board testing routine.

9. If you don't seem to be getting any of the above mentioned control strobes, check pin 4 of U19 for a low strobe when running any of the above programs. If not, either the address is set wrong or there is a defective switch, I.C. or board in the I/O address decoding circuitry. Also, pin 5 of U19 should be strobe low to indicate either a pDBIN or pWR.

PARALLEL SECTION TESTING

1. Verify that pin 11 of the input 74LS374 pulses high when the input is strobed.

2. Verify that pins 15, 13, 11 and 9 of U17 strobe low when you input from ports 0, 1, 2, and 3 respectively.

3. Verify that pins 14, 12, 10 and 7 of U17 strobe low when you output from ports 0, 1, 2, and 3 respectively.

4. If you haven't been getting the strobes in the two previous steps, check for port enable strobing low on pin 4 and check for pWR and pDBIN strobing low on pin 5 of U17.

THE SERIAL SECTION

The heart of the Serial Section of this board is a MOS LSI UART. The UART performs the complete parallel to serial and serial to parallel conversion, error detection, and serial format modification necessary for reliable and flexible serial communication. The Serial Section can be divided into seven subsections: I/O Port Select Logic, Bus Driver Logic, Hardware/Software Programming Logic, Baud Rate Select Logic, Interrupt Logic, Serial Line Level Conversion Logic, and the UART.

I/O PORT SELECT LOGIC

Address line A1 thru A7 each feed into one input of the 25LS2521 octal comparator (U28) with the other input connected to a position on the Channel select dip switch (S3). The input of the comparator is gated by the I/O detect logic consisting of an X-OR gate (U8) with sINP and sOUT as its inputs. When the I/O operation is decoded and the selected address is on the bus, the control line decoder (U19) is enabled. The proper strobe lines are decoded by U19 with address A0 and sOUT, and are strobed to the UART during pWR* or pDBIN.

BUS DRIVER LOGIC

Data from the S-100 bus is buffered onto the internal bi-directional data bus by octal buffer U32 whenever sINP is not high. Data from the internal bi-directional bus is buffered onto the S-100 bus by U33 whenever a valid board enable and a pDBIN strobe both occur.

HARDWARE/SOFTWARE PROGRAMMING LOGIC

The Hardware/Software Programming logic consists of U35, U36, J9, and J10. Quad 'D' type latches (U35, U36, 74LS175) are reset by either POC or pRESET to a known state. This establishes defined levels on one side of the jumper sockets (J9, J10) which can be wired to each of the four signal lines on the opposite side of the jumper socket. Since the latches bring out both Q and Q* outputs, each of the eight control lines can be tied either high or low for any power-on or reset parameter setting. The control strobe output of U19 allows writing into these latches for software modification of the eight parameters by outputting a '1' to the bit corresponding to the parameter to be changed. Outputting a '0' to the bit will return it to its initial setting.

BAUD RATE SELECT LOGIC

The Baud Rate Select Logic is the simplest section of the board and consists of the baud rate generator (23), a 5.0688 MHz crystal (X1), one half of dip switch S2, and the minus 5 volt regulator (R6 and D1). The baud rate is set in a binary fashion on positions 1-4 of S2 for both the transmit and receive sections of the UART. Positions 5-8 of S2 select the base interrupt rate for the interrupt timer.

INTERRUPT LOGIC

The Interrupt Logic consists of two AND gates (U21) and two open collector inverters (U26). When the Hardware/Software programming logic is set so that the interrupts are enabled, a high level on either DAV or TBMT will generate a DATA AVAILABLE or TRANSMITTER BUFFER EMPTY interrupt through the open collector inverters. When the interrupt is processed and either the data read or written, the interrupt is removed from the bus.

SERIAL LINE LEVEL CONVERSION LOGIC

The Serial Line Level Conversion Logic consists of two main parts: the RS-232 - TTL level converters and the current loop and TTL level converters. All the signals from the channel connector J4 are brought out to jumper sockets J5 and J6 for user programming. All RS-232 level signals are taken from J5 and are fed to and from level converters U13 and U14 (1489 and 1488). The 1488 (the industry standard EIA RS-232-C line driver) converts the TTL level signals to the +12 and -12 volt signals to drive the transmitted data (TxD) and two RS-232 handshaking signals CA and CD. Holes for disc capacitors (C7-C9) are provided on the output of these drivers to limit slew rate to less than 30V/uSEC for compatibility with the RS-232-C specifications. For very short cables, capacitors with values up to 400 pF may be installed. For very long cables, no capacitance should be added due to the capacitance of the cables already limiting the slew rate. The 1489 (industry standard EIA RS-232-C line receiver) converts the +12 and -12 volt levels back to TTL levels for the UART and the 3 handshaking lines CB, CC, and CF (OPT.). Holes are provided on the board for adding the response control capacitors (C10-C13) for increased noise immunity.

The current loop and TTL level signals all enter and exit thru J6. The +IN and -IN signals are designed to feed opto-isolator U14 either through the on-board current source (R10), or directly from an external current source. The output of the opto-isolator is combined with the TTL IN signal, inverted (U27), ANDed (U30) with the data from the RS232 level converted data, and fed to the UART (U34) serial input line (SI). Transmit data (TxD) is inverted (U27), fed to J6 for TTL data and drives the LED of opto-isolator U15. The output of U15 is buffered by Q1-D2-R11 and fed to J6 where is uses either the on-board current source (R9) or an external current source to drive the +OUT and -OUT lines.

UART

The UART (U34) takes the parallel input data from the internal bus, serial parameters from the programming logic, the baud clock, and outputs serial data for the level conversion logic. It also takes the serial input data from the level converters, the baud clock, and the serial parameters, to yield parallel converted data for the internal bus as well as status through status buffer U24 and interrupts for use by the host processor.

THE PARALLEL SECTION

The parallel section consists of five major subsections: the I/O Port Select Logic, the Status Port, Interrupt Logic/Interrupt Mask Port, the Port Latches, and the Interrupt Timer.

I/O PORT SELECT LOGIC

Address line A2 thru A7 each feed one input of the 25LS2521 octal comparator (U31) with the other input connected to a section of the port select DIP switch S4. The input of the comparator is gated by the I/O detect logic described in the serial section. The output of the comparator enables the port decoder (U17), which generates the proper strobe pulses for the six latches, the status port and the interrupt mask port depending on the three select inputs (A0, A1, and sOUT) and when either a pWR* or pDBIN occurs.

STATUS PORT

The Status Port gates its information onto the internal bus with Hex Tri-State buffer (U18) when pin 9 of the port decoder (U17) strobes low. Data bits D0, D2, and D4 carry the status information from the input port on J1, J2, and J3 respectively. A high level on these lines indicates that data has been strobed into the input buffer and has not been read by the processor. Data bits D1, D3, and D5 carry the attention bit status from channels J1, J2, and J3 respectively. A high level on these lines indicates that the processor has output data to the ports that has not yet been accepted by the external device. A low on this input indicates that the data has been accepted. This bit has no significance when the output register is enabled at all times since the attention flag is being held clear. The status port always resides as the last port in the block of four parallel channels.

INTERRUPT LOGIC/INTERRUPT MASK PORT

The Interrupt Logic consists a quad 'D' type latch (U23), three 'D' type flip flops (U16 and U22a), four 2 input AND gates (U22), and four open collector inverters (U26). The quad latch is cleared on power-up or reset to a known state that can be jumpered across J8 to the inputs of the AND gates to act as enables for the interrupts. The latch can also be written into from the internal bus when strobed by decoder U17, allowing the alteration of the interrupt mask under software control. Data bits D0, D1, and D2 control the interrupt enables for the channels on J1, J2, and J3 respectively. Data bit D3 controls the starting and stopping of the timer and will be discussed in a following section. A strobe bit from any of the input channels will set the appropriate 'D' flip flop, and if enabled will provide a high level to the O.C. inverter which drives the interrupt lines. When the input data is read from the latch, the 'D' flip flop is cleared and the interrupt is removed from the S-100 bus.

PORT LATCHES

The port latches (U2, U3, U5, U6, U9, and U19) accept data either from the internal bus or from an external device. 'D' flip flops U1, U7, and U11 act as the status flip flops for the above latches. When the input strobe passes thru the polarity select X-OR gates, the selected transition will latch the incoming data into the 74LS373 or LS374 and set the status flip flop. When this data is read by the processor, the enable strobe gates the data onto the internal bus and clears the status flag. When the processor outputs data to an output register, the clock inputs of the latch and the attention flip flop are strobed, the output strobes are generated and the attention line is set (if the output is not enabled), and the data is latched. The attention flip flop is cleared when the output enable line enables the output register. The output strobes are as long as the pWR* strobe in the computer system.

INTERRUPT TIMER

The Interrupt Timer consists of one half of the baud rate generator (U20), a dual 4 bit counter (U29), an AND gate (U22) and an open collector inverter (U29). The output of the baud rate generator is divided by 16 by one half of the counter and the output is fed to the other half for further dividing and clearing. After power-up or reset, the second counter is held cleared until a '1' is written into the interrupt mask register bit D3. When enabled, the counter will increment and when the jumpered output goes high (J12), an interrupt is generated. When recognized, the enable counter should be cleared (removing the interrupt from the bus) by outputting a '0' and then a '1' to the interrupt mask bit D3. This action resets the counter and readys it for another interrupt.

Notes

Notes

Parts List

☐	(1)	Circuit board	

INTEGRATED CIRCUITS (Note: the following parts may have letter suffixes and prefixes along with key numbers given below).

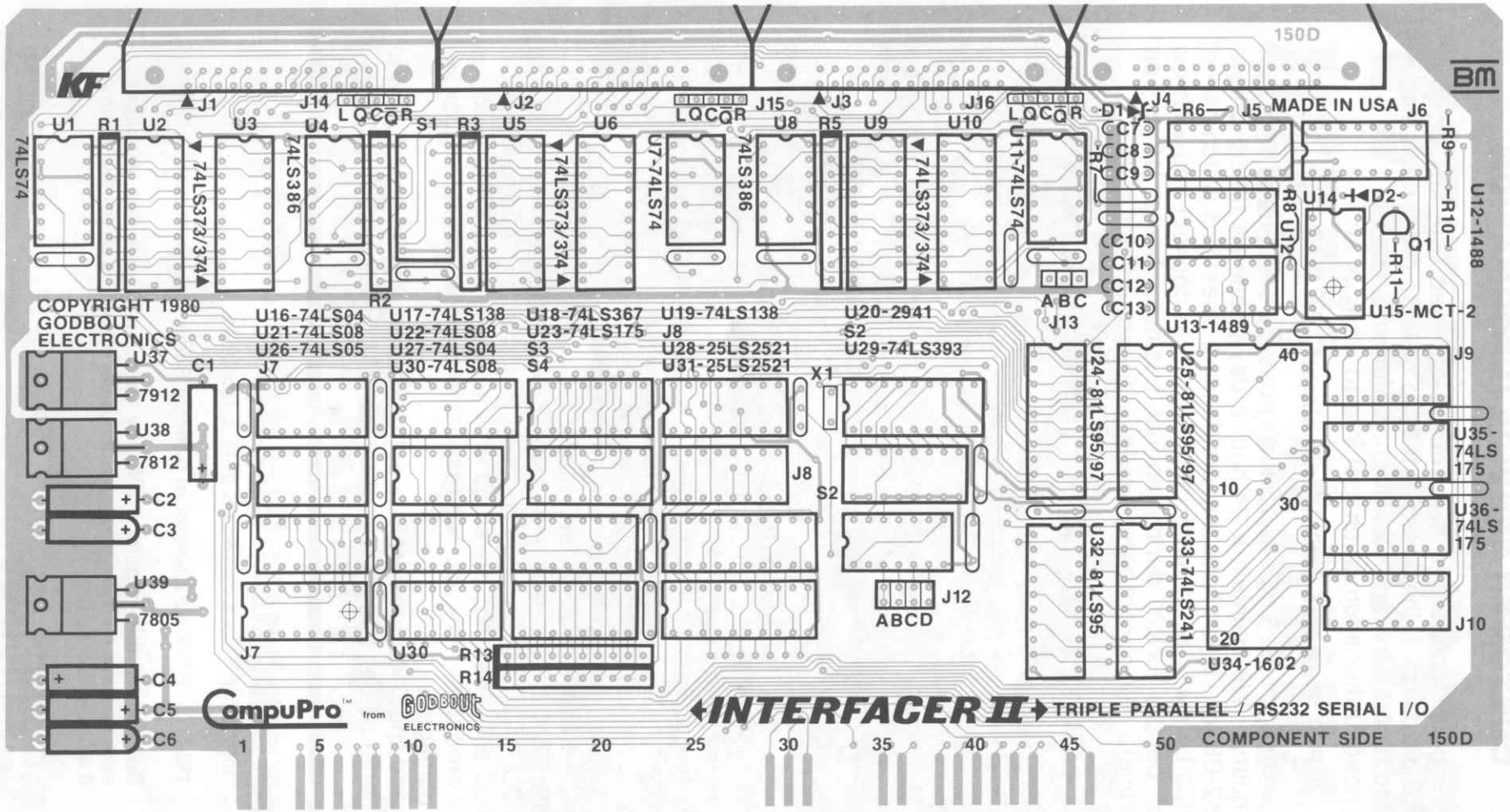
☐	(2)	74LS04 hex inverter	U16, U27
☐	(1)	74LS05 hex o.c. inverter	U26
☐	(3)	74LS08 quad AND gate	U21, U22, U30
☐	(3)	74LS74 dual 'D' flop	U1, U7, U11
☐	(2)	74LS138 3-8 decoder	U17, U19
☐	(3)	74LS175 quad 'D' latch	U23, U35, U36
☐	(1)	74LS241 octal bus driver	U33
☐	(1)	74LS367 hex bus driver	U18
☐	(3)	74LS373 octal latch	U2, U5, U9
☐	(3)	74LS374 octal 'D' latch	U3, U6, U10
☐	(2)	74LS386 quad X-OR gate	U4, U8
☐	(1)	74LS393 dual 4 bit counter	U29
☐	(2)	81LS95/97 octal bus driver	U24, U25
☐	(1)	81LS95 octal bus driver	U32
☐	(2)	25LS2521 octal comparator	U28, U31
☐	(1)	1602/1863 UART	U34
☐	(1)	1941 baud rate generator	U20
☐	(1)	1488 RS232 driver	U12
☐	(1)	1489 RS232 receiver	U13
☐	(2)	MCT-2 opto isolator	U14, U15
☐	(1)	7805 + 5V regulator	U39
☐	(1)	7812 + 12V regulator	U38
☐	(1)	7912 - 12V regulator	U37

OTHER ELECTRICAL COMPONENTS

☐	(1)	NPN transistor - 2N3904	Q1*
☐	(1)	1N914/806-36 signal diode	D2*
☐	(1)	1N751A 5V Zener diode	D1*
☐	(6)	SIPS resistor pack	R1, R2, R3, R5, R13, R14*
☐	(1)	470 ohm resistor	R8*
☐	(2)	560 ohm resistor	R9, R10*
☐	(3)	2.7K resistor	R6, R7, R12*
☐	(1)	4.7K resistor	R11*
☐	(1)	5.0688 MHz crystal	X1
☐	(4)	1.8 uF 35V tantalum cap	C1, C2, C4, C5
☐	(2)	39 uF 10V tantalum cap	C3, C6
☐	(27)	disc caps*	

MECHANICAL COMPONENTS

☐	(40)	low profile sockets*	
☐	(4)	dip switches 8-pin	S1, S4
☐	(1)	heat sink for U39	
☐	(3)	sets 6-32 hardware	
☐	(4)	26-pin I/O connector	J1 - J4
☐	(3)	16-pin dip platform	J5 - J7
☐	(3)	16-pin dip shunt	J8 - J10
☐	(1)	instruction book	



Component Layout

CUSTOMER SERVICE INFORMATION

Our paramount concern is that you be satisfied with any Godbout CompuPro product. If this product fails to operate properly, it may be returned to us for service; see warranty information below.

If you need further information feel free to write us at:

P.O. Box 2355, Oakland Airport, CA 94614.

When writing, please be as specific as possible concerning the nature of your query. We maintain a 24 hour a day phone for taking orders, (415) 562-0636. If you have any problems or questions which cannot be handled by mail, this number can be used to connect you with our technical people ONLY during normal business hours (10am-5pm Pacific Time). We cannot return calls or accept collect calls.

LIMITED WARRANTY INFORMATION

Godbout Electronics will repair or replace, at our option, any parts found to be defective in either materials or workmanship for a period of 1 year from date of invoice. Defective parts *MUST* be returned for replacement.

If a defective part causes a Godbout Electronics product to operate improperly during the 1 year warranty period, we will service it free (original owner only) if delivered and shipped at owner's expense to and from Godbout Electronics. If improper operation is due to an error or errors on the part of the purchaser, there may be a repair charge. Purchaser will be notified if this charge exceeds $10.00.

We are not responsible for damage caused by the use of solder intended for purposes other than electronic equipment construction, failure to follow printed instructions, misuse or abuse, unauthorized modifications, use of our products in applications other than those intended by Godbout Electronics, theft, fire, or accidents.

Return to purchaser of a fully functioning unit meeting all advertised specifications in effect as of date of purchase is considered to be complete fulfillment of all warranty obligations assumed by Godbout Electronics. This warranty covers only products marketed by Godbout Electronics and does not cover other equipment used in conjunction with said products. We are not responsible for incidental or consequential damages.

Prices and specifications are subject to change without notice, owing to the volatile nature and pricing structure of the electronics industry.