Heathkit® Manual

for the

VIDEO TERMINAL

Model H9

OPERATION 595-2017-03

HEATH COMPANY
BENTON HARBOR, MICHIGAN 49022

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INTRODUCTION

The Heathkit Model H9 Video Terminal can display information coming from a digital computer or information typed in from the keyboard. This information is displayed on a 12" (diagonal) cathode ray tube (CRT) that is capable of displaying 960 characters at one time (12 rows with 80 characters per row).

A 67-key ASCII keyboard, which permits you to compose and edit directly on the CRT, has a capability of 64 different characters and 24 different functions. This message or program can be transmitted through the standard serial I/O interface (EIA, TTL, or 20 mA current loop) to a digital computer or through the parallel I/O interface to a paper tape reader/punch.

The Video Terminal can be used with any digital computer in a dedicated format, in a stand-alone application, or in a time-sharing system. It lets you communicate with a digital computer in higher-level language (Basic, Assembler, etc.) rather than just using toggle switches. The Video Terminal is also much faster (up to 9600 baud) than the standard electro-mechanical teletypewriter systems. You can select any data rate between 110 and 9600 baud.

Other important features include:

- Automatic scrolling
- Cursor controls
- Erase to end of line
- Erase page
- Short form (four 12-line columns of 20 characters)
- Automatic line carryover
- Plot mode
- Built-in speaker (audible bell)
- Transmit page

These features, along with the attractively-styled cabinet, make the Video Terminal a versatile peripheral for your computer system.

OPERATION

The Video Terminal will generate and display 64 ASCII coded characters. They include the alphabet (upper case only), numbers, punctuation, and many symbols. Thirty-two standard control characters and twenty-four special functions can also be generated. Pictorial 1-1 (Illustration Booklet, Page 1) shows the location of the keys described in the following paragraphs.

LOCAL FUNCTION KEYS

The local function keys do not transmit ASCII characters; they only affect the display.

CURSOR CONTROL KEYS

These keys are on the far right of the keyboard and they are labeled with arrows.

UP CURSOR (↑)
DOWN CURSOR (↓)
RIGHT CURSOR (→)
LEFT CURSOR (←)

} These keys move the cursor one character position or one character line as indicated by the arrow.

HOME

This key moves the cursor to the first character location on the first line.

ERASE EOL (End Of Line)

This key erases the text from the current cursor location to the end of that line.

ERASE PAGE

This key erases all text and fills the page (screen) with spaces. It also places the cursor in the home position.

AUTO CARRY

When this key is pushed in, the cursor automatically goes to the beginning of the next line after a full line of text is typed. At the end of the bottom line of text, the cursor will start over at the beginning of the first line (home position), providing the Terminal is not in scroll mode (SCROLL key released). Also, refer to "Hold Screen" on Page 8.

SHORT FORM

When this key is pushed in, the display format is changed from twelve lines of 80 characters (key released) to four columns — each column consisting of twelve lines of 20 characters. Short form is useful for writing programs in machine language where entries are short.

SCROLL

When this key is pushed in, and after the first twelve lines of text are typed, the first line is erased (scrolled upward) and lost. Each remaining character line moves up one line position and the cursor moves to the bottom line. In short form, the left column of 240 characters (12 lines of 20 characters) is erased and lost. The remaining three columns move to the left one column position, and the cursor moves to the right column. When the SCROLL key is released (in the non-scroll position), and after the first twelve lines of text are typed, the cursor returns to and flashes at the start of page position. Further typed entries will write over the existing text on the first line. Also, refer to "Hold Screen" on Page 8.

SPECIAL FUNCTION KEYS

RETURN (Carriage Return)

This key moves the cursor to the first character position of the line it is currently in and it transmits the Return ASCII code (control M). Return can be written into a RAM location only if that location contains a space. That is, a carriage return will not write over any other character. Return is a non-displayable character, except in the plot mode.

LINE FEED

This key moves the cursor down one line and it transmits the line feed ASCII code (control J). Line feed does not write into RAM and it is not a displayable character, except in the plot mode.

RUB OUT

This key transmits an ASCII rub out code (delete). Rub out does not write into RAM and it is a non-displayable character, except in the plot mode.

ESC (Escape)

This key transmits an ASCII escape code. Escape does not write into RAM and it is a non-displayable character, except in the plot mode.

REPT (Repeat)

When this key is held in, along with another key, it will repeat the function of the other key at a preset rate as long as both keys are held down. The presettable repeat rates are 3.7-, 7.5-, 15-, or 30-characters per second. If the baud rate that has been selected is less than the repeat rate, the repeat function will operate at the slower rate.

PLOT

When this key is pushed in, the text is blanked except for the first line of the page. This first line, however, is displayed on each of the four bottom lines of the screen. The screen area above the bottom four lines is divided into 128 scan lines. See Pictorial 1-2. A dash, one character wide, will appear above each of the characters displayed in the bottom four lines. The position of the dash above the bottom line (line 0) is proportional to the binary value of the 7-bit ASCII code for that character. For example, a CTRL/SHIFT P, or ASCII null, is all zeros, so its binary value is zero, and it appears at the bottom of the 128 line space directly above the ASCII null. Pictorial 1-3 (Illustration Booklet, Page 2) gives the line number and the ASCII code for each key entry. A RUB OUT (delete) or all ASCII 1's has a binary value of 127, so the dash appears at the top line (line 128) in the space above the rub out character.

In the plot mode, all characters are written into RAM, but their special cursor movements are not implemented. That is, a RETURN (carriage return) is written into RAM, but the cursor does not move. Any control character that appears in the text will flash.

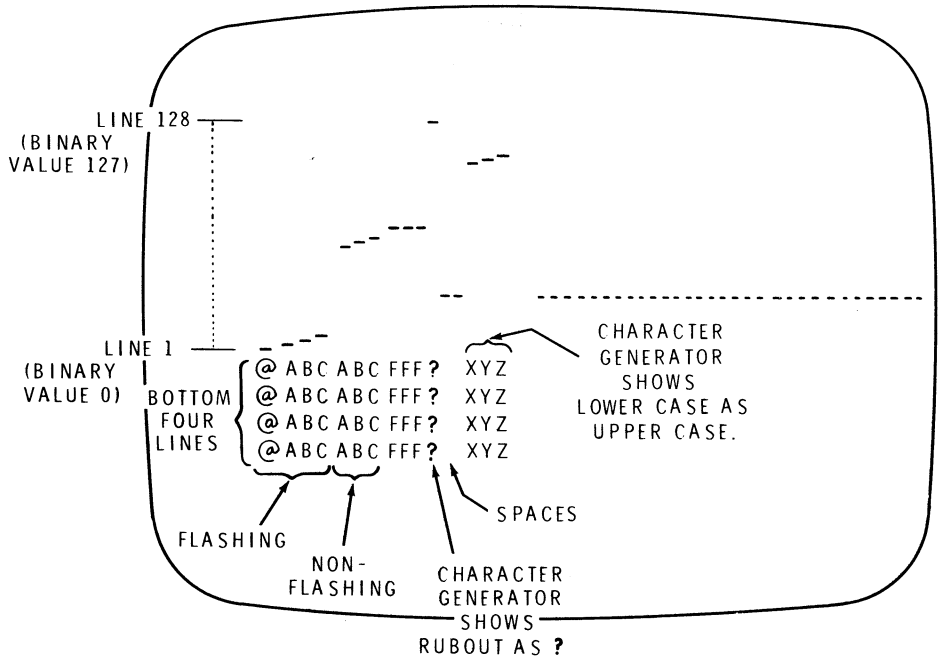
Even though the lower-case alphabetic characters cannot be generated from the keyboard, they can be entered into RAM from the digital computer. Like all other characters, the binary value of the lower case characters is stored in RAM and the dash is displayed on the appropriate line in the 128-line space. Lower case characters stored in RAM are displayed as the characters represented by the ASCII words 010 0000 through 011 1111.

BAUD RATE

When this key is released (out), the Terminal will operate at 110 baud. When this key is pushed in, the rate is set by the BAUD RATE switch on the rear panel. The rear panel switch selects either 300 baud or the preset baud. The preset baud is determined by a jumper wire on the I/O circuit board.

OFF LINE

When this key is pushed in, the Terminal is inhibited from transmitting or receiving data from the serial I/O, but it does not interrupt transmission or reception through the parallel I/O port. This lets you punch or read tape on the paper tape reader/punch while the Terminal is off line from the digital computer.



PICTORIAL 1-2

BREAK

When this key is pushed in, it generates a continuous space at the serial output. It is generally used to tell the computer that you wish to interrupt execution. Do not confuse this space with an ASCII space. It is defined as zero current in a 20 mA current loop, an EIA positive voltage, or a TTL logic 0. The BREAK key can be pressed any time you want to terminate the transmit page function.

FULL DUPLEX

When this key is released (out), the Terminal operates in the half duplex mode. That is, data from the keyboard or parallel input is written directly into RAM and, at the same time, ASCII characters are sent out the serial and parallel outputs. When the FULL DUPLEX key is pushed in, the Terminal operates in the full duplex mode. Data from the parallel input or from the keyboard is sent to the computer and echoed back to the Terminal before it is written into RAM and displayed on the screen.

XMIT PAGE (Transmit Page)

When you momentarily press this key, data is transmitted from the RAM (screen), starting from the current cursor location and proceeding to the end of the page. When it has completed the page, the cursor returns home and the transmit page mode stops. The data is transmitted simultaneously out both the parallel and serial ports at a rate determined by the slower of the two ports. Press the BREAK key to interrupt the transmit page function.

CTRL (Control)

When this key is used in conjunction with some of the other keys, it changes those keys to special function keys. For instance, CTRL M is equivalent to a return (carriage return). The control key combinations are shown in Pictorial 1-3.

SHIFT

When this key is used in conjunction with another key, the character printed on the upper portion of that key will be displayed. Since the Terminal does not generate lower-case alphabetic characters, it is not necessary to push the shift key to generate upper-case alphabetic characters — they are shifted automatically in the keyboard encoder.

CTRL/SHIFT

These two keys are used in conjunction with other keys to provide additional special function keys. For instance, CTRL/SHIFT P (which means, press the CTRL, the SHIFT, and the P keys at the same time) puts an ASCII null (all zeros) on the bus.

CONTROL CHARACTERS

The Terminal generates all 32 ASCII control characters from the keyboard. Normally these characters do not write into RAM, nor are they displayed on the screen. Exceptions are outlined in the description of the plot mode. The Terminal recognizes only four of the control characters. It will recognize these from the keyboard or from the parallel or serial input ports. The four characters are:

Line Feed (LF or CTRL J) — This character duplicates the LINE FEED key.

Carriage Return (CR or CTRL M) — This character duplicates the RETURN key.

Back Space (BS or CTRL H) — This character moves the cursor to the left one character position without disturbing the character being displayed.

Bell (Bel or CTRL G) — This character causes the Terminal to sound a short audible tone through an internal speaker. Pictorial 1-3 shows the control and normal characters that the Terminal can generate.

HOLD SCREEN

If the screen has been filled, and a scroll function should occur, but can't because the SCROLL key is not pushed in, the Terminal goes into the hold screen mode. The cursor returns to the start of page location and blinks. All external inputs are disabled when this occurs. Data can only be transmitted out of the Terminal by the keyboard. The Terminal stays in the hold screen mode until the SCROLL key is pushed in or until the ERASE PAGE key is pressed.

You can use this feature in conjunction with the paper tape reader/punch for reviewing program tapes. The reader/punch can read the tape at its maximum speed to fill up the screen quickly, then after the last line has been written, the hold screen mode disables the handshake signal coming from the Terminal. This stops the tape from running. You can then review the contents of the screen. When you are finished, just press the ERASE PAGE key and receive another screen full of program information automatically.

SYSTEM CONSIDERATIONS

The following section "Heathkit Computer System Interface Standards" explains how to interface the Heathkit H9 Video Terminal to the Heathkit H8 Digital Computer. Refer to this section if you have the Heathkit Computer System. If you are using a non-Heathkit digital computer with your H9 Video Terminal, refer to the "General Interfacing" section and select the suitable interface scheme.

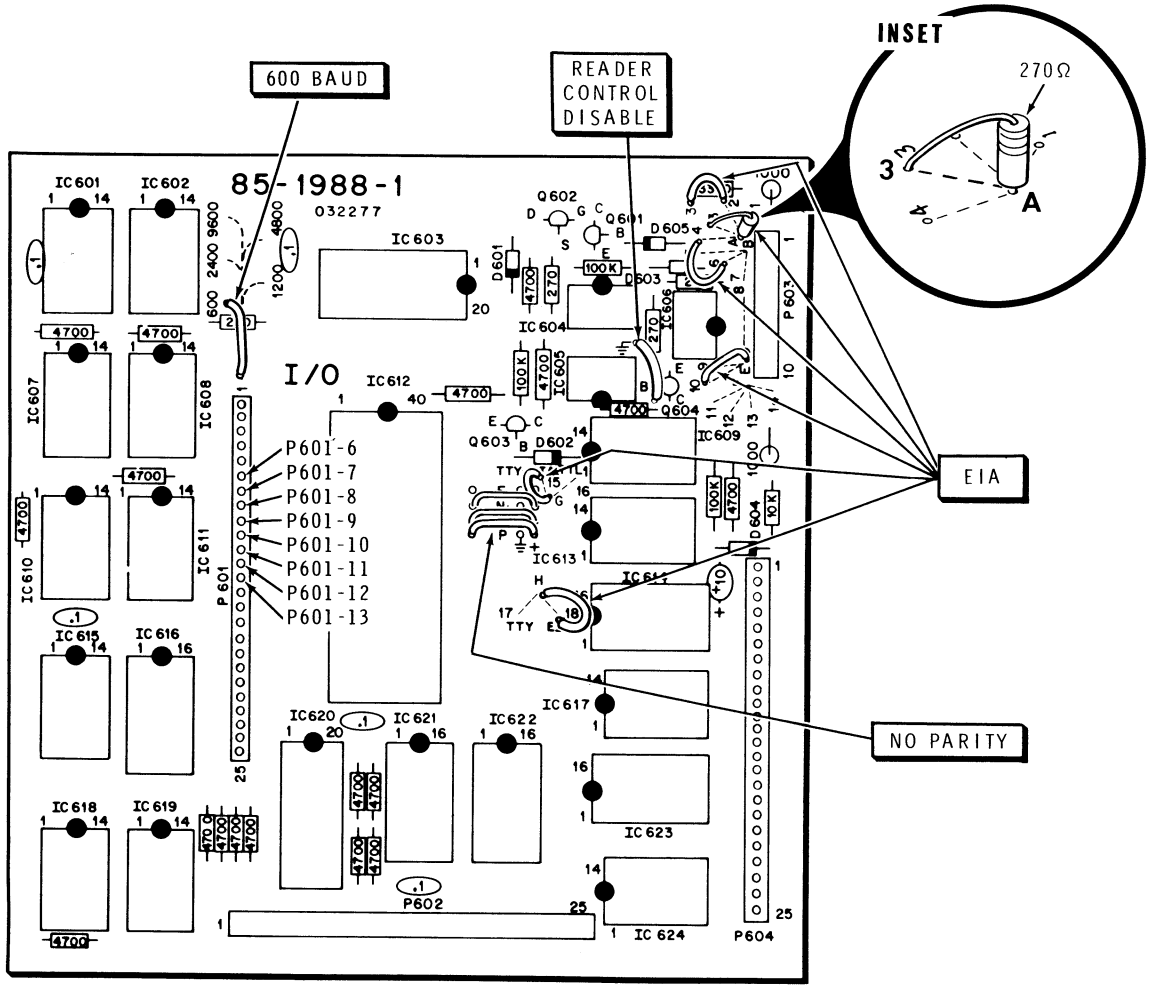
HEATHKIT COMPUTER SYSTEM INTERFACE STANDARDS

The following interface configuration has been designated as the Heathkit Computer System Interface Standard. Use these standards when you interface the H9 Video Terminal with the H8 Digital Computer. Both the Video Terminal and the Digital Computer must be wired to operate in the following standard format:

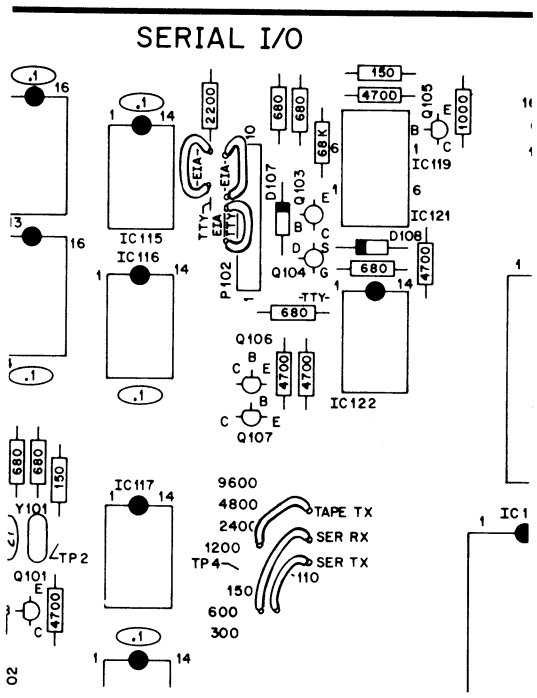
Data Rate	—	600 Baud
Signal Level	—	EIA or RS-232C
Word Length	—	8 Bits
Parity	—	None

To do this:

1. Examine the I/O circuit board in the H9 Video Terminal to make sure it is wired as shown in Pictorial 2-1.
2. Examine the Serial I/O circuit board in the H8 Digital Computer to make sure it is wired as shown in Pictorial 2-2.
3. Examine the interconnecting cable (between the H9 and the H8) to make sure it is wired as shown in Pictorial 2-3 (Illustration Booklet, Page 3).



PICTORIAL 2-1



PICTORIAL 2-2

MODEL	H8-5	H8	H9	H9
LOCATION	Circuit Board	Rear Panel	Rear Panel	I/O Circuit Board
PLUG NUMBER	P102	P3	Serial I/O Connector	P603
	PIN No.	PIN No.	PIN No.	PIN No.
DATA →	8 — Blu	8 — Red	4 — Blk	9
DATA ←	5 — Org	5 — Wht	1 — Grn	1
GROUND	4 — Red	4 — Brn	9 — Brn	4,7

PICTORIAL 2-3

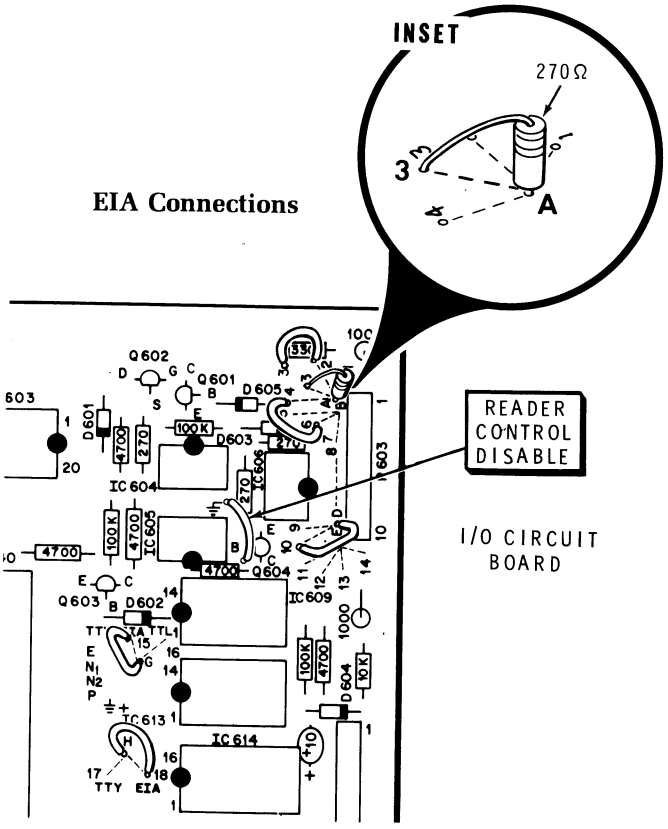
GENERAL INTERFACING

I/O CIRCUIT BOARD PROGRAMMING

The I/O circuit board can be programmed (wired) to operate in one of three serial input/output modes:

- EIA RS-232C
- TTL
- TTY (20 mA current loop)

You can also select one of five baud rates (600 to 9600), select the word length (5-, 6-, 7-, or 8-bit), as well as generate a parity bit (odd or even).



EIA Connections

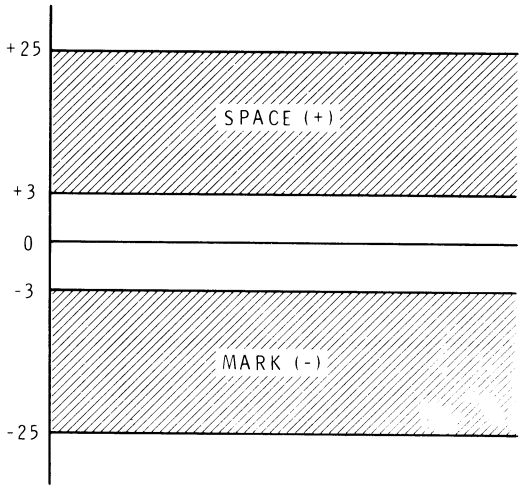
PICTORIAL 2-4

The Video Terminal is wired initially so that it is compatible with the Heathkit H8 Digital Computer System. The various serial input and output levels and configurations are explained in the following paragraphs. This information will help you interface the Terminal with your particular system.

Always remove the I/O circuit board from the Terminal before you make any wiring (programming) changes.

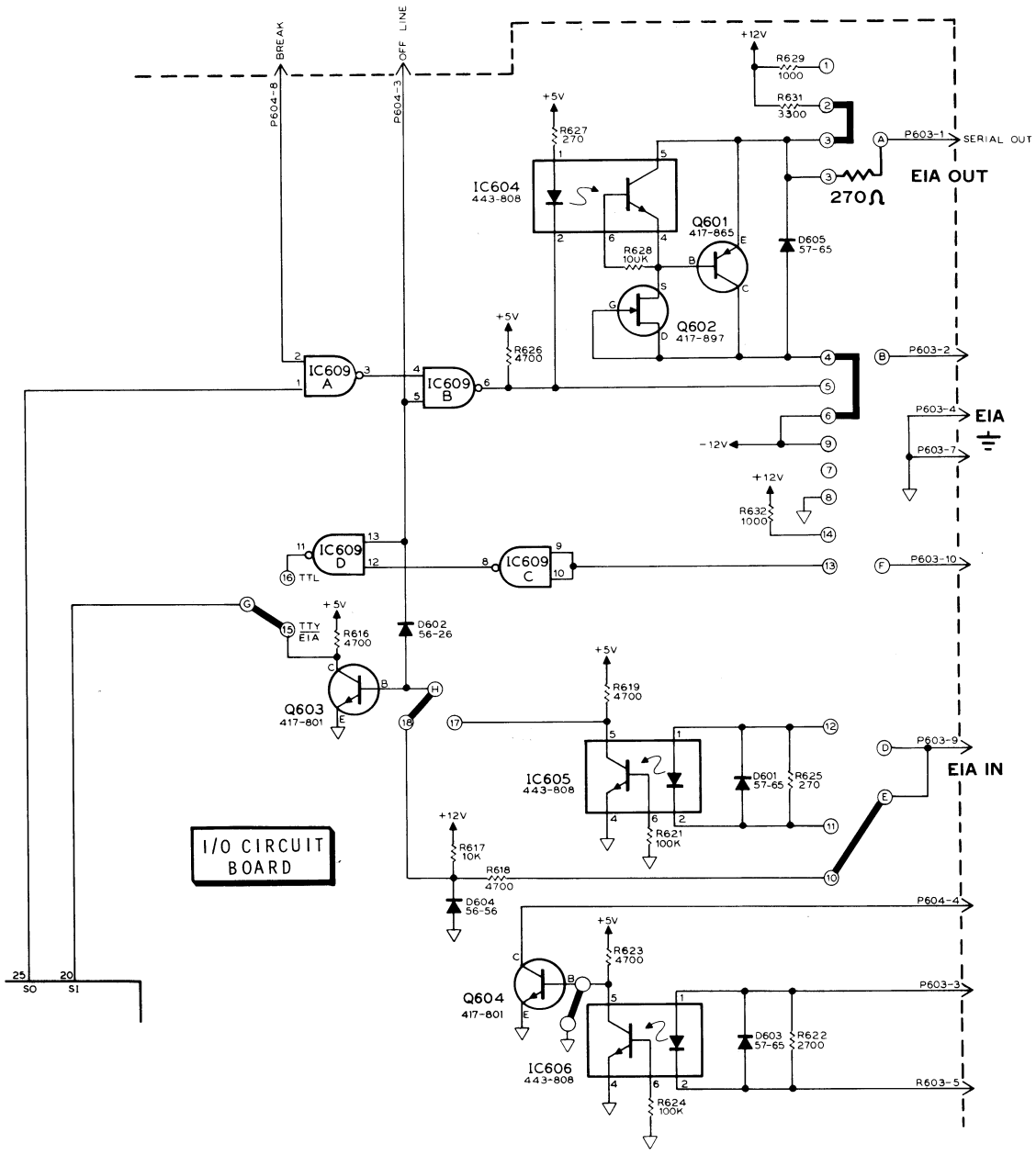
EIA RS-232C Serial Input/Output

The Terminal is initially wired for an EIA serial input/output. Pictorial 2-4 shows the jumper wires necessary for this configuration. The EIA input levels are shown in Pictorial 2-5. A space is defined as a positive voltage between +3 and +25 volts. A mark is defined as a negative voltage between −3 and −25 volts. Pictorial 2-6 shows the partial schematic of the EIA wiring on the I/O circuit board. The jumper wire that disables the reader control is shown in Pictorials 2-4 and 2-6. Refer to "Reader Control" on Page 18.



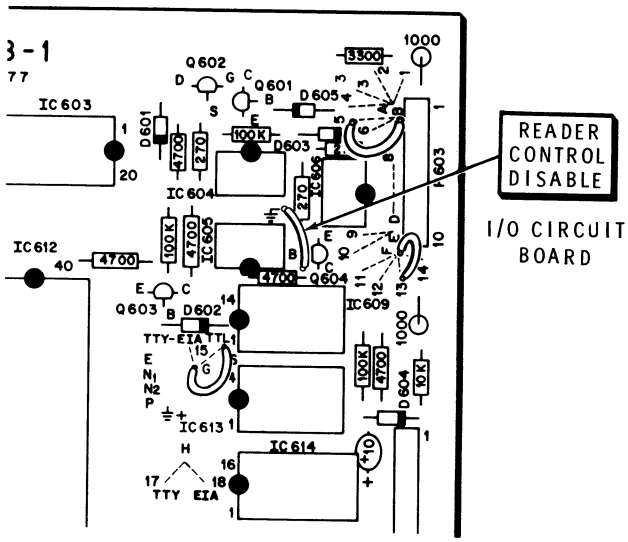
PICTORIAL 2-5

EIA Connections

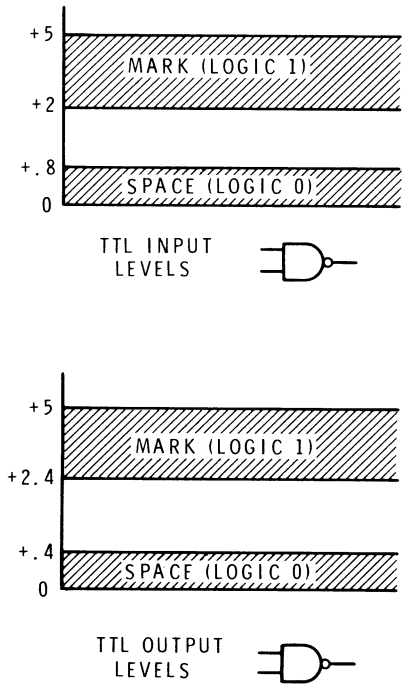


PICTORIAL 2-6

TTL Connections



PICTORIAL 2-7



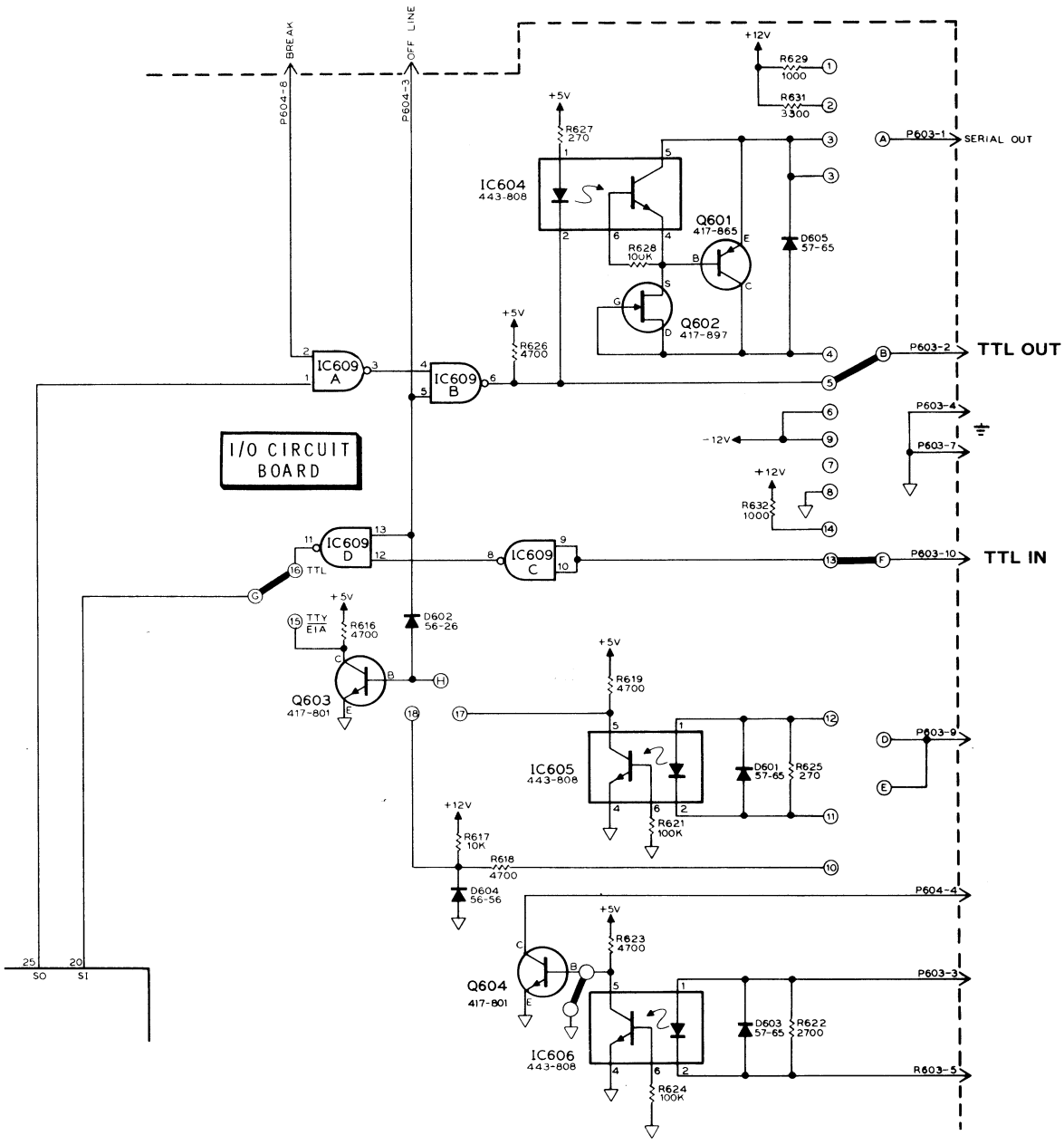
PICTORIAL 2-8

TTL Serial Input/Output

Pictorial 2-7 shows the jumper wires necessary for the TTL configuration. The TTL inputs are standard TTL logic levels as shown in Pictorial 2-8. A mark is defined as a logic 1 and a space is defined as a logic 0.

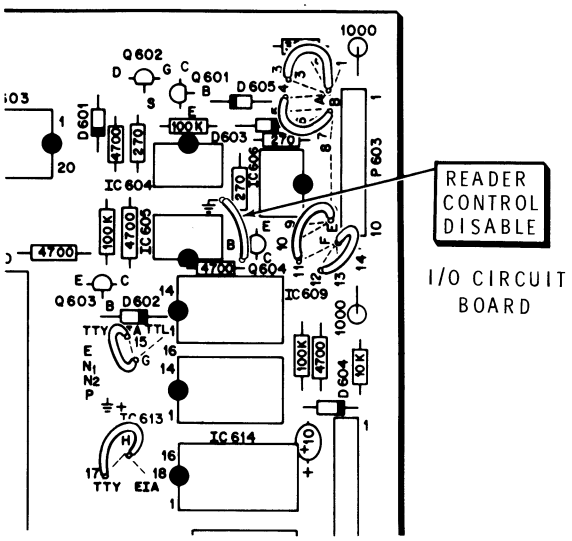
Pictorial 2-9 shows the partial schematic of the TTL wiring on the I/O circuit board. The jumper wire that disables the reader control is shown in Pictorials 2-7 and 2-9. Refer to "Reader Control" on Page 18.

TTL Connections



PICTORIAL 2-9

TTY (Passive) Connections



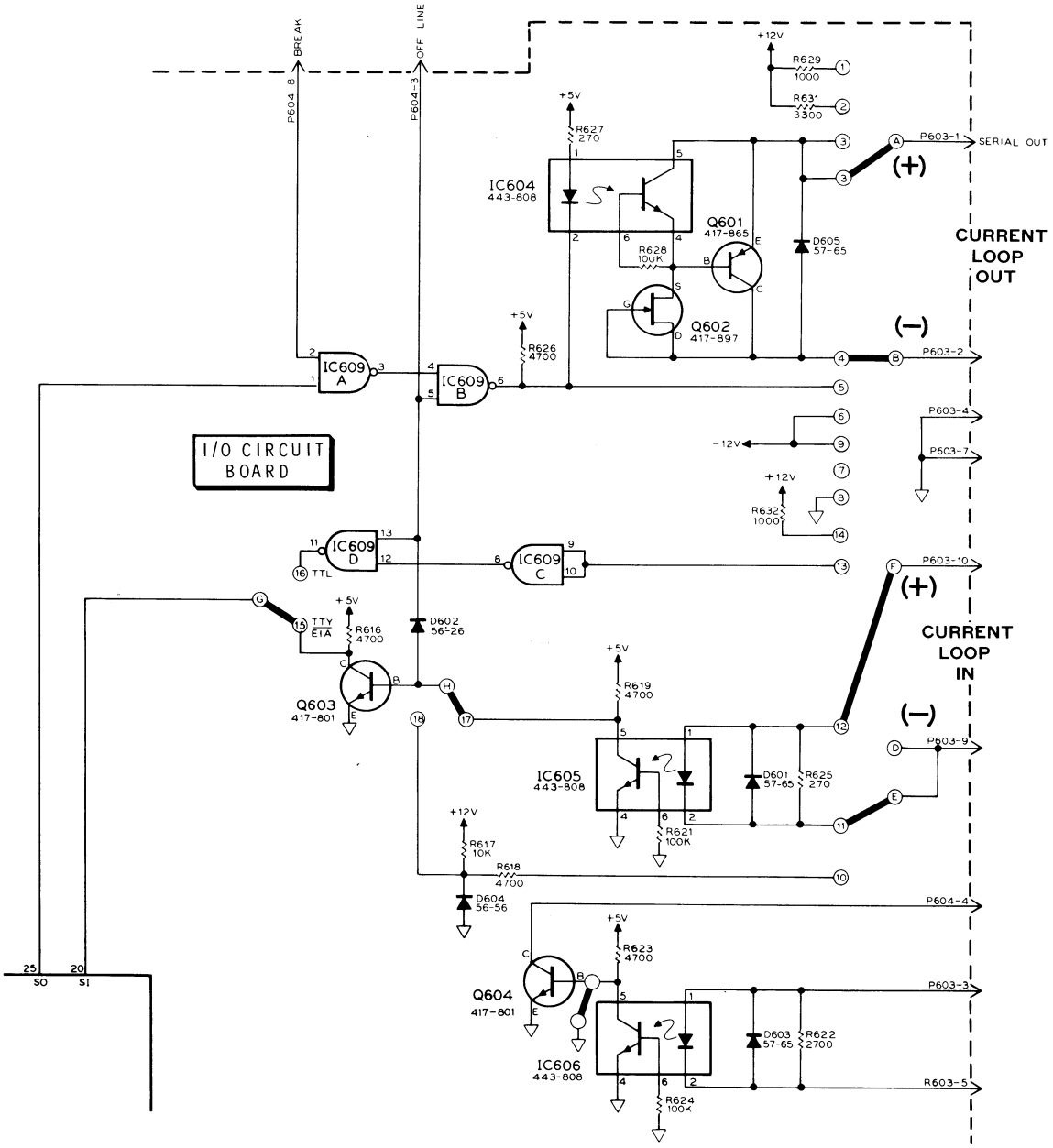
PICTORIAL 2-10

TTY (20 mA current loop) Serial Input/Output

Passive

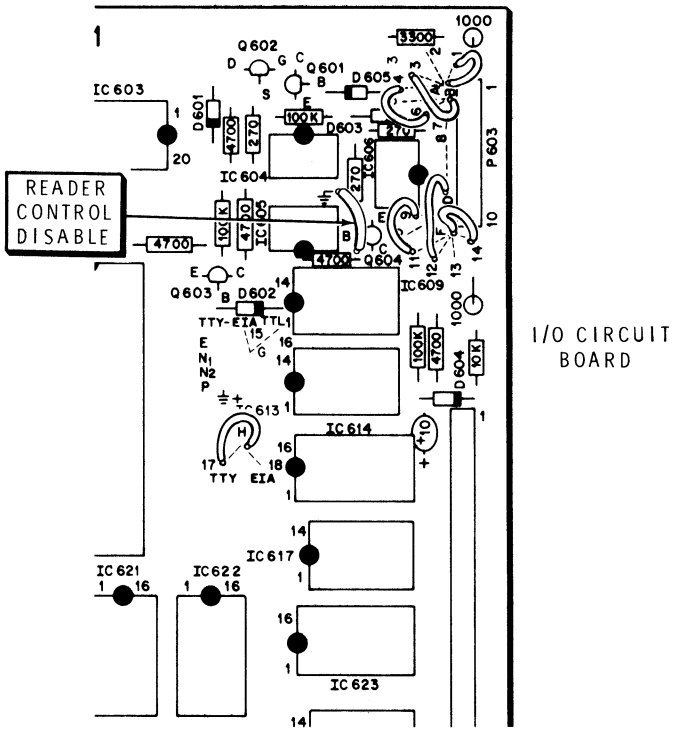
In the passive configuration, the 20 mA loop current is supplied by the external device. Pictorial 2-10 shows the jumper wires necessary for the TTY (passive) configuration on the I/O circuit board. A mark is defined as 20 mA flowing in the current loop. A space is defined as less than 4 mA flowing in the current loop. Pictorial 2-11 shows the partial schematic of the TTY (passive) wiring. The jumper wire that disables the reader control is shown in Pictorials 2-10 and 2-11. Refer to "Reader Control" on Page 18.

TTY (Passive) Connections



PICTORIAL 2-11

TTY (Active) Connections



PICTORIAL 2-12

Active

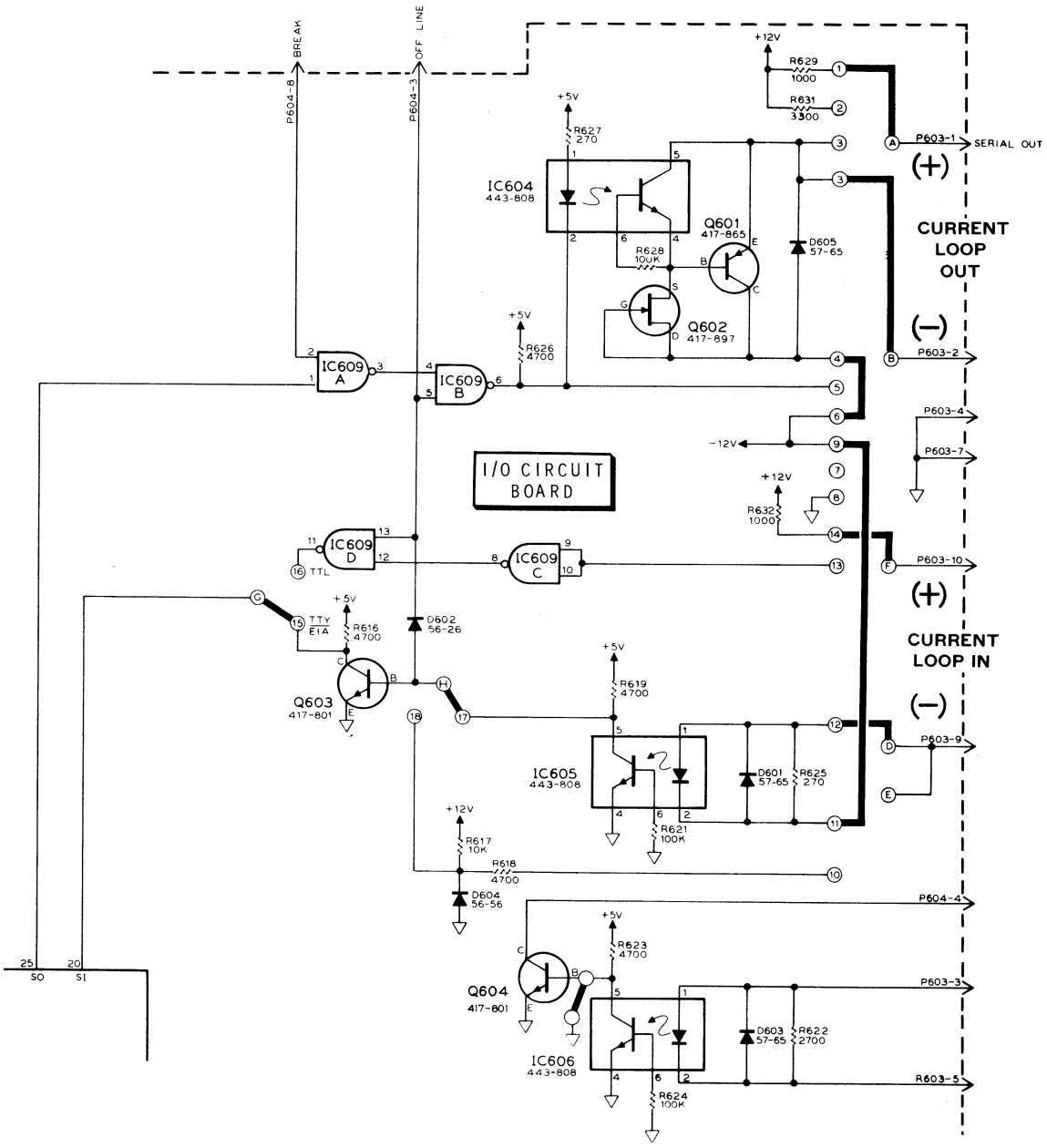
In the active configuration, the 20 mA loop current is supplied by the Terminal, usually through resistors R629 or R631. Pictorial 2-12 shows the jumper wires necessary for the TTY (active) configuration on the I/O circuit board. A mark is defined as 20 mA flowing in the current loop. A space is defined as less than 4 mA flowing in the current loop. Pictorial 2-13, Page 19 shows the partial schematic of the TTY (active) wiring. The jumper wire that disables the reader control is shown in Pictorials 2-12 and 2-13. Refer to "Reader Control" on this Page.

READER CONTROL

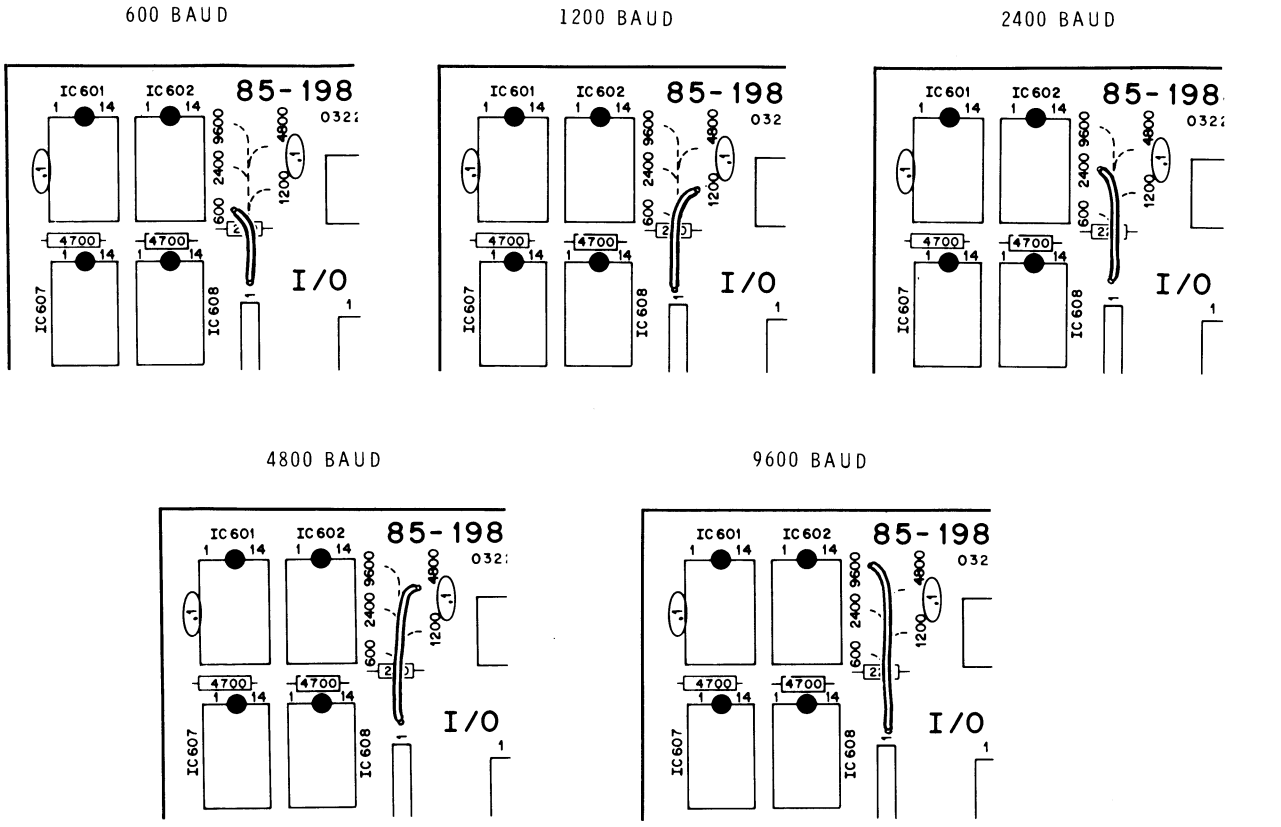
The reader control circuit is a serial handshake that allows a computer to control a paper tape reader through the Terminal Serial I/O. Normally, the reader control is accomplished by connecting the tape reader to the parallel I/O of the computer. If this is not possible, and if the computer has a spare serial port, the tape reader can be connected to the Terminal and controlled with the reader control current loop. A mark in the loop enables the reader; a space disables the reader.

If your system does not require this type of reader control (and most won't), the circuit must be disabled by connecting a jumper wire from the base (B) of transistor Q604 to ground (⏚).

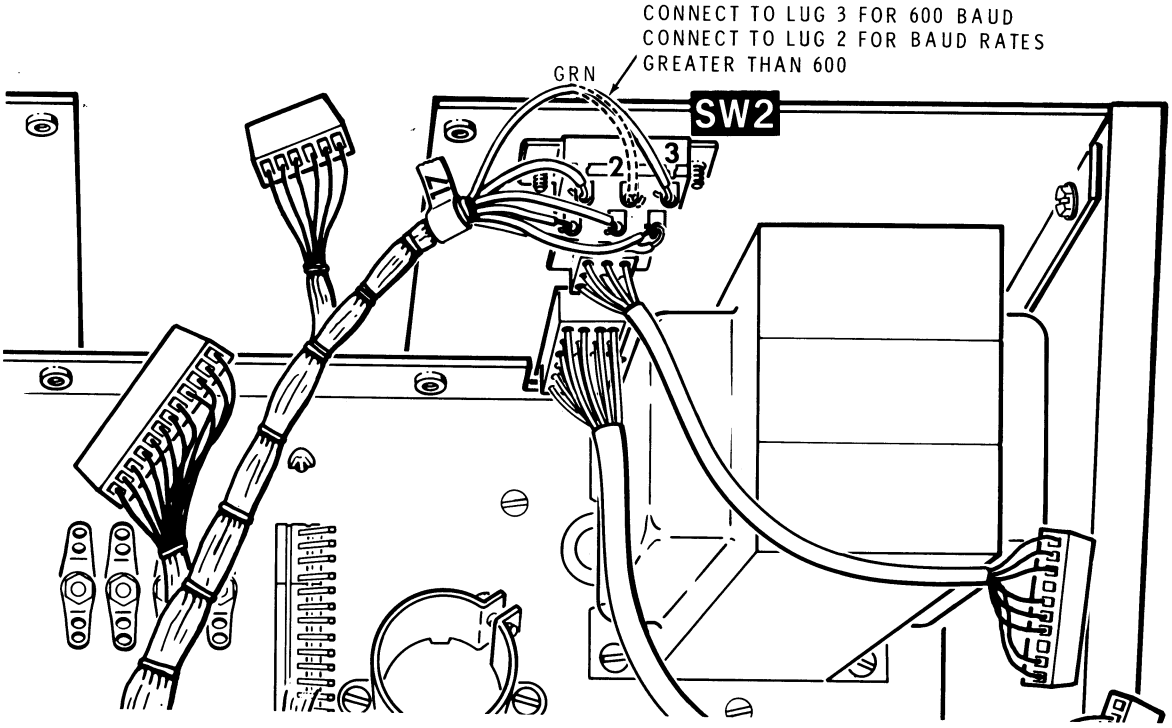
TTY (Active) Connections



PICTORIAL 2-13

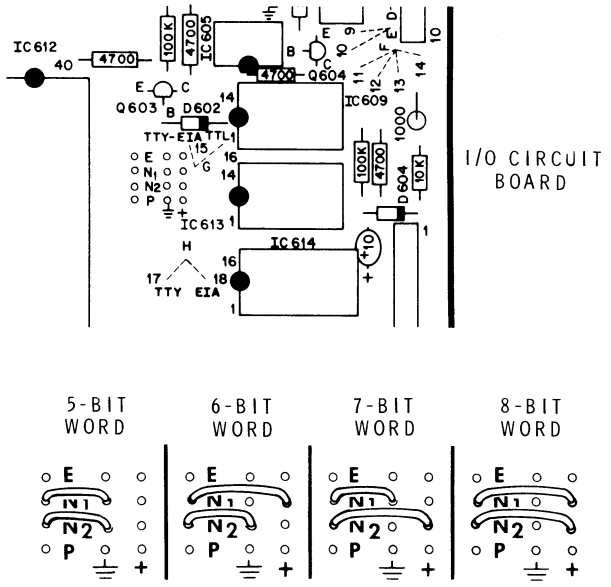


PICTORIAL 2-14



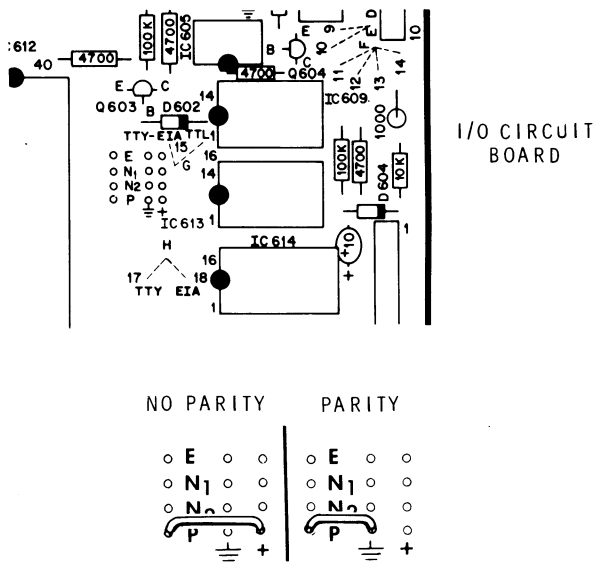
Detail 2-14A

Word Length



PICTORIAL 2-15

Parity



PICTORIAL 2-16

BAUD RATE

Pictorial 2-14 shows the jumper wire configuration for each of the five preset baud rates (600 to 9600). The baud rate that you select appears on the Baud Rate switch, SW2, on the back panel on the Terminal. This lets you select one of two baud rates, 300 baud or the rate that you programmed on the I/O circuit board.

NOTE: For baud rates greater than 600, refer to Detail 2-14A and move the green harness wire on switch SW2 lug 3 to lug 2. Be sure to solder this connection.

WORD LENGTH (N1, N2)

The number of bits per word is determined by the N1 and N2 inputs (pins 37 and 38) to the UART. The word length may be programmed for 5-, 6-, 7-, or 8-bits as shown below.

WORD LENGTH	N2 (pin 38)	N1 (pin 37)
5	0	0
6	0	1
7	1	0
8	1	1

The Terminal was initially wired for an 8-bit word. You can, however, change the word length to suit your particular application. To do this, remove the wires from the holes labeled N1 and N2 on the I/O circuit board. Then install wires to correspond to the word length you desire. Pictorial 2-15 shows how to connect jumper wires to select a 5-, 6-, 7-, or 8-bit word. The four holes directly above the ground symbol (⏚) connect to ground (logic 0). The four holes directly above the plus symbol (+) connect to the +5-volt supply (logic 1).

PARITY (P)

The UART (IC612) can be programmed to either generate a parity bit for the serial output or to eliminate the parity bit. A logic 1 on the P input (pin 35) to the UART eliminates the parity bit from the transmitted or received word. The stop bit (s) will immediately follow the last data bit. A logic 0 on the P input causes the UART to generate a parity bit.

The Terminal was initially wired for no parity. See Pictorial 2-16 (Illustration Booklet, Page 5). This occurs when a wire is connected between holes P and + on the I/O circuit board. The parity bit is **not** used with the H9 system. However, if your own special application requires the parity bit, connect a wire between holes P and ⏚ .

ODD/EVEN PARITY (E)

This input (E) to the UART selects the type of parity that is checked by the receiver and generated by the transmitter if parity was selected as explained above. A logic 0 on the E input (pin 36) will insert odd parity immediately after the data bits. A logic 1 on this input inserts even parity immediately after the data bits. Since the Terminal does not use the parity bit, the E input is not connected. If your special application requires a parity bit, Pictorial 2-17 shows how to select odd or even parity.

KEYBOARD PROGRAMMING

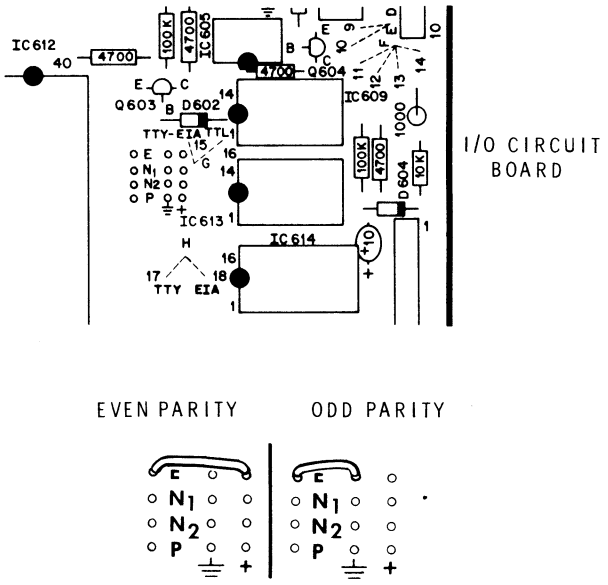
A jumper wire connection on the bottom of the keyboard circuit board lets you select one of four repeat rates; 3.7-, 7.5-, 15-, or 30-characters per second. This is the rate at which characters are written on the screen when the REPT (repeat) key and a character key are held down at the same time. Refer to the "Repeat Rate" instructions in the "Readjustment" section of this Manual if you want to change the repeat rate.

TYPICAL TERMINAL/COMPUTER SYSTEMS

Parallel Input/Output Connections

The following parallel I/O connector chart describes the signal on each pin of the parallel I/O connector on the rear panel.

Odd/Even Parity



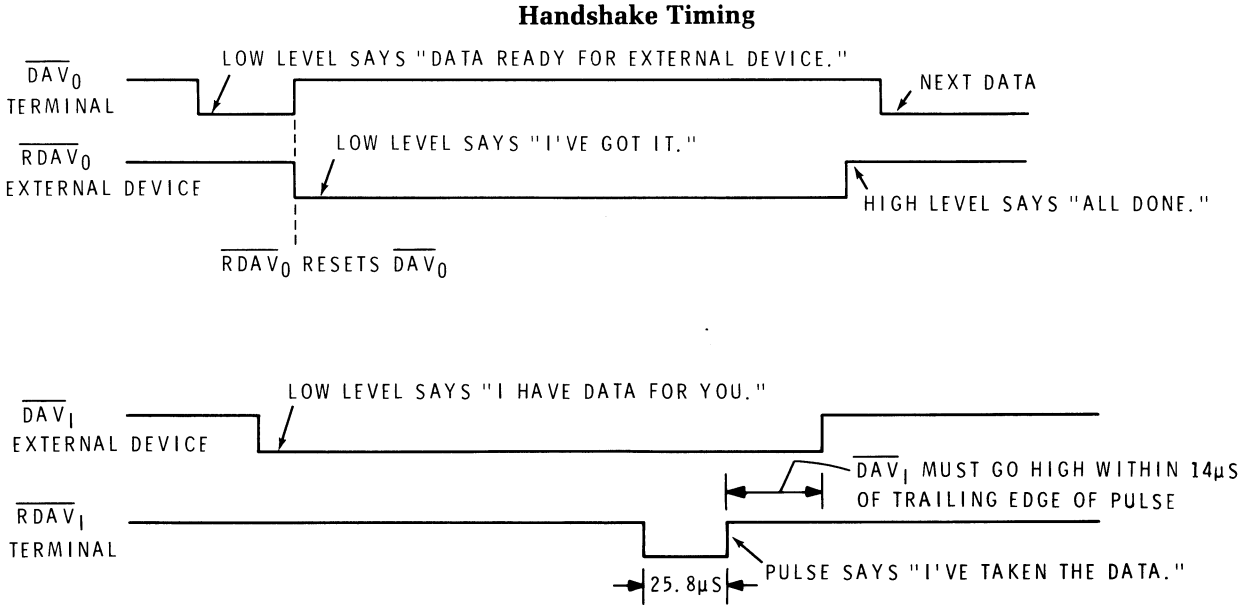
PICTORIAL 2-17

PIN #	DATA	DESCRIPTION	
1 2 3 4 5 6 7 8	Bit 1 Bit 2 Bit 3 Bit 4 Bit 5 Bit 6 Bit 7 Bit 8	Parallel Output	• Positive true logic. • High Level Output Voltage (V_{OH}) = 2.7 min. @ −400 μA (High Level Output Current). • Low Level Output Voltage (V_{OL}) = 0.4 V max. @ 4 mA (Low Level Output Current). • Standard 74LS175 latches.
9	$\overline{DAV_0}$	Take Data	• Output Data Available — Normally high. The Video Terminal will hold this line low to indicate that there is data available at the parallel output for the external device. • High Level Output Voltage (V_{OH}) = 2.7 V min. @ −400 μA (High Level Output Current). • Low Level Output Voltage (V_{OL}) = 0.4 V max. @ 4 mA (Low Level Output Current). • Refer to the "Handshake Timing" section.
10	— — —		

PIN #	DATA	DESCRIPTION	
11 12 13 14 15 16 17 18	Bit 1 Bit 2 Bit 3 Bit 4 Bit 5 Bit 6 Bit 7 Bit 8	Parallel Input	• Positive true logic. • High Level Input Voltage (V_{IH}) = 2 V min. • Low Level Input Voltage (V_{IL}) = 0.8 V max. • Low Level Input Current (I_{IL}) = −200 μA max. @ 0.4 V_{IL}. • Standard 74LS244 input buffer.
19	$\overline{RDAV_0}$	Data Taken	• Reset Output Data Available — Normally high. • The external device will pull this line low to indicate to the Terminal that it has received the data. The Terminal will not send new data until $\overline{RDAV_0}$ has returned high. • High Level Input Voltage (V_{IH}) = 2 V min. • Low Level Input Voltage (V_{IL}) = 0.8 V max. • Low Level Input Current (I_{IL}) = 2.8 mA max. • Refer to the "Handshake Timing" section.
20	$\overline{DAV_I}$	Data Sent	• Input Data Available — Normally high. The external device will pull this line low to indicate that there is data ready to be inputted to the parallel input. • High Level Input Voltage (V_{IH}) = 2 V min. • Low Level Input Voltage (V_{IL}) = 0.8 V max. • Low Level Input Current (I_{IL}) = 1.8 mA max. • Refer to the "Handshake Timing" section.
21	$\overline{RDAV_I}$	Data Received	• Reset Input Data Available — Normally high. The Terminal sends a negative-going pluse (≈ 25 μS wide) on this line to indicate to the external device that the Terminal has received and is finished with the data. • High Level Output Voltage (V_{OH}) = 2.7 V min. @ −400 μA (I_{OH}). • Low Level Output Voltage (V_{OL}) = 0.4 V max. @ 4 mA (I_{OL}). • Refer to the "Handshake Timing" section.
22	- - -		
23	- - -		
24	Ground		

Parallel Handshake Timing

Pictorial 2-18 shows the timing waveforms of the handshake signals associated with the parallel I/O port.



PICTORIAL 2-18

Serial I/O Connections

The following serial I/O connector chart describes the signals on each pin of the serial I/O connector on the rear panel.

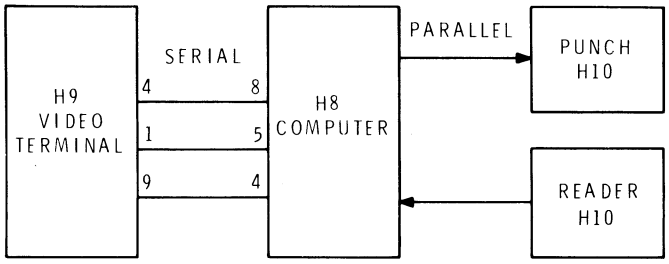
PIN #	SERIAL PORT NOMENCLATURE		
	TTY (ACTIVE AND PASSIVE)	EIA RS-232C	TTL
1	Serial Out (+)	Serial Out	—
2	Serial Out (−)	—	Serial Out
3	Serial In (+)	—	Serial In
4	Serial In (−)	Serial In	—
5	Reader Start (+)	—	—
6	Reader Start (−)	—	—
7	Baud Rate Out	Baud Rate Out	Baud Rate Out
8	- - -	—	—
9	Ground	Ground	Ground

Typical System

Pictorial 2-19 shows the typical interface (Heath Computer System Interface Standard) between the Video Terminal and a digital computer.

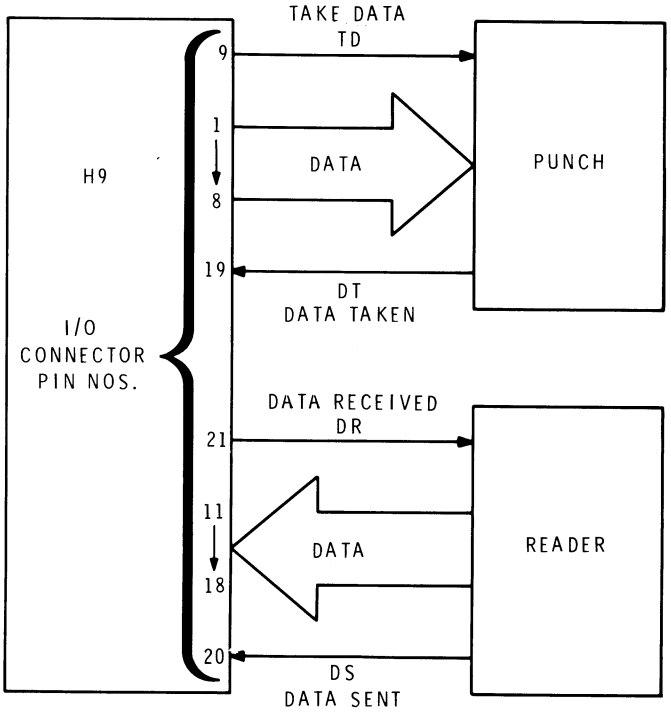
Pictorial 2-20 shows the typical I/O connections between the Video Terminal and a paper tape reader/punch.

Typical Computer Systems



PICTORIAL 2-19

Typical I/O Connections



PICTORIAL 2-20

READJUSTMENT

This section contains several adjustments that you may need to make to properly maintain your Video Terminal. Each of the adjustments (except for Brightness and Focus) can be adjusted separately without affecting other adjustments.

BRIGHTNESS

Adjust the display brightness to suit your own needs. A dim display is easier on your eyes when you look at the screen for extended periods of time. Whenever you change the brightness, it is also a good idea to readjust the focus.

The BRIGHTNESS control (on the video circuit board) is shown in Pictorial 3-1.

To adjust the brightness:

1. Remove the cabinet shell and set it aside.
2. Fill the screen with characters.
3. Adjust the BRIGHTNESS control to obtain a desirable character brightness.
4. Reinstall the cabinet shell.

FOCUS

The focus adjustment, which should be made whenever the brightness is readjusted, assures distinct characters on the screen.

The FOCUS control (on the video circuit board) is shown in Pictorial 3-1.

To adjust the focus:

1. Remove the cabinet shell and set it aside.
2. Fill the screen with characters.
3. Adjust the FOCUS control to obtain the best focus. Look at the characters at the edges and corners of the screen as you make this adjustment.
4. Reinstall the cabinet shell.

CENTERING

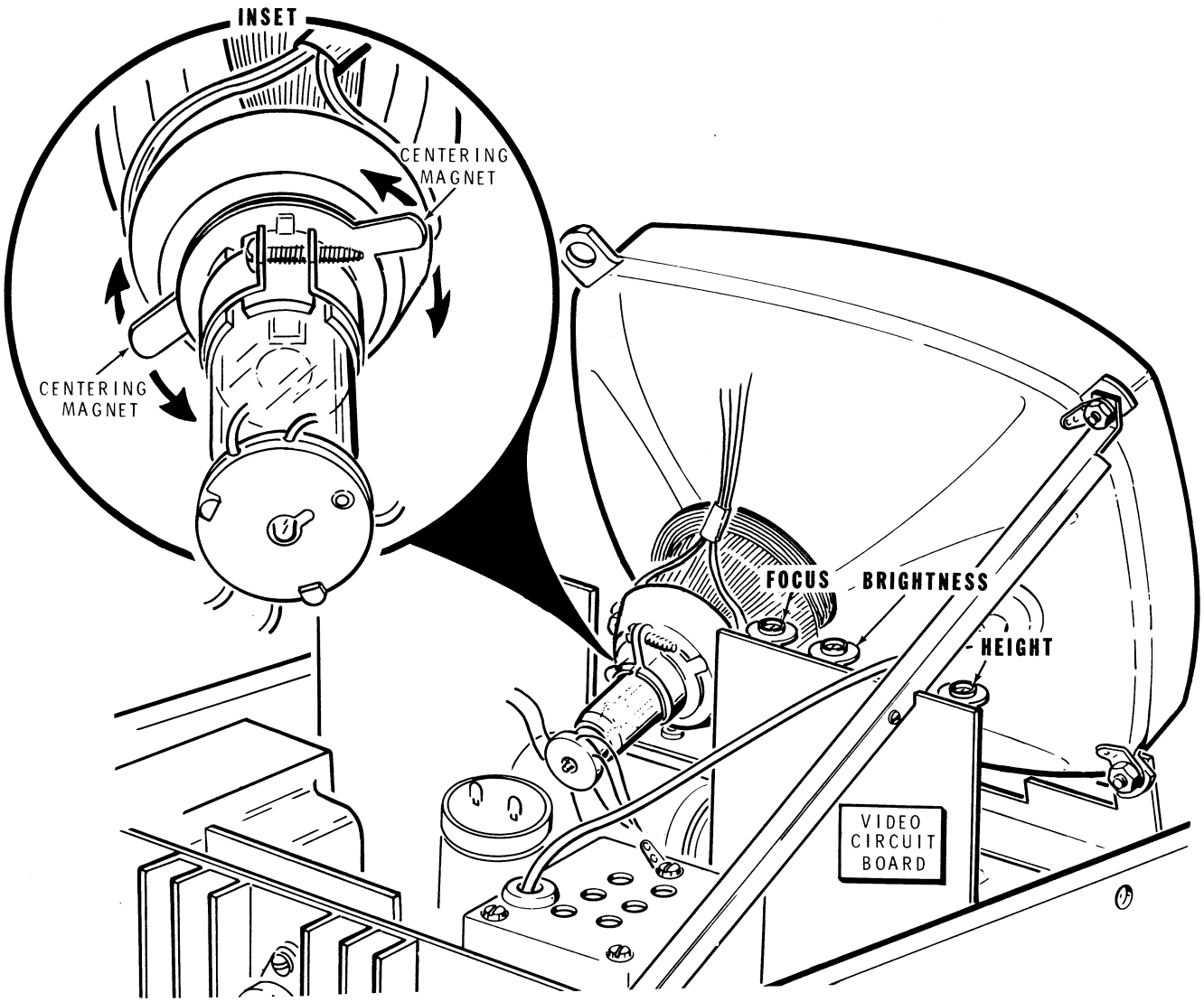
The display should be centered on the screen. It should have the same amount of space on the right as it does on the left, and the same amount of space on the top as it does on the bottom.

To adjust the centering:

1. Remove the cabinet shell and set it aside.
2. Fill the screen with characters.

NOTE: Use an insulated screwdriver and be careful you do not touch the video circuit board or the anode lead when you make the following adjustments.

3. Refer to Pictorial 3-1 and rotate the centering magnets, first one, then the other, to center the display on the screen. Because the centering magnets will affect the vertical and horizontal linearity of the display, use the minimum amount of correction (magnet tabs spread as far apart as possible) that is necessary. Sometimes you will have to compromise between perfect centering and perfect linearity.
4. Reinstall the cabinet shell.



PICTORIAL 3-1

HEIGHT

The exact height of the display is not critical. However, the dots that form the characters become more apparent on a large display. A small display provides sharper, more distinct characters.

The HEIGHT control (on the video circuit board) is shown in Pictorial 3-1.

To adjust the height of the display:

1. Remove the cabinet shell and set it aside.
2. Fill the screen with characters.
3. Turn the HEIGHT control through its range while you watch the display. Leave the control at the position that provides the most appealing display. If you prefer a large display, make sure all twelve character lines appear on the screen.
4. Reinstall the cabinet shell.

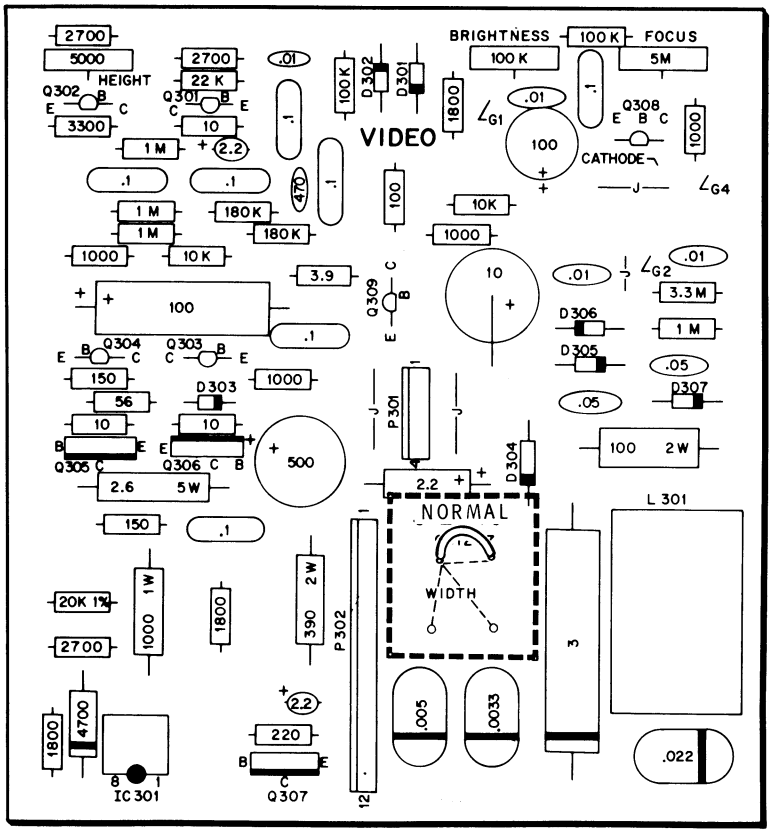
WIDTH

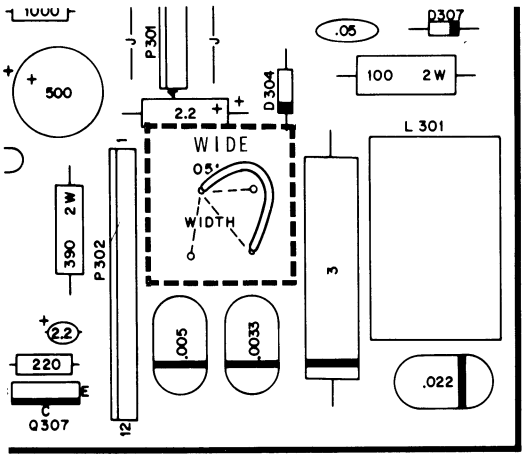
A width jumper wire on the video circuit board can select one of three display widths; normal, wide, and extra wide. Pictorial 3-2 shows the jumper wire connection for each of these settings. The width of the display should normally be about 1/2" - 1" from the right and left sides of the screen. In most cases, the normal setting will provide adequate width. The wide and extra wide settings are usually required only in low line voltage areas.

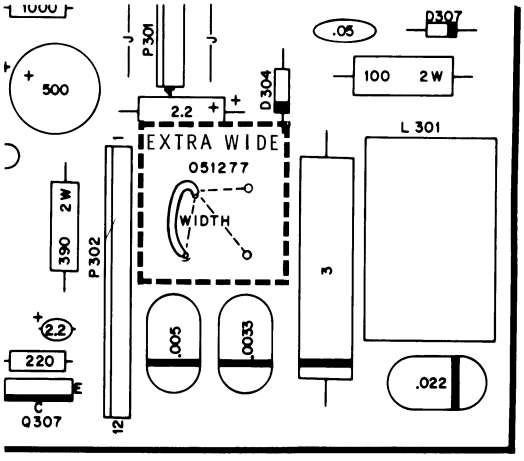
WARNING: There is high voltage present on the video circuit board. DO NOT attempt to change the width jumper when the power is turned on.

To change the display width:

1. Turn the ON/OFF switch to OFF.
2. Remove the cabinet shell and set it aside.
3. Remove the video circuit board from the chassis.
4. Pull the jumper wire out of the connector pin.
5. Insert the jumper wire into the connector pin that corresponds to the width you desire.
6. Reinstall the circuit board in the chassis.
7. Reinstall the cabinet shell.







PICTORIAL 3-2

REPEAT RATE

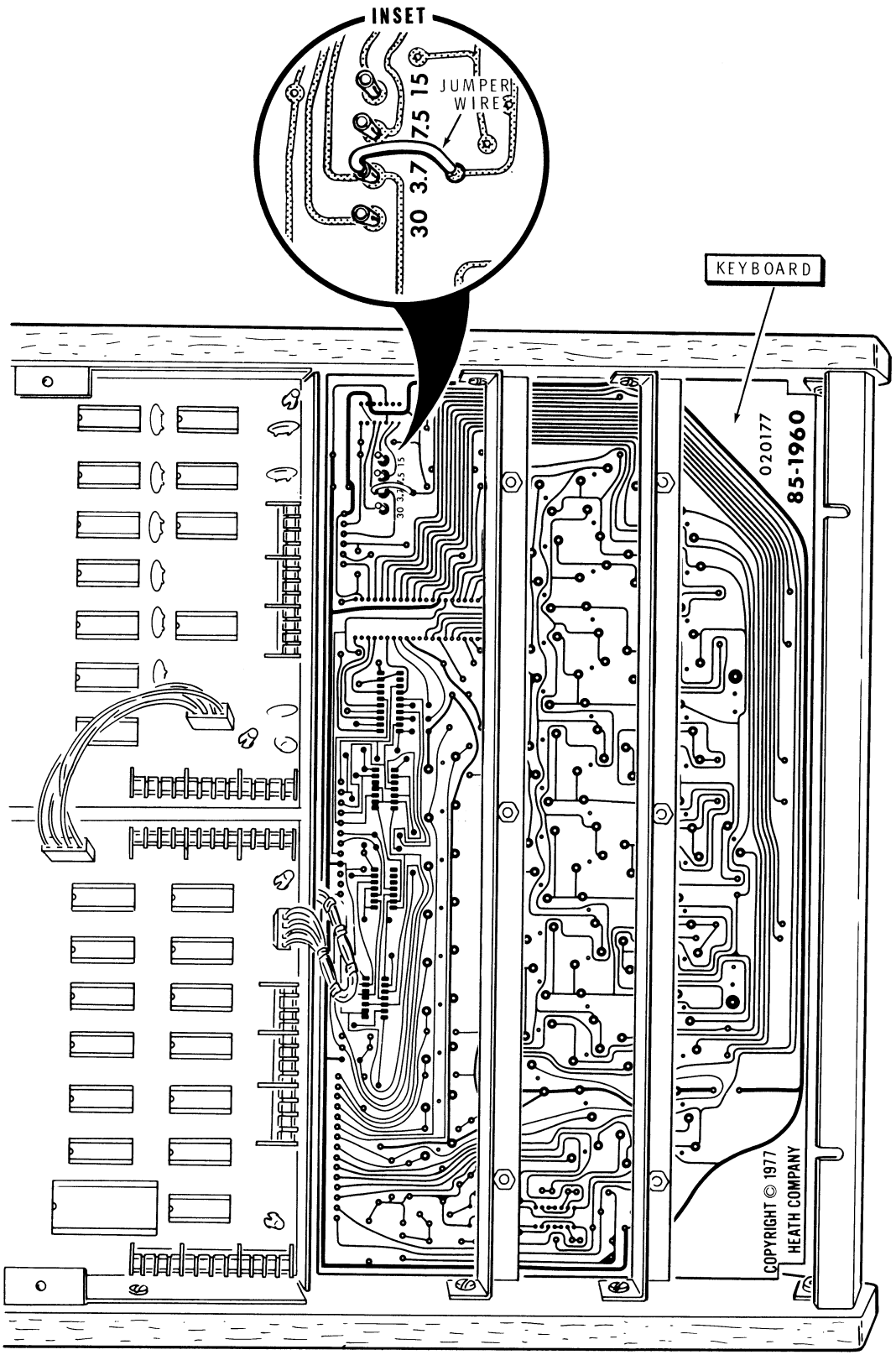
When the REPT (repeat) key and any character key are held down at the same time, the character is repeatedly written on the screen. The repeat rate can be set at 3.7, 7.5, 15, or 30 characters per second. Pictorial 3-3 shows the jumper wire connection (on the bottom of the keyboard circuit board) for each of the repeat rates. You may want to try all of the repeat rates to determine which one best suits your needs.

To change the repeat rate:

1. Turn the ON/OFF switch OFF.
2. Remove the bottom panel and set it aside.
3. Pull the jumper wire out of the connector pin.
4. Insert the jumper wire into the connector pin that corresponds to the repeat rate you desire.
5. Reinstall the bottom panel.

CLEANING

You can use any mild household detergent and a soft cloth to clean the cabinet of the Video Terminal. Wipe the dust from the window with a soft cloth. If smudges still remain, clean the window carefully with a mild soap and a soft cloth. Be careful you do not scratch the plastic window.



PICTORIAL 3-3

SPECIFICATIONS

CRT	12″ diagonal, P4 phosphor. Glare-free neutral front panel filter.
Display Format	960 characters. Normal mode — 12 lines of 80 characters. Short form — 48 lines of 20 characters.
Keyboard	67 keys including: 52-key ASCII keyboard 5 cursor control keys 10 special function/mode keys
Interfaces	Serial (full or half duplex): EIA/RS-232C TTY (20 mA current loop) TTL Reader Control (20 mA current loop) Parallel (TTL loads): 8-bit input 8-bit output 4 handshakes
BAUD Rates	Seven, user selectable — 110, 300, 600, 1200, 2400, 4800, and 9600.
Characters	5 × 7 dot matrix. ASCII upper case alphabet, numbers, and punctuation.
Operating Temperature	0° to 40°C.
Power Requirements	120 VAC, 50/60 Hz, 50 watts. 240 VAC, 50/60 Hz, 50 watts.
Voltage Requirements	120 VAC (100 — 135 VAC), 50/60 Hz. 240 VAC (200 — 270 VAC), 50/60 Hz.
Dimensions	15-5/8″ W × 20-3/4″ D × 12-1/2″ H. (39.7 × 52.7 × 31.8 cm.)
Weight	32 lbs. (14.5 kg).

The Heath Company reserves the right to discontinue instruments and to change specifications at any time without incurring any obligation to incorporate new feautres in instruments previously sold.

TROUBLESHOOTING

This section of the Manual is divided into four parts. The first part, titled "General Troubleshooting Information," describes what to do about difficulties that may occur during or right after you assemble the Terminal.

The second part, titled "Troubleshooting Charts," lists problems or conditions that might occur. The "Possible Cause" column lists the components associated with the problem. In many cases, the name of the circuits involved with the problem are also given. this will help you relate a problem to the Schematic and Circuit Description.

The third section, titled "Troubleshooting Waveforms," provides several important waveforms and their respective test points. If the CRT screen is blank, always check the horizontal and vertical sync waveforms.

The fourth part, titled "Shipping Information," explains how to prepare your Terminal for shipping.

Refer to the "X-Ray Views" for the physical location of parts on the circuit boards.

General Troubleshooting Information

NOTE: The following checks will be most effective if you apply them to one part of the kit at a time.

1. Recheck the wiring. Trace each lead in colored pencil on the Pictorial as it is checked. It is frequently helpful to have a friend check your work. Someone who is not familiar with the unit may notice something you have consistently overlooked.

2. About 90% of the kits that are returned for repair do not function properly due to poor connections and soldering. Therefore, many troubles can be eliminated by a careful inspection of connections to make sure they are soldered as described in the "Soldering" information at the beginning of the Assembly manual. Reheat any doubtful connections. Be sure all wires are soldered at places where several wires are connected.

3. Check each circuit board foil to be sure there are no solder bridges between adjacent connections. Remove any solder bridges by holding a clean soldering iron tip between the two points that are bridged until the excess solder flows **down** onto the tip of the soldering iron.

4. Check each resistor value carefully. A resistor that is discolored, or cracked, or shows any sign of bulging would indicate that it is faulty and should be replaced.

5. Be sure each diode is installed with the banded end positioned correctly.

6. Check all component leads connected to the circuit boards. Make sure the leads do not extend through the circuit board and come in contact with other connections or parts.

7. The components listed in the "Possible Cause" column of the "Troubleshooting Chart" are the most likely causes (but not necessarily the only causes) of a problem. When you check these components, look first for the following items:

   — Parts installed incorrectly or backwards. This pertains especially to diodes, electrolytic and tantalum capacitors, and transistors.

   — Unsoldered or inadequately soldered parts. Reheat the connections in the area of a problem.

   — Incorrect or interchanged parts. Check the part numbers on the diodes and transistors.

NOTE: In an extreme case where you are unable to resolve a difficulty, refer to the "Customer Service" information inside the rear cover of the Manual. Your "Warranty" is located inside the front cover.

TROUBLESHOOTING CHARTS

POWER SUPPLY PROBLEMS

CONDITION	POSSIBLE CAUSE
1. Nothing happens at turn on.	1. Terminal not plugged in. 2. Fuse F1 blown. 3. Primary/line cord wiring. 4. Switch S1 wiring. 5. Fuseholder wiring. 6. Power transformer T1.
2. Fuse blows.	1. Check primary wiring. 2. Short circuit on the power supply circuit board. 3. Short circuit across transformer secondary. 4. Shorted rectifier diodes. D101-D112. 5. Check for shorts at the outputs of the bridge rectifiers. C1, C2, and C105. 6. Shorted regulators. IC101, IC102, IC103. 7. Check for a short between the collector of Q101 and the heat sink. 8. Incorrect fuse. 9. Power transformer. 10. Shorted regulator outputs. P101-1, -2, -3, -4, -5, & -11.
3. No 5-volt output or 5-volt supply incorrect (too high or too low).	1. IC101, IC102. 2. D101 — D104. 3. C1. 4. +5-volt reference ⏚ (ground) not grounded at P101-6.
4. No +12 volts, or it measures too high or too low.	1. If the +26-volt supply is below +15 volts, the +12-volt supply will also be low. 2. If the 26-volt supply is OK, check IC104 and the +12-volt reference ground.
5. No −12 volts, or it measures too high or too low.	1. IC105. 2. R105 and R106 interchanged or wrong values. 3. D109 — D112. 4. C107 installed backward. 5. −12-volt reference ground not grounded at P101-6.
6. No +26 volts, or it measures too high or too low.	1. IC103. 2. R103 and R104 interchanged or wrong value. 3. Q101, Q102. 4. D105 — D108. 5. +26-volt reference ground not grounded at P101-12.
7. No +36 volts, or it measures too high or too low.	1. C2. 2. D105 — D108. 3. Transformer T1.
8. No anode voltage when other voltages are OK. **CAUTION:** Measure the high voltage only with an approved high voltage probe.	1. Flyback transformer T2. 2. Q1, Q307. 3. IC301. 4. L301, deflection yoke. 5. Shorted foil on the video circuit board.

CONDITION	POSSIBLE CAUSE
9. −150 volts is incorrect.	1. D304. 2. C323.
10. +400 volts is incorrect.	1. R335. 2. D305 — D307. 3. C324 — C327.

VIDEO RELATED PROBLEMS

CONDITION	POSSIBLE CAUSE
11. No video (blank screen).	1. Anode voltage incorrect. 2. Grid voltages incorrect (G1, G2, G4). 3. No cathode drive. 4. Q308, Q309. 5. IC222A ($\overline{\text{video}}$ out of character generator circuit board). 6. Video/blanking chain on the character generator circuit board. 7. Brightness control R338 turned down. 8. IC217A (blanking in).
12. Screen all white (raster).	1. Check grid voltages. 2. Q308 or Q309 shorted. 3. IC222A. 4. Video/blanking chain on the character generator circuit board. 5. Brightness control R338 turned up.
13. Insufficient brightness or contrast.	1. Q308, Q309. 2. R342, R343. 3. C328, C329. 4. Check grid voltages.
14. A single bright horizontal line appears on the screen.	1. Vertical amplifier. 2. Deflection yoke (vertical). 3. Q301 — Q306. 4. IC221A (V sync) on the character generator circuit board. 5. IC216 (sync/frame counter) on the character generator circuit board.
15. Too much or too little height.	1. Height control R303 misadjusted. 2. Q301, Q302. 3. C303 wrong value or installed backward.
16. Too much or to little width.	1. Adjust width jumper. 2. C321. 3. Deflection yoke or L301. 4. Flyback transformer T2.
17. No horizontal sync.	1. R325. 2. C312, C314. 3. IC301, IC211A.
18. No vertical sync.	1. IC221A. 2. Q301.

CHARACTER WRITING PROBLEMS

CONDITION	POSSIBLE CAUSE
19. Characters don't write on the screen.	1. Duplex switch in "full" position when it should be in "half". 1. DAV latch (IC616) — No DAV signal. 3. DAV priority encoder (IC611A, C, D, IC610D, IC619B). 4. Three-state enables (IC608B, C, D). 5. RAM $\overline{WE}$. OC if DAV timing pulse (IC737A). 6. RAM $\overline{CS}$. OC if DAV timing pulse (IC719B, D). 7. DAV from IC719C, IC725A, IC713C. 8. Special character generator IC404, IC405, IC406 latched on (A1 or A2 high).
20. Wrong characters write on the screen.	1. Keyboard encoder IC402. 2. Keyboard buffer IC403. 3. Bus wires interchanged. 4. Bus wires shorted to + or ground. 5. Bus buffers IC603, IC620. 6. Shorted bus foil. 7. BAUD rate set wrong.
21. Screen filled with same character.	1. RAM counters not counting: IC722C, D. IC502. IC219F, IC217D. 2. Keyboard output enable always on: P402-8 always logic 0. Check DAV latch and three-state enables IC616, IC608, IC610, IC619. 3. Parallel input enable always on: Check items listed under 2 above. 4. UART $\overline{RDE}$ enable always on: Check items listed under 2 above.
22. Same line is repeated 12 times.	1. ÷12 counter not counting up. 2. IC519, IC511C, IC515B, IC716A, IC715C.
23. Blocks of characters are repeated left to right.	1. ÷4 counter not counting. 2. IC513, IC514B, IC510C.
24. Writes two characters.	1. Full Duplex key set for half duplex (released) instead of full duplex (pushed in).
25. Characters write erratically.	1. Wrong baud rate.
26. Misses characters coming from the computer.	1. Refresh interrupt not enabled at the rear panel baud rate switch. Connect the green wire to lug 2 of SW2 (for BAUD rates greater than 600). 2. At 110 baud, the computer may not be programmed for two stop bits.
27. Characters write in more than one position on the screen.	1. Address encoder. IC512, IC526A, IC526D, & IC527B. 2. RAM address lines shorted or open. 3. Counters not counting up (see "Conditions 22 & 23" above). 4. Check the counter cascade controls. IC730, IC724 (÷20 → ÷4, ÷4 → ÷12, ÷20 → ÷12, etc).
28. Writes control characters.	1. Control character decoder. IC703C, IC703B, IC707C, and IC702. 2. Control character detector. IC617A.

CONDITION	POSSIBLE CAUSE
29. Writes wrong character from keyboard.	1. Shorts between the X and Y scan and address lines of the keyboard encoder. IC402. 2. IC402, IC403.
30. Cannot write from the keyboard.	1. No output enable (OE). IC608D, IC611D, IC619B, IC616. 2. Keyboard bus harness plug P402 disconnected.
31. Control characters do not blink in plot mode.	1. No 3.75 Hz. IC741D, IC401. 2. Control character video/decoder. IC201A, IC207B, IC210D, IC219D.

CURSOR PROBLEMS

CONDITION	POSSIBLE CAUSE
32. No cursor.	1. Cursor coincidence gate. IC503, IC508, IC520. 2. TPU cursor gates. IC710C, IC710D. 3. Character generator cursor chain. IC202, IC201C, IC208A, IC218B.
33. No cursor movement when characters are written on the screen.	1. No ÷20 count up. IC734B (1C if DAV), IC722B, IC729A. 2. ÷20 counter. IC502. 3. ÷20 count up defeated. IC708D, IC720, IC729A.
34. Cursor controls will not move cursor.	1. IC727. 2. No 1C pulse. IC728. 3. Cursor movement latches on the keyboard. IC407, IC408. 4. Q401.
35. Cursor moves continuously.	1. Cursor movement latches not being reset. IC407, IC408. 2. Make sure TPU cycle ⌐3⌐ resets all four latches. IC407, IC408.
36. 960 cursors.	1. IC710C. 2. Character generator cursor chain. IC201C, IC202, IC208A, IC218B.
37. Wrong cursor movements from cursor controls.	1. S701 plugged in backward. 2. Wires in plug S701 interchanged.
38. Wrong cursor movements from ASCII data.	1. Special character movement circuits. IC703A, IC703B, IC703D, IC707C, IC720, IC740B, IC740C, IC740D, IC721C, IC721D, IC708D.
39. Cursor won't home.	1. Cursor home switch. 2. Cursor latch enable. IC728. 3. Cursor latches. IC501, IC518, IC512. 4. Select, select cursor, or select scroll lines. IC706A, IC711D, IC734A, IC504A, IC505D, IC529B, IC529C, IC511C, IC524A, IC524B, IC524C, IC504D, IC517C, IC517D, IC528A, IC528B.
40. Cursor moves on control characters or rubouts when the Terminal is NOT in the plot mode.	1. Control character detector. IC617A. 2. Rubout detector. IC613. 3. CC+R decoder. IC703B, IC703C, IC797, IC702. 4. ÷20 count up defeat. IC708D, IC720, IC729A.

CONDITION	POSSIBLE CAUSE
41. Multiple cursor movements.	1. Cursor movement latches on the keyboard circuit board. IC407, IC408, Q401.
42. Cursor does not blink for hold screen.	1. No 3.75 Hz. IC401. 2. IC741C. 3. Cursor chain on character generator circuit board. IC202, IC201C, IC298A, IC218B.
43. No cursor movement on line feed, carriage return, or back space (control H).	1. Special character detector. IC617A, IC614, IC623, IC617B, IC617C, IC617D, IC624C, IC624D. 2. Special character decoder. IC703A, IC703B, IC703C, IC704B, IC707C, IC702. 3. Special character latch. IC720, IC740C, IC740D, IC721C, IC721D, IC708D. 4. No 1C signal. IC728.
44. Cursor (or the blank line) moves to the wrong position after a scroll.	1. More than one scroll count up. IC506, IC522, IC724, IC730.
45. Cursor dosen't home following the erase page function.	1. IC723B, IC740A.

I/O PROBLEMS

CONDITION	POSSIBLE CAUSE
46. No serial input or output (general).	1. Serial cable incorrectly wired. 2. I/O circuit board not jumper wired for the proper serial configuration. 3. Wrong baud rate. 4. No baud rate. IC601, IC602, IC607, IC608A. 5. UART IC612. 6. UART pins NP, NB1, NB2, or EPS incorrectly wired (jumpers). 7. Off Line key pushed in. 8. Reader start must be operative (Q604 must have the base grounded or current must be flowing in the reader start loop).
47. No serial EIA input.	1. Jumper wires incorreclty installed. 2. D604, D602 installed backward. 3. Q603. 4. Check the DAV output of IC719C (DAV'), IC725A, IC713C.
48. No TTY input.	1. Jumper wires incorrectly installed. 2. D603, D602 installed backward. 3. Q603. 4. Check the DAV output of IC719C (DAV'); IC725A, IC713C.
49. No TTL input.	1. Jumper wires incorrectly installed. 2. IC609C, IC609D. 3. Check the DAV output of IC719C (DAV'), IC725A, IC713C.
50. No input from parallel or UART.	1. Terminal in hold screen mode. IC615B, IC615D. 2. Plug P601-23 shorted to ground.

CONDITION	POSSIBLE CAUSE
51. No EIA output.	1. Jumper wires incorrectly installed. 2. Off Line or Break keys pushed in. 3. IC609A, IC609B, IC604. 4. Q601, Q602. 5. D605 installed backward.
52. No TTY output.	1. Jumper wires incorrectly wired. 2. Off Line or Break key pushed in. 3. IC609A, IC609B, IC604. 4. Q601, Q602. 5. D605 installed backward.
53. No TTL output.	1. Jumper wires incorrectly installed. 2. Off Line or Break key pushed in. 3. IC609A, IC609B.
54. No parallel input or output (general).	1. Check all handshakes: $\overline{DAV_O}$ — IC618B, IC624A, IC702. $\overline{DAV_I}$ — IC610A, IC615D, $\overline{Hold\ screen}$. $\overline{RDAV_O}$ — From the external device. $\overline{RDAV_I}$ — IC610B, IC615A, IC615B, IC618A, IC619C, IC624B. 2. Check the data priority latch and encoder. IC615B, IC616, IC611, IC610D, IC619B, IC608B, IC608C, IC608D. 3. Check for defective or incorrectly wired interconnect cables.
55. No parallel input.	1. Input buffer. IC620, IC608C. 2. XBE' IC707A, IC713A. 3. IC702.
56. No parallel output.	1. Output latches. IC621, IC622. 2. Load parallel signal from IC702. 3. Check the handshakes (see item 54 above). 4. XBE' IC707A, IC713A. XBE' is generated from the UART TBMT (XBE_u), parallel $\overline{RDAV}$ (XBE_p), and reader control. All three signals must be high for XBE'.
57. No handshake.	1. Check handshakes (see item 54 above).
58. No echo back on full duplex.	1. Computer not set for echo back. 2. No serial input.
59. Stays off line or won't go off line.	1. Off Line switch on the keyboard. 2. IC609B, IC609D. 3. Q603. 4. D602 defective or installed backward.
60. Reader start doesn't work.	1. Install a jumper from the base to ground of Q604 if there is no external current loop. 2. D603 installed backward. 3. IC606, IC707A, IC713A. 4. Q604.
61. Wrong baud rates even if the Terminal is programmed correctly.	1. IC601, IC602, IC607A, IC608A. 2. 4800/9600 baud lines interchanged in harness P601-2, P601-3.
62. No baud rate output.	1. Check item 61 above. 2. IC607B, IC607C.

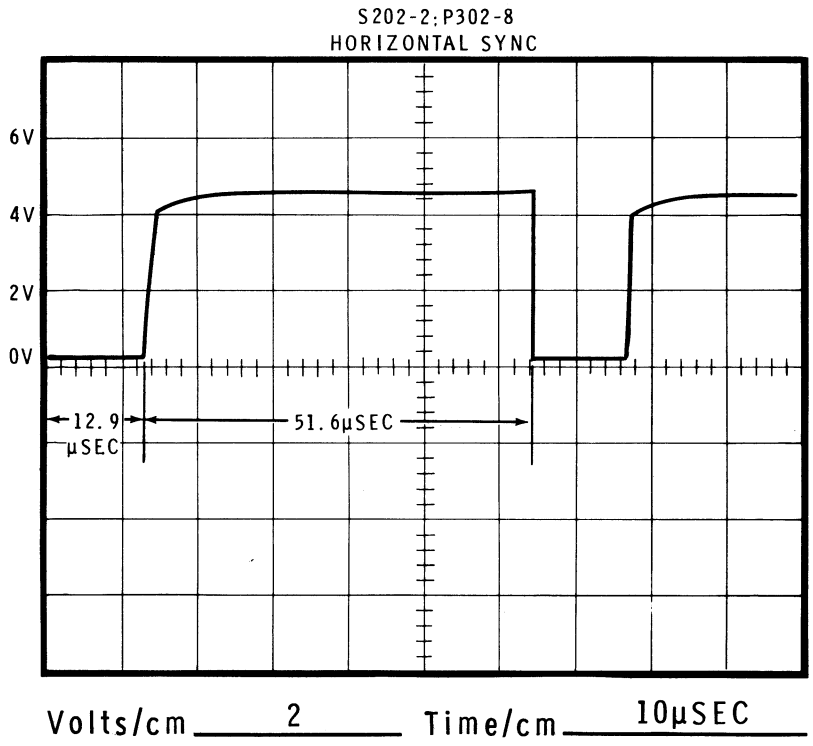
MISCELLANEOUS PROBLEMS

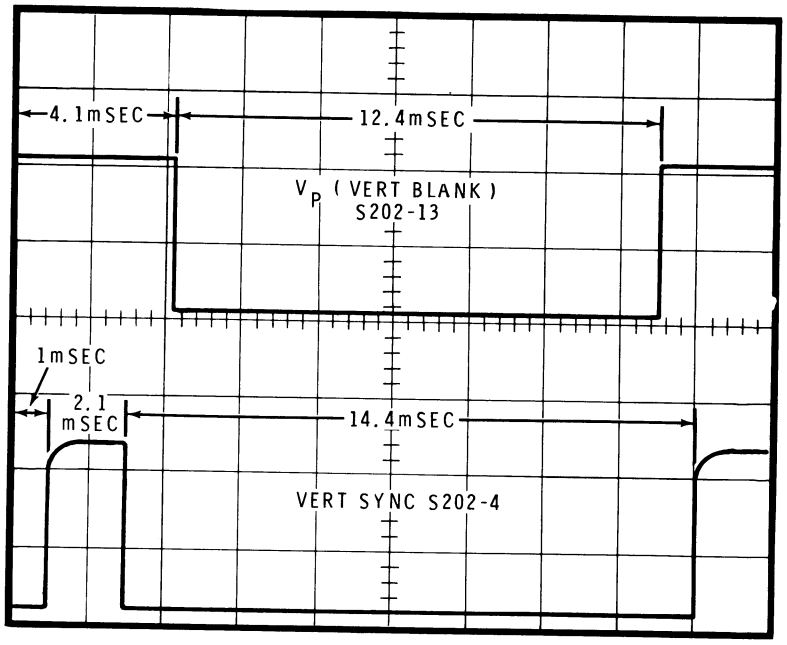
CONDITION	POSSIBLE CAUSE
63. No erase to end of line.	1. Space generator on the keyboard (special character generator). IC404, IC405, IC406. A1= 0, A2= 1 for a space. 2. Erase flip-flop is not being set. IC737D, IC723A. 3. A write is not turning on the space (A2) or enabling RAM WE. IC737A, IC737C, IC717F, IC726A. 4. RAM counter is not counting up on erase. IC722C, IC737B.
64. No erase page.	1. Check the items in condition 63 above. 2. Erase filp-flop is not being set by IC715A.
65. Erase continues forever (blank screen).	1. Erase flip-flop IC723A is not being cleared. 2. IC730 or timing signals.
66. No scroll.	1. Scroll key not pushed in. 2. Cursor/scroll coincidence is not being clocked into IC709B. IC733A, IC733B, IC705C, IC710B. 3. ÷12 or ÷4 count up not being clocked into IC709A. IC735A, IC735B, IC735D. 4. Scroll logic. IC715B, IC739, IC733C, IC733D, IC741A, IC741B, IC742C.
67. No erase on scroll.	1. IC722A not setting erase flip-flop. 2. Check the items in condition 64 above. 3. IC724 (since the same pin of IC724 controls both the scroll count up and the scroll erase, IC724 is OK if either the scroll count up or the scroll erase work).
68. The erased line, the erased block, or the cursor move to the wrong position after a scroll operation.	1. No scroll count up. IC506, IC522. 2. No count up scroll ÷4/scroll ÷12 signal from IC724 (since the same pin of IC724 controls both the scroll count up and the scroll erase, IC724 is OK if either the scroll count up or the scroll erase work). 3. The 47 Ω resistor between plug G pin 5 and plug C pin 5 on the chassis is missing.
69. Scrolls regardless of the position of the Scroll key.	1. Scroll key. 2. Scroll logic (see condition 66 above).
70. No short form.	1. Short Form key. 2. Counter controls. IC724, IC730. 3. Counter multiplexers on the RAM and counter circuit board: IC514A, IC514D (÷20 → ÷12). IC530A, IC530D (÷12 → ÷4). 4. Check ÷20 counter. IC502, IC509, IC510B, IC510C.
71. No long form.	1. Short Form key. 2. Counter controls. IC724, IC730. 3. Counter multiplexers on the RAM and counter circuit board: IC514B, IC514C (÷20 → ÷4). IC511A, IC511C (÷4 → ÷12). 4. Check ÷20 counter. IC502, IC509, IC510B, IC510C.
72. No auto carry.	1. Auto Carry key not pushed in. 2. Counter controls. IC724, IC730. 3. Counter not counting up: No carry output from ÷4 (long form) IC515B, IC530B. No carry output from ÷20 (short form) IC510C. Counter multiplexers IC514, IC511A, IC511C, IC530A, IC530D, IC528D.

CONDITION	POSSIBLE CAUSE
73. No plot.	1. Plot key not pushed in. 2. No plot coincidence. IC206, IC209A, IC209B, IC209D, IC212, IC219A. 3. Plot video. IC210B, IC208A, IC218A. 4. IC221B, IC221C.
74. Plot line appears in wrong place.	1. Plot coincidence. IC206, IC209A, IC209B, IC209D. 2. Plot inverters. IC212, IC219A.
75. No repeat (characters or cursor).	1. IC401. 2. Vn' input to keyboard open. 3. D401. 4. Repeat Key.
76. No cursor repeat.	1. D401. 2. Q401. 3. R403.
77. No refresh interrupt.	1. No refresh interrupt signal. IC610C, P601-21, S703-3. 2. Rear panel Baud switch not wired correctly for > 600 baud. 3. IC705A, IC706B.
78. Screen blinks at low baud rates.	1. Rear panel Baud switch wired for > 600 baud. 2. IC705A.
79. No hold screen mode.	1. IC733C, IC733D, IC739A.
80. Locks up in hold screen mode.	1. IC739B, IC739D, IC739A, IC739C.
81. No transmit page.	1. XP flip-flop not being set. IC731C, IC731D, IC732C, IC732D. 2. 7C pulse. 3. No OB2XP load pulse. IC701A, IC701B, IC704A, IC702. No OB2 pulse into IC702. 4. Count up not happening: Duplex key in Full Duplex (pushed in) instead of Half Duplex (released). IC704. IC725A, IC719C (fake DAV).
82. Transmit page won't stop.	1. IC725B, IC721A. 2. Transmit page was started in the hold screen mode. Press and release the Scroll or Break keys to exit the transmit page mode.
83. No end of line bell.	1. End of line decoder. IC716B, IC716C, IC718A, IC735C. 2. Monostable IC736, R717, C717. 3. Speaker driver IC742A.
84. No bell from control G.	1. Bell detector on the I/O circuit board. IC617D, IC614, IC623. 2. IC724B. 3. Monostable IC736, R717, C717. 4. Speaker driver IC742A.
85. Screen is not erased when the Terminal is turned on.	1. Power up reset. Q701, IC717A, IC717B, IC717C, IC717D, IC717E, D701. 2. Erase circuit. IC715A, IC723A.
86. Cursor is moving when the Terminal is turned on.	1. Terminal is in transmit page mode. 2. XP flip-flop (IC731C, IC731D) did not get reset by the power up reset.

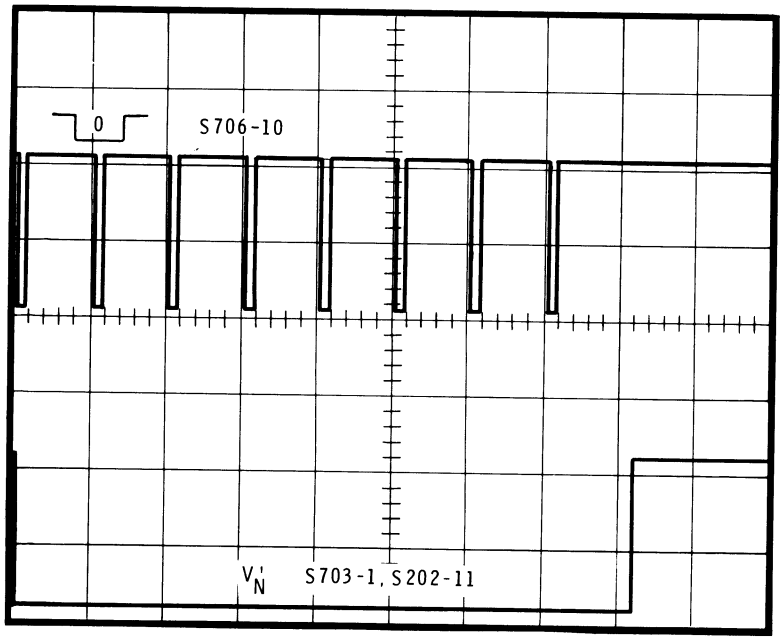
TROUBLESHOOTING WAVEFORMS

If you encounter a problem, check the following waveforms. Use a dual-trace oscilloscope to compare the time-related signals to the TPU timing signals. Timing Diagrams #1 - #4 (in the Illustration Booklet, Pages 3 through 6) and the Circuit Description will also help you understand the timing relationships of the Terminal functions.

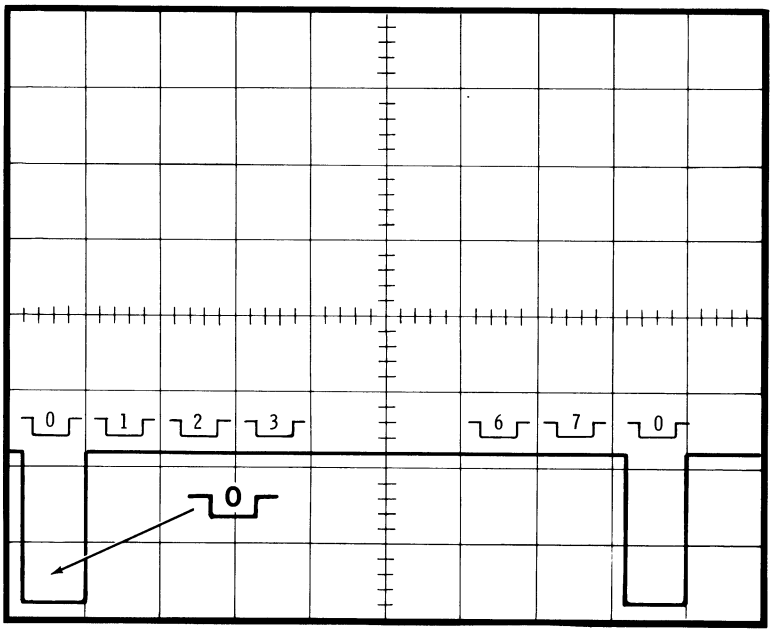




Volts/cm 2 Time/cm 2mSEC



Volts/cm 2 Time/cm .5mSEC



Volts/cm 2 Time/cm 50µSEC (UNCAL) See text

This is the basic troubleshooting waveform. It is triggered externally (EXT) from Vp (+ trigger) or from Vn' (– trigger). Decrease the horizontal sweep vernier until the trace appears as shown. This puts each TPU pulse (0 thru 7) in its own centimeter division (pulse 0 in the first division, through pulse 7 in the eighth division, then a repeat of pulse 0 in the ninth division, etc.). This lets you relate other timing sequences to the various TPU cycles. Refer to the TPU Schematic for the location of each TPU pulse test point.

SHIPPING INFORMATION

In an extreme case where you are unable to resolve a difficulty, you may want to take your Video Terminal to your local Heathkit Service Center or ship it to the Heath Company.

If you can isolate the problem to a particular circuit board, take (or send) only that circuit board for repair. This will save shipping cost and service expense.

Whenever possible, take your Video Terminal (or circuit board) to your local Heathkit Electronic Center for service. Consult your Heathkit Catalog for the locations of the Electronic Centers.

However, if it becomes necessary to ship the complete unit to the Heath Company, do it as follows:

1. Remove the cabinet shell. Do not send this part.
2. Remove the CRT from the chassis. Do not send this part. Store it where it will not get damaged.
3. Remove the angle brackets from the chassis (the brackets that support the top of the CRT). Do not send these parts.
4. Remove the Video circuit board and the I/O circuit board from the chassis. Carefully wrap these circuit boards to prevent them from being damaged.
5. Tape a small piece of cardboard over the speaker to protect the speaker cone.
6. Install all remaining panels, components, and hardware.
7. Refer to the "Customer Service" information inside the rear cover of the Manual and carefully pack the Video Terminal and the two circuit boards as instructed.

IMPORTANT: Include the following information with your Terminal. It will be helpful in diagnosing and repairing your unit.

a. The problem you are having.

b. Name and model of your computer system.

c. Name and model of the cassette recorder (if used).

d. Name and model of the paper tape reader/punch (if used).

e. Amount of memory.

f. Baud rate.

g. System configuration.

h. Any additional information that will help describe your system.

CIRCUIT DESCRIPTION

Refer to the Schematic Diagrams and to the Block Diagram (Illustration Booklet, Page 7) while you read this "Circuit Description."

To help you locate specific parts in the Terminal or on the Schematic, the circuit component numbers (R1, C101, L301, etc.) for resistors, capacitors, coils, transistors, and integrated circuits are in the following groups:

1-99	Parts on the chassis.
100-199	Parts on the power supply circuit board.
200-299	Parts on the character generator circuit board.
300-399	Parts on the video circuit board.
400-499	Parts on the keyboard circuit board.
500-599	Parts on the RAM and counter circuit board.
600-699	Parts on the I/O circuit board
700-799	Parts on the TPU circuit board.

Each of the circuits listed above will be described separately.

BASIC OVERVIEW

The Block Diagram shows how the Video Terminal can be divided into a series of functional blocks that coordinate the movement of data on an 8-bit ASCII bus. These blocks, which include the character generator, the RAM and counter, the keyboard, and the I/O (Input/Output), are connected directly to the ASCII bus. Data is transferred from one block to another and to the external devices over the ASCII bus under the control of the timing and processing unit (TPU). Other functional blocks include the video circuits, a line operated power supply, and a high voltage power supply, or flyback system, which is operated from the video circuits.

The character generator has a master oscillator and dividers that generate the timing signals for all of the functional modules within the Terminal. Basically, the character generator takes data from the RAM (Random Access Memory) and converts it from 8-bit parallel ASCII information to serial dot information. The serial dot information is then used to modulate the raster scan on the CRT screen.

The video module contains a video amplifier that converts the TTL dot data from the character generator into voltage levels that drive the cathode of the CRT. The video circuits also have a vertical oscillator and amplifier that generates the vertical sweep and drives the vertical portion of the CRT yoke. It also contains the horizontal oscillator and driver that drives the horizontal flyback and sweep systems. The vertical and horizontal oscillators are synchronized by sync pulses generated by the character generator.

The Ram and counter board contains the memory that stores the information to be displayed on the screen. Everything that appears on the face of the CRT is stored in the RAM. The RAM and counter circuit board also contains the RAM address counter, a cursor latch, which remembers where the cursor is supposed to appear on the screen, and scroll counters that remember the start of page, or scroll information.

The keyboard contains a standard ASCII keyboard and a series of other special function keys that control

the operation of the Terminal. It includes five cursor control keys, a number of keys that control the operation of the serial I/O, erase keys, and screen display mode keys. It also includes a special character generator that puts selected ASCII information on the bus whenever it is required.

The I/O board contains latches and buffers to control parallel data transfers between the Terminal and any external devices. It also contains the UART (universal asynchronous receiver/transmitter) that controls serial data transfers between the Terminal and any external devices. The I/O circuit board also has a special character detector that monitors the bus and looks for special characters such as carriage returns, bells, control characters, etc.

The timing and processing unit (TPU) controls all of the other functional blocks. It is the decision-making module within the Terminal. Data is moved, written, or transmitted under the control of the TPU as a function of the front panel switches and the data itself. It also controls cursor movements, scrolling operations, erasing, and the RAM counter configurations.

POWER SUPPLY

The primary of the power supply consists of slow-blow fuse F1, ON/OFF switch SW1, and the dual primary windings of transformer T1. The dual primary windings may be connected in series for 240-volt operation or in parallel for 120-volt operation.

The red secondary winding of the power transformer supplies 9 volts AC to the diode bridge rectifier D101 through D104. The rectified output of the bridge rectifier is filtered by capacitor C1.

Integrated circuits IC101 and IC102 provide two regulated 5-volt supplies. The integrated circuits are internally protected against short circuits, overloads, and high temperature. Capacitors C101 and C102 stabilize the regulators.

The orange secondary winding supplies 28 volts AC to diode bridge rectifier D105 through D108. The 36-volt output of the bridge rectifier is filtered by capacitor C2. This 36-volt supply is one of the outputs of the power supply.

IC103 is a 20-volt regulator, but its output is programmed by resistors R103 and R104 to supply 26 volts. IC103 draws its input current from the base of transistor Q101. Q101 in turn provides the larger currents required by the video circuits and regulates the output at 26 volts. Transistor Q102 and resistor R102 limit the short circuit current to about 2 amperes. Capacitor C103 provides stability for IC103.

IC104 is a 12-volt regulator. The input to this IC comes from the 26-volt supply. Capacitor C104 provides stability for IC104.

The green secondary winding supplies 15 volts AC to diode bridge rectifier D109 through D112. The DC output voltage is filtered by capacitor C105. IC105 is a negative, adjustable voltage regulator that is programmed to −12 volts by resistors R105 and R106. Capacitor C106 provides stability for IC105, while C107 lowers the high frequency output impedance.

Resistor R107 reduces the 15 volts AC from the green secondary winding to provide 11 VAC to power the CRT filament.

VIDEO CIRCUITS

VERTICAL SWEEP CIRCUITS

At the beginning of each vertical scan cycle the vertical sync pulse turns on transistor Q301. This discharges the voltage across capacitor C303. At the end of the sync pulse, Q301 turns off. Transistor Q302, a current source, charges capacitor C303 with a constant current. This generates a linear ramp that is coupled through resistor R307 and capacitor C304 to the base of transistor Q303.

Transistors Q303, Q304, Q305, and Q306 form a conventional class B amplifier that amplifies the ramp to drive the vertical deflection yoke. Resistor R323 samples the current through the yoke and provides a feedback voltage through divider R313, R314, and R315 to the base of Q303. Diodes D301 and D302 increase the amount of feedback applied at the extremes of the scan. This, in effect, keeps the scan linear from the top to the bottom of the screen. The vertical scan rate is 60.5 Hz.

HORIZONTAL SWEEP CIRCUITS

The horizontal sweep system is controlled by triggered oscillator, IC301. The free-running frequency of this oscillator, which is set by resistor R325 and capacitor C312, is slightly less than the 15494 Hz horizontal sweep rate. Horizontal sync pulses are coupled through C314 to the +Vcc input (pin 6) of IC301. The sync pulse changes an internal reference voltage that causes the oscillator to reset prematurely and oscillate at the desired horizontal rate.

The output (pin 1) of IC301 drives transistor Q307 which, in turn, drives the horizontal output transistor, Q1. The duty cycle (the on-to-off ratio) of Q1 is determined by R328 and R329. The collector of Q1 drives the primary of the horizontal output transformer T2. The high voltage secondary is rectified internally to provide 12 kV for the anode of the CRT.

When the horizontal oscillator causes Q1 to turn off, the rapid collapse of the flux in transformer T2 generates a 200-volt pulse across the primary winding. Capacitor C321 charges immediately to the maximum of this pulse. C321 then discharges quickly through linearity coil L301, the horizontal deflection yoke, and capacitor C322 until the yoke current is maximum. The current through the yoke at this point is considered negative (flowing from C321 down through the linearity coil, the yoke, and C322). This negative current causes the magnetic field of the yoke to quickly pull the electron beam to the extreme left side of the CRT screen (retrace). The yoke field begins to collapse as it tries to keep the current flowing in the same direction.

Diode D_B, which is part of Q1, now conducts and effectively removes C321 (shorts it out) from the circuit. As the yoke field continues to collapse, the charge on C322 continues to increase. This action produces a near linear change (decrease) in current, which causes a linear change in the yoke field. As the yoke field decreases, the electron beam moves from the left toward the center of the CRT screen.

Before the yoke current reaches zero at the center of the screen, transistor Q1 is turned on by the horizontal oscillator. Transistor Q1 also keeps C321 out of the circuit. Current will cease to flow when the yoke field collapses completely. At this point, the electron beam will be at the center of the CRT screen. The charge stored in C322 now begins to discharge through the horizontal deflection yoke, linearity coil L301, and transistor Q1 in a positive direction. The current through the yoke is considered positive (flowing from C352 up through the yoke, the linearity coil, and transistor Q1). Diode D_B is now reverse biased and out of the circuit. The change in polarity of the yoke field, as the yoke current increases in a positive direction, moves the electron beam from the center toward the right side of the CRT screen. Capacitor C322 continues to discharge until the beam is at the right side of the screen and Q1 turns off again. This process repeats for each horizontal scan line.

HIGH VOLTAGE SUPPLY

During retrace, the 200-volt pulse across the primary of T2 is coupled through resistor R335 to voltage doubler D305, D306 and D307, C324, C326, and C327. This provides a 300-volt supply for grid 2 of the CRT.

The voltage from the blanking winding of T2 is rectified by diode D304 to produce a −150-volt supply for the focus control.

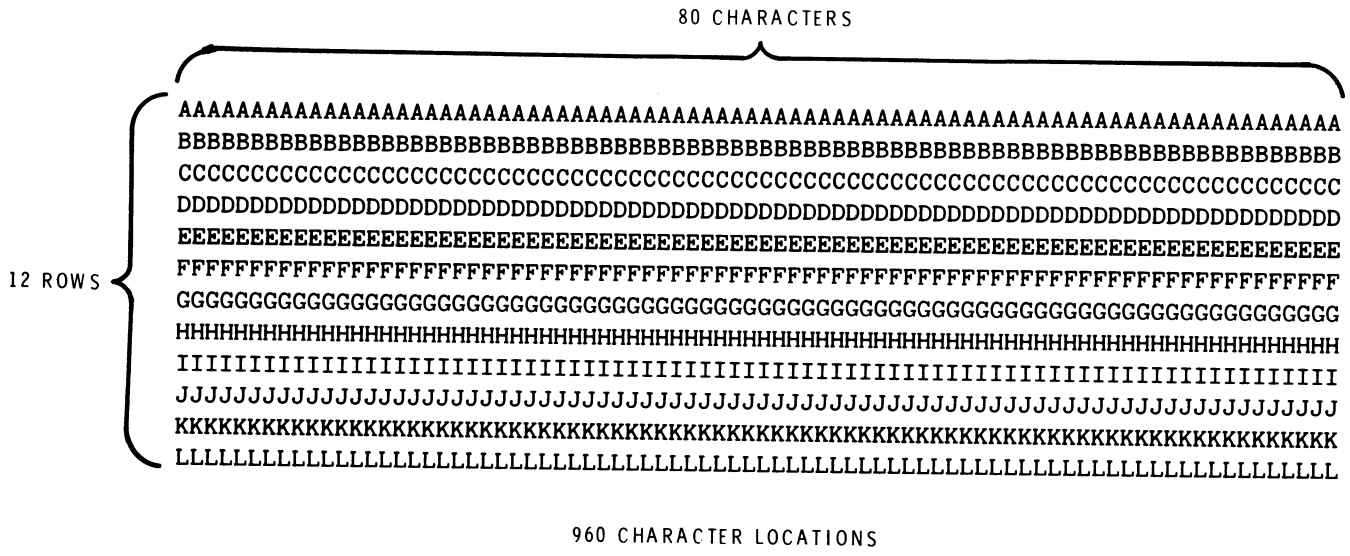
VIDEO AMPLIFIER

The video information that comes from the character generator is a string of 1's and 0's. This data is coupled to the base of Q309, which drives the emitter of video output transistor Q308. The collector of Q308 drives the cathode of the CRT. The brightness control, R338 which sets the voltage on grid 1 of the CRT, controls the brightness of the displayed characters.

CHARACTER GENERATOR

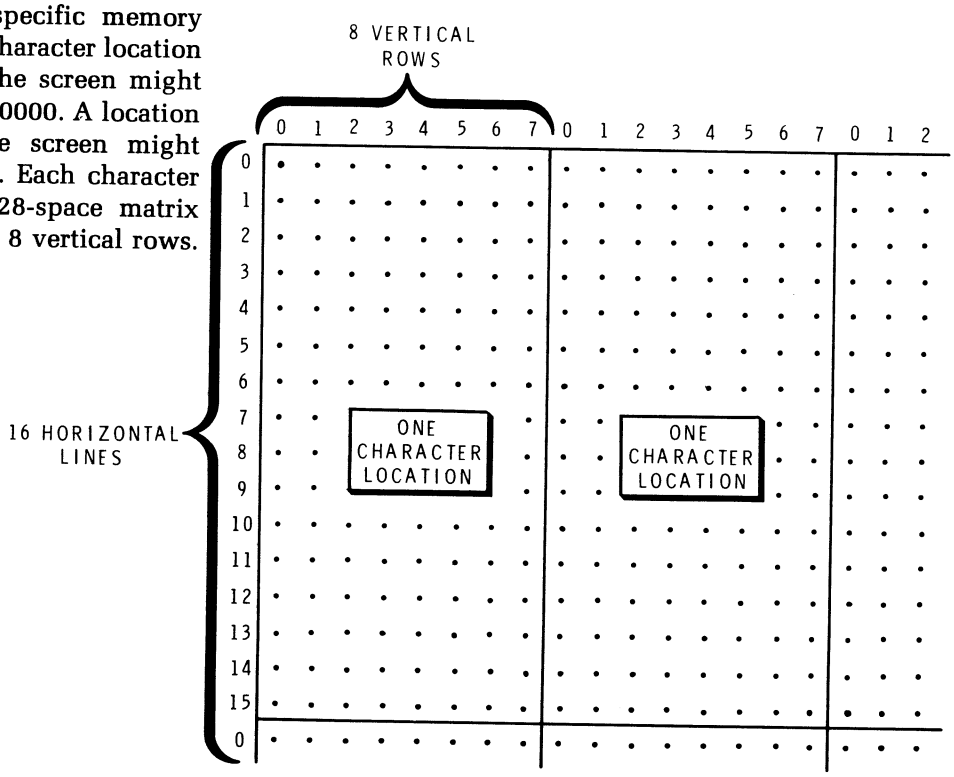
GENERAL DESCRIPTION

The CRT screen is divided into 12 lines, each having 80 character locations, for a total of 960 character locations. See Pictorial 4-1.



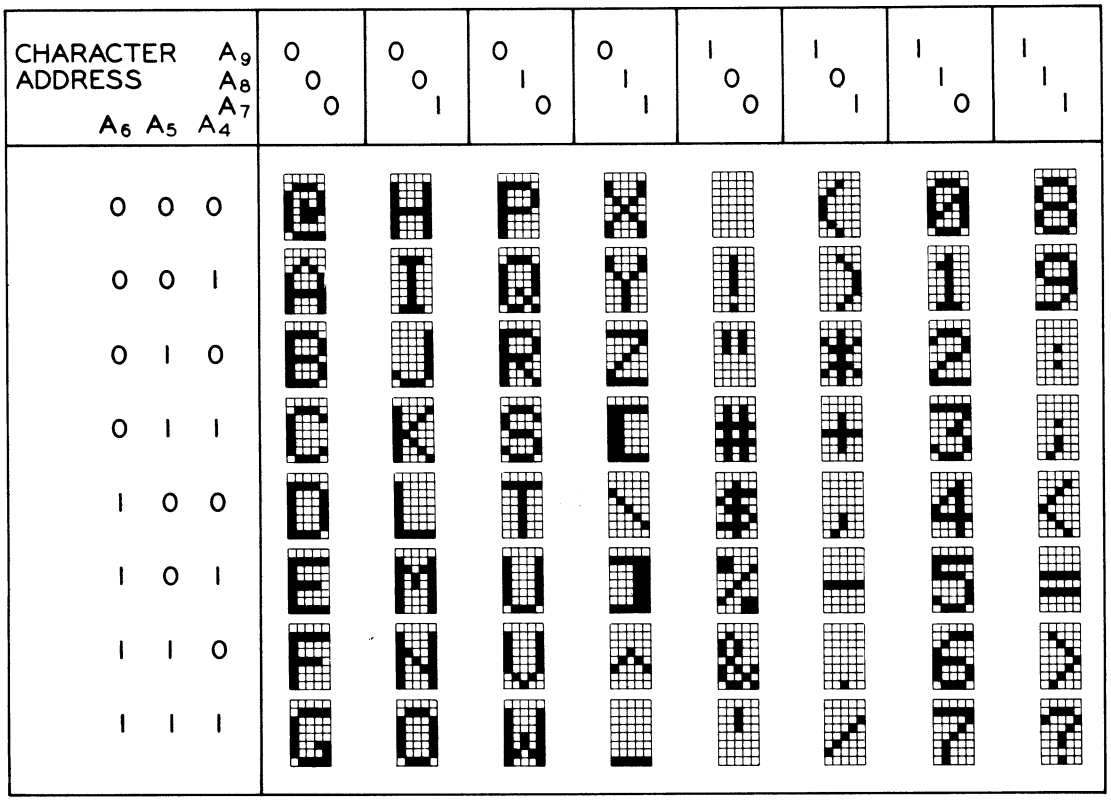
PICTORIAL 4-1

Each location corresponds to a specific memory address in RAM. For instance, the character location at the upper left hand corner of the screen might correspond to RAM address 0000000000. A location somewhere in the middle of the screen might correspond to address 0111101011. Each character location on the screen is in a 128-space matrix arranged in 16 horizontal lines and 8 vertical rows. See Pictorial 4-2.



PICTORIAL 4-2

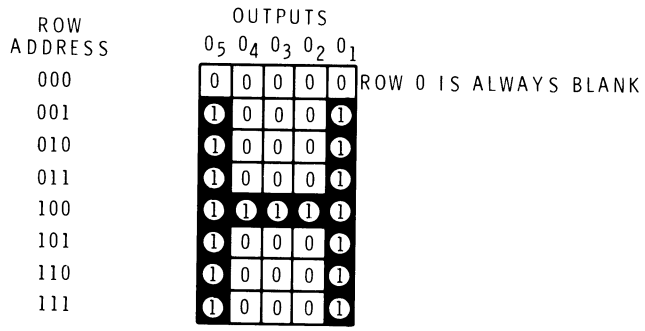
Pictorial 4-3 (Illustration Booklet, Page 8) shows the block diagram of the character generator circuits. At the end of vertical retrace, the RAM address counter is initialized to the address for the upper left corner of the screen. The address counter addresses one of the 960 RAM locations. Each memory location contains the ASCII code for the character to be displayed. The ASCII code is applied through a latch to the character generator. However, only the six least significant bits of the 7-bit ASCII word are used to address the character generator. Sixty-four characters are stored in the character generator ROM, each at its own address as shown in Pictorial 4-4. For instance, the 6-bit ASCII word 001000 addresses the character H.



Character H

ASCII BIT	6	5	4	3	2	1
CHARACTER GENERATOR INPUT	A_9	A_8	A_7	A_6	A_5	A_4
6-BIT ASCII WORD	0	0	1	0	0	0

PICTORIAL 4-4



PICTORIAL 4-5

Since the electron beam in the CRT scans only one line at a time, the dots that make up the characters must be shifted out serially, one row at a time. To do this, the character generator puts out up to five dots in a row for each character. Pictorial 4-5 shows the row outputs for the character H. The 5-bit dot data is always followed by three spaces (the absence of dots) before the dots for the next character are shifted out.

Since the CRT scanning process requires the dots data to be applied to the video circuits in a serial format, the 5-bit dot data is loaded into a shift register and shifted eight times. This shifts out the five bits of dot data followed by three spaces. The three spaces are formed when a blanking signal is applied to the video circuits during the fifth through seventh shift sequences. They are also necessary because the character location on the screen has been defined as being eight rows wide. The spaces provide space between characters.

During the fifth through the seventh shift sequence, the shift register is loaded with new dot data for the next character. The RAM address counter is also incremented to its next address. This process of addressing succeeding RAM location and outputting dot data continues until a horizontal sync pulse is generated at the end of a scan line. The horizontal sync pulse increments the row counter and causes the electron beam to begin a new scan line. The character generator now outputs dot data for the next row in the dot matrix. This process continues until all seven rows of dot data have been outputted. Horizontal scan lines 8 through 15 are normally blanked. The cursor, will appear on lines 12 and 13. A new character line (16 scan lines) begins after scan line 15 is completed.

The cursor is displayed on scan lines 12 and 13 when an unblanking signal is applied to the video circuits. This happens when the cursor location, which is stored in the cursor latch, is coincident with the address coming from the RAM address counter.

TECHNICAL DESCRIPTION

The master clock of the entire Terminal is located on the character generator circuit board and it is composed of IC210B, crystal Y201, and transistor Q201. The clock frequency is 12.395 MHz. The true and the complemented outputs are provided for the dot clock and the other system timing. IC's 214, 210C, 221D, 217C, and 207A generate timing signals A, E, and F from the master clock signal. Refer to timing diagram #1 for these waveforms. Keep in mind as you study the waveforms, that the trailing edge (the negative transition) of the clock pulse always preceeds any logic level transitions of the other IC's by approximately 30 nanoseconds.

At the start of the character generation cycle, the RAM counter (on the RAM and counter circuit board) is told by the trailing edge of waveform F to count up. After 565 nS, the RAM data is latched into IC202 and IC203 and then transferred to the input of the character generator by the next leading edge of waveform F. Eighty nS later, the trailing edge of waveform F tells the RAM to count up again. In the meantime, the character generator is starting to access its internal dot information and, after approximately 450 nS, the five bits of dot data appear at the output of the character generator. Waveform A is used as a load pulse for shift register IC204. The dots are latched into the shift register by the trailing edge of the dot clock before the load pulse goes back to zero. Actually, the shift register is loaded three times (at t6, t7, and t0), but only the load at t0 is used. The next five cycles of the dot clock shift dots out serially as video information, which, in turn, is applied to the CRT. At the end of the fifth pulse, waveform A is used as a blanking signal to provide inter-character blanking. Besides latching RAM data for the character generator, waveform F is used in increment the character counter, which is composed of IC's 215 and 220. After 80 characters have been accessed and shifted out, the D output of IC215 provides a retrace blanking signal. This signal blanks the video during the retrace time and it also inhibits further RAM count-ups.

Actually, the D output of IC215 does not turn on the blanking directly. It is delayed by two character times in IC211 to allow time for the last character accessed to be shifted out. The outputs of IC211A generate blanking and sync pulses and count up IC213, the row counter, which tells the character generator to access the next row of dot information. When the retrace blanking period is over, the process is repeated until all eight scan lines of information for the same 80 characters have been shifted out, and a complete row of characters is displayed on the screen. During the next eight scan lines, the entire process is repeated and the same 80 characters are shifted out once again, but the video is blanked to provide spacing between character lines. IC222C decodes the row counter output of IC213 so that the cursor information can only appear in scan rows 12 and 13 of the character row cycle.

At the end of the 16th scan line, the D output of IC213 (the row counter) is used to count up the ÷12 (divide-by-12) counter in the RAM to access the next row of 80 characters. It is also used to increment the sync or frame counter, IC216, which keeps track of the number of rows of characters that are displayed on the screen. At the end of the 16th scan line of the 12th character row, the C and D outputs of IC216 generate the vertical blanking signal. IC's 209C and 221A, in conjunction with the vertical blanking signal, generate the vertical sync pulse to start vertical retrace. Refer to waveforms 1 through 22 on timing diagram #2 for a description of the scan and frame cycles.

Cursor information from the RAM and TPU is latched into IC202 along with the ASCII data by waveform F. This cursor signal is delayed by IC208A for the duration of the character generator access time and it appears as video information at inputs 1 and 4 of IC218 in the video chain.

If the ASCII character latched in IC's 202 and 203 is a control character, bits 6 and 7 will be 0 and the $\overline{Q}$ outputs of the latches will both be high causing the output of IC201A to go to a logic 0. This logic 0 is delayed by IC207B for the duration of the character generator access time and it is used to blank the dot information for that control character. The preset input of IC207B is driven by a 4 Hz clock pulse, which will unblank the control character dots 4 times a second, causing the character to appear to blink on the screen.

In the plot mode, the first 128 scan lines are used to display information that corresponds to the binary value of a 7-bit ASCII word. In this mode, the first row of characters that would normally be seen on the screen is repeated 4 times, starting with the 129th scan line (in the 9th, 10th, 11th, and 12th character lines). In the space directly above each character, the beam is turned on to display a lighted dash in the scan line that corresponds to the binary value of that character. The 128 scan lines are arranged so that the 128th line (line 127) is at the top of the screen and the first line (line 0) is at the bottom of the 8th character line (128 lines from the top). For example, if the character was a rubout, which is all 1's the dash would appear at the very top of the screen. If the character was a K (binary 1001011), its value would be 75 and it would appear on plot line 75. Refer to Pictorials 1-2 (Page 6) and 1-3 (Illustration Booklet, Page 2).

The four outputs of IC213 and the A, B, and C outputs of IC216, count the scan lines from 0 at the top to 127 at the end of the 8th character row. The seven outputs are inverted by IC212 and IC219A so that the count will be 127 at the top and 0 on the 127th row. The outputs of the inverters are applied to the inputs of exclusive NOR gates (IC206 and IC209A, B, and D). The other inputs to the NOR gates are connected to corresponding bits from the outputs of latches IC202 and IC203. When the seven data bits at the latches are exactly coincident with the outputs of the inverters, a logic 1 will appear at the outputs of IC206 and IC209. If the plot function has been selected by the Plot button on the keyboard, this coincidence signal is gated through IC201B to the input of IC208A. After a delay of one character time, the plot coincidence signal will appear at the output of IC208A as a plot video signal that will then be displayed on the screen as a short dash. During the plot time, the cursor information is blanked by the output of IC201D and the ASCII dot information is blanked by the output of IC221B.

The video and blanking channels can be broken down into three video channels and two basic blanking channels. The dot information video channel consists of IC210D, IC219D, and IC218C. If there are no dot blanking signals present, the dots that shift out of IC204 will appear directly at pin 8 of IC218C. The dot video will be blanked by the output of IC207B if the dots represent a control character by the 9-to-15 line

blanking signal from the D output of IC213, or by the plot blanking signal from pin 10 of IC221C which blanks the first 128 scan lines.

The cursor video channel consists of IC201C, IC208A, and IC218B. In the absence of cursor blanking signals, the cursor video signal from pin 2 of IC202 will appear (after the proper delay) at pin 6 of IC218B. The cursor can be blanked by a cursor blanking signal from the TPU or by a plot signal, both of which appear at pin 10 of IC201C. The cursor is also normally blanked by the output of IC219B, except during the 12th and 13th scan rows. This blanking signal appears at pin 5 of IC218B.

The plot video channel consists of IC201B, IC208A, and IC218A. The plot video signal that appears at the outputs of IC206 and IC209 will appear after the proper delay at the output of IC218A. This video signal can be blanked by the plot blanking signal that comes from the output of IC221C.

The dot, cursor, and plot video signals are logic 1's in the absence of any video information. They drive the inputs of a 3-input NAND gate, IC222B, and any video information (0's) will appear at the output of IC222B as logic 1's. This is the composite video output.

The vertical blanking information appears as a negative logic signal at pin 3 of IC217A. The blanking signal will be developed for the vertical retrace period and for the duration of a refresh interrupt signal from the TPU circuit board.

Horizontal blanking information appears as a negative logic signal at the output of IC217B. This signal is developed during the horizontal retrace time and during the three dot spaces between characters.

The vertical and horizontal blanking and the video signals drive the inputs of NAND gate IC222A. The output appears as negative logic video information. That is, a logic 0 will turn on the electron beam in the CRT.

The A write pulse, which is used in the screen erase cycle, is generated by IC221D from the A and D outputs of the master clock divider, IC214.

KEYBOARD CIRCUIT BOARD

The keyboard contains a 52-key ASCII keyboard and encoder, a special ASCII character generator, four cursor control latches, and twelve mode control switches.

The ASCII keyboard is a matrix of single-pole, normally-open switches that are scanned by IC402, the keyboard encoder. The X2 through X9 outputs are scanned with a series of pulses. When a key is pressed, one of these pulses appears at one of the eight Y inputs. After an appropriate debounce period, the encoder recognizes the pulse as a valid key depression, decodes the X and Y pulse data into the appropriate 7-bit ASCII word, latches the word in buffer IC403, and puts a logic 1 on the data strobe output to indicate that there is valid data present in the buffer. The negative true logic output of the keyboard encoder IC402 is inverted (to positive true logic) by inverter/buffer IC403 to provide positive true logic for the bus. The table in Pictorial 4-6 (Illustration Booklet, Page 9) shows the 7-bit ASCII codes, generated by the keyboard encoder, as they will appear at the output of inverter/buffer IC403. It also shows the key entries that are needed to produce these outputs. When the output enable line (OE) is brought to a logic 0, the 3-state buffers are turned on and the ASCII data is put on the bus. A logic 0 on the output enable line also resets the data strobe output of IC402 to indicate that the data in the buffer has been read.

IC401 is a ÷16 counter that generates four repeat rates from the 60.5 Hz vertical frequency. The frequencies set the rate of the repeat (REPT) function.

A special character generator composed of IC404, IC405, and IC406 is also connected to the ASCII bus. IC406 decodes inputs A1 and A2 into four states; 1) a 3-state OFF, 2) and ASCII carriage return, 3) an ASCII line feed , 4) an ASCII space. When both inputs are low, the 3-state outputs of IC404 and IC405 are turned

off. When A1 is high, a carriage return is put on the bus; when A2 is high, a space is put on the bus; and when both are high, a line feed is put on the bus. These characters are used in the transmit page mode and during the erase cycle.

IC407 and IC408 are latches that are set by the four cursor control keys. During the vertical scan cycle, Q401 is turned on, enabling the cursor controls. When any of the cursor keys is pressed, the corresponding latch is set so that the data can be remembered until the next TPU cycle. During the TPU cycle (vertical retrace time), Q401 turns off so that the data in the latches cannot change and confuse the TPU circuits.

The 12 function keys at the upper right of the Schematic are single-pole, single-throw; normally-open switches with pull-up resistors. These switches generate logic 1's and 0's to convey the proper operating mode to the TPU circuits.

RAM AND COUNTER

The RAM and Counter circuit board contains a 1k × 8 static RAM, an address decoder, and a RAM address counter. Twelve character lines can be displayed on the screen. Each line is composed of four blocks of 20 characters. See Pictorial 4-7. The RAM address counter can be broken down into a ÷20 counter, a ÷4 counter, and a ÷12 counter.

LINE	COLUMN 0	COLUMN 1	COLUMN 2	COLUMN 3
0	20 CHAR	20 CHAR	20 CHAR	20 CHAR
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				

PICTORIAL 4-7

During scan, the ÷20 counter, IC502, IC504B, IC509, IC510B, and IC510C cascades into the ÷4 counter, IC513, to access a block of 80 characters for one character line. The count-up signal that moves this address counter from character to character during scan comes from the F pulse on the character generator circuit board. Also during scan, the ÷12 address counter is counted up by the D output of the scan row counter (IC213 on the character generator circuit board) that drives the character generator row address.

The three RAM address counters (÷20, ÷4, ÷12) output a total of 11 bits, which is one more than is required to address the 1k × 4 RAMs, IC507 and IC516. IC's 512, 526A, 526D, and 527B form an address decoder that eliminates unused address codes and redundancies, and decodes the 11 bits down to 10 bits.

The 1k × 8 memory is made up of two 1k × 4 memories, IC507 and IC516, whose 10 inputs are connected in parallel. The chip select inputs ($\overline{CS}_1$) and the write enable inputs ($\overline{WE}$) are also connected in parallel. When the write inputs are high and the chip select inputs are low, eight bits of data is read from the I/O ports of the RAM's. When the write inputs are brought low, data on the bus can be written into the RAM and latched into a specific memory location that is determined by the address inputs when the write inputs go high. When the chip select inputs are high, the three state I/O ports are turned off and data can neither be read from nor written into the RAM.

The cursor latches (IC's 501, 521D, 521C, 521B, and 518) in the counter modules store the RAM address location where the cursor is located; that is, the current location where a character can be written. As the RAM address counters access RAM locations during scan, the coincidence gates compare the RAM

address with the address stored in the cursor latches and they will output logic 1's when the two addresses are exactly coincident. These coincidence gates, or comparators, are composed of exclusive NOR gates, IC's 508, 503, and 520. The three outputs, ÷20 coincidence, ÷4 coincidence, and ÷12 coincidence, are processed in the TPU to generate a single coincidence signal. This coincidence signal is used in the character generator circuit board to generate the dashed cursor line on the screen. At the end of the last scan line of the twelfth character row, the screen refresh cycle has been completed and the RAM address counters have accessed, in sequence, all of the active RAM locations. As the vertical blanking cycle begins, the cursor address is loaded from the cursor latches into the RAM address counters. The RAM is then addressed to the cursor location and data can be read from or written into that location in RAM by the TPU. If data was written into the RAM, the TPU will count up the RAM address counters to the next cursor location. The new cursor address is then loaded and latched in the cursor address latches.

The ÷4 and ÷12 scroll counters contain the start of page or start of scan information. The ÷12 scroll counter, IC's 517A, 517B, and 522 stores the address for one of the 12 character rows of 80 characters. The ÷4 scroll counter, IC506, stores the address for one of the four blocks of 12 rows of 20 characters. Just before the vertical blanking period ends, and the screen refresh period begins, the scroll, or start of page information is loaded from the scroll counters into the RAM address counters. In long form, the ÷4 scroll counter is always held cleared; therefore, the ÷4 start of page information is always block number 0. In short form, the ÷12 scroll counter is held cleared and the start of page information is always line number 0. The ÷20 address counter module does not have a scroll counter because it always starts at character 0 regardless of whether the mode is long or short form. As the scan cycle begins, the RAM address counters sequence through the RAM, starting with the location specified by the scroll counters.

Each of the counter modules has a number of controls associated with it. The ÷20 module has count-up, count-down, load, and clear inputs and two inputs that determine whether it cascades into the ÷4 counter or the ÷12 counter. The load input loads the outputs of the ÷20 counter with the data contained in the 5-bit cursor latch, IC501 and IC521D. The clear input sets all five bits to logic 0. The ÷20 → ÷4 control connects the carry and borrow outputs of the ÷20 counter to the count-up and count-down inputs of the ÷4 counter. The ÷20 → ÷12 control connects the carry and borrow outputs to the count-up and count-down inputs of the ÷12 counter.

The ÷4 module has count-up, count-down, load and clear inputs for the RAM address counter, and count-up and clear inputs for the ÷4 scroll counter. There is also an input called "select scroll ÷4" (Sel S ÷4) that determines whether the output of the cursor latch or the output of the scroll counter will appear at the input of the RAM address counter during the load cycle. There is also a ÷4 → ÷12 input that connects the carry and borrow outputs of the ÷4 counter to the input of the ÷12 counter. The ÷12 module contains count-up, load, and clear inputs for the RAM address counter, and count-up and clear inputs for the scroll counter. There is a ÷12 → ÷4 input that connects the carry and borrow outputs of the counter to the count-up and count-down inputs of the ÷4 RAM address counter. There are also three select inputs that determine whether the RAM address counter is loaded with cursor information, scroll information, or a binary 11. The ÷12 RAM address counter, IC519, is made from a ÷16 counter, whose modulus is controlled by IC515A. When the output of the counter reaches binary 12, IC515A immediately clears all four outputs, effectively making it a 0-through-11 counter. In the count-down mode, as the count passes through 0 to 15, IC525A immediately loads the counter with the binary 11 that is generated by the three select lines and the counter continues to count down, not from 15, but from 11.

The ÷20 and the ÷4 counter modules each contain an end-of-line indicator The ÷20 end-of-line indication is a binary 19 that is decoded by IC525B and IC527A. A logic 1 at the output of IC527A indicates that the ÷20 counter has reached its highest address. The ÷4 end-of-line indication is a binary 3 that is decoded by IC511D and appears at the output as a logic 0. All three counter modules share a common cursor latch enable or cursor load input.

TIMING AND PROCESSING UNIT (TPU)

The timing and processing unit is the central controller for all Terminal functions. It manages the reading, writing, and all data transfers, scrolling, and erasing. It generates an end-of-line bell signal, a power up reset routine, it handles cursor movements, and implements the transmit page function. All of these activities happen during the vertical retrace period.

To visualize what is going on in the TPU, it is helpful to remember that there are two distinct modes of operation within the Terminal. One is the scan cycle and the other is the TPU cycle. During the scan cycle, characters are being displayed on the screen by the RAM and counter circuit board and the character generator circuit board. Also, during this time, the TPU is idle and there is little or no logic activity on the TPU circuit board. The RAM address counter on the RAM and counter circuit board is, however, being operated at maximum speed to put characters on the screen.

As soon as the vertical retrace period (TPU cycle) begins, the TPU begins to perform all of the housekeeping chores within the Terminal. Since the RAM address counter is no longer being used to refresh the screen, the TPU can access it and use the RAM for reading, writing, and data transfers. The TPU can also access the scroll counter and the cursor latches to perform scrolling operations and cursor movements.

If data is coming into the Terminal faster than the TPU can handle during the vertical retrace period, the TPU interrupts the screen refresh cycle and starts an extended TPU cycle. After the incoming data has been serviced, screen refresh can start again, but only at the start of the next refresh cycle. Then, it will go back and pick up where it left off.

TPU TIMING

The basic TPU timing signals are generated by the A, B, and C outputs of the scan row counter, IC213 on the character generator circuit board. These signals are applied to IC712 where they divide the vertical retrace period into eight complete TPU cycles. Each cycle contains eight sub-cycles. Timing Diagram #3 illustrates how the A, B, and C outputs and $\overline{H_1}$ generate a series of non-overlapping pulses. These pulses are labeled 0 thru 7 and each defines a specific time for a particular TPU operation to occur. The 0, 1, 2, and 7 cycles are subdivided even further by ANDing them with the C (IC710B & IC728) and B (IC710A & IC718C) outputs of the horizontal character counter (IC215 on the character generator circuit board).

In general, all reading, writing, and data manipulation operations occur during the 0 pulse. See Timing Diagram #4. The 1 pulse is used for all counting operations. That is, the RAM address counters can be counted up and down, the cursor can be counted in any direction, and the scroll counter can be counted. The 2 pulse is used to check for scroll coincidence and generate the scroll command. The time between the 3 pulse and the 6 pulse is used for scroll erase and erase to end of line. The 7 pulse is used to wrap up all of the TPU operations and to return the RAM counters to their start of page position.

COUNTER CONTROLS

During the screen refresh cycle, the ÷20 RAM counter always cascades into the ÷4 counter. The ÷12 counter is driven by the character row counter on the character generator circuit board. This counter setup is always the same regardless of whether the Terminal is in the long form or short form mode.

Long Form

During retrace, the counters are cascaded differently to alter the format of how the cursor moves through the RAM locations. In long form, the cursor moves from left to right through all 80 RAM locations on a single line before it moves down to the next line. This is accomplished by the ÷20 and ÷4 counters. The cursor starts at the extreme left end of the line with both the ÷20 and ÷4 counters cleared (each reset to zero). The ÷20 counter is incremented by the C.U. ÷20 (count up ÷20) signal to move the cursor to the right. After the ÷20 counter reaches 19 (11001), the next C.U. ÷20 pulse causes the counter to count up to zero (00000). This generates a carry pulse that increments the ÷4 counter from 0 (00) to 1 (01). The ÷20 counter then accesses the 20 locations in block #1 of the ÷4 locations.

When the counters reach 19 and 3, respectively, the C.U. ÷20 pulse increments both counters to zero. This causes a carry pulse from the ÷4 counter that incre-

ments the ÷12 counter. This addresses the next line of information if the Auto Carry key is pressed in. If the Auto Carry key is released, and end of line indication will keep the counters from going to zero (the carry pulse will not get to the ÷12 counter). The cursor will then stay at the right end of the line.

A logic 1 from pin 2 of IC730 (S706 pin 9) causes the carry and borrow pulses from the ÷20 counter to cascade into the ÷4 counter. A logic 1 from pin 2 of IC724 (S707 pin 10) causes the carry and borrow pulses from the ÷4 counter to cascade into the ÷12 counter. These two logic signals are generated in the ROMs (IC724 & IC730) as a function of Vp', Short Form, Auto Carry, Scroll, ÷20 EOL (End Of Line), and ÷4 EOL.

- Vp' comes from the master TPU timing (IC705B pin 4) and it is logic 1 during retrace.
- Short Form comes from the Short Form key on the keyboard (S704 pin 10). When the short form input is logic 1, the Terminal is in the long form mode. When the short form input is logic 0, the Terminal is in the short form mode.
- Auto Carry comes from the Auto Carry key on the keyboard (S703 pin 10). The Terminal is in the auto carry mode when the auto carry input is logic 0.
- Scroll comes from the scroll command (IC741A pin 3). The scroll command is logic 0 during a scroll operation.
- ÷20 EOL comes from the RAM and counter circuit board (S705 pin 4). The ÷20 EOL input is logic 1 when the count in the ÷20 counter is 19.
- ÷4 EOL comes from the RAM and counter circuit board (S707 pin 7). The ÷4 EOL input is logic 0 when the count in the ÷4 counter is 3.

The EOL and auto carry signals defeat the C.U. ÷20 signal whenever the auto carry function is not selected.

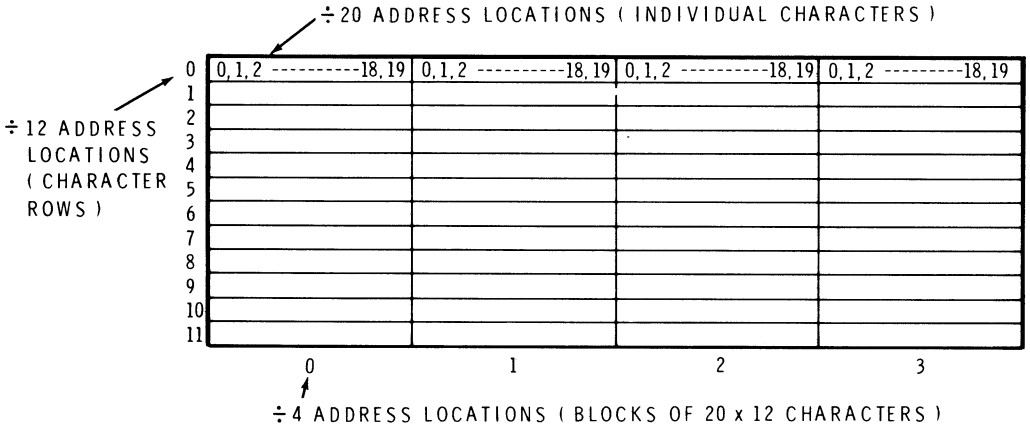
Short Form

In short form, the cursor moves from the left to right through a block of only 20 characters before being returned to the start position of the next line. When it fills up a block of 240 characters, it moves to the top/start position of the next block of characters.

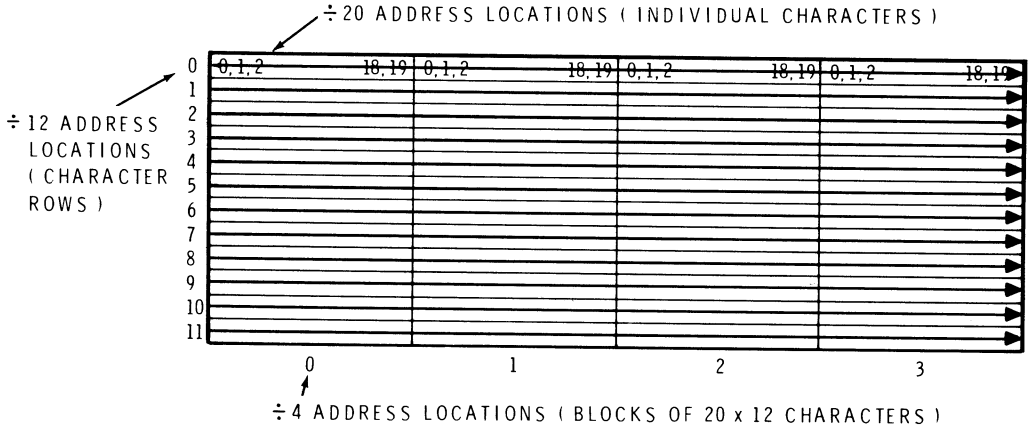
The ÷20 carry pulses increment the ÷12 counter if the Auto Carry key is pushed in. This accesses the entire first block of characters (when the ÷4 counter outputs are zero). When the ÷12 counter reaches 11 (1011), and the ÷20 counter reaches 19 (11001), the next count up pulse causes the ÷12 carry pulse to increment the ÷4 counter to 1 (01). This process continues until all four blocks have been accessed.

A logic 1 from pin 2 of IC730 (S706 pin 11) causes the carry pulses from the ÷20 counter to cascade into the ÷12 counter. A logic 1 from pin 1 of IC724 (S707 pin 8) causes the carry pulses from the ÷12 counter to increment the ÷4 counter. These logic signals are also generated as a function of Vp', Short Form, Auto Carry, Scroll, ÷4 EOL, and ÷20 EOL. Refer to the "ROM Programs" section (in the "Semiconductor Identification" section of the Manual) for the truth tables for ROMs IC724 (444-12) and IC730 (444-11).

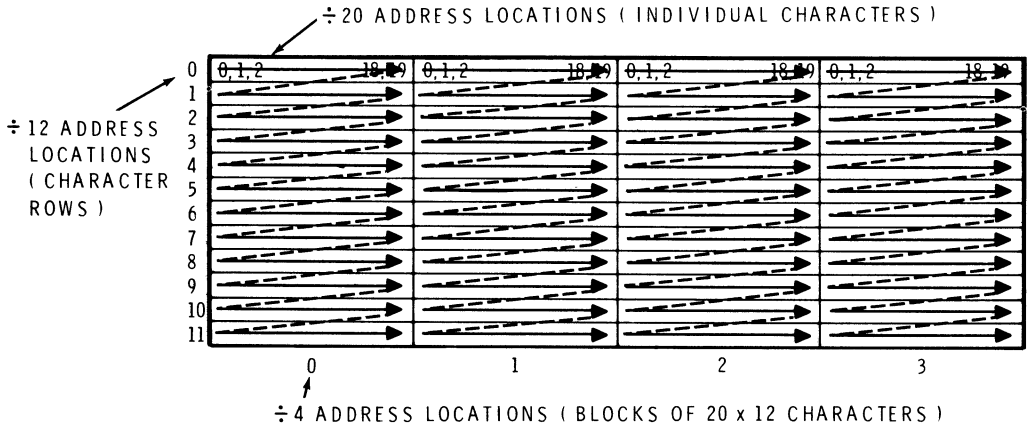
Remember, the cursor always indicates the RAM location where data will be written. Also, in long form, data will enter the RAM in 80 character lines, while in short form, data will enter the RAM in 240 character columns. Refer to Pictorials 4-8, 4-9, and 4-10 for a summary of RAM locations and cursor movements.



PICTORIAL 4-8



PICTORIAL 4-9



PICTORIAL 4-10

IC724 and IC730 control the counter modes as a function of short form, auto carry, and vertical retrace signal. Pictorial 4-11 shows a summary of the counter controls.

COUNTER CONTROLS

During Scan

÷20 → ÷4
÷12 is: counted up by the character generator board.

During Retrace

Long Form

÷20 → ÷4
÷4 → ÷12 if auto carry button is depressed.

Short Form

÷20 → ÷12 if auto carry button is depressed
÷12 → ÷4

÷20 → ÷4	Scan + Long Form
÷20 → ÷12	Retrace • Short Form • Auto Carry
÷4 → ÷12	Retrace • Long Form • Auto carry
÷12 → ÷4	Retrace • Short Form

→ means "cascades into"

PICTORIAL 4-11

SCROLLING

When the screen (RAM) has been filled with characters, the cursor can return to the start of RAM location (home) and write new characters over the old ones, or the screen can be cleaned up and rearranged with a scrolling operation. This consists of erasing a row or block of characters and juggling RAM addresses so that the empty row appears at the bottom of the screen or the empty column appears at the right of the screen. Data is not actually moved around within the RAM. The screen refresh starts at a different RAM location to give the appearance on the screen that the data has moved around.

To determine whether a scrolling operation should occur, the TPU checks for three conditions. First of all, the Scroll key must be pushed in (logic 0 at S704 pin 7) so that the Terminal is in the scrolling mode. Next, it checks to see if there was a ÷12 or ÷4 count up, which occurs if the cursor changes from one line or column to another. The Timing Diagrams show that the cursor count-ups occur only on TPU cycle 1C. IC735A, B, and D decode the C.U. ÷4 (S707 pin 9) and the C.U. ÷12 (S707 pin 2) as functions of the short form signal (S704 pin 10). The output (IC735D pin 13) is applied to the D input (pin 2) of flip-flop IC709A. If either one (C.U. ÷4 or C.U. ÷12) is low (0) during $\overline{TPU}$ cycle $\overline{1C}$ ($\overline{1C}$ is the clock input to the flip-flop), the $\overline{Q}$ output (pin 6) goes high (1).

Next, the TPU checks to see if the cursor address is coincident with the scroll or start of page information. The ÷12 and ÷4 scroll coincidence signals come from the RAM and counter circuit board (S702 pin 4 and S705 pin 11 respectively). IC710D and IC733A decode the coincidence signals as a function of short form and apply the output to the D input (pin 12) of flip-flop IC709B. The scroll coincidence information comes from the RAM and counter circuit board during TPU cycle 2C. If there is scroll coincidence, TPU pulse 2C clocks a logic 0 into flip-flop IC709B, and the $\overline{Q}$ output (pin 8) of the flip-flop goes high.

When all three conditions have been met, the TPU knows that the cursor was counted away from the last column or the last row on the screen and a scroll operation should be performed.

The outputs of flip-flops IC709A and B are ANDed in IC715B. The output of IC715B drives one input (pin 5) of NAND gate IC741B. The other input (pin 4) is driven from the $\overline{Q}$ output (pin 8) of flip-flop IC733C and D, which is normally reset ($\overline{Q}$ = 1). If the Scroll key is pushed in (S704 pin 7 = logic 0), the output (pin 6) of IC741B goes low to indicate to the rest of the TPU that a scroll operation should occur. If the Scroll key is up (released), the output (pin 3) of IC739A goes low and sets flip-flop IC733C and D ($\overline{Q}$ = 1). This holds the input (pin 4) to IC741B low, which keeps the output (pin 6) of IC741B from going low to indicate that the scroll operation should take place. This is the "hold screen" mode. IC733 stays preset until the Scroll key is pushed in. The $\overline{Q}$ outputs of IC709A and B also stay high for the duration. They are normally preset ($\overline{Q}$ = 0) by TPU pulse 7C that is applied through IC739C. However, during the hold screen mode, the $\overline{Q}$ output (pin 8) of IC733C inhibits IC739 (and the 7C pulse). Therefore, since one input (pin 4) of IC715B is high, the output (pin 6) stays high. The $\overline{Q}$ output ($\overline{\text{hold screen}}$) of IC733C is also sent to the I/O circuit board (S702 pin 10) to inhibit external data inputs.

The Terminal is released from the hold screen mode by pressing either the Scroll key (S704 pin 7 = logic 1) or the Erase Page key (S704 pin 2 = logic 1). When either key is pressed the output (pin 11) of IC739D goes high and the next 7C pulse resets flip-flop IC733C and D. The $\overline{Q}$ output (pin 8) goes high, enabling IC739C. This lets the 7C pulse preset flip-flops IC709A and IC709B ($\overline{Q}$ = 1). All three flip-flops are then back to their normal states.

The scroll command from IC741B pin 6 is inverted and applied to one input (pin 1) of NAND gate IC741A. The other input (pin 2) is driven by the $\overline{Q}$ output (pin 8) of the transmit page flip-flop, IC731C. The scroll is inhibited when the Terminal is in the transmit page mode ($\overline{Q}$ = 0).

The scroll command from pin 3 of IC741A drives one input (pin 14) of ROM IC724. The ROM outputs a logic 1 (from pin 3) to the RAM and counter circuit board (on TPU cycle 3). This signal counts up the scroll counter and changes the start of page address. Simultaneously, it drives one input (pin 2) of NAND gate IC722A. The other input is connected to the Plot key (S704 pin 1).

Scroll erase is inhibited when the plot mode is selected. The plot signal (S704 pin 1) is logic 1 for the normal mode and logic 0 for the plot mode.

If the Terminal is not in the plot mode and the scroll command occurs, the output (pin 3) of IC722A goes low. This presets flip-flop IC723A, which starts the erase cycle.

When the $\overline{Q}$ output (pin 8) of IC723A goes low, the RAM write signal ($\overline{A}$ write), coming from the character generator (S705 pin 8) appears at the output (pin 10) of IC737C. This causes IC726A to turn on the special character generator on the keyboard (via A2, S704 pin 8) which puts a space on the bus. Simultaneously, through the output of IC737A (S706 pin 3), the RAMs are put into the write mode and the space that was on the bus is now stored in the RAM. The RAM count-up signal, coming from the character generator circuit board (S705 pin 7) addresses the next RAM location and another space is stored in the RAM. The RAM counter continues to access all of the RAM locations in the same row or block of characters until spaces have been written in the entire row or block. During TPU cycle 6 the erase flip-flop (IC723A) is cleared (the clear comes from IC724 pin 4) and the erase procedure stops. While erasing was going on, TPU cycle 3 counted up the scroll counter to move the start of page address to the next line or block of characters. See Pictorials 4-12 and 4-13 (Illustration Booklet, Page 10) for a summary of the scrolling operation.

ERASING

Erasing the page or erasing to the end of line are accomplished in basically the same manner as the scroll erase. The write (S705-8) and count-up (S705-7) signals from the character generator circuit board put spaces on the bus and generate write signals for the RAMs. The erase to end of line (EOL) function (from keyboard key ERASE EOL, S704-12) causes the erase flip-flop (IC723A) to be set on TPU cycle 2 by the output (pin 13) of IC737D. The RAM counts up and writes a space in each location until an end of line signal is received. IC730 generates the end of line indication. In short form a ÷20 end of line signal stops the RAM counter from counting up. In long form the ÷20 end of line signal is ANDed with the ÷4 end of line signal to stop the RAM counter. This EOL signal comes from pin 7 of IC730. It drives one input (pin 5) of AND gate IC729B. The other input is driven from the scroll command When both inputs to NAND gate IC729B are high, the output (pin 6) places a logic 0 on one input (pin 6) of NAND gate IC737B. This forces the output (pin 4) of IC737B to logic 0. A logic 0 on one input (pin 9) of IC722C causes a logic 0 at the output (pin 8), which stops the RAM count up (C.U. ÷20).

During TPU cycle 3, pin 4 of IC724 clears erase flip-flop IC723A and the erasing will stop. Whenever the Erase Page key is pressed (S704-2), the output (pin 3) of open collector buffer IC715A holds the erase flip-flop (IC723A) preset. Erasing 960 characters takes less than 1 millisecond so the screen is totally erased many times while the key is held down. The erase page key presets IC723B, which automatically puts the cursor at the start of page (home) position at the end of the erase. It does this by driving open collector buffer IC715D and forcing a logic 0 at the "cursor home" input (pin 13) of IC728.

CURSOR

The RAM and counter circuit description describes how the cursor moves as a result of a writing operation; however, the cursor can also be moved independently of writing operations by the cursor controls and through some non-writing data coming in on the bus. The cursor controls on the keyboard set latches (on the keyboard) during the scan time. The latch outputs enter the TPU circuit board at P701-1, -2, -3, and -4. They each drive one input of NAND gates IC727A, B, C, and D. When a latch is set, the corres-

ponding input of IC727 goes to a logic 1. Then the next 1C pulse from the TPU, which drives inputs 2, 4, 10, and 12 of IC727, causes the proper output (3, 6, 8, or 11) to go low (logic 0). This counts up the proper RAM counter.

A ÷20 count up (S706-5) moves the cursor to the right, a count down (S706-6) moves it to the left. A ÷12 count up (S707-2) moves the cursor down the screen and a ÷12 count down (S706-12) moves the cursor up the screen. TPU cycle 3 (S707-3) resets all four cursor movement latches on the keyboard circuit board.

Pressing the cursor Home key (S704-3) latches the scroll information, that was loaded into the RAM counters during TPU cycle 7, into the cursor latches on the RAM and counter circuit board. The cursor latches are actually latched by the trailing edge of TPU cycle 7C.

The cursor home signal (a logic 0) from the keyboard circuit board drives input pin 13 of ROM IC728. This causes a logic 1 output from pin 9 (cursor latch enable, S706-1) during TPU cycle 7C. Refer to Timing Diagram #4.

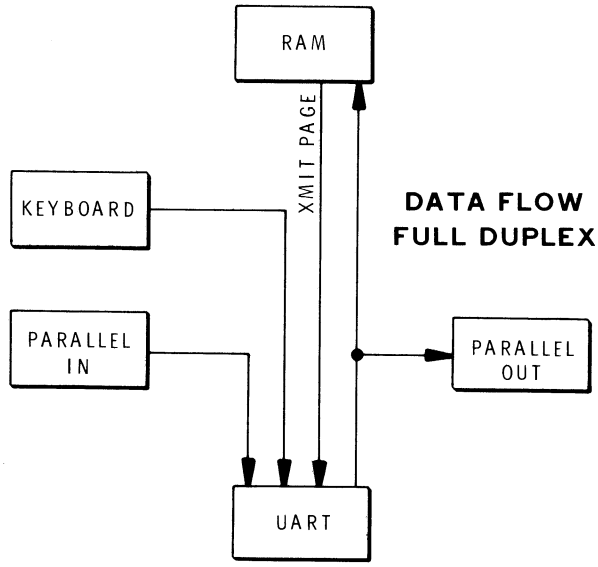
Since the scroll information is also the start of page information, the cursor will automatically appear in the upper left hand corner of the screen. Refer to Timing Diagram #4 for the cursor timing relationships.

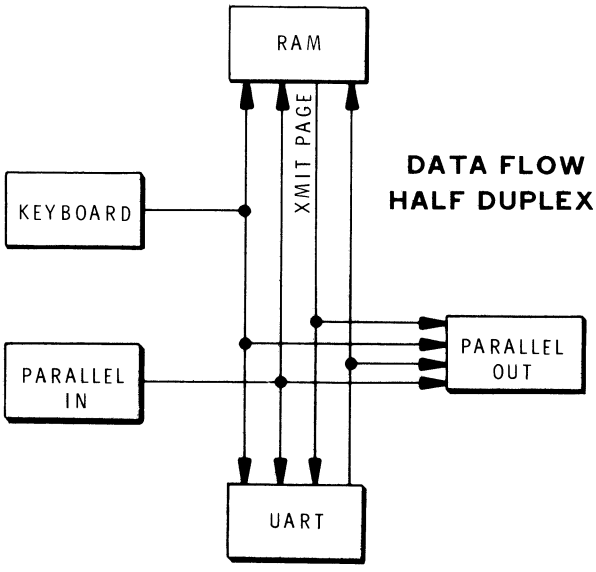
Gates IC716A (NAND) and IC715C (AND) control the ÷12 count up signals coming from the character generator circuit board (S705-5). During scan and at the end of each character row, the D output (S707-2) of the scan row counter counts up the ÷12 counter (IC715 pin 8). However, when the vertical blanking signal appears (Vn' from IC705D pin 13) the count up is defeated (when the pin 2 input to IC716A is logic 0) for the duration of the vertical retrace time. The count up is also defeated when the Terminal is in the plot mode and the first character line is the only one that is displayed. IC722D and IC722C control the RAM count up signal (C.U. ÷20, S705-7) coming from the character generator. During scan the ÷20 counter is counted up by the output (pin 11 of IC722D), but it is inhibited when the vertical blanking signal appears (Vn' at pin 12 of IC722D). During the erase cycle the ÷20 counter is counted up by the output (pin 8) of IC722C as long as the output (pin 4) of IC737B is high (refer to the section on scrolling and erasing). IC722B controls the ÷20 count up for write operations. The ÷20 counter can be inhibited by the ÷20 count up defeat signal coming from the special character latch (IC720 pin 2 and IC708D pin 13) or by the end of line and no auto carry signals (EOL•$\overline{AC}$) coming from IC730 pin 6.

WRITING DATA/DATA FLOW

Data is manipulated within the Terminal primarily by logic array IC702, as a function of where data is coming from, where it is going, the mode the Terminal is in, the TPU timing pulses, and whether or not the external devices are ready to accept data.

Data flows on the bus according to the two diagrams in Pictorial 4-14. All of the devices are tied directly to





PICTORIAL 4-14

the 8-bit bus and the direction of data flow is controlled by turning the appropriate buffers and latches on and off at the proper time in the TPU cycle. When data becomes available from the UART, parallel input, or keyboard, the I/O circuit board sends an appropriate data available signal (DAV_u at S701-3 or DAV_{p+k} at S701-4) to logic array IC702 on the TPU circuit board. The logic array then checks a number of other inputs to determine which buffers and latches on the RAM and counter circuit board, parallel I/O, serial I/O, or keyboard circuit board will be turned on by TPU pulse 0B2 during the write cycle. External devices must be ready to accept new data, that is, the UART transmit-buffer must be empty (XBEU, S701-11) and the parallel output buffer must be empty (XBEP, S701-12).

The special character inputs (pins 1, 2, 8, and 11 to logic array IC702) are also checked to determine whether or not the character on the bus is a valid character. The special character detector is on the I/O circuit board, and its outputs enter the TPU circuit board as follows:

Carriage Return	S701-7
Space	S702-8
Rubout	S702-3
Control Character	S702-2
Line Feed	S701-9
Back Space	S701-8
Bell	S703-12

Control characters and rubouts are not generally written into the RAM unless the plot function is chosen. However, they are always loaded into the UART and the parallel output buffers. In the plot mode, all characters are written into the RAM. In the normal mode, the only control character that can be written into the RAM is a carriage return, but only if there is a space at the cursor location. Flip-flop IC704B checks for a space indication before the carriage return is written.

After all input conditions have settled, TPU cycle 0B2 enables the RAM, parallel, and UART outputs appropriately at pins 13 (ANDed with the 4800 Baud clock), 14 (load parallel), and 17 (re-select RAM) of IC702. See Pictorial 4-15 for a summary of how special characters are loaded to and from the bus.

CHARACTER	DOES CHARACTER LOAD INTO — RAM	UART	PARALLEL OUT	CURSOR MOVEMENT
ALL CONTROL CHARACTERS *	NORMAL - No Plot - Yes	Yes	Yes	Normal - None Plot - One space to right
* Except for: CARRIAGE RETURN	Normal - Yes If space, Plot - Yes	Yes	Yes	Normal - To start of line Plot - one space to right
LINE FEED	Normal - No Plot - Yes	Yes	Yes	Normal - Down one line Plot - One space to right
BACK SPACE	Normal - No Plot - Yes	Yes	Yes	Normal - One space to left Plot - one space to right
BELL	Normal - No Plot - Yes	Yes	Yes	Normal - None Plot - One space to right } Bell Rings
RUBOUT	Normal - No Plot - Yes	Yes	Yes	Normal - None Plot - One space ro right

PICTORIAL 4-15

SPECIAL CURSOR MOVEMENTS

Whenever the logic array (IC702) moves things around on the bus in response to a data available signal, the TPU assumes that a write operation has been performed and it automatically counts the cursor to the next RAM location.

The two inputs to IC713C monitor the two data available signals (DAV_u and DAV_{p+k}) coming from the I/O circuit board. If either goes high, pin 8 of IC713C goes low. This causes the output (pin 8) of NAND gate IC719C to go high. This is the internal DAV signal that is ANDed with various TPU cycles to generate 0C if DAV, 1C if DAV, and 0B2 if DAV. The 1C if DAV signal (from IC734 pin 6) drives one input (pin 4) of IC722B. The other input (pin 5) is normally high (it goes low to defeat the count up) and the output (pin 6) goes low to count up the ÷20 RAM counter.

If a control character or rubout was put on the bus, the CC+R output (from pin 18 of the logic array) is latched into flip-flop IC720A. The Q output (pin 2) of this flip-flop disables the cursor count up (C.U. ÷20) through IC708D and IC729A. In addition, if the special character was a carriage return, line feed, or back space, an additional signal is latched into one of the flip-flops of IC720 and the appropriate Q output is ANDed with TPU cycle 1C (in IC740D, IC721C, and IC721D) to perform the appropriate cursor movement. If the character is a carriage return, the ÷20 counter is cleared (S706-7). If it was a line feed, the ÷12 counter is counted up (S707-2); or if it was a back space, the ÷20 counter is counted down (S706-6).

REFRESH INTERRUPT

Normally, the Terminal handles data at a rate of one character per vertical retrace period, or sixty characters per second (600 BAUD). IC705A, IC705D, IC706B, and IC718B form a circuit that interrupts the screen refresh and starts an extended TPU cycle whenever data appears at rates greater than 600 BAUD. One input (pin 2) of IC705A is tied to a logic 0 (through the rear panel BAUD rate switch) whenever the BAUD rate is greater than 600. The refresh interrupt signal coming from the I/O circuit board (S703-3) appears at pin 3 of IC705A and it goes low whenever data is available from the UART or the parallel interface. This causes a logic 1 to appear at the data input of IC706B. The next time that the A_s, B_s, and C_s inputs (S703-7, -8, & -9) of IC718B go low, the output goes high. This clocks the logic 1 at the D input through IC706B and starts an artificial vertical retrace period through IC705D (pin 13). This stops the screen refresh cycle and the TPU can service the incoming data within approximately one-half millisecond. It stops the cycle by stopping the count ups and blanking the screen. The ÷12 count up is defeated by forcing an input (pin 2) of IC716A to a logic 0. The screen is blanked by sending a logic 0 (Vn') to the character generator circuit board (S703-1). This artificial vertical cycle continues until flip-flop IC706B is reset by the "real" vertical retrace signal (Vp) coming from the character generator circuit board (S703-2) ANDed with TPU cycle $\overline{1}$. After the flip-flop is reset, the normal TPU cycle continues under the control of the vertical retrace signal coming from the character generator circuit board.

TRANSMIT PAGE

During the transmit page mode, the TPU reads a character from the RAM at the current cursor address and loads it into the UART and parallel output buffers. In half duplex, it waits for the transmit buffers to empty. In full duplex, it waits for the buffers to empty and it also waits for the character to be echoed back. When these conditions are satisfied, the TPU counts the cursor to the next RAM location. This process is repeated until the cursor reaches the end of the page. When the last character has been sent, and the cursor has been counted up to the start of page position, the TPU senses that a scroll possibility exists, so it turns off the transmit page mode without performing the scrolling operation.

The Transmit Page button on the keyboard (S704-9) initiates the process by setting flip-flops IC731C, IC731D during TPU cycle 7C. The $\overline{Q}$ output (pin 8) signals to logic array IC702 that the transmit page mode should begin. On the next TPU 0B2 cycle (0B2 comes from pin 3 of IC710), the logic array loads data from the RAM location addressed by the cursor into the parallel and UART output buffers. Simultaneously, it sets flip-flop IC704A to indicate that a character has been transmitted. The $\overline{Q}$ output of IC704A inhibits any further character transmissions until the cursor has been counted to the next RAM location. In half duplex, the cursor is counted up automatically during TPU cycle 1C. In full duplex, the character must be echoed back from the external device and then counted up. The automatic count up happens whenever there is a DAV signal. For half duplex, a "fake" DAV signal is generated by IC725A. (The duplex button drives the D input of IC725A.) In half duplex, a logic 1 appears at the D input, while in

duplex, a logic 0 appears at the D input. The load pulse (0B2•XP•LOAD) from pin 15 of the logic array clocks the level at the D input through flip-flop IC725A. The $\overline{Q}$ output (pin 6) goes low if the duplex switch is up, which forces pin 8 of IC719C to go high — indicating "DAV." In full duplex the fake DAV does not occur, so the count up has to wait for the character to be echoed back through the UART.

Flip-flop IC725A is reset by pin 16 of the logic array as a function of the count up signal and the duplex button. After the flip-flop has been cleared, another character will be transmitted on the next 0B2 TPU cycle. When the cursor encounters a carriage return stored in a RAM location, the ÷20 cursor count up is inhibited as before, and the ÷20 counter is cleared. At the same time, the carriage return output from special character latch IC720 (pin 7) is clocked into flip-flop IC738A by the 0B2•XP•LOAD pulse. This is called the carriage return flip-flop and the Q output (pin 5) is referred to on the Schematic as CRFF. On the next 0B2•XP•LOAD cycle the Q output addresses pin 9 of the logic array, which prevents a character from being loaded from the RAM. Instead, it puts a line feed character on the bus via IC707B, IC719A, IC726A, IC726B, and IC726D. The A1 and A2 outputs (S704-4 and S704-8) of these decoding gates turn on the special character generator on the keyboard.

When the TPU senses that the cursor has reached the end of a line and it has not yet encountered and transmitted a carriage return and that the auto carry button is not pressed, flip-flop IC738B is set and further character loads from the RAM are inhibited. IC714B monitors the $\overline{CR}$ output (pin 6) of special character latch IC720 and the EOL•$\overline{AC}$ output (pin 5) of RAM IC730.

When both inputs of IC714B are high, pin 6 goes high. This means end of line•no auto carry•no carriage return. The logic 1 is clocked into flip-flop IC738B by the 0B2•XP•LOAD pulse. On the next 0B2 load cycle, the $\overline{Q}$ output (pin 8) of this flip-flop causes a carriage return to be put on the bus by outputs A1 and A2. IC738A senses the carriage return and is set by the 0B2•XP•LOAD pulse. The next 0B2•XP•LOAD pulse causes a line feed to be sent. Flip-flop IC738A is reset by the output of NAND gate IC721B. The output of IC721B goes low for line feed (from pin 10 of IC720) and TPU cycle 1C (from pin 4 of IC728). As soon as the flip-flop is cleared, the character transmission cycle can start again for the new line.

When the cursor reaches the end of the page and after it has been counted up to the start of page position, a scroll possibility exists and a scroll command is generated. However, since the $\overline{Q}$ output (pin 8) of the transmit page flip-flop (IC731C and IC731D) appears at one input (pin 2) of IC741A, the scroll is inhibited. The scroll command does, however, preset flip-flop IC725B, which, in turn, lets the next 7C TPU cycle reset the transmit page flip-flop, terminating the transmit page mode. IC725B is then reset by the next TPU 0 cycle.

BELL DETECT

IC716B and IC718A decode the outputs of the ÷20 cursor latch (P702-1, -2, -3, -4, and -5) to determine when the cursor is in position number thirteen (seven from the end) of the 20 character block. This information is ANDed in IC716C and IC735C with the end of line signal (from pin 9 of IC730), the data available keyboard signal (S702-6), and TPU cycle 1C. The output (pin 10) of IC735C triggers monostable IC736, which, in turn, enables pin 1 of speaker driver IC742A for approximately 30 milliseconds. The 300 BAUD rate clock then drives the speaker through IC742A.

The end of line signal operates only from the keyboard. IC742B ANDs the bell signal from the I/O circuit board (S703-12) with TPU cycle 0B2DAV. It also triggers the monostable whenever an ASCII bell signal (or control G) is detected during a write cycle.

POWER UP RESET

When the Terminal is first turned on, Q701 and IC717A generate a positive going pulse, approximately 200 milliseconds wide, that is used for a power up reset. Capacitor C719 is totally discharged before power is turned on. When the 5-volt supply comes on, C719 begins to charge through resistor R725 and the base of Q701. This turns Q701 on and causes a logic 1 to appear at the output (pin 2) of IC717A. As the charging current decays, Q701 turns off and the output of IC717A drops back to a logic 0. R728 applies positive feedback to the base of Q701 to speed the transition between logic states. The positive going pulse is used to initialize the UART (UART XR, S702-9). IC717D inverts the reset pulse and holds the erase flip-flop, IC723, cleared for the duration of the 200 millisecond pulse. This causes a page erase. IC717E inverts the pulse and momentarily puts the Terminal in the short form mode. This clears the ÷4 scroll counter and puts character block zero at the left hand side of the screen. IC717C and IC717B also invert the reset pulse and then clear the transmit page and carriage return flip-flops.

I/O (Input/Output)

The I/O (input/output) circuit board handles all data transfers between the Terminal and all external devices, such as a reader/punch or a digital computer. See Pictorial 4-16 (Illustration Booklet, Page 11). These circuits contain separate 8-bit parallel input and output ports and a 4-bit parallel handshake. It also contains a serial input, serial output, and a UART (universal asynchronous receiver/transmitter) circuit that interfaces the 8-bit parallel system bus with the serial I/O ports. A special character detector, a baud rate generator, a data priority latch, and a reader start-stop control are also located on the I/O circuit board.

The parallel input connects to the master ASCII bus through IC620, an octal tri-state buffer that is normally turned off. An external device can signal to the Terminal that there is parallel data available at the parallel input by setting the $\overline{DAV}_i$ input to zero. This causes a logic 1 to appear at the data input of IC616, the data priority latch. At the start of the TPU cycle, the logic 1 is clocked through the latch and into a priority encoder, IC's 611C, 619A, 619B. The priority encoder permits only one data available signal (DAV) to be transmitted to the TPU at a given time. The UART data available signal (DAV_u) has the highest priority, the parallel data available (DAV_p) is next, and the keyboard data available signal (DAV_k) has the lowest priority. The TPU reacts to the parallel DAV signal by turning on the outputs of the tri-state buffers, IC620. This puts the parallel input data on the master bus, which allows it to be written into the RAM at the cursor location.

When the Terminal is finished writing the parallel input data into the RAM, it tells the external device that it is finished by transmitting a negative going pulse on the $\overline{RDAV}_i$ output.

If the Terminal has data to transmit to an external device, it will first load that data from the bus into parallel output latches IC621 and IC622. It then transmits a $\overline{DAV}_0$ signal to the external device by setting flip-flop IC618B. When the external device has finished reading the data, a negative-going pulse is transmitted to the $\overline{RDAV}_0$ input.

The serial input and output can be jumper-wired for standard TTL. EIA, or TTY (20 mA current loop) input and output signals. The two logic states of a serial input or output are called a "mark" and a "space." A mark is defined as a TTL logic 1, an EIA minus voltage, or 20 milliamperes flowing in the current loop. A space is defined as a TTL zero, and EIA positive voltage, or zero current flowing in the 20 mA current loop. The idle state of both the input and output is defined as a mark.

Pictorial 4-17 (Illustration Booklet, Page 12) shows EIA input connections. In its idle state, the EIA input is a negative voltage and it keeps transistor Q603 biased off. Since the collector voltage of the transistor is 5 volts, it places a logic 1 at the input (pin 20) of the UART. When the EIA input voltage goes high, Q603 turns on and its collector voltage goes low. This places a space (logic 0) at the input of the UART. The serial output from the UART (pin 25) drives IC609A, which, in turn, drives IC609B. The output of IC609B drives opto-isolator IC604. When the output is a mark, the photo transistor in IC604 turns off and Q602, a constant current source, turns Q601 on. The current flows from the +12-volt supply through R631 and Q601 to the −12-volt supply. This makes the EIA output approximately −10 to −12 volts. As the output of IC609B goes low, the LED (light emitting diode) in the opto-isolator turns on the photo transistor, which turns Q601 off. This causes the EIA output to go to approximately +12 volts.

Refer to Pictorial 4-18 (Illustration Booklet, Page 12) for the 20 mA current loop connections. When a mark is applied, loop current passes through diode D601 and opto-isolator IC605, which turns Q603 off. A logic 1 then appears at the serial input to the UART. When the loop current changes to a space (or zero current), the photo transistor turns off and Q603 turns on. A logic 0 then appears at the serial input to the UART. The reader start/stop circuitry works in exactly the same manner. It is composed of opto-isolator IC606 and transistor Q604. As long as there is a mark current flowing in the loop, the collector of Q604 is high. This tells the TPU that the external device wishes to see another character.

Refer to Pictorial 4-19 (Illustration Booklet, Page 13) for TTL I/O connections. A TTL input signal is coupled to pins 9 and 10 of IC609C. The output of IC609C drives IC609D, which drives the serial input of the UART. The TTL output signal comes directly from the output of IC609B.

The input labeled "break" at pin 2 of IC609A generates a continuous space at the serial output as long as the break key on the keyboard is pressed. The "off line" input at pin 5 of IC609B causes a continuous mark to be generated at both the serial output and the serial input. This effectively inhibits the Terminal from either transmitting or receiving.

IC602 successively divides the 4800 baud rate clock by two to produce the 2400, 1200, 600, and 300 baud rate clocks. IC601, in conjunction with IC607A and IC608A, divides the 1200 baud rate clock by 11 to generate the 110 baud rate clock. One of the baud rate clocks (600 - 9600) can be jumper-connected to the "preset baud out" from the I/O circuit board. This output and the 300 baud rate output are connected to Baud rate switch, SW2, on the back panel of the Terminal. This switch selects either 300 baud or the preset baud rate. IC607B, IC607C, and IC607D, in conjunction with the keyboard baud rate key drive the clock pulse inputs of the UART with either 110 baud or the baud rate selected by the Baud Rate switch.

Integrated circuits IC613, IC614, IC617, IC623, IC624C, and IC624D form a special character detector that monitors the ASCII bus to detect the presence of certain special characters. IC613 and IC617A detect a rubout and a control character, respectively. The remaining IC's detect a Back Space, Line Feed, Bell, Space, and Carriage Return. These outputs are used by the TPU for cursor movements and sepcial writing operations.

SEMICONDUCTOR IDENTIFICATION

This section is divided into three parts; Component Number Index, Part Number Index, and ROM and PLA Programs. The first section provides a cross-reference between semiconductor component numbers and their respective Part Numbers. The component numbers are listed in numerical order. The second section provides a lead configuration detail (basing diagram) for each semiconductor Part Number. The Part Numbers in the second section are also listed in numerical order. The third section provides a program for each of the four specially "programmed" integrated circuits.

COMPONENT NUMBER INDEX

This index shows the Part number of each semiconductor in the Terminal.

DIODES

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
D1	56-56
D2	56-26
D101-D104	57-42
D105-D109	57-27
D111-D112	57-27
D301, D302	56-56
D303	56-73
D304	57-27
D305-D307	57-64
D401-D404	56-56

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
D401	56-26
D402	56-56
D501	56-87
D501	56-87
D601	57-65
D602	56-26
D603	57-65
D604	56-56
D605	57-65

TRANSISTORS

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
Q1	417-894
Q101	417-899
Q102	417-819
Q201	417-881
Q301	417-864
Q302	417-235
Q303	417-881
Q304	417-864
Q305	417-818

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
Q306	417-819
Q307	417-818
Q308	417-875
Q309	417-874
Q401	417-801
Q601	417-865
Q602	417-897
Q603, Q604	417-801
Q701	417-801

INTEGRATED CIRCUITS

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
IC101, IC102	442-54
IC103	442-609
IC104	442-644
IC105	442-618
IC201	443-745
IC202, IC203	443-752
IC204	443-814
IC205	443-812
IC206	443-719
IC207, IC208	443-730
IC209	443-719
IC210	443-26
IC211	443-730
IC212	443-755
IC213	443-612
IC214, IC215	443-813
IC216	443-838
IC217	443-780
IC218	443-728
IC219	443-755
IC220	443-813
IC221	443-46
IC222	443-12
IC301	442-620
IC401	443-838
IC402	443-767
IC403	443-754
IC404, IC405	443-811
IC406	443-779
IC407, IC408	443-728

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
IC501	443-781
IC502	443-817
IC503	443-719
IC504	443-728
IC505	443-745
IC506	443-5
IC507	443-764
IC508	443-719
IC509	443-4
IC510	443-800
IC511	443-745
IC512	443-779
IC513	443-815
IC514	443-745
IC515	443-816
IC516	443-764
IC517	443-728
IC518	443-781
IC519	443-815
IC520	443-719
IC521	443-781
IC522	443-733
IC523	443-728
IC524	443-797
IC525	443-798
IC526	443-780
IC527	443-779
IC528	443-728
IC529, IC530	443-745

Integrated Circuits (cont'd.)

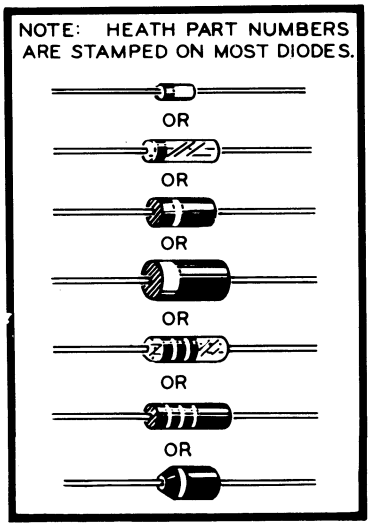
CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
IC601, IC602	443-733
IC603	443-791
IC604-IC606	443-808
IC607	443-745
IC608	443-728
IC609	443-1
IC610	443-779
IC611	443-728
IC612	443-761
IC613	443-732
IC614	443-807
IC615	443-780
IC616	443-752
IC617	443-779
IC618	443-730
IC619	443-797
IC620	443-791
IC621, IC622	443-752
IC623	443-807
IC624	443-779
IC701	443-780
IC702	443-787
IC703	443-728
IC704	443-730
IC705	443-779
IC706	443-730
IC707	443-797
IC708	443-779
IC709	443-730
IC710	443-780
IC711	443-728

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
IC712	443-807
IC713	443-800
IC714	443-780
IC715	443-816
IC716	443-797
IC717	443-818
IC718	443-800
IC719	443-728
IC720	443-752
IC721, IC722	443-745
IC723	443-730
IC724	444-12
IC725	443-730
IC726	443-728
IC727	443-745
IC728	444-10
IC729	443-780
IC730	444-11
IC731, IC732	443-728
IC733	443-745
IC734	443-780
IC735	443-779
IC736	443-22
IC737	443-779
IC738	443-730
IC739-IC741	443-728
IC742	443-745

PART NUMBER INDEX

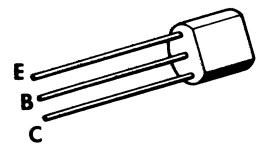
This index shows a load configuration detail (basing diagram) of each semiconductor Part Number.

DIODES

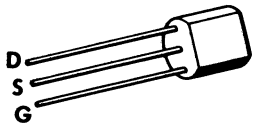
HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
56-26	1N191	GE DIODE 45 mA, 90 V	
56-56	1N4149	SI DIODE 10 mA, 75 V	
56-73	MZ2360	COMPENSATING DIODE	
56-87	FH1100	SI, HOT CARRIER 10 mA, 5 V	
57-27	1N2071	SI RECT. 1 A, 600 V	
57-42	3A1	SI RECT. 3 A, 100 V	
57-64	DRS-110	SI RECT. 1 A, 1000 V	
57-65	1N4002	SI RECT. 1 A, 100 V	

TRANSISTORS

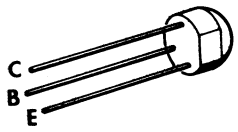
HEATH PART NUMBER	MAY BE REPLACED WITH	BASING DIAGRAM
417-874 417-875 417-235	2N3906 2N3904 2N4121	A A A or C
417-801	MPSA20	A
417-818	MJE181	D
417-819	MJE171	D
417-864	MPSA05	A
417-865	MPSA55	A
417-881	MPSA13	A
417-894	BU180A	E
417-897	HEATH 417-897 ONLY	B
417-899	MJ2955	F



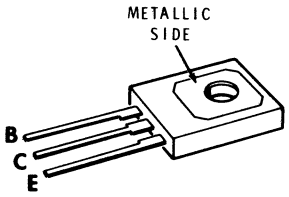
A



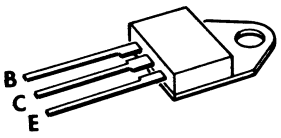
B



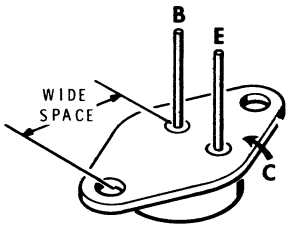
C



D

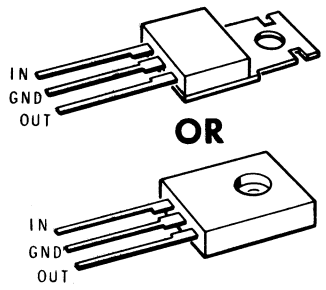
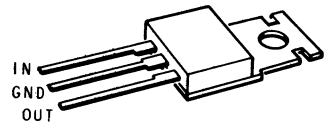
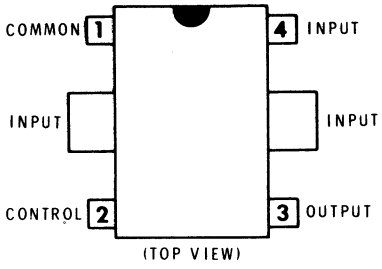
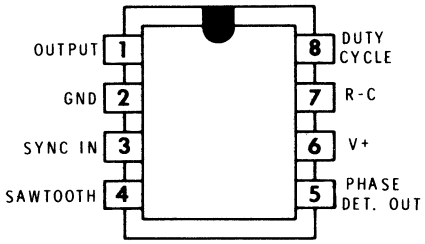
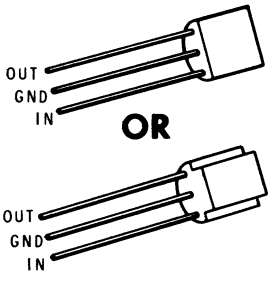


E

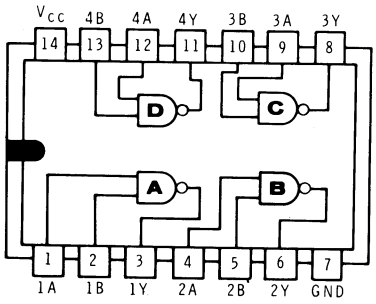
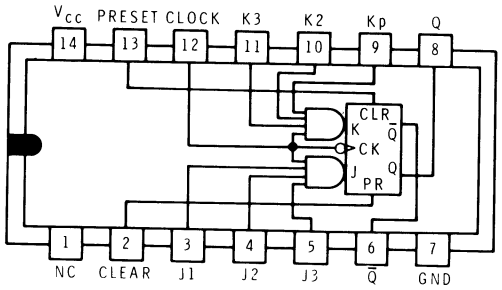
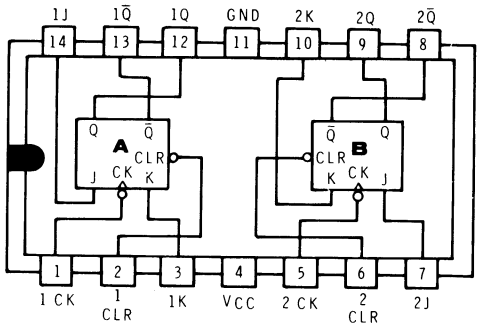
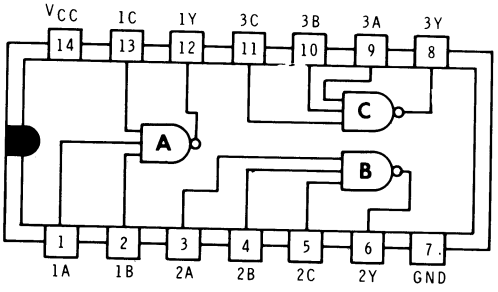


F

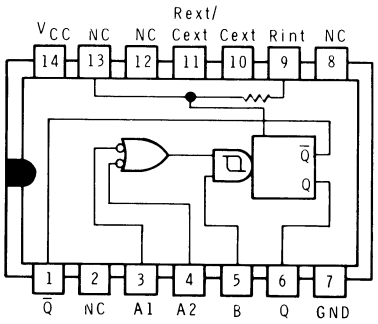
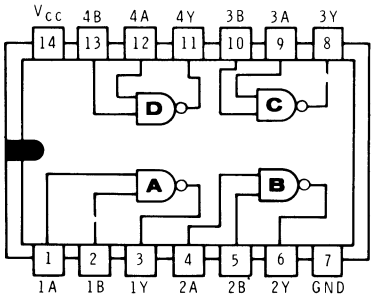
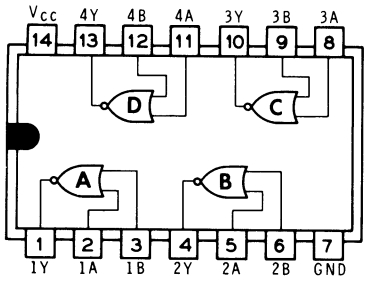
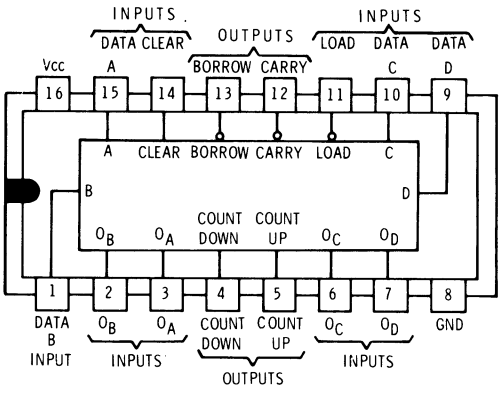
INTEGRATED CIRCUITS

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
442-54	7805	5-VOLT REGULATOR	
442-609	78M20C	20-VOLT REGULATOR	
442-618	79MG	−2.2/−30 VOLT REGULATOR	
442-620	1391	PHASE-LOCKED LOOP OSCILLATOR	
442-644	78L12	12-VOLT REGULATOR	

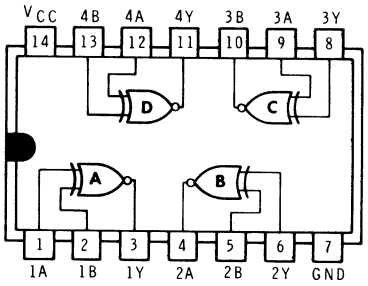
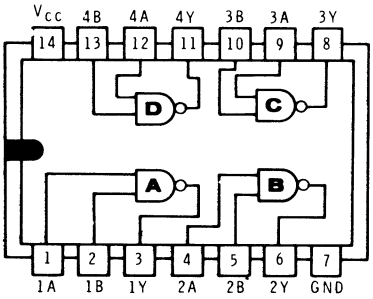
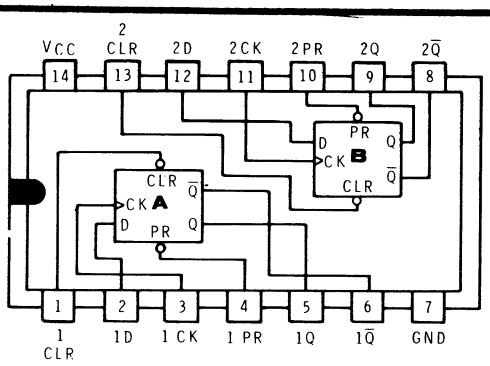
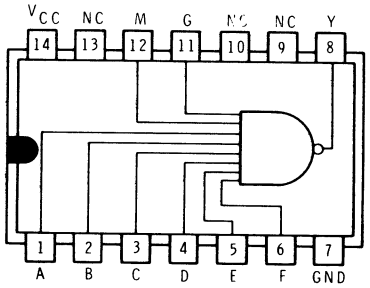
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-1	7400	QUADRUPLE 2-INPUT POSITIVE NAND GATE	
443-4	7472	AND-GATED J-K MASTER SLAVE FLIP-FLOP WITH PRESET AND CLEAR	
443-5	7473	DUAL J-K FLIP-FLOP WITH CLEAR	
443-12	7410	TRIPLE 3-INPUT POSITIVE-NAND GATE	

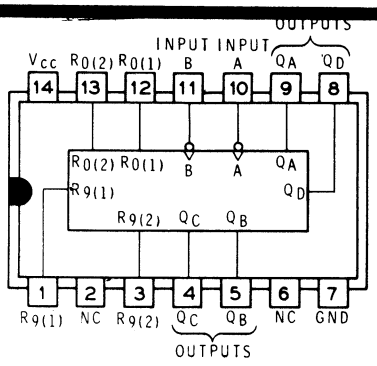
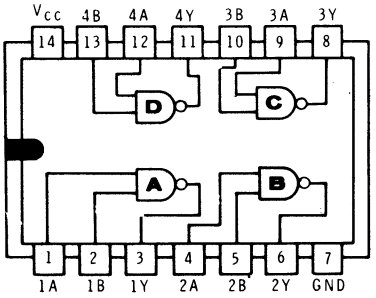
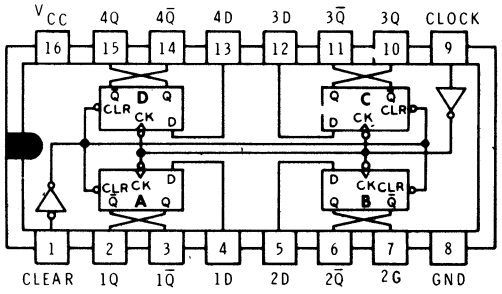
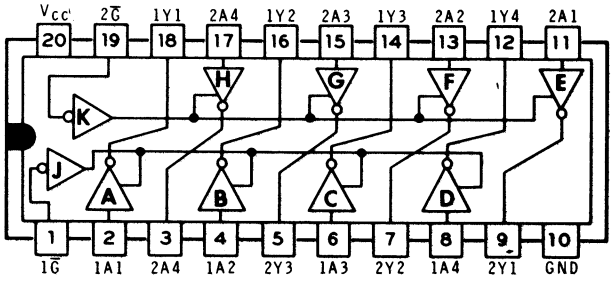
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-22	74121	MONOSTABLE MULTIVIBRATOR	
443-26	74S00	QUADRUPLE 2-INPUT POSITIVE-NAND GATE	
443-46	7402	QUADRUPLE 2-INPUT POSITIVE-NOR GATE	
443-612	74193	SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTER BINARY WITH CLEAR	

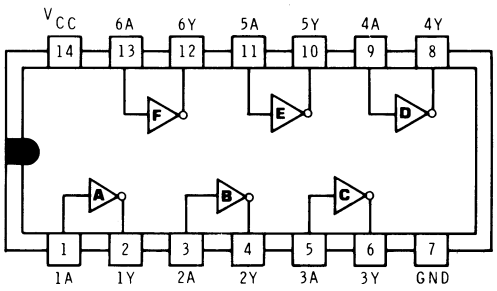
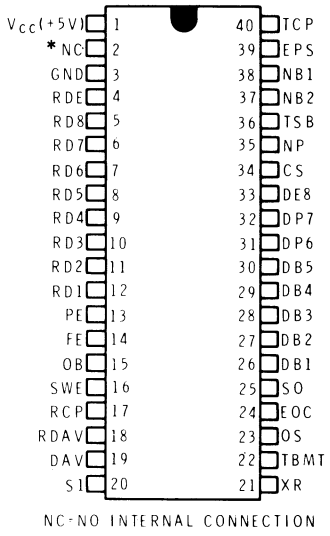
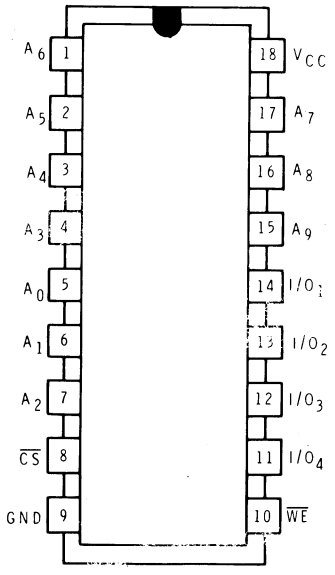
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-719	74LS266	QUAD 2-INPUT EXCLUSIVE-NOR GATE WITH OPEN-COLLECTOR OUTPUTS	
443-728	74LS00	QUADRUPLE 2-INPUT POSITIVE-NAND GATE	
443-730	74LS74	DUAL D-TYPE POSITIVE-EDGE TRIGGERED FLIP-FLOP WITH PRESET AND CLEAR	
443-732	74LS30	8-INPUT POSITIVE-NAND GATE	

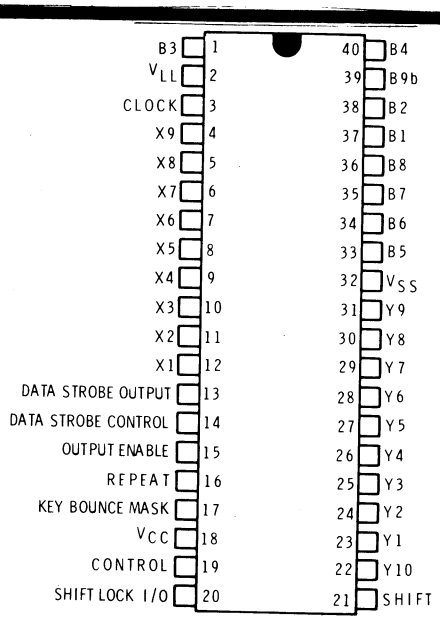
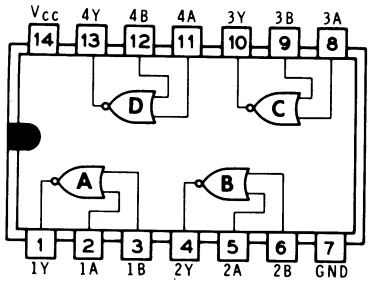
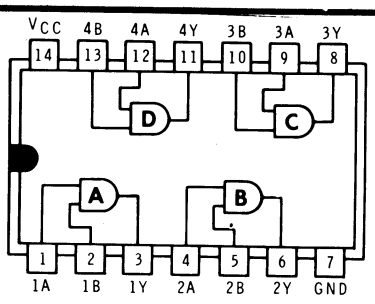
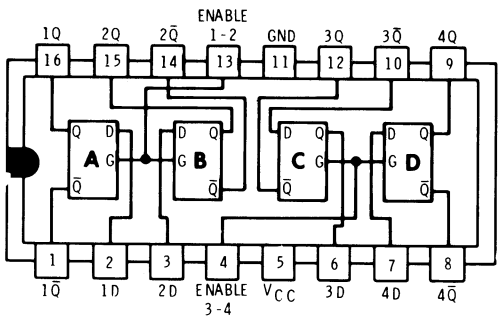
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-733	74LS293	DIVIDE-BY-TWO AND DIVIDE-BY-EIGHT 4-BIT BINARY COUNTER	
443-745	74LS03	QUADRUPLE 2-INPUT POSITIVE-NAND GATE WITH OPEN COLLECTOR OUTPUT	
443-752	74LS175	QUAD-TYPE FLIP-FLOP COMPLEMENTARY OUTPUTS COMMON DIRECT CLEAR	
443-754	74LS240	OCTAL BUFFERS/LINE DRIVERS/ LINE RECEIVERS INVERTED 3-STATE OUTPUTS	

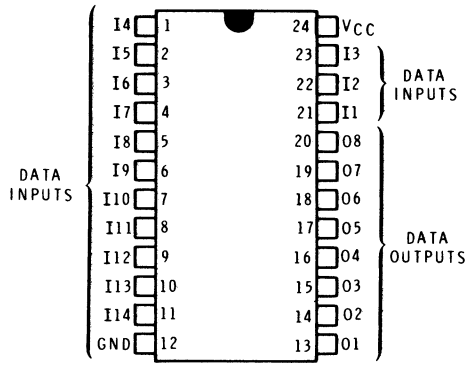
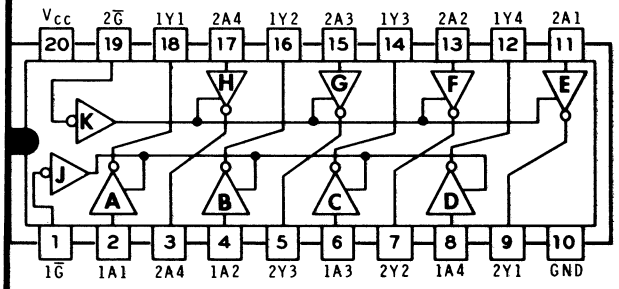
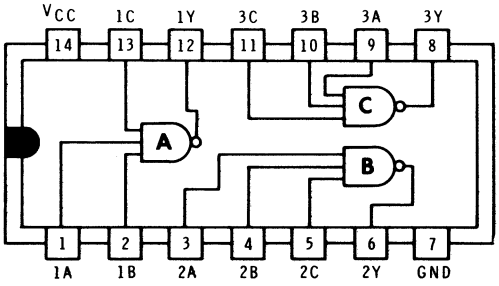
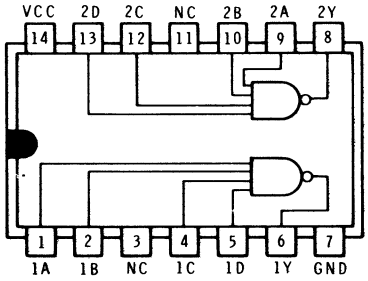
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-755	74LS04	HEX INVERTER	
443-859	AY-3-1015 TMS6011N IM6402	UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER	 NC-NO INTERNAL CONNECTION
443-764	2114	4 K (1024 × 4) STATIC RAM	

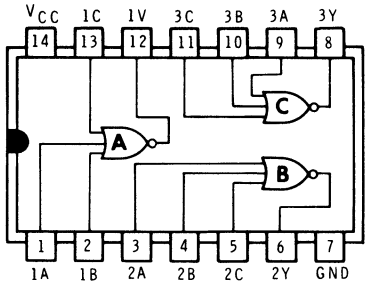
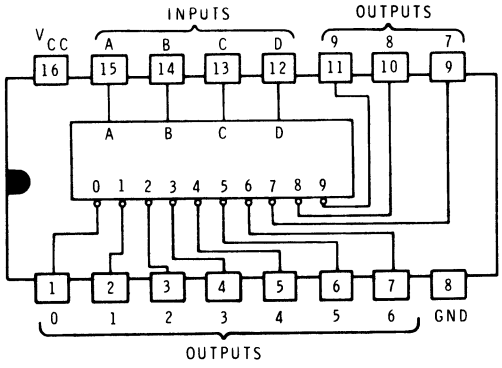
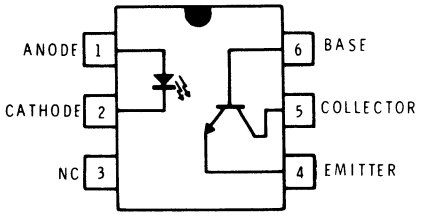
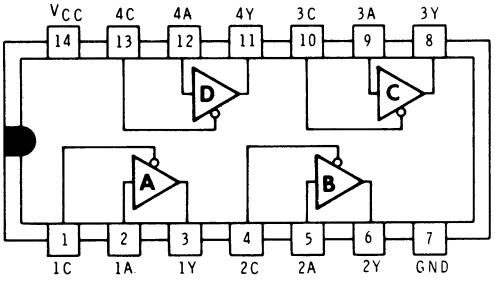
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-767	MM5740	KEYBOARD ENCODER	
443-779	74LS02	QUADRUPLE 2-INPUT POSITIVE-NOR GATE	
443-780	74LS08	QUADRUPLE 2-INPUT POSITIVE-AND GATE	
443-781	74LS75	4-BIT BISTABLE LATCH	

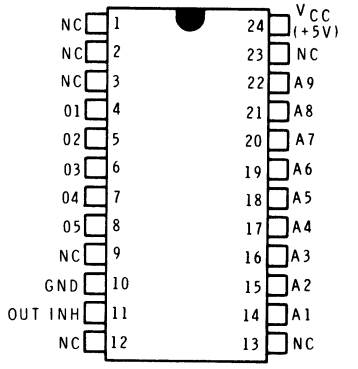
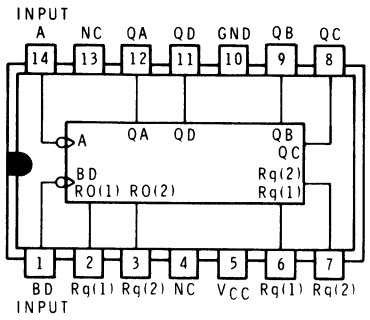
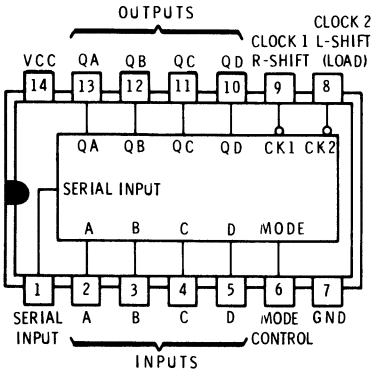
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-787	DM8575	PROGRAMMED LOGIC ARRAY	
443-791	74LS244	OCTAL BUFFERS/LINE DRIVERS/ LINE RECEIVERS NONINVERTED 3-STATE OUTPUTS	
443-797	74LS10	TRIPLE 3-INPUT POSITIVE-NAND GATE	
443-798	74LS20	DUAL 4-INPUT POSITIVE-NAND GATE	

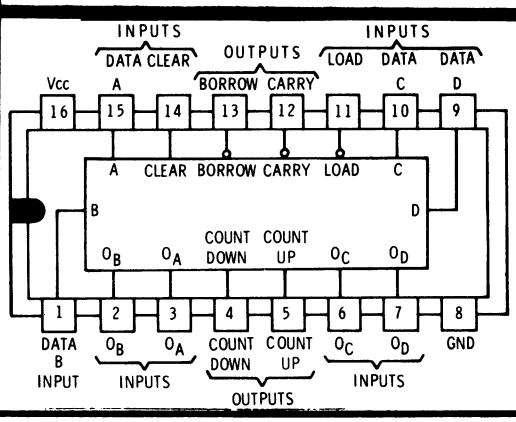
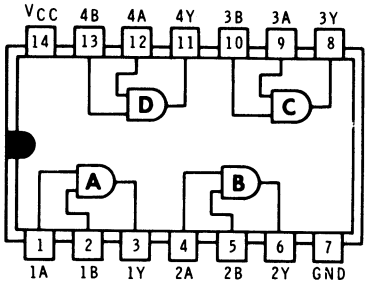
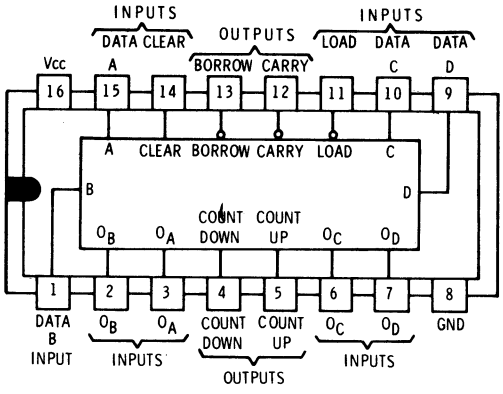
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-800	74LS27	TRIPLE 3-INPUT POSITIVE-NOR GATE	
443-807	74LS42	BCD-TO-DECIMAL DECODER	
443-808	4N26	PHOTOTRANSISTOR OPTO-COUPLER	
443-811	74LS125	QUADRUPLE BUS BUFFER GATE WITH THREE STATE OUTPUTS	

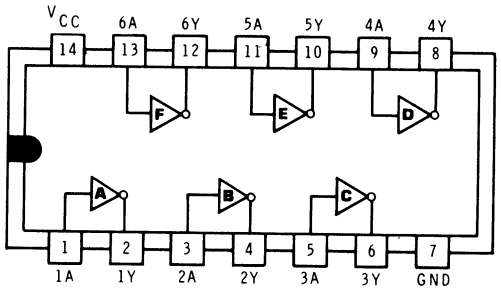
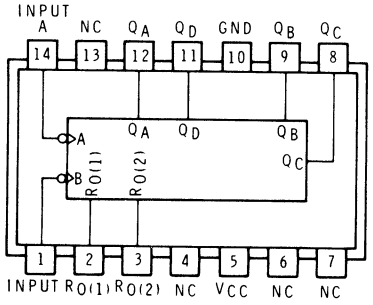
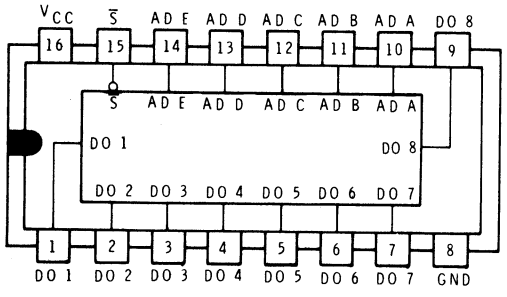
Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-812	R032513	CHARACTER GENERATOR	
443-813	74LS90	DECADE COUNTER	
443-814	74LS95	4-BIT SHIFT REGISTER	

Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-815	74LS193	SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTER BINARY WITH CLEAR	
443-816	74LS09	QUADRUPLE 2-INPUT POSITIVE-AND GATE WITH OPEN-COLLECTOR OUTPUTS	
443-817	74LS192	SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTER BCD WITH CLEAR	

Integrated Circuits (cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-818	74LS05	HEX INVERTER WITH OPEN-COLLECTOR OUTPUTS	
443-838	74LS93	4-BIT BINARY COUNTER	
444-10 444-11 444-12		256-BIT READ-ONLY MEMORIES	

ROM AND PLA PROGRAMS

This section contains a PLA (Programmed Logic Array) program and three ROM (Read Only Memory) programs.

ROM PROGRAM

444-12 IC724

ADDRESS

Logic Term	SCROLL COMMAND	6 ⊓⊔	3 ⊓⊔	÷4 → ÷12 SUB	÷20 → ÷4
Input	E	D	C	B	A
Pin #	14	13	12	11	10
	0	0	0	0	0
	0	0	0	0	1
	0	0	0	1	0
	0	0	0	1	1
	0	0	1	0	0
	0	0	1	0	1
	0	0	1	1	0
	0	0	1	1	1
	0	1	0	0	0
	0	1	0	0	1
	0	1	0	1	0
	0	1	0	1	1
	0	1	1	0	0
	0	1	1	0	1
	0	1	1	1	0
	0	1	1	1	1
	1	0	0	0	0
	1	0	0	0	1
	1	0	0	1	0
	1	0	0	1	1
	1	0	1	0	0
	1	0	1	0	1
	1	0	1	1	0
	1	0	1	1	1
	1	1	0	0	0
	1	1	0	0	1
	1	1	0	1	0
	1	1	0	1	1
	1	1	1	0	0
	1	1	1	0	1
	1	1	1	1	0
	1	1	1	1	1

DATA

Logic Term	DON'T CARE			FORCE AC	CLEAR ERASE FF	÷12/4 SCROLL C.U.	÷4 → ÷12	÷12 → ÷4
Output	8	7	6	5	4	3	2	1
Pin #	9	7	6	5	4	3	2	1
				0	0	1	0	0
				0	0	1	0	0
				0	0	1	0	0
				0	0	1	0	0
				0	0	0	0	0
				0	0	0	0	0
				0	0	0	0	0
				0	0	0	0	0
				0	1	1	0	0
				0	1	1	0	0
				0	1	1	0	0
				0	1	1	0	0
				0	1	0	0	0
				0	1	0	0	0
				0	1	0	0	0
				0	1	0	0	0
				1	0	0	0	1
				1	0	0	0	0
				1	0	0	1	1
				1	0	0	1	0
				1	1	0	0	1
				1	1	0	0	0
				1	1	0	1	1
				1	1	0	1	0
				1	0	0	0	1
				1	0	0	0	0
				1	0	0	1	1
				1	0	0	1	0
				1	1	0	0	1
				1	1	0	0	0
				1	1	0	1	1
				1	1	0	1	0

ROM PROGRAM

444-11 IC730

ADDRESS

Logic Term	AUTO CARRY	÷20 EOL	SHORT FORM	VN'	÷4 EOL
Input	E	D	C	B	A
PIN #	14	13	12	11	10
	0	0	0	0	0
	0	0	0	0	1
	0	0	0	1	0
	0	0	0	1	1
	0	0	1	0	0
	0	0	1	0	1
	0	0	1	1	0
	0	0	1	1	1
	0	1	0	0	0
	0	1	0	0	1
	0	1	0	1	0
	0	1	0	1	1
	0	1	1	0	0
	0	1	1	0	1
	0	1	1	1	0
	0	1	1	1	1
	1	0	0	0	0
	1	0	0	0	1
	1	0	0	1	0
	1	0	0	1	1
	1	0	1	0	0
	1	0	1	0	1
	1	0	1	1	0
	1	0	1	1	1
	1	1	0	0	0
	1	1	0	0	1
	1	1	0	1	0
	1	1	0	1	1
	1	1	1	0	0
	1	1	1	0	1
	1	1	1	1	0
	1	1	1	1	1

DATA

Logic Term	$\overline{\div 4\ EOL} \cdot SF$	EOL	$\overline{EOL \cdot \overline{AC}}$	$EOL \cdot \overline{AC}$	÷20 → ÷4	÷4 → ÷12	÷20 → ÷12	$\overline{SF}$
Output	8	7	6	5	4	3	2	1
Pin #	9	7	6	5	4	3	2	1
	0	0	1	0	1	0	0	1
	0	0	1	0	1	0	0	1
	0	0	1	0	0	0	1	1
	0	0	1	0	0	0	1	1
	0	0	1	0	1	0	0	0
	1	0	1	0	1	0	0	0
	0	0	1	0	1	1	0	0
	1	0	1	0	1	1	0	0
	0	1	1	0	1	0	0	1
	0	1	1	0	1	0	0	1
	0	1	1	0	0	0	1	1
	0	1	1	0	0	0	1	1
	0	1	1	0	1	0	0	0
	1	0	1	0	1	0	0	0
	0	1	1	0	1	1	0	0
	1	0	1	0	1	1	0	0
	0	0	1	0	1	0	0	1
	0	0	1	0	1	0	0	1
	0	0	1	0	0	0	0	1
	0	0	1	0	0	0	0	1
	0	0	1	0	1	0	0	0
	1	0	1	0	1	0	0	0
	0	0	1	0	1	0	0	0
	1	0	1	0	1	0	0	0
	0	1	0	1	1	0	0	1
	0	1	0	1	1	0	0	1
	0	1	0	1	0	0	0	1
	0	1	0	1	0	0	0	1
	0	1	0	1	1	0	0	0
	1	0	1	0	1	0	0	0
	0	1	0	1	1	0	0	0
	1	0	1	0	1	0	0	0

HEATHKIT®

ROM PROGRAM

444-10 IC728

ADDRESS						DATA								
Logic Term	CH	CURSOR HOME	7	1	0	Logic Term	CURSOR LATCH	LOAD ÷12	LOAD ÷4	OC	1C	7C	$\overline{1C}$	$\overline{1}$
Input	E	D	C	B	A	Output	8	7	6	5	4	3	2	1
Pin #	14	13	12	11	10	Pin #	9	7	6	5	4	3	2	1
	0	0	0	0	0		1	0	0	0	0	0	1	1
	0	0	0	0	1		1	1	1	0	0	0	1	1
	0	0	0	1	0		0	0	0	0	0	0	1	0
	0	0	0	1	1		0	1	1	0	0	0	1	0
	0	0	1	0	0		1	0	0	0	0	0	1	1
	0	0	1	0	1		1	1	1	0	0	0	1	1
	0	0	1	1	0		0	0	0	0	0	0	1	0
	0	0	1	1	1		0	1	1	0	0	0	1	0
	0	1	0	0	0		1	0	0	0	0	0	1	1
	0	1	0	0	1		1	1	1	0	0	0	1	1
	0	1	0	1	0		0	0	0	0	0	0	1	0
	0	1	0	1	1		0	1	1	0	0	0	1	0
	0	1	1	0	0		1	0	0	0	0	0	1	1
	0	1	1	0	1		1	1	1	0	0	0	1	1
	0	1	1	1	0		0	0	0	0	0	0	1	0
	0	1	1	1	1		0	1	1	0	0	0	1	0
	1	0	0	0	0		1	0	0	1	1	1	0	1
	1	0	0	0	1		1	0	0	0	1	1	0	1
	1	0	0	1	0		1	0	0	1	0	1	1	0
	1	0	0	1	1		1	0	0	0	0	1	1	0
	1	0	1	0	0		1	0	0	1	1	0	0	1
	1	0	1	0	1		1	1	1	0	1	0	0	1
	1	0	1	1	0		0	0	0	1	0	0	1	0
	1	0	1	1	1		0	1	1	0	0	0	1	0
	1	1	0	0	0		1	0	0	1	1	1	0	1
	1	1	0	0	1		1	0	0	0	1	1	0	1
	1	1	0	1	0		0	0	0	1	0	1	1	0
	1	1	0	1	1		0	0	0	0	0	1	1	0
	1	1	1	0	0		1	0	0	1	1	0	0	1
	1	1	1	0	1		1	1	1	0	1	0	0	1
	1	1	1	1	0		0	0	0	0	0	0	1	0
	1	1	1	1	1		0	1	1	0	0	0	1	0

PROGRAMMED LOGIC ARRAY PROGRAM

443-787 IC702

INPUTS

LOGIC TERM	INPUT	PIN #	21	22	23	1	2	3	4	5	6	7	8	9	10	11
LF	I_{14}	11												H		H
$\overline{XP}$	I_{13}	10								H					L	
CR FF	I_{12}	9												H		H
CR	I_{11}	8				H							H			
DAV_u	I_{10}	7							H			H				H
DAV_{p+k}	I_9	6									H					
$\overline{Q'}$	I_8	5								H					H	
IC DAV	I_7	4							H							
OB_2	I_6	3		H	H			H								
"ADDRESS"	I_5	2					H									
CC + R	I_4	1				H										
DUPLEX	I_3	23			H											
XBEP	I_2	22	H													
XPEU	I_1	21		H												

OUTPUTS

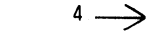
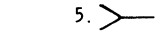
LOGIC TERM	OUTPUT	PIN #	20	19	18	17	16	15	14	13
XBE	O_8	20								
LF	O_7	19		H						
CC + R	O_6	18			H					
Re-select RAM	O_5	17				L				
CLR $\overline{Q}$	O_4	16					L			
OB_2 XP LOAD	O_3	15						L		
LOAD PARALLEL	O_2	14							H	
LOAD UART	O_1	13								L

BLANK = DON'T CARE
H = HIGH
L = LOW

The inputs specified are "ANDed" to form the indicated outputs.

SCHEMATIC OF THE HEATHKIT® VIDEO TERMINAL MODEL H9

NOTES:

1.  INDICATES A CONNECTION TO A CIRCUIT BOARD HOLE.
2. INDICATES A CHASSIS GROUND.
3. INDICATES A CIRCUIT BOARD GROUND.
4.  INDICATES A MALE CONNECTOR PIN. THE NUMBER FOLLOWING THE CONNECTOR NUMBER INDICATES THE PARTICULAR PIN NUMBER. FOR EXAMPLE: P604-11 MEANS PLUG P604, PIN 11.
5.  INDICATES A FEMALE CONNECTOR PIN. THE NUMBER FOLLOWING THE CONNECTOR NUMBER INDICATES THE PARTICULAR PIN NUMBER.
6. ALL RESISTORS ARE 1/2 WATT, 10% UNLESS THEY ARE MARKED OTHERWISE.
7. ALL RESISTORS VALUES ARE IN OHMS (k=1000, M=1,000,000).
8. ALL CAPACITOR VALUES LARGER THAN 1 ARE IN pF UNLESS OTHERWISE INDICATED. CAPACITOR VALUES LESS THAN 1 ARE IN µF.
9. REFER TO THE "X-RAY VIEWS" FOR THE PHYSICAL LOCATION OF COMPONENTS.