Schulungszentrum München
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Logic Chassis Control
MCCbus Cable Connection
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CABLES
BK5 - RMO3
BK8 - RMO3

Comparison Chart of PDP-11 DECDisk Specifications

Digital
MÜNCHEN
Schüller-Zentrum
Can stretch wires between B/P's.

by massbus problems only.

Up to 4 RH70, 2 B/P's.

Prewired B/P.

<table>
<thead>
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<th>MASSBUS</th>
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<td>BCTC</td>
<td>Unibus Interrupt Logic</td>
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<tr>
<td>BCTD</td>
<td>Unibus Data Transceivers</td>
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<td>PE, NEM, and Memory Cycle Control</td>
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<td>BUSI MUX (DB and CS3 Register) and START Logic</td>
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<td>MBSN</td>
<td>Massbus Transceiver (Massbus Cable C)</td>
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RH70 SIMPLIFIED DATA PATH DIAGRAM

RH70 I/O CONTROLLER
REGISTER ACCESS CONTROL PATH

RH70 DEVICE REGISTERS
CS1 CONTROL AND STATUS1  (SHARED WITH THE DRIVE)
CS2 CONTROL AND STATUS 2
DB DATA BUFFER
WC WORD COUNT
BA BUS ADDRESS
BE BUS ADDRESS
EXTENSION
CS3 CONTROL AND STATUS 3
REMOTE REGISTERS

DMA DATA PATH (DIRECT MEMORY ACCESS)

DATA TO MEMORY
DATA TO MASSBUS

OBUF FULL FLAG
ORDY (OUTPUT READY FLAG)

DATA FROM MEMORY
DATA FROM MASSBUS

CS1 776700  VECT 254
RMCS2 776710
RMDC 776734

1.5
MASSBUS INTERFACE LINES

DATA AND PARITY [D(17:00) & DPA]
- RUN (when power failure fall)
- OCCUPIED (OCC)
- END-OF-BLOCK (EBl)
- EXCEPTION (EXC)
- SYNC CLK (SCLK) 1.65 MS clock ramp 2.48 ramp
- WRITE CLK (WCLK)
- CONTROL, STATUS & PARITY [C(15:00) & CPA]

MASSBUS CONTROLLER
- DRIVE SELECT (DS02-DS00)
- CONTROL TO DRIVE (CTOD) Active for cont. to drive
- REGISTER SELECT (RS04-RS00)
- DEMAND (DEM)
- TRANSFER (TRA) Within 1.5 MS if drive exists
- ATTENTION (ATTN) For any drive interrupt if enabled
- INITIALIZE (INIT)
- FAIL Mass bus fail e.g. RH70 power fail.
  ECO to take away units select logic.

DATA / ECC

If an error then exception signal

1.6
WRITE COMMAND DATA PATH

RH70 DATA BUFFER (DB)

M ASSBUS

OBUF <PA, 15:00>

PARITY GENERATOR

MDPE

RG <15:00>

MDPF

RF <15:00>

MDPF

RE <15:00>

MDPE, MDPF

MXR SEL

MDPD

MXR

MDPB

RD <15:00>

MPDC

RB <PAHDB, PALB, 15:00>

PARITY CHECKER

MBX

MEM. D <31:16> & MEM. BYTE <3:2> PAR (ODD DATA WORD)

31 - 16

MEM. D <15:00> & MEM. BYTE <1:0> PAR (EVEN DATA WORD)

15 - 0

MEMORY

Cache I/F & bus.

Registers have full F/F's

Empty before RA clocked.

Parity before Memory.

If all full, we get 0100. A generate line gated to time data.
DECK MAINTENANCE POSITION

KEEPER HOLE
REAR DECK HOLDDOWN SCREW

SPACER

PACK COVER

DECK HOLDOWN SCREWS

DECK SUPPORT BRACKET

DECK CASTING

SHIPPING BRACKET MOUNTS HERE

SHOCK MOUNT

Spacer must be in maintain position.
CHASSIS MAP

Module AΦ3

031-035  Sheets 1-5

AΦ3 = AΦ3

131_13 = 603

**Revision important**

NOTE:
1. NOT USED
BACKPANEL LAYOUT

JA 80, 81: One to 41P, other to 210P board.

Right

When set on linear motor, which it must be for 81P access.

18, 19, 20

A09 - 04B

PIN COLUMN

PIN NUMBER

CARD LOCATION

VIEWED FROM WIREWRAP SIDE

JA 83

A cable not used.
Logical State | Nominal Voltage | Typical Range
---|---|---
TTL "1" | +3 V | +2.5 V to +4.0 V *
TTL "0" | 0 V | 0 V to +0.9 V
ECL "1" | -0.9 V | -0.61 V to -0.97 V
ECL "0" | -1.8 V | -1.52 V to -2.38 V

* Measuring a TTL open collector voltage may result in a reading that is close to the actual power supply voltage.
An enable signal. A visible output from the microcircuit depends upon the presence (active state) of the G modifier. Hence, G is often referred to as a dependency modifier.

A differential input, or a differential output, respectively. The microcircuit derives the differential by comparing the input signals appearing at the two pins spanned by the bracket, or by applying the generated differential signal to the two bracketed output pins.

The heavy vertical bar is a mnemonic device to aid in distinguishing line drivers and receivers from other microcircuits using the same distinctive shape (amplifier) symbol. The bar always appears within the symbol (as do all modifiers). It is near the input (left) side of the symbol for receivers and near the output side (right) for drivers.

Non-standard logic level: The slash on an input or output line identifies a binary level that differs from that considered standard. (Refer to standard levels for TTL, ECL, CMOS as given in section 1.)

Analog sign indicators: The plus sign indicates the normal (non-inverting) analog input or output; the minus sign identifies the inverting input or output. Analog signals most frequently appear in pairs. When they do not, only the inverting signal (-) is identified; the lack of a + indicator, then, implies a non-inverting input or output.

Analog signal: The inverted "U" (input or output) on a signal line is used only if confusion between analog and digital signals might otherwise arise. It is not used, for example, in conjunction with the + and - modifiers that in themselves define a signal as analog.

Binary (digital) logic: This symbol differentiates binary from analog signals (input or output). It is used only if confusion might otherwise arise.

Open-collector output: If the open-collector output line is continued on another diagram sheet, the diamond may be repeated just to the left of the off-sheet indication. This serves as a reminder that the pull-up resistor is shown elsewhere.
DISC PACK
DRIVE FUNCTIONAL BLOCK DIAGRAM

STORAGE CANNISTER

DISK PACK

BOTTOM DUST COVER

Disk Pack

POWER SYSTEM

UNIT SELECTION LOGIC

HEAD SELECTION LOGIC

READ/WRITE LOGIC

SEEK LOGIC

TRACK ORIENTATION LOGIC

ERROR DETECTION LOGIC

DATA RECORDED IN CONCENTRIC TRACKS

Heads

Controller

I/O LINES

INTERFACE

POSITIONING DEVICE
When Writing, we rewrite
pre-header Sync byte
& Header gap.
POSITIVE AND NEGATIVE DIBIT PATTERN

DIBIT PATTERN

**Positive Dibits**

- N N S S N N S S

**Disk Movement Relative to Head**

DIBIT PATTERN

**Negative Dibits**

- S S N N S S N N

**Disk Movement Relative to Head**

**Signal from Servo Head**

- Odd
  - N N S S N N S S
  - N N S S N N S S

- Even
  - S S N N S S N N
  - S S N N S S N N

- Disk Movement Relative to Head Somewhere Between Inner and Outer Guard Bands.

2.48 ms used to sync.

Servo track.

Dibit period.
REVS SK: \( T \leq 7 \)
ANALOG GATE 093

FDW SK: \( T \leq 7 \)
ANALOG GATE 093

LOAD HEADS
+15V
Q1

-15V
RTZ

COARSE POSITION
ERROR

COARSE

ANALOG GATE 072

VELOCITY TRANSDUCER

SUMMING amp.

HEADS LOADED \( T \leq 7 \)

H@LOAD \( (T \leq 7 + T \geq 256) \)

Coarse to fine mode (next page) when \( T = 1 \)

ACCEL COAST:

Max. speed 55''/sec
Head load 7''/sec
also RTZ.
POWER CONTROL PANEL
AND DISTRIBUTION DIAGRAM

Power Control Panel Switches and Indicators

Power Distribution Diagram

3.8
AC POWER WIRING
POWER SUPPLY ADJUSTMENT LOCATIONS

NOTES: ➥ CONNECTIONS DEPEND ON SITE POWER.
        ➥ INDICATES 16 AWG JUMPER WIRE.

**Example:** Jumper 2 - 3 for 240V 50Hz

CB1-B2 always to 1
CB2-2 to TBI-6

-5 V ADJUSTMENT
-5 V ADJUSTMENT

Must be measured on B/P with DVM
+5.1 V with 32 cyl. seek
+5.15 V without seeks.

Check voltages before head alignment.

3.9
Power Sequence Blockdiagramm

Diagram showing electrical connections and control signals for a power sequence. The diagram includes various components such as timers, relays, and power sequence logic. Specific labels like 'UNIT READY', 'PWR SEQ HOLD', and 'PWR SEQ PICK' indicate different stages of the sequence. The diagram is complex and requires detailed understanding of electrical and control systems.
DECK INTERLOCK SW 302

NORMAL

THRMO SW 302

CLOSED

START RUN TRIACS 302

PACK AT SPEED

NO

22 SECONDS ELAPSED 104

YES

TURN OFF TRIACS APPLY BRAKE 104

--- START "ON" READY "BLINKS"

GENERATE UP TO SPEED DELAYED 104

HEADS LOADED 194

YES

UPON DEPRESSION OF START, HEADS ARE RETRACTED. SEQUENCE IS TEMPORARILY HALTED UNTIL HEADS LOADED SW. IS OPEN.

NO

SET HEAD LOAD LATCH 194

B

3.13
GENERATE ~(LOAD+RTZ) 194

START 350ms TIMER (184)
CLEAR CYL ADDRESS (162)
CLEAR HEAD ADDRESS (113)

GENERATE +DRIVE
FWD AT 7 IPS.

SENSING OOD DIBITS 183

NO
YES

RESET HEAD LOAD LATCH 194

ON CYL SENSE 092

NO
YES

SET ON CYLF/F ON CYL PULSE 192

SERVO READY 194

SET RTZ LATCH 183

SERVO FAULT 194

~DRIVE SERVO AMP 093

UNLOAD HEAD

OVERSPEED 112 5V TO MBA

FAULT +5V 1252
RETURN TO ZERO SEEK TIMING

RTZ COMMAND

RTZ LATCH

VELOCITY

VELOCITY INTEGRATOR

CYLINDER PULSES

REV EOT ENABLE

FWD EOT ENABLE

REVERSE EOT FF

REVERSE EOT PULSE

RTZ START FWD/NO SR TRK UNLDD FF

LOAD LATCH

FINE LATCH

OUTPUT FROM FINE GATE

ON CYLINDER

NOTES:

1. CLEARING RTZ AND SETTING LOAD LATCH CAUSES CARRIAGE TO REVERSE DIRECTION AND MOVE FWD.
2. CYLINDER PULSES RESET VELOCITY INTEGRATOR.
3. REV EOT FF CLEARED WHEN NEGATIVE-EVEN DIBITS ARE DETECTED AS HEADS APPROACH 000.
4. FINE LATCH IS JAMMED (BOTH INPUTS HIGH) THUS DISABLING BOTH COARSE AND FINE GATES AS LONG AS EITHER LOAD OR RTZ LATCH IS SET.

3.16
- (ODD + EVEN DIBITS)

Index, Sector Ref
Write PLO (Servo Clock)
VCO

+ INDEX REF. CLK. (403 KHz)
+ SECTOR CLK. PULSE (806 kHz)
+ SERVO CLK. (9.67 MHz)
+ READ REF. CLK. (4.84 MHz)
- READ REF. CLK.

Index, Sector decode
182

Servo & Read Clk. VCO
013
+ HIGH FREQ. CLK.
(19.34 MHz)
Used to change between NRZ and FMF recording

Xmitter
112
+ SERVO CLK.
To MBA
To sync MBA with spindle speed

Read PLO
064
READ CLK.
I/O CABLES (SHEET 2 OF 2)

CONTROLLER

GROUND
- SERVO CLOCK
+ SERVO CLOCK
GROUND
- READ DATA
+ READ DATA
GROUND
- READ CLOCK
+ READ CLOCK
GROUND
- WRITE CLOCK
+ WRITE CLOCK
GROUND
- WRITE DATA
+ WRITE DATA
GROUND
- SECTOR 30+32
+ SECTOR 30+32
- START ENABLE
+ START ENABLE
GROUND
SPARE
SPARE
GROUND
+ INITIALIZE
- INITIALIZE

DRIVE

1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26

8 CABLE

26 mm²
HF Signals

3.21
Indicates peak shift on peak. Hence to pre-compensate when writing 6uS pre-comp used.

Recording on pack: current waveform MFM from O/P of head read amps.

<table>
<thead>
<tr>
<th>Data to Be Written</th>
<th>RZ</th>
<th>1 1 1 1</th>
<th>0 0 0 0</th>
<th>1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Recording Method</td>
<td>NRZ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>NRZI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F.M. (Modified NRZI: Frequency Modulation)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P.E. (Phase Encoding: Manchester Method)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M.F.M. (Modified Frequency Modulation: Miller Encoding)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

One of original recording techniques, now obsolete.

1st modification: used on magnetic devices built in 1950's.

Used on most tape drives (up to 800 BPI) including DEC's TU10, plus DF-32, RS4, and RS8 DEC disks.

Used on most moving head disk drives during 1960's (including RK5 and RP8).

Used with newer tape drives (1600 BPI) and some hi-density disk packs (plus Dectape).

Newer method allows extremely hi-density coupled with very reliable read-back. Used on very high-density tapes and disks such as the fixed-head RS4, the moving-head RP4/5/6 line, the RK6, and the new RL and RM product lines.
## PROM OUTPUTS

This tells us where we are. What signals are active at 160 sector word count.

### WRITE HEADER AND DATA

<table>
<thead>
<tr>
<th>WORD COUNT</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>000-131</td>
<td>P EN CRC / ECC</td>
</tr>
<tr>
<td>001</td>
<td>PRE CLEAR CRC / ECC</td>
</tr>
<tr>
<td>001-419</td>
<td>P WRITE GATE</td>
</tr>
<tr>
<td>014</td>
<td>P EN SYNC, P EN LOAD SR</td>
</tr>
<tr>
<td>128</td>
<td>To</td>
</tr>
<tr>
<td>129</td>
<td>P DATA EN SCLK, BRANCH (128)</td>
</tr>
<tr>
<td>130</td>
<td>P EN LOAD SR, P DATA EN SCLK</td>
</tr>
<tr>
<td>139</td>
<td>P HEADER AREA</td>
</tr>
<tr>
<td>161-415</td>
<td>P EN LOAD SR, P HEADER AREA</td>
</tr>
<tr>
<td>416</td>
<td>P EN CRC OUT, BR RD TO WRT</td>
</tr>
<tr>
<td>417-418</td>
<td>P EN SYNC, P EN LOAD SR</td>
</tr>
<tr>
<td>419</td>
<td>To</td>
</tr>
<tr>
<td>161-415</td>
<td>P DATA EN SCLK, BRANCH (161)</td>
</tr>
</tbody>
</table>

### WRITE DATA

<table>
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<th>FUNCTION</th>
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</tr>
<tr>
<td>001</td>
<td>PRE CLEAR CRC / ECC</td>
</tr>
<tr>
<td>004-129</td>
<td>P READ GATE</td>
</tr>
<tr>
<td>011</td>
<td>To</td>
</tr>
<tr>
<td>128</td>
<td>P LFS, BRANCH (128)</td>
</tr>
<tr>
<td>129</td>
<td>P HEADER AREA (FMT + CYL COMPARE)</td>
</tr>
<tr>
<td>130</td>
<td>P HEADER AREA (TRACK + SECTOR COMPARE)</td>
</tr>
<tr>
<td>131-419</td>
<td>P EN CRC OUT, BR RD TO WRT</td>
</tr>
<tr>
<td>139</td>
<td>P WRITE GATE</td>
</tr>
<tr>
<td>161-415</td>
<td>P EN SYNC, P EN LOAD SR</td>
</tr>
<tr>
<td>416</td>
<td>To</td>
</tr>
<tr>
<td>417-418</td>
<td>P DATA EN SCLK, BRANCH (161)</td>
</tr>
<tr>
<td>419</td>
<td>P EN LOAD SR</td>
</tr>
<tr>
<td></td>
<td>P EN ECC OUT</td>
</tr>
<tr>
<td></td>
<td>P EN EBL</td>
</tr>
</tbody>
</table>

End of block. (Stop writing before next index pulse.)

4.3
D/A

WC-6
CAR6
7, 8 & 9

To modify WRT AMP cell,
less WRT current
for inner cylinders.

See also
Page 4.1
WRITE COMPENSATION TIMING

Nominal is already 6ns late. Hence 16ns is nominal 12ns is late

8ns 16ns or 24ns

1 WRT PLO CLK (9.67 MHz)
2 WRT CLK (19.3 MHz)
3 WRT DATA (NRZ)
4 RAW MFM DATA
5 EARLY PATTERN
6 LATE PATTERN
7 EARLY DATA ENABLE
8 LATE DATA ENABLE
9 NOMINAL DATA ENABLE
10 COMPENSATED MFM DATA

Increasing Frequency
0 0 1 1 0 1 1 0
Decreasing Frequency

Note:
1. NUMBERS REFER TO LOGIC FOR WRT COMPENSATION/NRZ TO MFM CONVERTER CIRCUITS.
2. NUMBERS REFER TO TIMING ON WRITE COMPENSATION TIMING DIAGRAM.
## PROM OUTPUTS

### READ HEADER AND DATA

<table>
<thead>
<tr>
<th>WORD COUNT</th>
<th>FUNCTION</th>
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</thead>
<tbody>
<tr>
<td>000→131</td>
<td>P EN / CRC / ECC</td>
</tr>
<tr>
<td>001</td>
<td>P PRECLEAR CRC / ECC</td>
</tr>
<tr>
<td>004→129</td>
<td>P READ GATE To</td>
</tr>
<tr>
<td>011</td>
<td>P LFS, BRANCH (128)</td>
</tr>
<tr>
<td>128</td>
<td>P HEADER AREA (FMT and CYL) Gen SCLK (SYS clock)</td>
</tr>
<tr>
<td>129</td>
<td>P HEADER AREA (TRACK and SECTOR) Gen SCLK</td>
</tr>
<tr>
<td>130</td>
<td>P EN CRC OUT, BR RD TO WRT</td>
</tr>
<tr>
<td>132→417</td>
<td>P READ GATE To</td>
</tr>
<tr>
<td>136</td>
<td>P LFS, BRANCH (161)</td>
</tr>
<tr>
<td>161→416</td>
<td>P DATA EN SCLK</td>
</tr>
<tr>
<td>416</td>
<td>LAST READ DATA</td>
</tr>
<tr>
<td>417→418</td>
<td>P EN ECC OUT</td>
</tr>
<tr>
<td>419</td>
<td>P EN EBL</td>
</tr>
</tbody>
</table>

### READ DATA

Same as READ HEADER AND DATA except there is no SCLK generated at word counts 128 and 129. Header read & compared but not sent to RH78.
NOTE:
IF THIS IS THE LAST DRIVE IN THE CHAIN, INSTALL TERMINATORS ON PORT B OUTPUT (J8) AND PORT A OUTPUT (J2)