SMDC CONTROLLER WITH CACHE

The SMDC brings the high speed and large capacity of today’s (and tomorrow’s) SMD and HSMD drives to your LSI-11 or MicroVAX II system. The SMDC is compatible with ALL SMD and HSMD drives. It’s EASILY configured by the user to match any set of drive parameters. Its MSCP protocol is compatible with ALL DEC operating systems. These are things you’ve come to expect from an ANDROMEDA disk controller.

What’s unexpected is the sheer, flat-out performance of the SMDC. Under typical system operation, its 1 Megabyte on-board cache experiences a hit rate of over 80% percent. This means that, using the SMDC, seek time and rotational latency are reduced to ZERO over 80 percent of the time. The only thing left is DMA time, and the SMDC performs block-mode DMA just about as fast as Q-Bus specifications allow (up to 4.0 Mbytes/second).

Caching technology isn’t the only area where the SMDC is setting new standards. With the multi-function ‘User Access Port’, terms like ‘on-shelf obsolescence’ will never again have any meaning. The ‘User Access Port’ allows the customer to upgrade the SMDC microcode via modem. The days of costly chip-set upgrades are gone forever. Rest assured, support is just a phone call away...

SPECIFICATIONS

Data Cache —
1 Mb dual-ported data cache providing at least an 80% hit rate. Caching parameters variable via the User Access Port.

Peripheral Expansion Port —
Connects to accessory modules allowing control of devices such as tape, optical disk, and others.

Field Loadable Microcode —
Firmware stored in EEPROM and can be loaded from diskette or through User Access Port.

User Access Port —
Allows console terminal access to controller functions such as caching statistics and parameters, as well as drive formatting and configuration. Allows new microcode to be loaded by modem from anywhere in the world!

Online Configuration Tool (OCT) —
Using EEPROMs, OCT allows the selection/alteration of caching parameters, drive configuration and formatting.

Emulation —
The SMDC uses DEC’s Mass Storage Control Protocol (MSCP).

Disk Interface —
The SMDC can control ANY drive with a Storage Module (SMD/HSMD) interface. ANY size, ANY capacity, with data rates up to 3.125 Mbytes/second (5.0 Mbytes/second).

Sector Interleave —
1 - 1 sector interleave.

Error Control —
On-board 48 bit ECC error detection/correction code.

Number of Drives —
Up to 2 physical drives and 16 logical units each with user definable capacities. OCT selectable.

Address Selection —

Data Transfer Rate —
Up to 4.0 Mbytes/second on the bus.

DMA Transfer Mode —
Block Mode DMA

Power —
+5 VDC, 1.5 amps maximum.

Bus Loads —
AC — 1; DC — 1.5

Board Size —
Dual - 22 cm x 13 cm (8.5’’ x 5.2’’)

Temperature —
Storage — -40°C to 70°C (-40°F to 158°F) Operating — 5°C to 60°C (41°F to 140°F)

Relative Humidity —
10% to 95%, noncondensing.

MicroVAX II, LSI-11, DEC and MSCP are trademarks of the Digital Equipment Corp.

If you would like to have the SMDC increase the performance of your system contact:

ANDROMEDA SYSTEMS

9000 Eton Avenue, Canoga Park, California 91304 U.S.A. (818) 709-7600 • TWX-910-494-1248
FEATURES

- FUNCTIONAL SUPERSET OF DEC™ ADV11-A
- 16 SINGLE-ENDED OR 8 DIFFERENTIAL INPUT CHANNELS
- 12 BIT RESOLUTION
- ENTIRE DATA ACQUISITION SYSTEM IS A DUAL-WIDTH CARD
- SHIELDED DATA ACQUISITION MODULE
- PLUGS INTO LSI-11 BACKPLANE
- USES STANDARD VOLTAGES (+5, +12)
- UP TO 50 kHz THROUGHPUT RATE
- BURST, AUTO SEQUENCE, AND TRUNCATION MODES FOR MAXIMUM THROUGHPUT
- ON-BOARD 16 WORD FIFO DATA BUFFER

DESCRIPTION

The ADC11 is a compact 16 channel/12 bit data acquisition system housed in a steel case, minimizing EMI.

The ADC11 provides jumper programmable input ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. Input configurations are 16 channel single-ended, 16 channel quasi-differential, and 8 channel fully differential (specify fully differential when ordering).

Precision reference voltages of +5.000V and -5.000V and a precision sawtooth of ±5V are available at the 40 pin flat cable connector to facilitate user calibration and checkout. Two Pin connectors allow simple connection of the External Strobe and Clock Strobe signals from the PRTC11 Real Time clock.

The ADC11 has data register and command status register mappings identical to the ADV11-A, assuring maximum compatibility with existing DEC software. Unused ADV11 bits are used to control additional functions in the ADC11.

A variety of data acquisition modes not found in the ADV11-A are implemented in the ADC11 providing maximum data throughput through minimum computer attention. These modes are completely programmable:

SEQUENCE MODE: Automatically advances the multiplexer one channel and digitizes one reading for each conversion strobe.

SEQUENCE/TRUNCATION MODE: Sequentially converts each channel up to a maximum channel number equal to the value stored in the truncation register.

BURST MODE: Once started by a single conversion strobe, converts a selected channel continuously at 20 μs/conversion until the on-board 16 word FIFO is full. (In maintenance mode, conversions occur continuously regardless of the state of the FIFO.)

BURST/SEQUENCE MODE: Once started by a single conversion strobe, converts channels (starting with selected channel) sequentially at 20 μs/conversion until channel 15 is converted or the truncation channel is converted (truncation mode).
SPECIFICATIONS

Compatibility: Superset of DEC ADV11-A (vernier DAC replaced by truncation register)

Power Requirements:
- .9A at +5VDC (TYP)
- .25A at +12VDC (TYP)

LSI-11 Bus Interface: 3 Registers (2 bus addresses)
- Command/Status (Read/Write)
- Data Buffer (Read - Only)
- Truncation Channel (Write - Only)

Register Bit Assignments:

- Command/Status
  - A/D Channel
  - Error
  - Interrupt
  - Enable
  - Burst
  - Enable
  - Done
  - Interrupt
  - Enable
  - External
  - Strobe
  - Enable
  - Truncation
  - Enable
  - Maintenance

Interrupts: 2, individually vectored:
- Data Ready
- Error

CB11-A CONNECTOR BOX

An optional termination box, the CB11-A, provides BNC connectors for all 16 channel inputs as well as 2 external conversion command inputs. The calibration outputs are also brought to BNC connectors. The CB11-A is a 3.5” high rack mountable or free-standing unit. It connects to the ADC11 40 pin external connector with an optional cable.

TO ORDER

ADC11: Analog to digital converter
ADC11D: ADC11 with 8 differential inputs
CB11-A: Connector box

TM: DEC and LSI-11 are trademarks of the Digital Equipment Corp.
FEATURES

- Up to 4 asynchronous serial interfaces on one dual width card
- A parallel printer interface may be substituted for one of the serial channels
- Each serial channel has both RS232 and 20mA current loop available
- 16 data rates from 50Bd to 19.2Kbd remotely selectable
- All standard data formats: 5-8 data bits, 1, 1.5, or 2 stop bits, even odd, or no parity
- Independent Q-Bus addresses for each channel and independent vector addresses

DESCRIPTION

The MSI11 is a dual width card that plugs directly into the LSI-11 Q-Bus. It enables the user to interface up to 4 asynchronous serial lines (or up to 3 serial lines and a parallel printer) to an LSI-11 computer system. Each serial channel is independent in regard to data rate, data format, Q-Bus address, and interrupt vector address. Each channel has its own RS232 and 20mA current loop interfaces. The data rate for each channel may be determined on the card or remotely by jumpers. The 16 data rates are: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, and 19200 baud. The data format is selected for each channel by jumpers on the card.

The MSI11 connects to external devices through a 40 pin connector (in serial-only versions, in serial-parallel versions, a 50 pin connector is used) and a variety of adapter cables. The external adapter cables are of two main types, individual and group. The "individual" cable is split into up to 4 groups of 10 lines which run to separate connector assemblies which provide a 25 pin D-type connector, a switch for remote control of the data rate, and jumpers for selecting the "terminal" or "modem" pinout. The "group" cable is simply a connector assembly that mounts the equivalent of up to 4 "individual" connector assemblies on a single, vertical (rather than horizontal) printed circuit board. Both the "individual" and "group" adapter cables provide for a separate printer adapter if the parallel printer interface is used.

The parallel printer interface may be specified in place of one of the serial channels of the MSI11. This interface will talk to LA180 or Centronics type interfaces with the appropriate external cable and jumper configuration on the MSI11 card.

Both the serial and parallel interfaces are compatible with existing software drivers. When ordering, the user must specify the Q-Bus and interrupt vector addresses of the interface channels. These addresses are fixed PROMS on the card. Standard addresses are available at no extra charge. There is one time tooling charge for non-standard addresses.
FEATURES

- FUNCTIONAL SUPERSET OF DEC™ KWV11-A
- 13 INTERNALLY GENERATED TIMING RATES
- 5 OPERATIONAL MODES
- 2 SCHMITT TRIGGER INPUTS
- 2 VECTORED INTERRUPTS
- ENTIRE CLOCK FITS ON A DUAL WIDTH CARD
- USES STANDARD VOLTAGES (+5, +12)
- PLUGS INTO LSI-11 BACKPLANE

DESCRIPTION

The PRTC11 is a programmable timer/counter that provides several ways of generating or measuring time intervals, counting events, and determining the frequency of a signal. It can interrupt the LSI-11 CPU at programmed intervals or upon the receipt of an external input. The PRTC11 can also be used to initiate external functions such as conversions by the ADC11 analog to digital converter. The PRTC11 is a functional superset of the DEC KWV11-A. The extra timing rates and operational mode of the PRTC11 are enabled by a switch on the card.

The PRTC11 contains a 16 bit counter that can be incremented at 13 internally generated, crystal controlled, rates. The LSI-11 line clock (BEVENT L) and one of the schmitt trigger channels may also be used to increment the counter. Five operational modes are available in the PRTC11: single programmable interval, repeated programmable interval, event timing (internal or external), event interval timing, and frequency counting. Simple event counting is also available via frequency counting with an indefinite interval.

The PRTC11 provides the user with two schmitt trigger channels. On-board slope and trigger level controls are included (remote control is possible via the I/O connector). The schmitt triggers are used for external event detection, external timebase input, and external frequency input. The schmitt trigger outputs are also available for controlling external functions.

The entire PRTC11 is contained on a dual width card which plugs into the O-8US (LSI-11 backplane). Only +5 and +12 volts, the standard LSI-11 voltages, are required. -12 volts is generated on the card for the schmitt triggers. External connections are made via a 40 pin flat cable connector (same pinning as KWV11-A). PIN connectors allow simple connection of schmitt trigger 1 and clock overflow outputs to the ADC11. Jumpers permit user selection of the device address and interrupt vectors. A switch pack allows the user to enable the extra timing rates and frequency count mode as well as control the trigger level and slope of the schmitt triggers. Two trimpots permit on-board setting of the schmitt trigger levels.

The 13 internally generated timing rates are: 1MHz, 100kHz, 10kHz, 1kHz, 100Hz, 10Hz*, 1Hz*, .1Hz*, .01Hz*, .01667Hz* (1 min.), .001667 Hz* (10 min.), .00027778Hz* (1 hour), and 50Hz*.

*These rates are not available with the DEC KWV11-A.
SPECIFICATIONS

Compatibility: Superset of KWV11A (extra rates and mode enabled via on-board switch)

Power Requirements: .7A at 5VDC (TYP)
.07A at 12VDC (TYP)

LSI-11 Bus Interface: 2 Registers:

- **Command/Status**
- **Buffer/Preset**

Interrupts: 2, individually vectored:
- Clock Overflow
- Schmitt Trigger 2 Event

CB11-B CONNECTOR BOX

An optional connector box, the CB11-B is available. The CB11-B provides a convenient method of connecting a variety of external devices to the PRTC11. BNC connectors are provided for schmitt trigger inputs, enable inputs, level outputs, and pulse outputs. The clock overflow output is also available as are remote slope and level controls for both schmitt triggers. The CB11-B connects to the PRTC11 40 pin external connector via an optional cable.

The CB11-B may be rack mounted (3½” H) or free stand on a table top.

TO ORDER

PRTC11: Programmable Real Time Clock
CB11-B: Connector Box
LABEX2: Driver software for PRTC11

TM: DEC and LSI-11 are trademarks of the Digital Equipment Corp.
FEATURES

- 1 MB Dual Ported Data Cache
- Controls up to 7 ESDI Drives
- Controls up to 3 RX50/33 Floppies
- Optional 16 MB Cache Expansion Board
- Microcode Stored in EEPROM
- Intelligent Port for Tape, CD ROM, Etc.
- User Service Port
- MSCP (DU) Emulation

DESCRIPTION

The ESDC brings the high speed and large capacity of today's (and tomorrow's) ESDI and floppy drives to your LSI-11 or Micro/VAX II system. The ESDC is compatible with ALL ESDI Winchester and RX50/RX33 interface floppy drives. It is EASILY configured by the user to match any set of drive parameters. Its MSCP protocol is compatible with ALL DEC operating systems. These are things you have come to expect from an ANDROMEDA disk controller.

What's unexpected is the sheer, flat-out performance of the ESDC. Under typical system operation, its 1 Megabyte on-board cache experiences a hit rate of over 80 percent. This means that, using the ESDC, seek time and rotational latency are reduced to ZERO over 80 percent of the time. The only thing left is DMA time, and the ESDC performs block-mode DMA just about as fast as Q-Bus specifications allow (up to 4.0 Mbytes/second).

Caching technology isn't the only area where the ESDC is setting new standards. With the multi-function User Service Port, terms like 'on-shelf obsolescence' will never again have any meaning. The User Service Port allows the customer to upgrade the ESDC microcode via modem. The days of costly chip-set upgrades are gone forever. Rest assured, support is just a phone call away...
MSCP EMULATION
The ESDC communicates with the host computer using MSCP (DU) protocol. This has the advantage over other emulations in that disk capacity is communicated to the host by the controller instead of being embedded in the handler, allowing any size disk to be fully utilized without software modification.

SEEK OPTIMIZATION
The ESDC is capable of stacking 32 MSCP commands. This allows the controller to execute commands in a sequence which minimizes disk head movement (seek optimization), improving throughput in multituser environments.

1 MBYTE CACHE
The performance of the Andromeda ESDC is greatly enhanced by the inclusion of a 1 Mbyte data cache and unique caching algorithms. Andromeda's caching scheme divides the cache into 1024 granules. Data is maintained for each 1 Kbyte granule dependent on select criteria, which includes the following: time of first access; number of times read; time of most recent read; and size of read. This data is then factored into an equation that approximates the probability that the granule will soon be requested again. Those granules with low probabilities are designated to be overwritten by the next disk read operation. During cache accesses, a memory mapper translates logical memory addresses into the physical addresses of the appropriate granule, in a manner similar to that of the Micro-Vax II memory, management unit.

ADAPTIVE READAHEAD
In a novel departure from most caching schemes, the ESDC caching mechanism tries to look into the future as well as the past with a dynamic read-ahead algorithm. The controller retrieves not only the requested data, but also reads additional blocks beyond the requested data. Since there is a high probability that the system will access files in a sequential manner, there is an excellent chance that the system will ask for the next block, and then the next block, and so forth. As the system requests the data that has been pre-fetched in the cache, the controller retrieves not only the requested data, but also pre-emptively reads additional blocks when specific probability conditions are met.

EEPROM MICROCODE
The ESDC uses EEPROM for its microcode store. This allows new microcode to be loaded without expensive prom replacements. When used with the USER SERVICE PORT Kit the customer can load new microcode via modem anywhere in the world.

GATE ARRAY LOGIC
The majority of the random logic on the ESDC is implemented using programmable Logic Cell Arrays (LCA). At the time the system is initialized these LCAs are loaded by the controller microcode with what is effectively their schematic diagrams. Thus, ECO revisions which would ordinarily result in the board being sent back to the factory, can be performed with the ESDC by loading new microcode via modem.

USER SERVICE PORT
The User Service Port (USP) is a 10-pin connector at the top of the ESDC which provides RS232 communication with ANSI video terminals. It offers a variety of features which include: disk formatting; logical unit assignment and sizing; cache performance monitor; I/O transaction logging; microcode loading; cache parameter control, as well as drive status and write protection.

USP FORMATTER
Among its many functions the USP allows the user to format and test drives. Bad blocks are automatically marked out during this procedure and a log is presented to the user detailing test results. The resulting media appear error free to the host, eliminating the system overhead and inconvenience ordinarily associated with defect management.

USP PERFORMANCE MONITOR
The ESDC provides a real time performance monitor when the USP is connected to an ANSI compatible terminal. Instantaneous data such as Read %, Write %, hit rate, read size, and write size are presented in bar graph format. Cumulative data such as total disk reads, disk writes, and cache reads are presented in tabular format. This tool has proven of great value in system tuning.

USER SERVICE PORT KIT
The User Service Port Kit consists of a B size BA-11 connector panel, two DB 25 serial cables, and a 10 line cable. It provides a convenient method of interfacing a video terminal and 1200 baud modem to the User Service Port. Switches on the connector panel allow the user to easily change between the USP's various modes: loading microcode, changing controller parameters and displaying cache performance.

PERIPHERAL EXPANSION PORT
A 50-pin connector in the center of the ESDC contains the data and control signals required to connect to a variety of dual width expansion boards. These boards mechanically and electrically connect to the ESDC forming a sandwich which is inserted into the backplane. Included among these expansion boards are interfaces for tape, optical disk and additional cache.

16 MBYTE EXPANSION
Up to four 16 Mbyte expansion boards may be connected to the ESDC. This additional memory can be partitioned as additional cache and/or additional logical DU units. That portion assigned as logical units forms an exceptionally high performance ram disk.

<table>
<thead>
<tr>
<th>ESDC CONTROLLER SPECIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus Interface</td>
</tr>
<tr>
<td>DEC Q-Bus</td>
</tr>
<tr>
<td>Disk Cache</td>
</tr>
<tr>
<td>1 Megabyte, N way mappable</td>
</tr>
<tr>
<td>Disk Interfaces</td>
</tr>
<tr>
<td>Enhanced Small Disk Interface</td>
</tr>
<tr>
<td>Winchester, RX50/RX33 floppy</td>
</tr>
<tr>
<td>Software Emulation</td>
</tr>
<tr>
<td>MSCP</td>
</tr>
<tr>
<td>Command Buffer</td>
</tr>
<tr>
<td>32 MSCP commands</td>
</tr>
<tr>
<td>Adaptive Readahead</td>
</tr>
<tr>
<td>Up to 128 blocks</td>
</tr>
<tr>
<td>Transfer Mode</td>
</tr>
<tr>
<td>Block mode DMA</td>
</tr>
<tr>
<td>Transfer Rate</td>
</tr>
<tr>
<td>Up to 4.0 MB/sec</td>
</tr>
<tr>
<td>Sector Interleave</td>
</tr>
<tr>
<td>1:1</td>
</tr>
<tr>
<td>Disk Sectors</td>
</tr>
<tr>
<td>Up to 128</td>
</tr>
<tr>
<td>Disk Heads</td>
</tr>
<tr>
<td>Up to 256</td>
</tr>
<tr>
<td>Disk Cylinders</td>
</tr>
<tr>
<td>Up to 4096</td>
</tr>
<tr>
<td>Error Control</td>
</tr>
<tr>
<td>On-board 48 bit ECC</td>
</tr>
<tr>
<td>Number of Drives</td>
</tr>
<tr>
<td>Up to 7 ESDC</td>
</tr>
<tr>
<td>Winchester, RX50/RX33 floppy</td>
</tr>
<tr>
<td>Logical Units</td>
</tr>
<tr>
<td>Winchester, RX50/RX33 floppy</td>
</tr>
<tr>
<td>Address Selection</td>
</tr>
<tr>
<td>Standard plus 15 alt. jumper selectable</td>
</tr>
<tr>
<td>Interrupt Vector</td>
</tr>
<tr>
<td>Software selectable</td>
</tr>
<tr>
<td>Interrupt Priority</td>
</tr>
<tr>
<td>Level 45.6. Jumper selectable</td>
</tr>
<tr>
<td>Power</td>
</tr>
<tr>
<td>+5 VDC, 1.5 Amps</td>
</tr>
<tr>
<td>Bus Loads</td>
</tr>
<tr>
<td>AC — 1, DC — 1.5</td>
</tr>
<tr>
<td>Board Size</td>
</tr>
<tr>
<td>Dual — 22 cm x 13 cm (8.6&quot; x 5.2&quot;)</td>
</tr>
<tr>
<td>Storage Temperature</td>
</tr>
<tr>
<td>—40° C to 70° C (—40° F to 158° F)</td>
</tr>
<tr>
<td>Relative Humidity</td>
</tr>
<tr>
<td>10% to 95%, noncondensing</td>
</tr>
</tbody>
</table>

Micro/VAX II, LSI-11, DEC and MSCP are trademarks of the Digital Equipment Corp.
The Andromeda MM22:

An extremely fast, very dense, Block Mode DMA memory.

The MM22 is a dual width Q bus memory designed to enhance the performance of DEC PDP-11/23, PDP-11/73 and MICRO/VAX I systems. Up to twice the Q bus throughput.

The MM22 can provide up to twice the Q bus DMA throughput when operated in Block Mode. Optimum Block Mode performance is assured when used with a suitable Block Mode controller, such as one of the Andromeda DC11 Series.

30 ns. access time improves system performance.

Reduced access time allows faster completion of memory cycles and facilitates Block Mode DMA transfers.

256Kb to 2Mb capacity.

One board accepts either 64K or 256K DRAMs. The MM22 fulfills a wide variety of memory requirements for OEM's.

Reliability by design.

The MM22 offers improved reliability through simple, double sided circuit board design. A crystal controlled clock is used instead of unreliable and less accurate delay lines. Easily configured jumper blocks replace prone DIP switches. Socketed RAM improves MTTR.

Other Andromeda features for system flexibility.

Jumper selectable starting address, on-board parity CSR, 22 bit addressing, jumper selectable DMA block size, and low power consumption contribute to system flexibility and reliable performance.

---

**MM22 Memory Specifications.**

<table>
<thead>
<tr>
<th>Memory Size</th>
<th>MM22-1 256K bytes</th>
<th>(282,144 bytes x 9 bits)</th>
<th>MM22-2 512K bytes</th>
<th>(524,288 bytes x 9 bits)</th>
<th>MM22-3 1M byte</th>
<th>(1,048,576 bytes x 9 bits)</th>
<th>MM22-4 2M bytes</th>
<th>(2,097,152 bytes x 9 bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Speed</td>
<td>DIN to RPLY</td>
<td>30 ns MAX</td>
<td>DIN to RPLY</td>
<td>65 ns typ</td>
<td>DIN to RPLY</td>
<td>30 ns typ</td>
<td>DIN to RPLY</td>
<td>200 ns typ</td>
</tr>
<tr>
<td></td>
<td>SYNC to RPLY (DIN cycle)</td>
<td>30 ns typ</td>
<td>SYNC to RPLY (DIN cycle)</td>
<td>30 ns typ</td>
<td>SYNC to RPLY (DIN cycle)</td>
<td>215 ns typ</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(For comparison, a DEC MV1-1P and an 11/23 have the following specifications:

| DIN to RPLY | 150 ns | SYNC to RPLY | 285 ns |

Power Requirements

+ 5 volts (+ 1.0 amps typ)

Bus Loading

All lines, 1 DC load MAX, 1 AC load MAX

Addressing

22 bit or 18 bit addressing.

Starting address on any 256Kb boundary.

Memory size of 256Kb, 512Kb, 1Mb, or 2Mb

4 Kw or 2Kw I/O page

256 word or 16 word Block Mode capability

Parity

Fully software and diagnostic compatible.

DIO may reside at any standard address from 17772100 thru 17772136, or may be disabled.

Parity logic may use the on-board CSR or an external CSR, or may be disabled.

LEDs for parity error and power

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Andromeda Systems, Inc.

9000 Eton Avenue

Canoga Park, California 91304

(818) 709-7600  TWX: 910-494-1248

DEC, PDP-11/23, PDP-11/73, MICRO/VAX I

Q bus are trademarks of Digital Equipment Corp.
User's Description

The EB11 is a hardware debugging tool designed for use with DEC Q-BUS systems. The EB11 is unique among extender boards because it allows the user to isolate the Device Under Test (DUT), a Dual or Quad-width Q-BUS card, from the system bus on a line-by-line basis. Each signal line on the bus has a switch associated with it (See Figure 3). If the switch is in the ‘ON’ position, that line of the DUT is connected to the system bus. If the switch is in the ‘OFF’ position that line of the DUT is disconnected from the system bus. Next to each switch are two .025” square pins. The pin closest to the switch (and closest to the system bus) is electrically on the bus side of the isolation switch. The other pin (closest to the DUT) is electrically on the DUT side of the isolation switch. In order to maintain a logic 0 condition (+5V) for the DUT when the switch is open, a 10K ohm pullup resistor is connected to the DUT side of each switch (See Figure 4). Another feature is that the switches and test points are not in the physical order of the Q-BUS connector pins, but are in the functional order of the Q-BUS. Signals that are functionally related are placed next to each other in the EB11 switch array. The Data/Address lines are not only in numerical order, but are divided into groups of three to facilitate octal decoding of their signals.

In addition to the signal test points, there are also test points provided for the +5V, Ground, and +12V power lines. The +5V and Ground lines have heavy duty terminals for powering user test equipment such as logic probes.

The EB11 is a quad-width card with isolation switches on the left half. The right half of the EB11 has direct connections from the system backplane to the DUT connectors. This card is suitable for use with all Q-BUS quad-width backplanes including those with the DEC “C-D Interconnect” on the right side. Most recently-introduced quad-width Q-Bus cards have all of their signal I/O on the left pair of connectors so that they will be compatible with backplanes that use the “C-D Interconnect”. Some older quad-width cards use both the left and right pairs of connectors for signal lines. In this case, you will not be able to isolate signals on the right pair of connectors with a standard EB11. (You could use a pair of EB11/2’s however; see below.)

For applications that use dual-width card cages, the EB11/2 is available. This is just an EB11 cut in half. The EB11/2 includes both halves of the EB11: The half with the isolation switches and the half with the direct connections.
DESCRIPTION

The 8LCC and the 8LCC/2 are Q-BUS compatible card cages. The 8LCC will hold up to 16 dual-width (8" x 5") or 8 quad-width (8" x 10") LSI-11 cards. The smaller 8LCC/2 will hold up to 8 dual-width (8" x 5") LSI-11 cards.

FEATURES

** Tapered entry connectors with gold plated, bifurcated contacts which results in a lower insertion force than comparable DEC connectors.

** Color coded card guides (blue and white) for easy alignment of quad-width cards. Thin, reinforced guides facilitate airflow through the cage.

** The 8LCC has optional expansion connectors to second card cage on the backplane to avoid the use of a slot and are DEC BCV compatible.

** Provision is made on the 8LCC backplanes for optional termination resistors.

** Units have the same mounting configuration as the MLSI-BPA84 from MDB but are structurally far superior.

** The 8LCC has a choice of two power input connection styles:
   - Standard screw terminations (8LCC-T)
   - Andromeda PDU compatible cable (8LCC)

The 8LCC and the 8LCC/2 are ideal foundations for LSI-11 computer systems. The 8LCC is also an excellent choice for expanding an existing system since the expansion connectors on the backplane do not require the use of a slot in the cage to connect to the first system cage.

Dec and LSI-11 are trademarks of the Digital Equipment Corp.