NOBODY DOES IT BETTER!
Our new QD01 Disk Controller is designed to interface any two ST506 5¼-inch Winchester disk drives to the Digital Equipment Corporation (DEC™) QBus™. This dual-wide, microprocessor-based controller emulates DEC's Mass Storage Control Protocol (MSCP) and is compatible with DEC's LSI-11™ MICRO/PDP and MicroVAX.

The QD01 incorporates a new custom, Emulex-designed Very Large Scale Integration (VLSI) chip that controls interface timing and signals to the QBus. By replacing as much as 50% of the control logic with one custom chip, we have reduced component count, cost and power consumption. Of course, the result is significantly-improved performance and reliability.

THE LEADING DUAL-WIDE, MSCP QBUS CONTROLLER OFFERS...

ADAPTIVE DMA. Multi-user systems requiring numerous DMA data transfers are very much enhanced by the QD01's use of adaptive DMA. Adaptive DMA releases the bus to other DMA devices with a lower priority based upon the bus requests, which facilitates multiple I/O operations and throughput.

NON-INTERLEAVED SECTORS. This feature gives you faster disk data throughput by enabling large data transfers from contiguous sectors. Emulex is the first company to offer a non-interleaving ST506/QBus micro-controller.

22-BIT ADDRESSING. Hardware addressing permits direct access to the full 4M byte memory range.

NOVRAM. This Nonvolatile static Random Access Memory (NOVRAM) device stores drive configurations. A user may alter the configuration of the QD01 at will.

COMMAND BUFFER. The QD01 provides the ability to prioritize commands and thereby optimize command execution and disk head movement. All this results in enhanced throughput.

INTERNAL SELF-TEST. Automatic self-test and operator-initiated subsystem diagnostics are contained in on-board firmware, supported by error display LEDs.

ECC/CRC HARDWARE. Forty-eight bit Error Correction Code (ECC) for data error detection/correction (single 11-bit error burst) and sixteen-bit CRC for header error detection is provided.
PRODUCT SPECIFICATIONS

FUNCTIONAL
Design:
Microprocessor-based MSCP disk controller.
Emulation:
DEC's MSCP.
Computer Interface:
Standard QBus (dual interface).
Peripheral Interface:
Seagate Technology (ST506).
DMA Address Range:
16-, 18- or 22-bit addressing modes.
Base Device Address:
Switch-selectable to LSI-11 and MicroWAX standard and alternate addresses.
DMA Transfers:
Up to 2M byte per second.
Number of Heads:
Up to 16 read/write heads.
Sector Size:
512 bytes.
ECC:
48-bit ECC on data; 16-bit CRC on headers.
Data Buffering:
Dynamically allocated 10K byte data buffer.
Self Test:
Controller automatically executes extensive power-up self-test diagnostics.
Fault/Activity Display:
LEDs indicate detected board fault and controller read/write activity, remotelable for subsystem integration.

User's Panel Connector:
Supports remote user panel status LEDs (controller-ready condition and write-protect switch status).
Option/Configuration Switches:
On-board switches are provided for alternate controller address, unit offsets and extended self-test, etc.

PHYSICAL
QD01/D Packaging:
One dual-wide PCB; standard QBus 2-conductor interface.
Cable Connectors:
20-pin Drive 0 data connector.
20-pin Drive 1 data connector.
34-pin drive control connector.
10-pin front panel connector.
Physical Drives:
2 physical drives.

ELECTRICAL
QBus Interface:
Approved line drivers/receivers used exclusively; one unit load per bus signal line.
Disk Interface:
Standard ST506 interface.
Power:
+5VDC (±5%), 2.6 amps maximum.
Bus Loads:
AC: 2.5; DC: 1.

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