APPENDIX B
VAX 8600 INTERNAL MEMORY SYSTEM

B.1 INTRODUCTION

This appendix describes the VAX 8600 internal memory system. The internal memory system consists of up to eight L0200 array boards and a single L0222 array bus terminator module. Each array board provides storage for 4 Mbytes of information (one mega-longword). If all eight boards are installed, the maximum storage capacity of 32 Mbytes is available. The design implementation of the L0200 module uses both ECL and TTL technologies and translators to interface the two. ECL is used for the main timing and control and array bus drivers, while TTL is used for the battery backup circuits.

B.2 MEMORY SPECIFICATIONS

Tables B-1 through B-3 describe the specifications of the L0200 memory array module in terms of memory capacity, access time, and dc power requirements.

Table B-1 Memory Capacity

Chip Size	Capacity Mbytes	Capacity MLW*
64 K	1	0.25
256 K	4	1.00

* mega-longwords

All timing within the array module is synchronized by a 40 ns (25.0 MHz) clock signal from the VAX 8600 system clock module. Each array module receives its own clock via CLK ARRAY<7:0>. The refresh interval is approximately 12 μs, about one cycle in 24 (worst case).

Table B-2 Cycle Times

Type	Conditions	Time
Read Cycle Times	Start to Word 0	400 ns
	Start to Word 3	640 ns
Repeat Read Time	Start to Start	560 ns
Repeat Write Time	Start to Start	640 ns

Table B-3 Array Module Power Requirements

Power Supply	I_{typ}	I_{wc}	P_{typ}	P_{wc}
+5 V (battery)				
Active board	9637 mA	10373 mA	49.19 W	54.46 W
Idle board	2237 mA	2973 mA	11.19 W	15.61 W
+5 V (normal)	1658 mA	2089 mA	8.29 W	10.97 W
−5.2 V	4287 mA	5171 mA	22.29 W	28.23 W
−2.0 V	1680 mA	1680 mA	3.36 W	3.52 W

typ = typical
wc = worst case

A green LED indicator, visible near the module handles, provides an indication that battery backup power is available to the module.

B.3 ARRAY BOARD FUNCTIONAL DESCRIPTION

The L0200 module consists of the following major functional logic areas (Figure B-1).

1. MOS ARRAY – This consists of 156 MOS RAM chips. Each RAM chip has a storage capacity of 262,144 (256 K) bits. The array is organized to store and retrieve information in units of 39 bits; 32 data plus 7 check bits.

2. DATA PATH – This consists of 20 DC109 data path chips. Each DC109 chip provides temporary storage for eight bits being transferred to/from the MOS RAMs. The DC109 chips are organized to hold four 40-bit units during a write and four 39-bit units during a read.

3. ADDRESS PATH – This consists of eight 10173 mixer/latch chips and 18 74S158 mixer chips that provide the address to the MOS RAMs, either from the array bus or from the refresh control logic.

4. REFRESH CONTROL – This consists of a binary counter along with the required timing and control logic that will periodically refresh the MOS RAMs to prevent loss of data.

5. TIMING and CONTROL – This consists of all the timing and control logic required to provide sequencing of the array bus interface, MOS RAMs, and the DC109 chips.

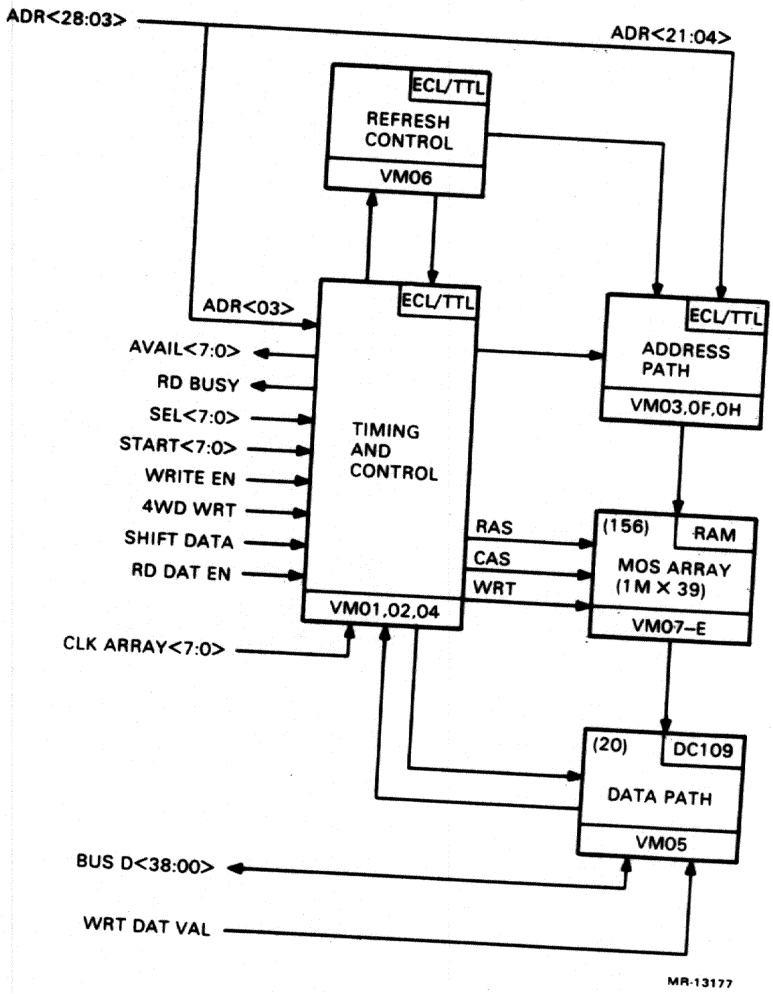

Figure B-1 Functional Block Diagram

B.3.1 MOS Array Organization

The 156 MOS RAM chips are logically organized into four rows and 39 columns (Figure B-2). Each row is 262,144 (256 K) bits deep and represents a longword of 39 bits; 32 data and 7 check bits. Each column represents a bit within a longword. The following scheme is used to label each bit.

nxx

where: n = which longword
xx = which bit

EXAMPLE: 236 indicates bit 36 in LW 2

The row/column organization is the same for the DC109 data path chips except for the addition of one column to store the Valid bits. Each row in the DC109 chip structure is only one deep. During a read, one 4 × 39 slice of the MOS RAMs is copied into the DC109 chips, and during a write, the 4 × 39 DC109 cell structure is copied into the addressed 4 × 39 slice of the MOS RAMs.

The table in Figure B-2 describes the physical partitioning of the bits within the DC109 chips.

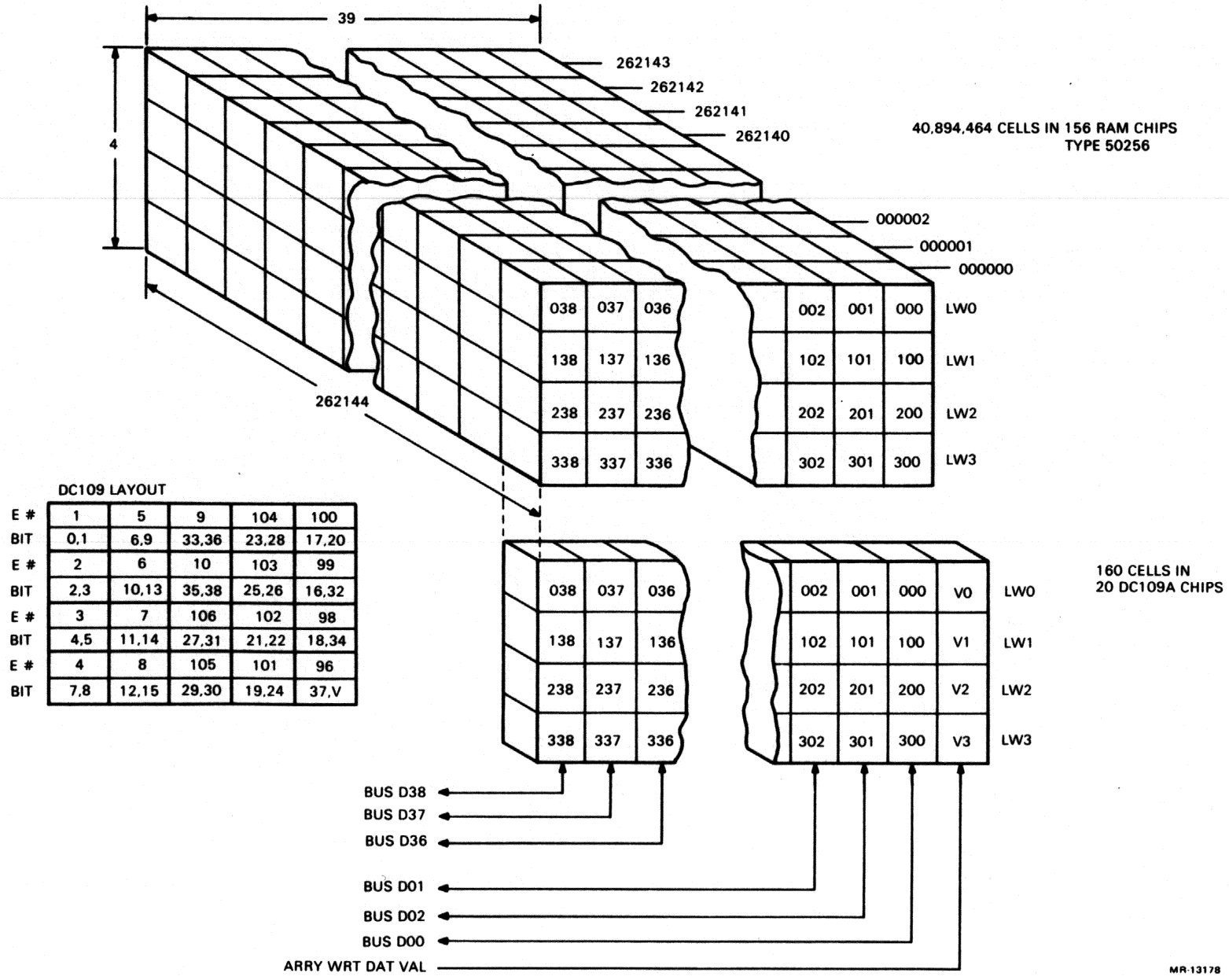

Figure B-2 MOS Array Organization

B.3.2 DC109 Data Path

Each DC109 chip consists of two identical sections that handle the routing of two data bits from the array bus to the MOS RAMs during a write and from the MOS RAMs to the array bus during a read. For write, the device performs serial-to-parallel conversion, and during a read it performs parallel-to-serial conversion. Figure B-3 uses <37> on VM05 to describe the operation.

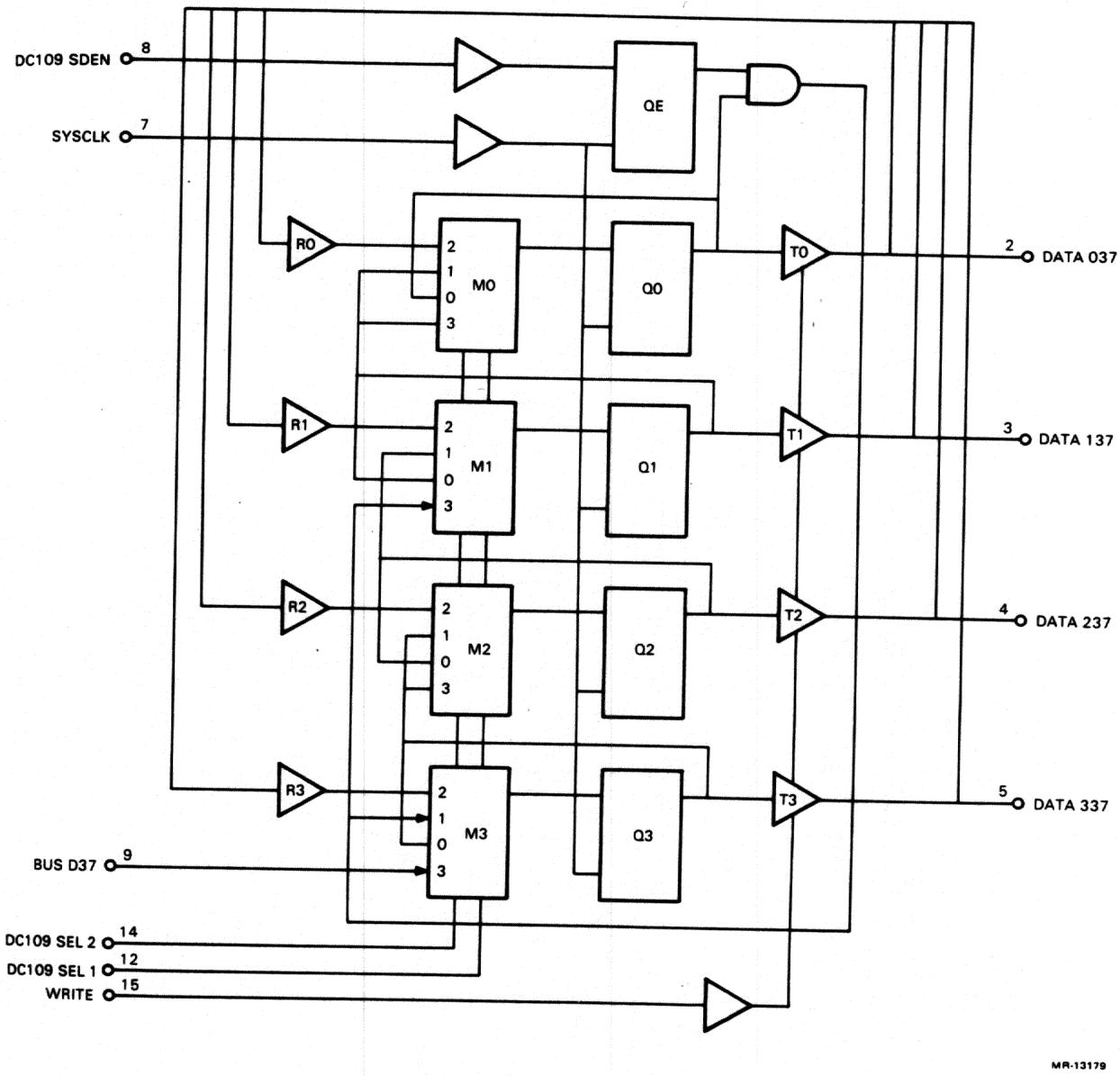

Figure B-3 DC109 Data Path

Each bit slice contains the following circuits.

1. Four data flops, Q<3:0>
2. Four 4 × 1 multiplexers, M<3:0>
3. Four ECL to TTL drivers, T<3:0>
4. Four TTL to ECL receivers, R<3:0>
5. One read enable latch, QE
6. Three buffers for SYSCLK, WRITE, and SDEN
7. One ECL driver for BUS D37

The four multiplexers provide the mechanism for loading and shifting the flops during conversion as shown in Table B-4.

Table B-4 DC109 Data Chip Control

SEL1	SEL2	Function	
0	0	HOLD Q<3:0>	
0	1	SHIFT Q<3:0>	(Read and 4WD write)
1	0	LOAD Q<3:0>	(Read only)
1	1	LOAD BUS D37	(2WD write)

During a read operation, DATA<337:037> are read from four MOS RAM chips routed through M<3:0> and clocked into Q<3:0>. SDEN is latched in QE to enable Q0 to be gated out to BUS D37. SEL<2:1> are set to 01 to allow SYSCLK to shift out the bits, one at a time in the following sequence: 0, 1, 2, 3. Note that the first bit (LW0) is available without a shift clock, which means that the MBox control need only generate three SHIFT DATA signals to retrieve the four longwords.

During a write operation, the process is reversed. BUS D37 is loaded into Q3 via M3 and shifted up through Q3, Q2, Q1, to Q0. After four shift operations, Q<3:0> contain bit 37 for four longwords. At this point, WRITE enables the four ECL/TTL drivers to write the four bits, D<337:037>, into four MOS RAM chips.

For a 2-word write, the data at BUS D37 gets clocked into Q3 and Q1 simultaneously. The second clock loads BUS D37 into Q3 and Q1 and simultaneously shifts the last data from Q1 into Q0 and Q3 into Q2. This results in Q<1:0> and Q<3:2> containing identical information. When the MOS RAMs are written, either Q<1:0> or Q<3:2> are written depending upon the state of ADR<03>.

B.3.3 Address Path

When the MBox asserts ARRAY START, the control logic generates VM01 LATADD to latch the address, ADR<21:04>, into a set of 10173 mixer/latches on VM03 (Figure B-4). During the memory cycle, the control logic asserts VM01 MUX ADD to switch the ADDRESS MIXER to multiplex the 18-bit address into two 9-bit slices, ADD<08:00>. Nine 10125 translators are used to interface the 10173 ECL circuits to the 74S158 TTL circuits. Finally, the mixer drivers on VM0F-H route the address to the MOS RAMs.

NOTE

Two jumpers on VM03, W1, and W2 must be set up to specify the RAM size as follows.

W2 IN, W1 OUT	**256 K RAMs**
W2 OUT, W1 IN	**64 K RAMs**

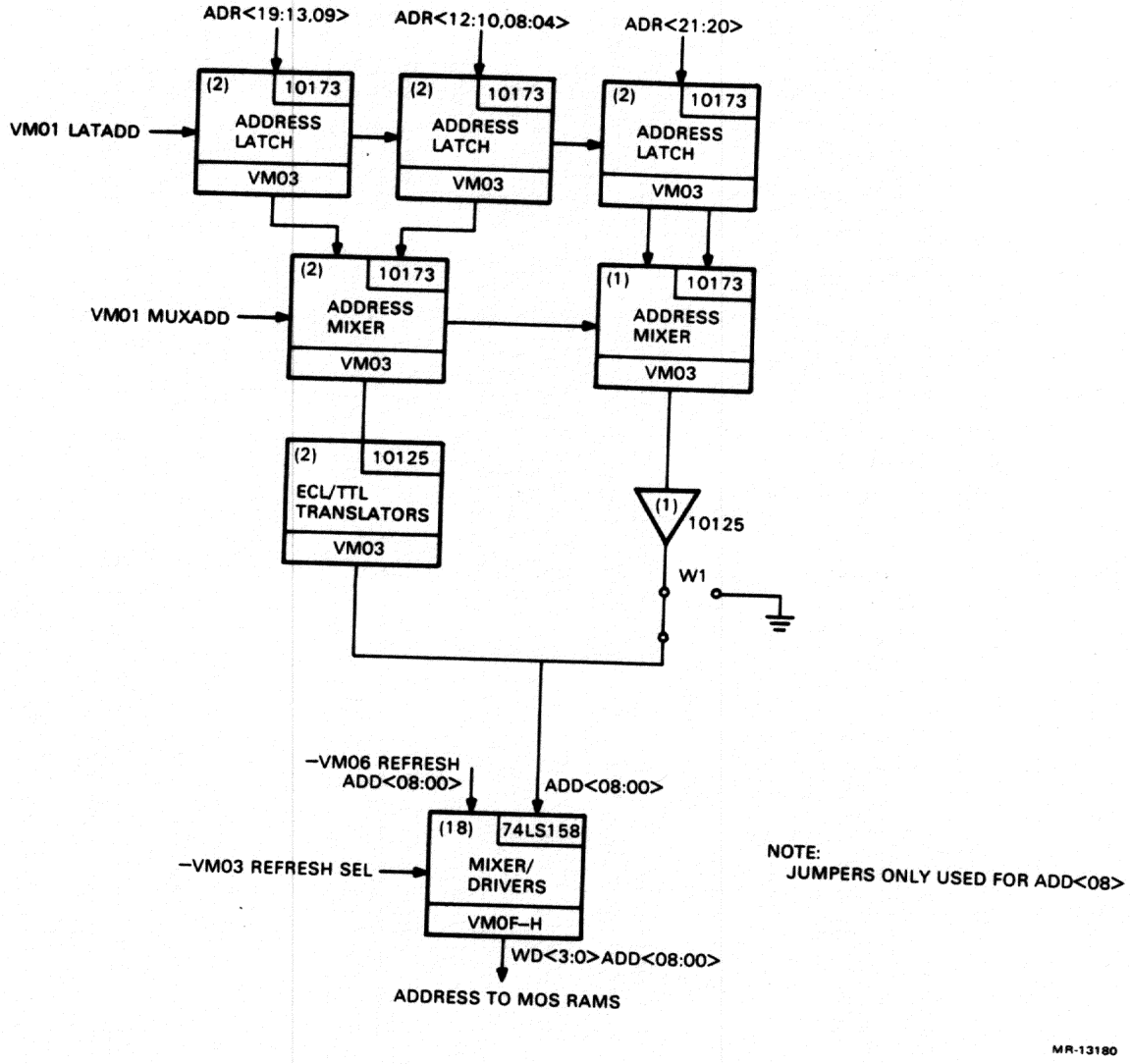

Figure B-4 Address Path

B.3.4 Refresh Control

MOS RAMs tend to lose information if not accessed periodically. To prevent this from occurring, the L0200 contains refresh logic that periodically accesses each of the 512 rows in each MOS RAM by turning on the RAS signal.

Most of the refresh control logic is shown on print VM06 in the L0200 module print set. Figure B-5 shows that the refresh control is comprised of the following major logic areas.

1. Refresh Timer
2. Refresh Control
3. Binary Counter
4. Dual Quad Buffer

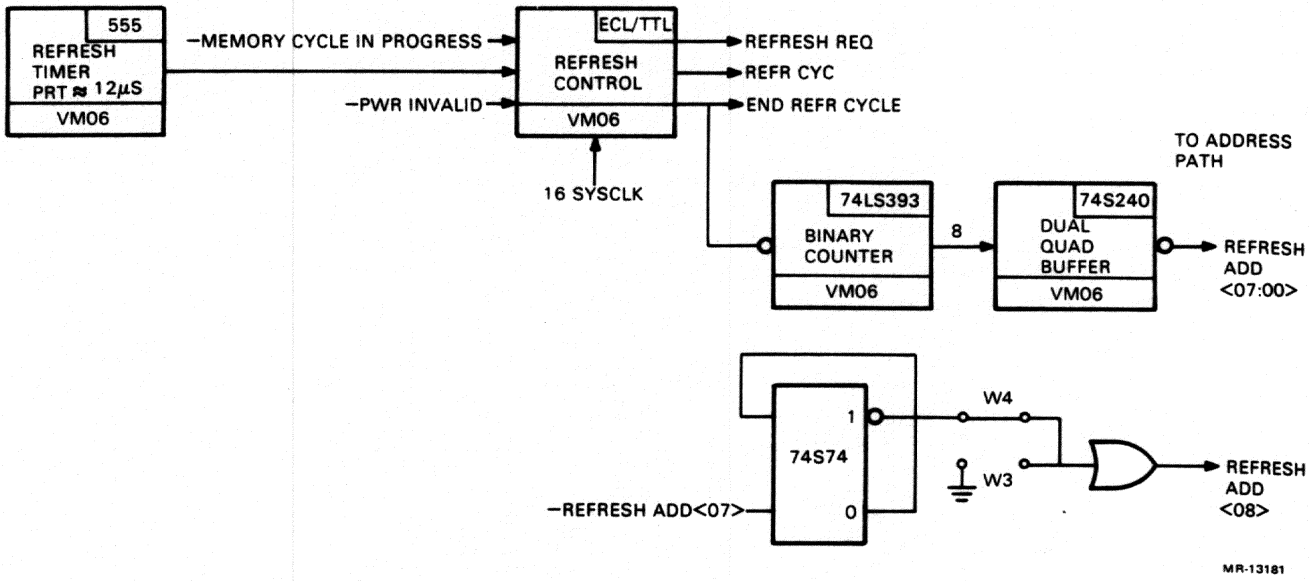

Figure B-5 Refresh Control

The 555 TIMER is a free-running oscillator with a Pulse Repetition Time (PRT) of approximately 12 μs. It generates a pulse every 12 μs to attempt to start a refresh cycle. The refresh control logic is a sequential logic network, consisting of both ECL and TTL circuits, that decides if the refresh cycle will be allowed. The signals PWR INVALID and MEMORY CYCLE IN PROGRESS must both be negated to start a refresh cycle. If allowed to occur, REFRESH REQ and REFR CYC are asserted and used as follows.

1. REFRESH REQ – Used by the timing and control logic on VM01 to start the memory cycle timing sequence.

2. REFR CYC – Used by the timing and control logic on VM01 to enable turning on the RAS signals to the MOS RAMs and used on VM04 to disable CAS<3:0> EN to prevent turning on the CAS signals to the MOS RAMs.

The 8-bit 74LS393 binary counter and the single 74S74 flop are used to generate the address to the MOS RAMs via the 74S240 dual quad buffer. The nine bit address, REFRESH ADD<08:00>, is routed to the MOS RAMs via the address path. At the end of each refresh cycle, END REFR CYCLE increments the binary counter to generate the next row address.

NOTE

Two jumpers, W3 and W4, are used to condition the high order address bit, REFRESH ADD<08>, as follows.

W4 IN, W3 OUT	**256 K RAMs**
W4 OUT, W3 IN	**64 K RAMs**

The approximate time required to refresh all cells in all RAMs is 3.07 ms for both 256 K and 64 K RAMs.

B.3.5 Timing and Control

This logic generates the required sequence of control signals to cycle the MOS RAMs during both refresh and memory read/write requests (Figure B-6). The start control logic is triggered either by ARRAY START for read/write requests or REFRESH REQUEST for refresh cycles. LATADD is asserted by ARRAY START and is used to latch the array bus address in the address path only for read/write requests. When the start control logic is triggered, it enables SYSCLK to shift a 1 down through the 10141 shift register to activate this sequence.

VM01 1 → VM01 2 → VM01 4 → VM01 5 → VM01 8.

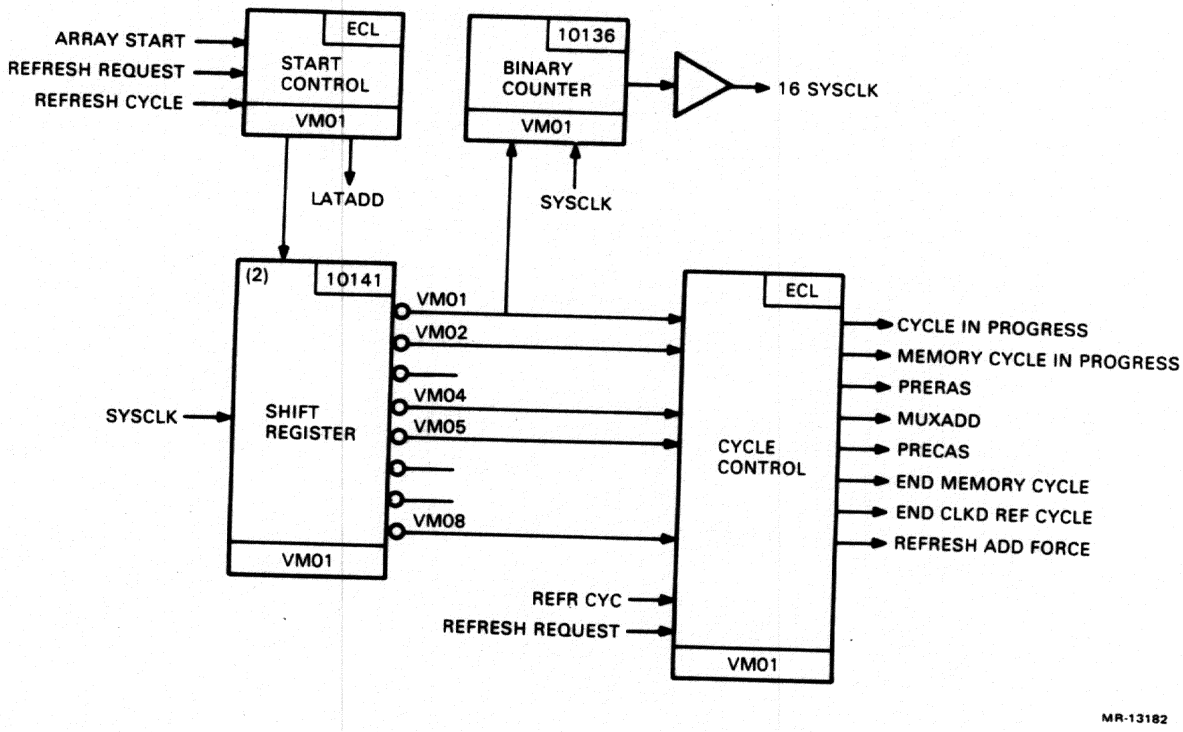

Figure B-6 Timing and Control

These outputs from the SHIFT REGISTER activate the CYCLE CONTROL logic to generate the following signals at the proper time to cycle the MOS RAMs.

1. PRERAS – This activates the row address strobe signals, RAS<3:0>, on VM04 to latch the row address in the MOS RAMs.

2. MUXADD – This switches the address path to select the column address.

3. PRECAS – This activates the column address strobe signals, CAS<3:0>, on VM04.

NOTE

CAS<3:0> are all activated for read, but are conditional during a write, dependent upon the signals WR 01, WR 23, and WRITE WORD<3:0>. During a 2-word write, WR 01 and WR 23 enable which pair of longwords will be written, either LW 0,1 or LW 2,3. WRITE WORD<3:0> are used for 2-word and 4-word writes to enable writing any combination dependent upon the state of the Valid bit shifted into the DC109 chips.

CYCLE IN PROGRESS, MEMORY CYCLE IN PROGRESS, END MEMORY CYCLE, and END CLKD REF CYCLE are used as state signals to ensure proper sequencing of the timing chain. REFRESH ADD FORCE is used on VM03 to force the address path to select REFRESH ADD<8:0> as the source of address to the MOS RAMs during a refresh cycle. Finally, a 10136 binary counter, incremented by SYSCLK, is used to generate 16 SYSCLKs to trigger the refresh control. The timing diagrams referenced in the next section describes this sequencing in more detail.

B.4 MEMORY OPERATIONS

The following sections refer to four timing diagrams that describe the key logic signal generation sequence for read, write, and refresh operations on the L0200 memory module.

B.4.1 Read Transaction

Figure B-7 describes the sequence of operations generated to read four longwords from the MOS RAMs into the DC109 chips and shift out the data to the array bus.

B.4.2 Write Transactions

There are two possible write sequences, depending upon the state of ARRAY 4WD WRT from the MBox.

B.4.2.1 4-Word Write – Figure B-8 describes the sequence of operations generated to load four longwords from the array bus into the DC109 chips and write the contents of the DC109 chips into the MOS RAMs.

B.4.2.2 2-Word Write – Figure B-9 describes the sequence of operations generated to load two longwords from the array bus into the DC109 chips and write the contents of the DC109 chips into the MOS RAMs.

B.4.3 Refresh

Figure B-10 describes the sequence of operations generated during a refresh cycle.

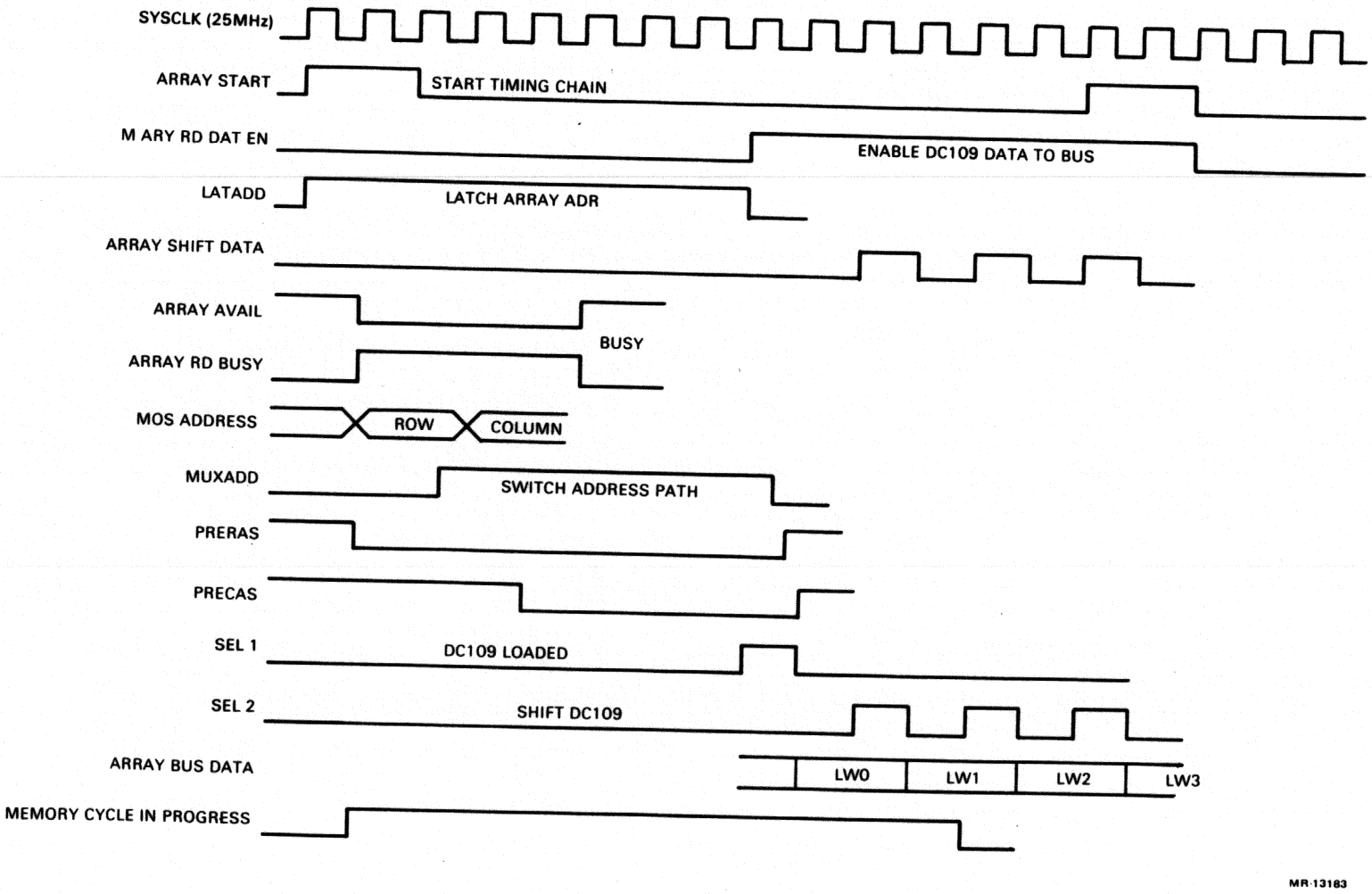

Figure B-7 Read Timing

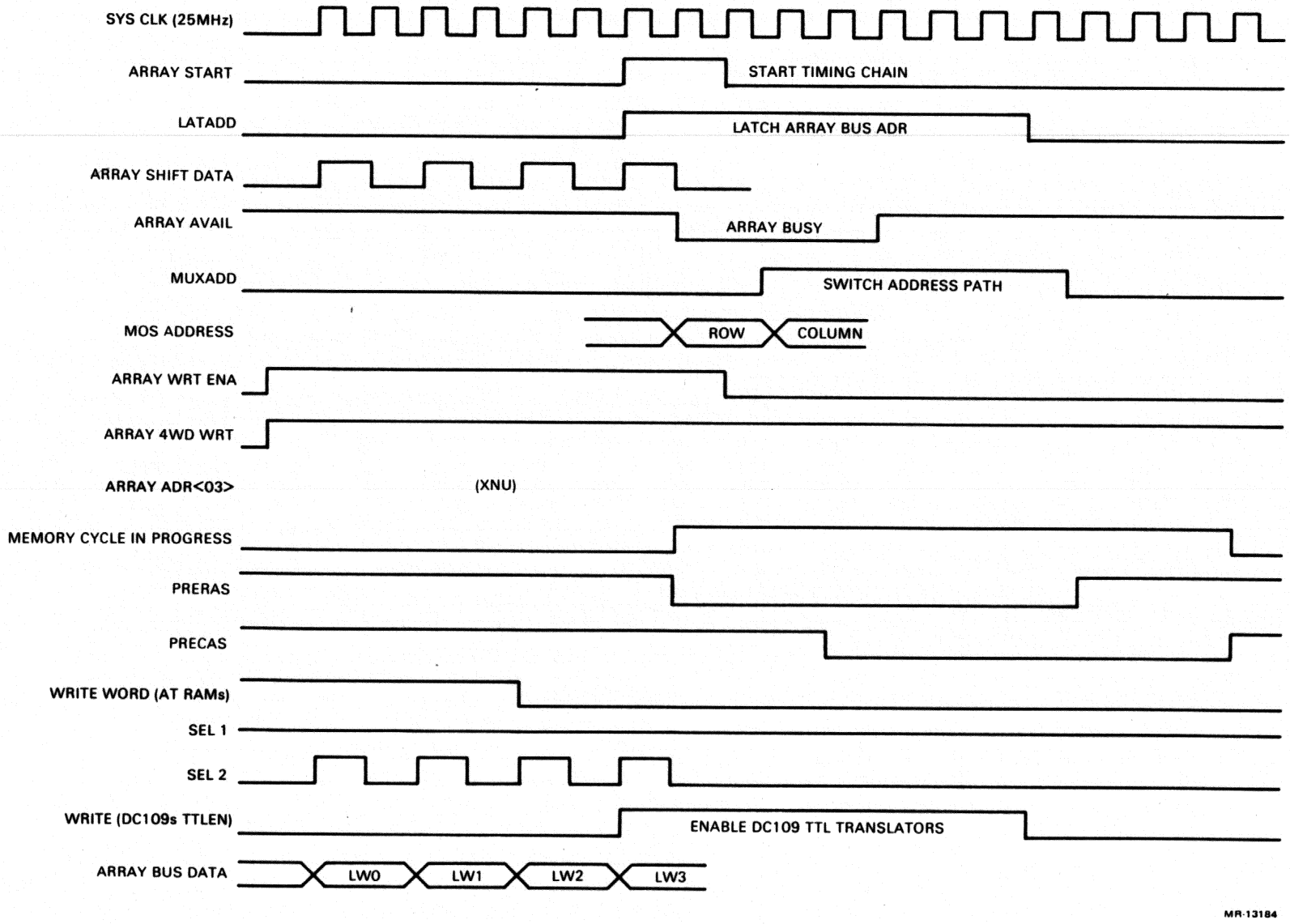

Figure B-8 4-Word Write Timing

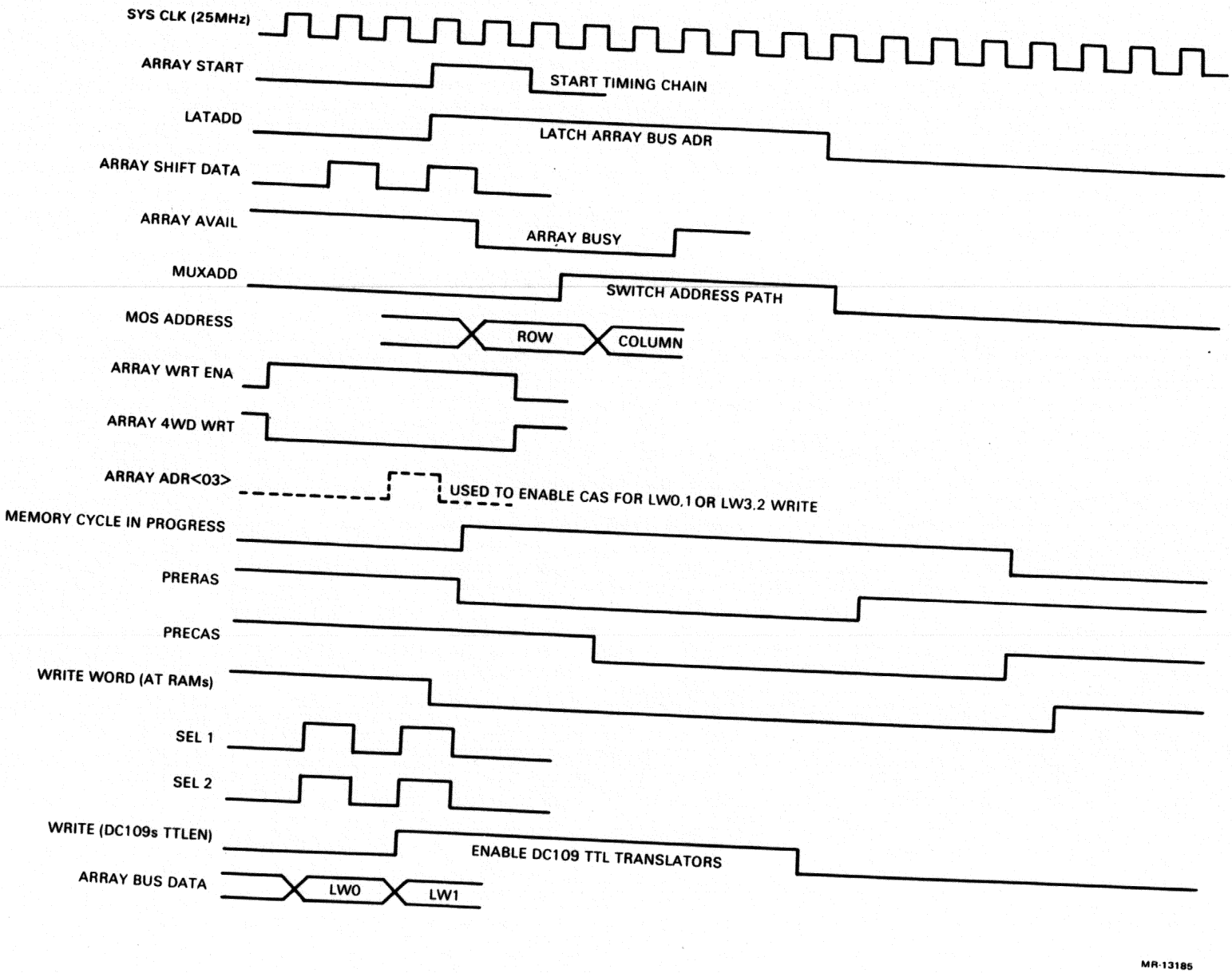

Figure B-9 2-Word Write Timing

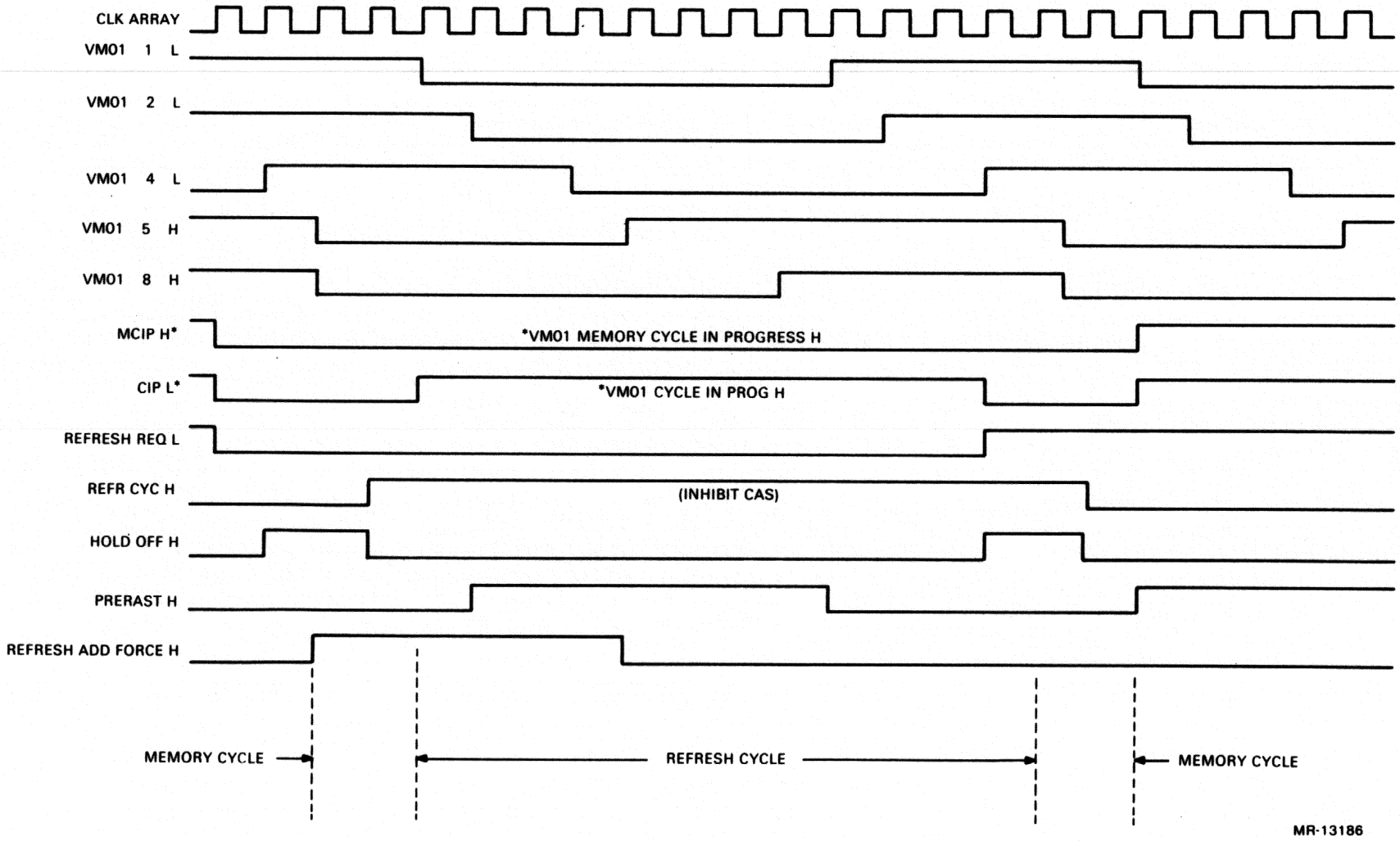

Figure B-10 Refresh Timing

B.5 L0222 TERMINATOR MODULE DESCRIPTION

The terminator module serves two functions. It provides the required termination resistance for each of the array bus lines. It also contains the SDB visibility logic that permits diagnostics to activate and retrieve the state of the array bus lines during diagnostic testing. Two 10141 4-bit shift registers and ten 10164 8 × 1 multiplexers provide the interface to the SDB. To snapshot the state of the array bus signals, the VAX 8600 console software shifts control information into the shift register via MTM3 SDB DATA IN to select one of the eight inputs to the visibility multiplexers and enable the multiplexers to be read. The output from the multiplexers is then clocked into the shift register with SDB CLOCK 19 and shifted back out to the console via SDB DATA OUT 19. This process is repeated until all inputs to all multiplexers have been read.

The following control signals are activated by the shift register output in control mode.

1. VIS MUX ENA 0 – When low, it enables E1,2,5,6,7,10,11, and 14.
2. VIS MUX ENA 1 – When low, it enables E15 and E16.
3. VIS MUX S<2:0> – It selects one of the eight inputs to the enabled multiplexers.

All SDB shift and load operations are synchronized with a transition of SDB CLOCK 19.

B.6 MICRODIAGNOSTICS

The set of VAX 8600 microdiagnostics include a test program, EDK5A, that provides the service engineer with a tool for testing the L0200 array modules. It is run from the DIAGNOSTIC context by typing the following command.

```
DC>@EDK5A
```

EDK5A contains a comprehensive set of microtests that test each available L0200 module and provide detailed fault isolation information. Refer to the *VAX 8600 System Diagnostics User's Guide* for a more detailed description of the available microdiagnostics.