

DRAWING PROCESSOR
 PROC
 Thu Nov 9 16:10:49 1995

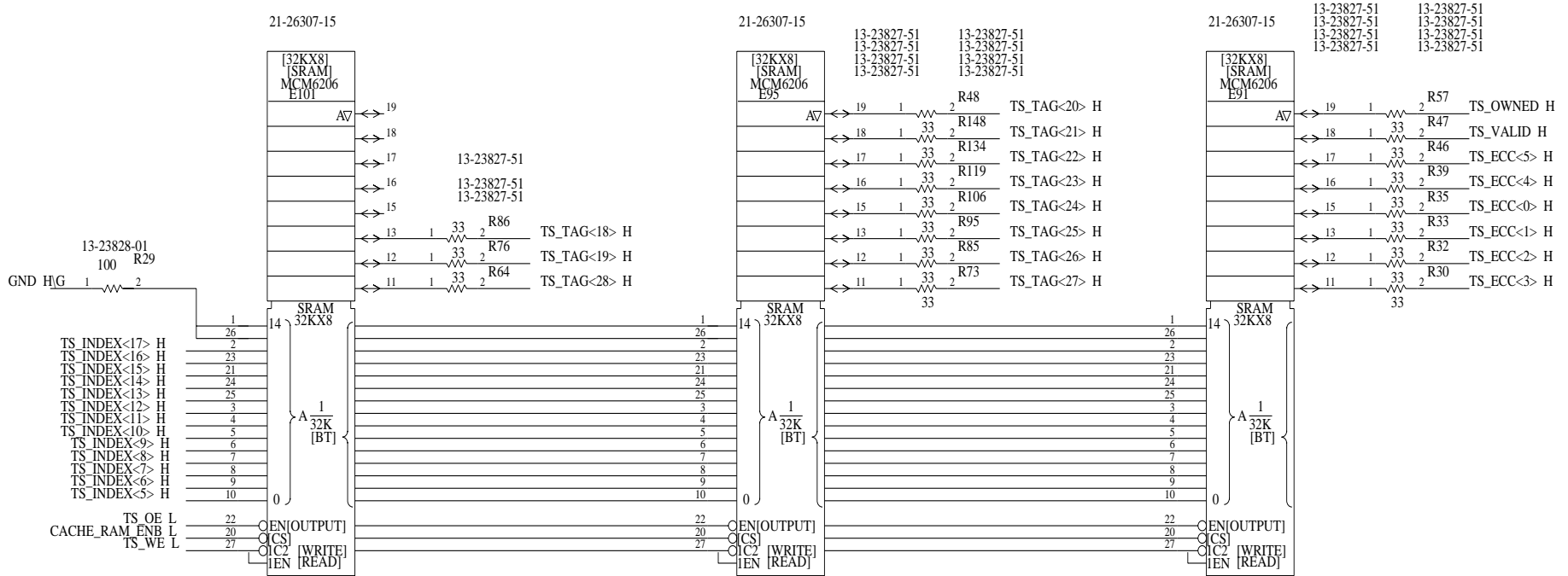
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REVISION	CHK	CHANGE NO.	REV

digital	DRN: JOHN BELL	DATE: 05-OCT-95	ENG: FRASER MURPHY	DATE: 25-OCT-95	TITLE:
	CHK'D: JOHN BELL	DATE: 25-OCT-95	BOARD LOCATION:	SHEET: 1 OF 20	PROCESSOR
USRA:	TOP DOCUMENT NUMBER:	K-DD-B1000-A-C		MEDIA CODE:	
FIRST USED ON OPTION MODEL:	DNSAN		REV: AX01		

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Cache Tag Store



PLACE SERIES RESISTORS CLOSE TO THE SRAMS

DRAWING

LAST_MODIFIED = Thu Nov 9 16:11:09 1995

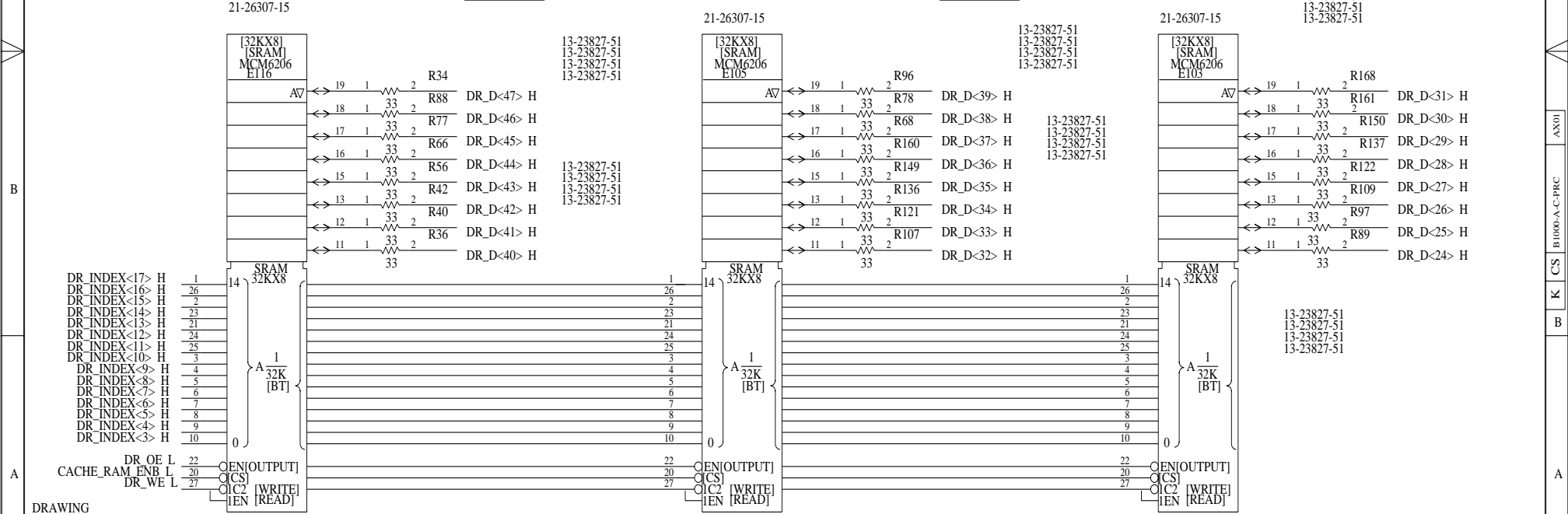
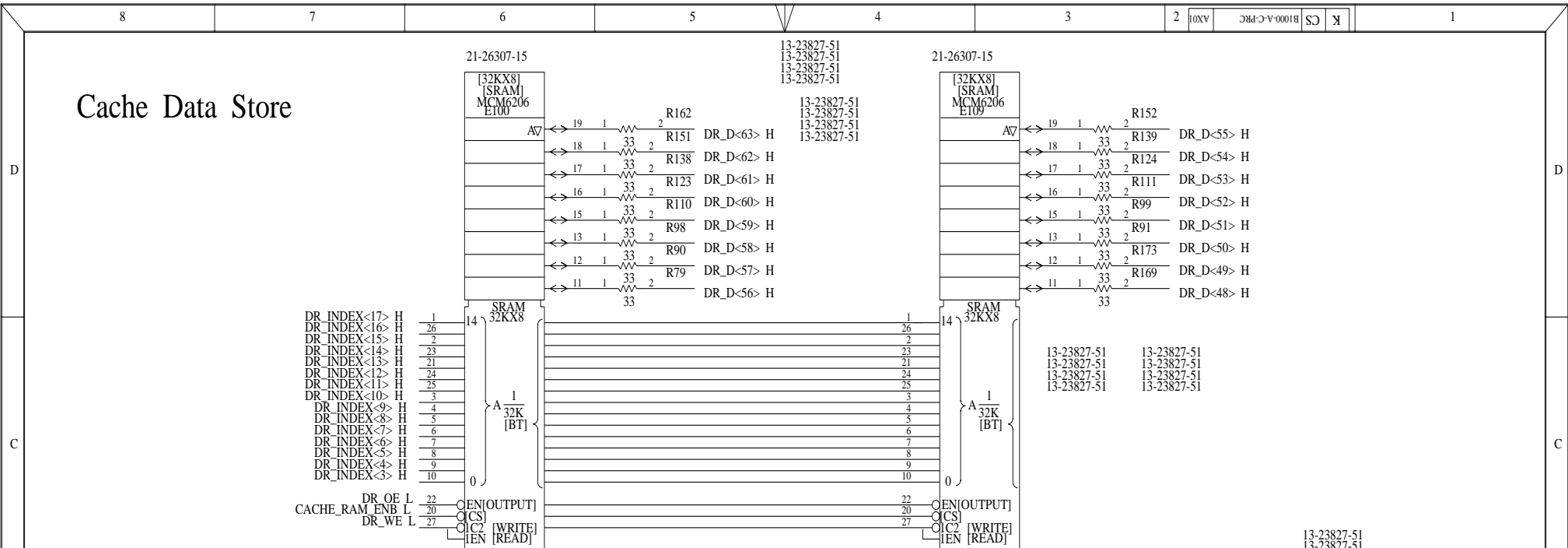
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REVISION	CHK	CHANGE NO.	REV

digital	DRN	DATE	ENG.	DATE	TITLE:
	JOHN BELL	05-OCT-95	FRASER MURPHY	24-OCT-95	PROCESSOR
CHK'D	DATE	BOARD LOCATION:	SHEET	TOP DOCUMENT NUMBER:	
JOHN BELL	24-OCT-95		2	OF 20	
USRA:	FIRST USED ON OPTION MODEL:	DNSAN	K-DD-B1000-A-C		

MEDIA	CODE	NUMBER	REV.
K	CS	B1000-A-C-PRC	AX01

Cache Data Store



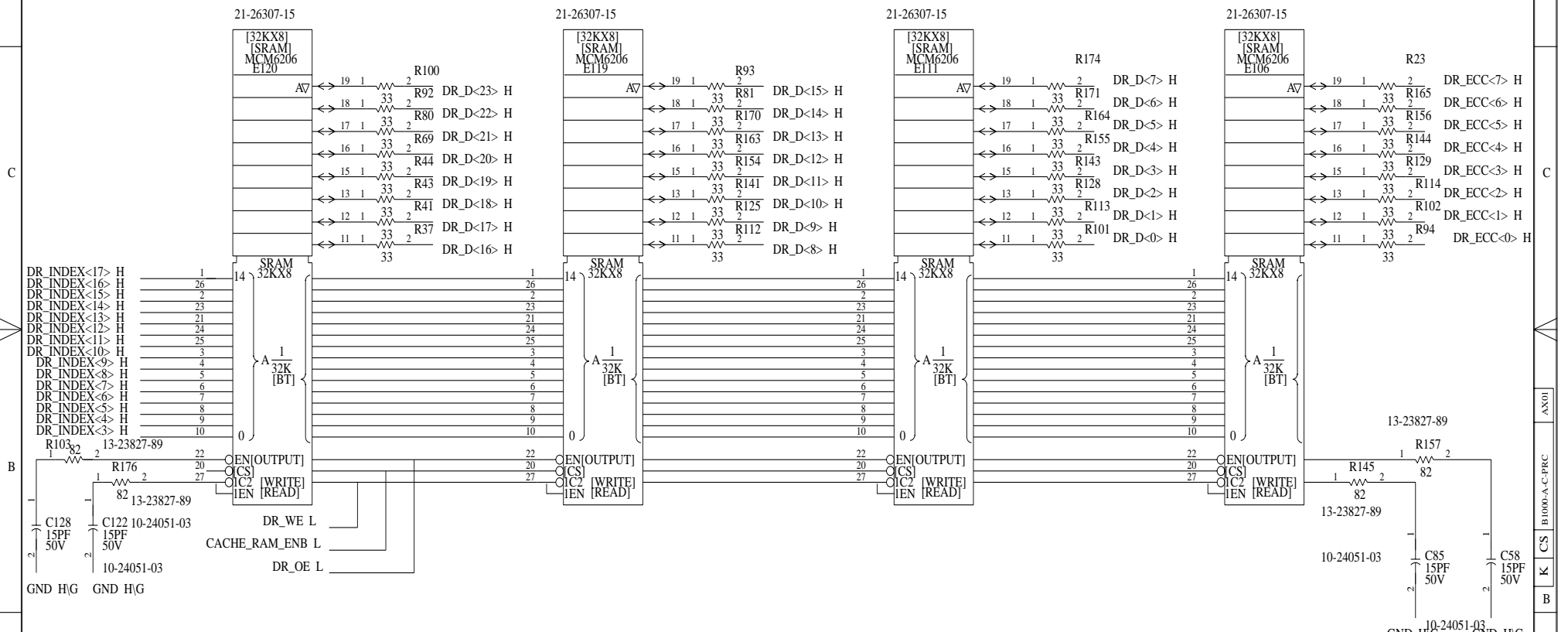
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REVISION	DATE
CHK CHANGE NO. REV	

	DRN: JOHN BELL	DATE: 05-OCT-95	ENG: FRASER MURPHY	DATE: 24-OCT-95	TITLE: PROCESSOR
	CHK'D: JOHN BELL	DATE: 24-OCT-95	SHEET: 3 OF 20	BOARD LOCATION: K CS	NUMBER: B1000-A-C-PRC
USRA: FIRST USED ON OPTION MODEL: DNSAN	TOP DOCUMENT NUMBER: K-DD-B1000-A-C		MEDIA: K	CODE: CS	REV: AX01

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Cache Data Store

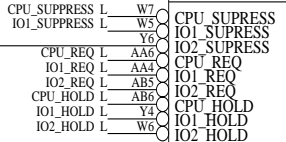
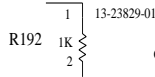
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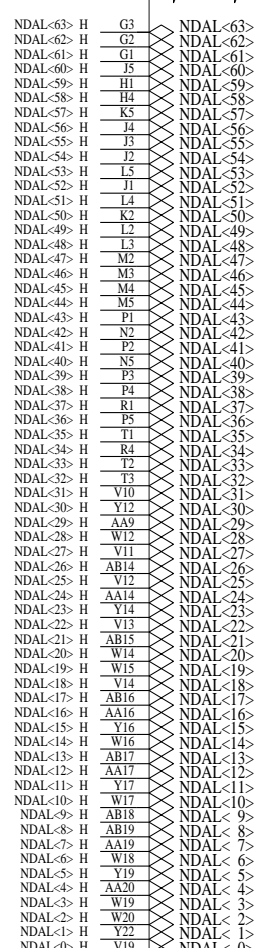
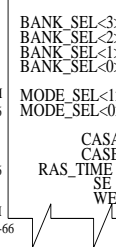
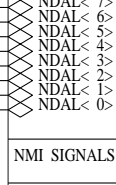
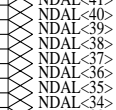
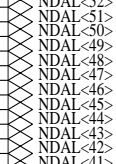
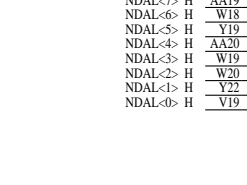
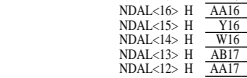
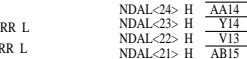
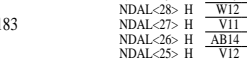
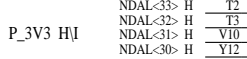
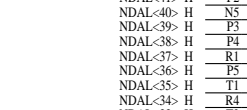
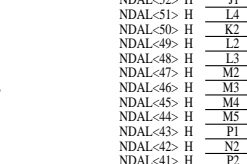
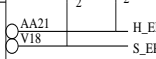
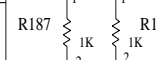
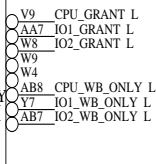
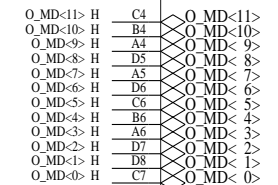
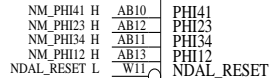
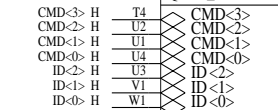
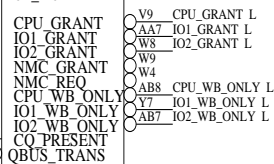
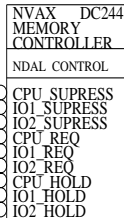
REVISION	DATE	BY
CHK CHANGE NO. REV		

digital	DRN JOHN BELL	DATE 05-OCT-95	ENG. FRASER MURPHY	DATE 25-OCT-95	TITLE:
	CHK D. JOHN BELL	DATE 25-OCT-95	BOARD LOCATION:	SHEET 4 OF 20	PROCESSOR
USRA:	TOP DOCUMENT NUMBER:	K-DD-B1000-A-C		MEDIA CODE:	NUMBER B1000-A-C-PRC
FIRST USED ON OPTION MODEL:	DNSAN			REV:	AX01

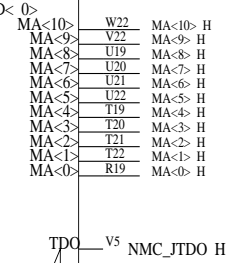
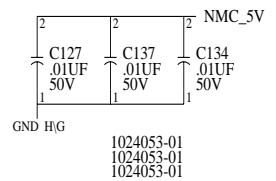
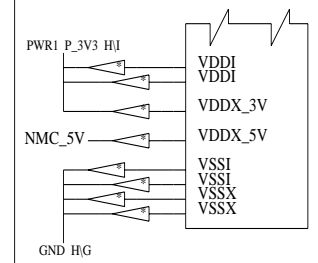
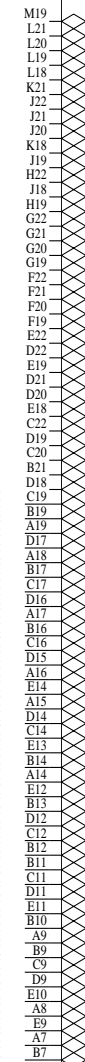
PWR1_P_3V3 HI



E66
21-33500-01



NOTE: CYCLOPS ONLY USES 32BITS AND 7BITS ECC



Memory Controller

DRAWING
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REVISION	CHK	CHANGE NO.	REV

digital	DRN	JOHN BELL	DATE	05-OCT-95	ENG.	FRASER MURPHY	DATE	25-OCT-95	TITLE:	PROCESSOR			
	CHK'D.	JOHN BELL	DATE	25-OCT-95	BOARD LOCATION:	SHEET	5	OF	20				
USRA:	FIRST USED ON OPTION MODEL:			DNSAN	TOP DOCUMENT NUMBER:	K-DD-B1000-A-C			MEDIA	CODE	NUMBER	REV.	
										K	CS	B1000-A-C-PRC	AX01

D

D

C

C

B

AX01

B1000-A-C-PRC

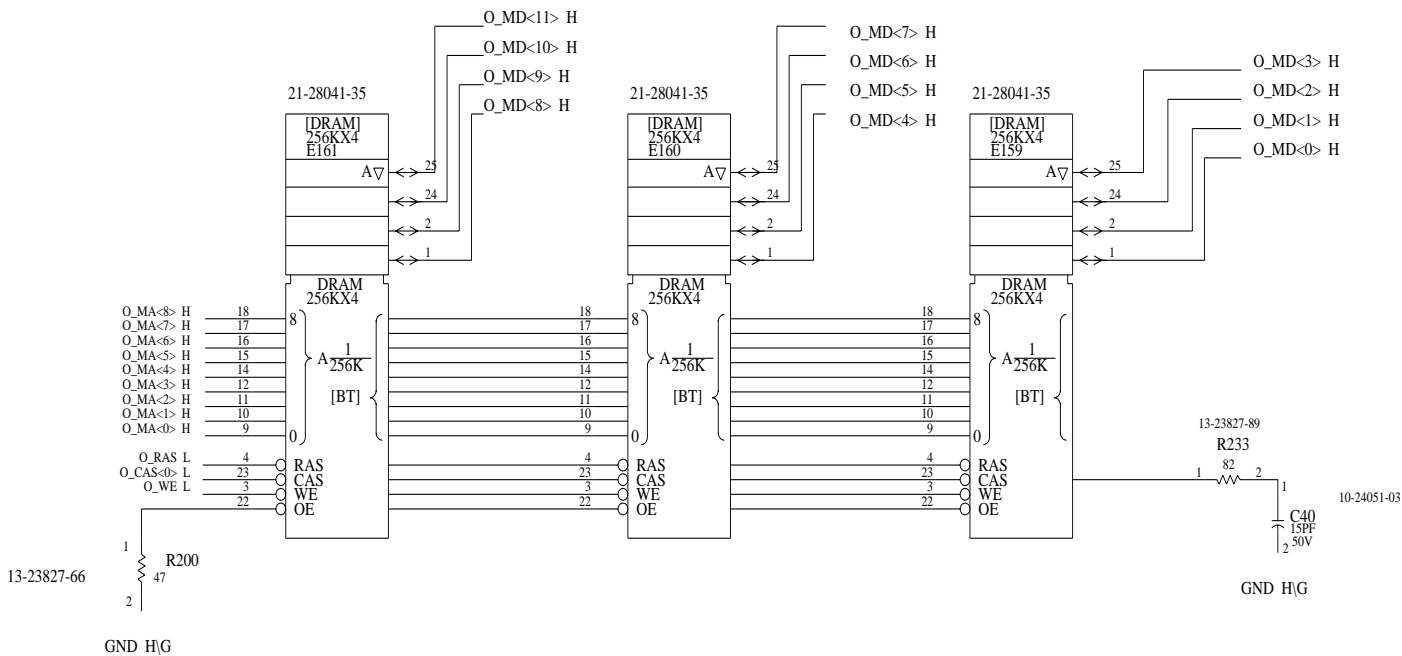
CS

K

B

A

A



Ownership RAMS

DRAWING
LAST_MODIFIED = Thu Nov 9 16:12:28 1995

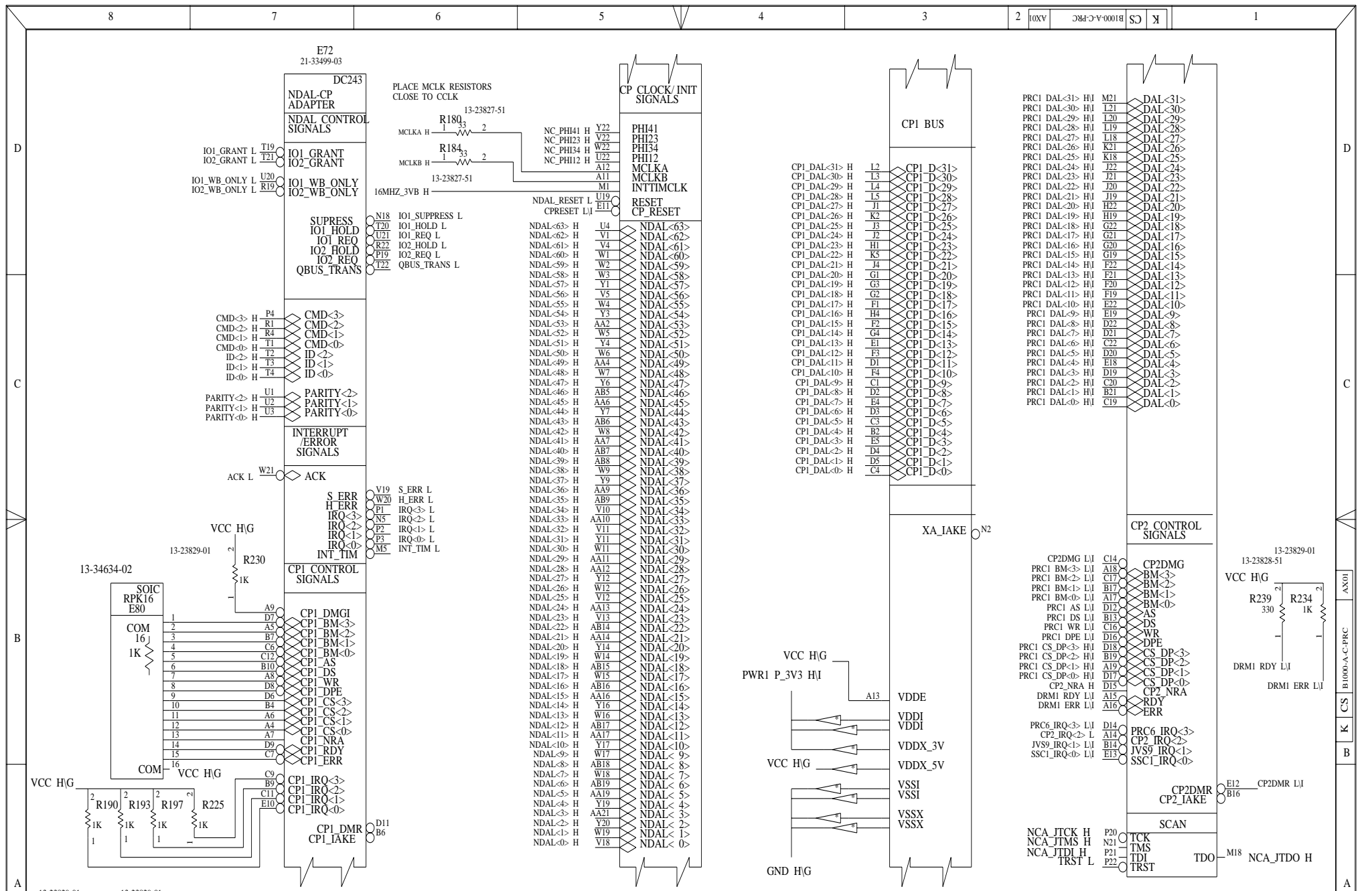
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CHK	CHANGE NO.	REV

DRN	JOHN BELL	DATE	05-OCT-95
CHK'D	JOHN BELL	DATE	25-OCT-95
USRA:	FIRST USED ON OPTION MODEL: DNSAN		

ENG.	FRASER MURPHY	DATE	25-OCT-95
BOARD LOCATION:			
SHEET	6	OF	20
TOP DOCUMENT NUMBER:	K-DD-B1000-A-C		

TITLE:	PROCESSOR		
MEDIA	CODE	NUMBER	REV.
K	CS	B1000-A-C-PRC	AX01



CP Bus Adapter

DRAWING 13-23829-01
 LAST_MODIFIED = Thu Nov 9 16:12:55 1995

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REVISION	CHK	CHANGE NO.	REV

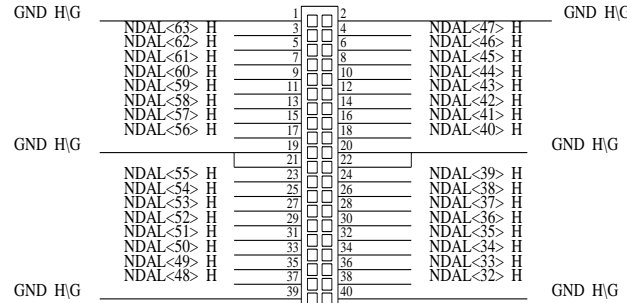
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CHK'D: JOHN BELL	DATE: 25-OCT-95	BOARD LOCATION: SHEET 7 OF 20	TITLE: PROCESSOR
USRA: FIRST USED ON OPTION MODEL: DNSAN	TOP DOCUMENT NUMBER: K-DD-B1000-A-C	MEDIA CODE: K CS	NUMBER: B1000-A-C-PRC

REV: AX01

ANALYSER CONNECTORS FOR NDAL

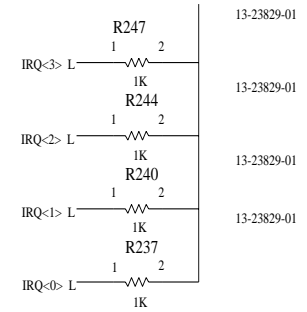
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J15



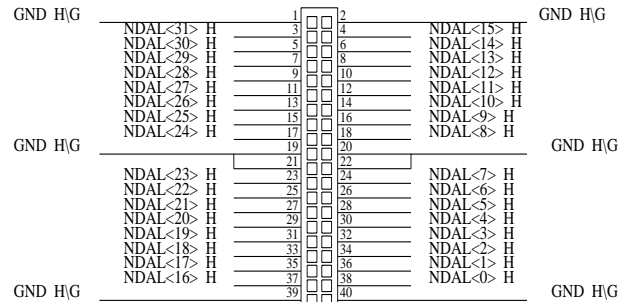
12-23627-06

PWR1 P_3V3 H/I



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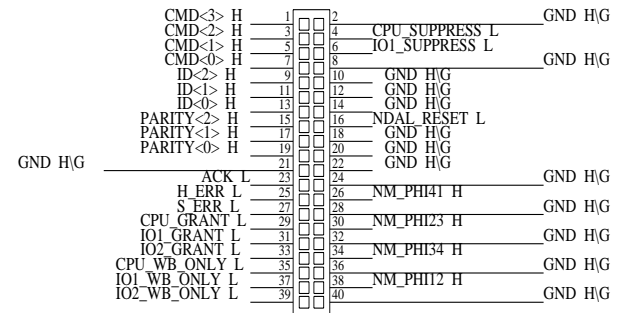
J17



12-23627-06

NDAL CONTROL/STATUS

J16



12-23627-06

NOTE : REMOVED NDAL ARB PINS FROM TEST CONNECTOR

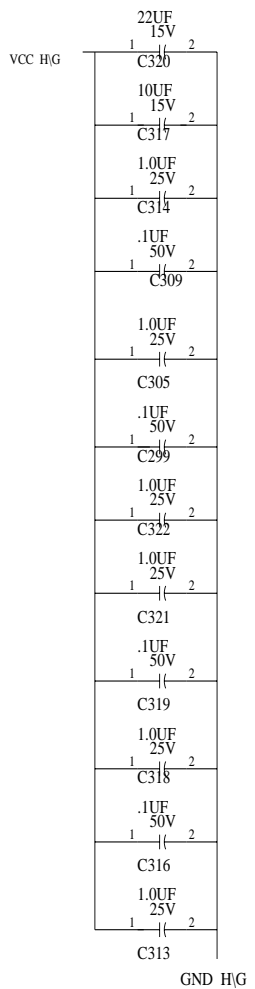
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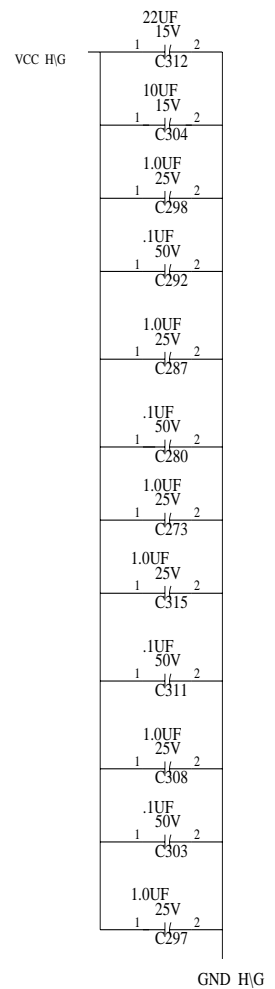
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digital	DRN JOHN BELL	DATE 05-OCT-95	ENG. FRASER MURPHY	DATE 25-OCT-95	TITLE:
	CHK'D JOHN BELL	DATE 25-OCT-95	BOARD LOCATION:	SHEET 8 OF 20	PROCESSOR
USRA:	FIRST USED ON OPTION MODEL: DNSAN		TOP DOCUMENT NUMBER: K-DD-B1000-A-C	MEDIA CODE K CS	NUMBER B1000-A-C-PRC
				REV. AX01	

AX01
B1000-A-C-PRC
CS
K
B



SIMM A



SIMM B

MEMORY SIMM DECOUPLING

D
C
B
A

D
C
B
A

AX01
B1000-A-C-PRC
CS
K
B

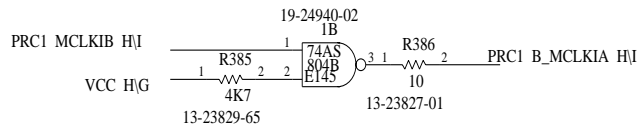
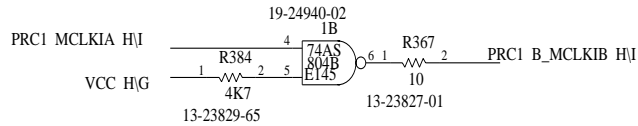
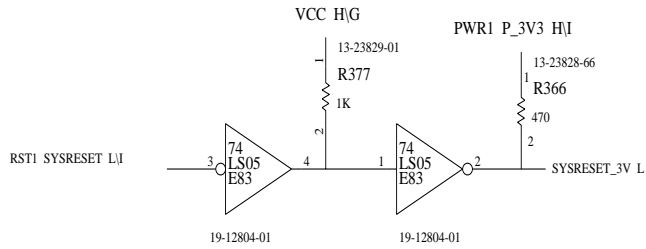
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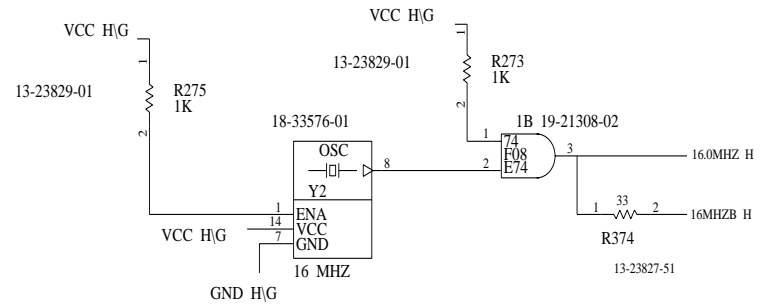
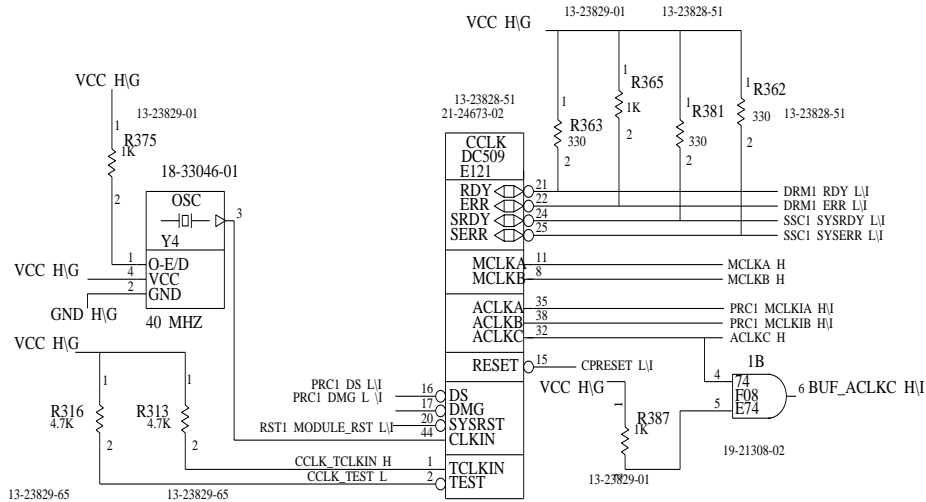
REVISION	CHK	CHANGE NO.	REV

digital	DRN	DATE	ENG.	DATE	TITLE:
	JOHN BELL	05-OCT-95	FRASER MURPHY	25-OCT-95	PROCESSOR
USKA:	CHK'D	DATE	BOARD LOCATION:	SHEET	TOP DOCUMENT NUMBER:
FIRST USED ON OPTION MODEL:	JOHN BELL	25-OCT-95	9	OF 20	K-DD-B1000-A-C
DNSAN	MEDIA CODE			NUMBER	REV.
	K	CS	B1000-A-C-PRC	AX01	

CP BUS Clocks, Oscillators

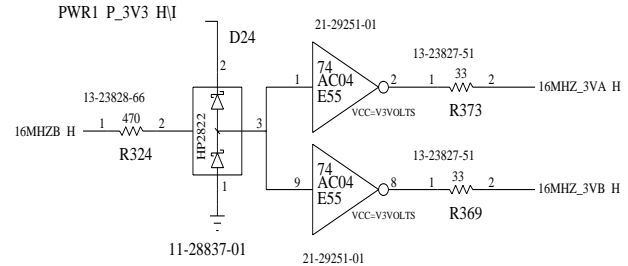
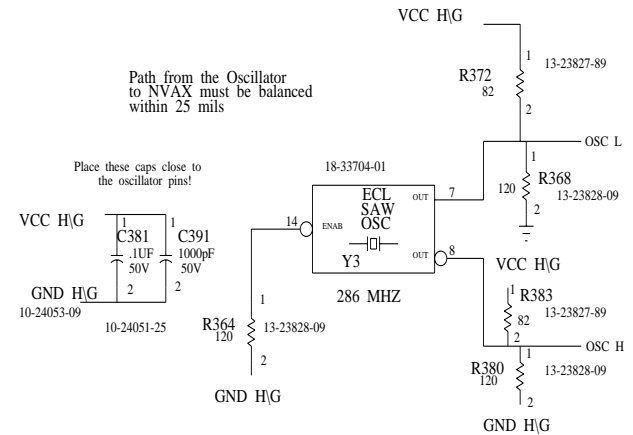


CP_BUS_CLOCK



Path from the Oscillator to NVAX must be balanced within 25 mils

Place these caps close to the oscillator pins!



NOTES:

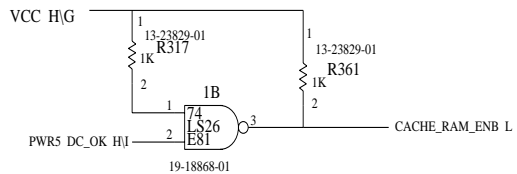
1. MCLK SERIES RESISTORS (NCA) TO BE PLACED AT TEE NEAR CCLK
2. DO NOT SHORT OR BACKDRIVE THE OSC_H OR OSC_L SIGNALS.

DRAWING
LAST_MODIFIED = Thu Nov 9 16:05:23 1995

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REVISION	DATE	BY
CHK CHANGE NO. REV		

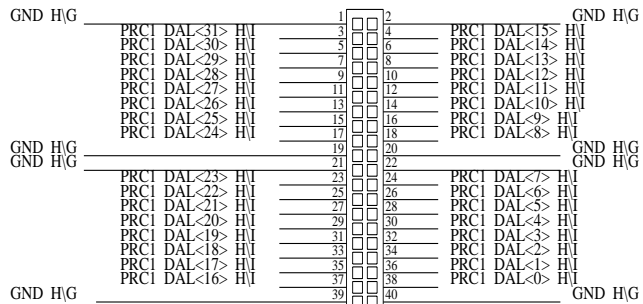
DIGITAL	DRN. JOHN BELL	DATE 05-OCT-95	ENG. FRASER MURPHY	DATE 25-OCT-95	TITLE: PROCESSOR
	CHK D. JOHN BELL	DATE 25-OCT-95	SHEET 10 OF 20	BOARD LOCATION: K CS	NUMBER B1000-A-C-PRC
USRA: FIRST USED ON OPTION MODEL: DNSAN	TOP DOCUMENT NUMBER: K-DD-B1000-A-C		MEDIA CODE: K CS	REV: AX01	



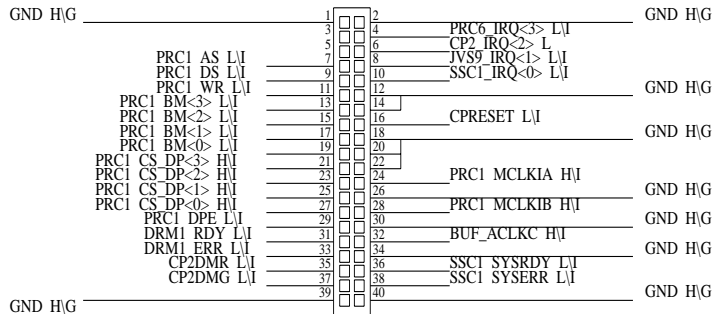
19-18868-01
CACHE DRIVER DISABLE LOGIC

ANALYSER CONNECTORS FOR CP2BUS

CP2_D<31:16>
12-23627-06
J21



CP2 CONTROL/STATUS
12-23627-06
J22



DRAWING
LAST_MODIFIED = Thu Nov 9 16:05:47 1995

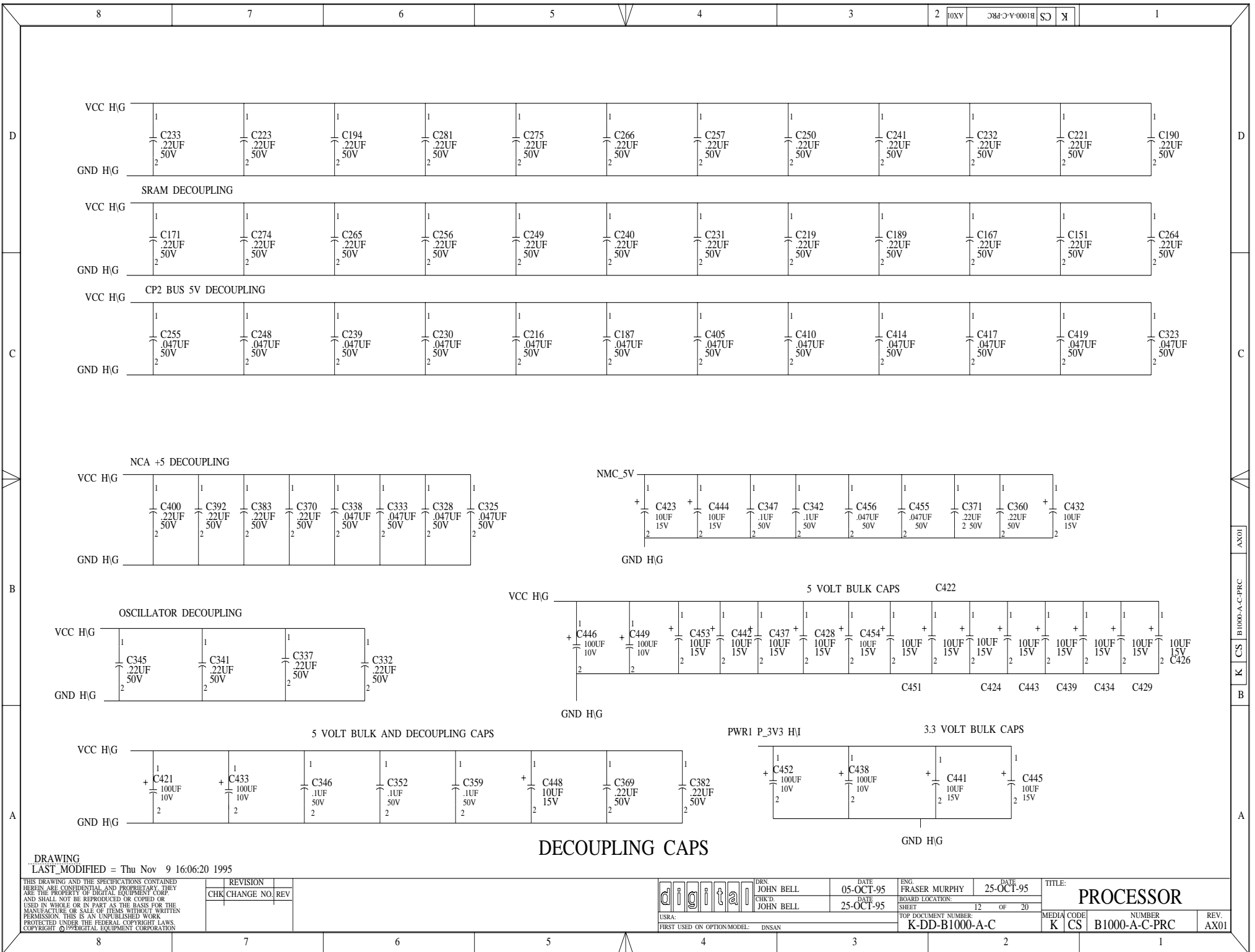
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digital	DRN:	JOHN BELL	DATE:	05-OCT-95
	CHK'D:	JOHN BELL	DATE:	25-OCT-95
USRA:		FIRST USED ON OPTION/MODEL: DNSAN		

ENG.:	FRASER MURPHY	DATE:	25-OCT-95
BOARD LOCATION:		SHEET 11 OF 20	
TOP DOCUMENT NUMBER:			
K-DD-B1000-A-C			

TITLE:		PROCESSOR	
MEDIA:	CODE:	NUMBER:	REV.
K	CS	B1000-A-C-PRC	AX01

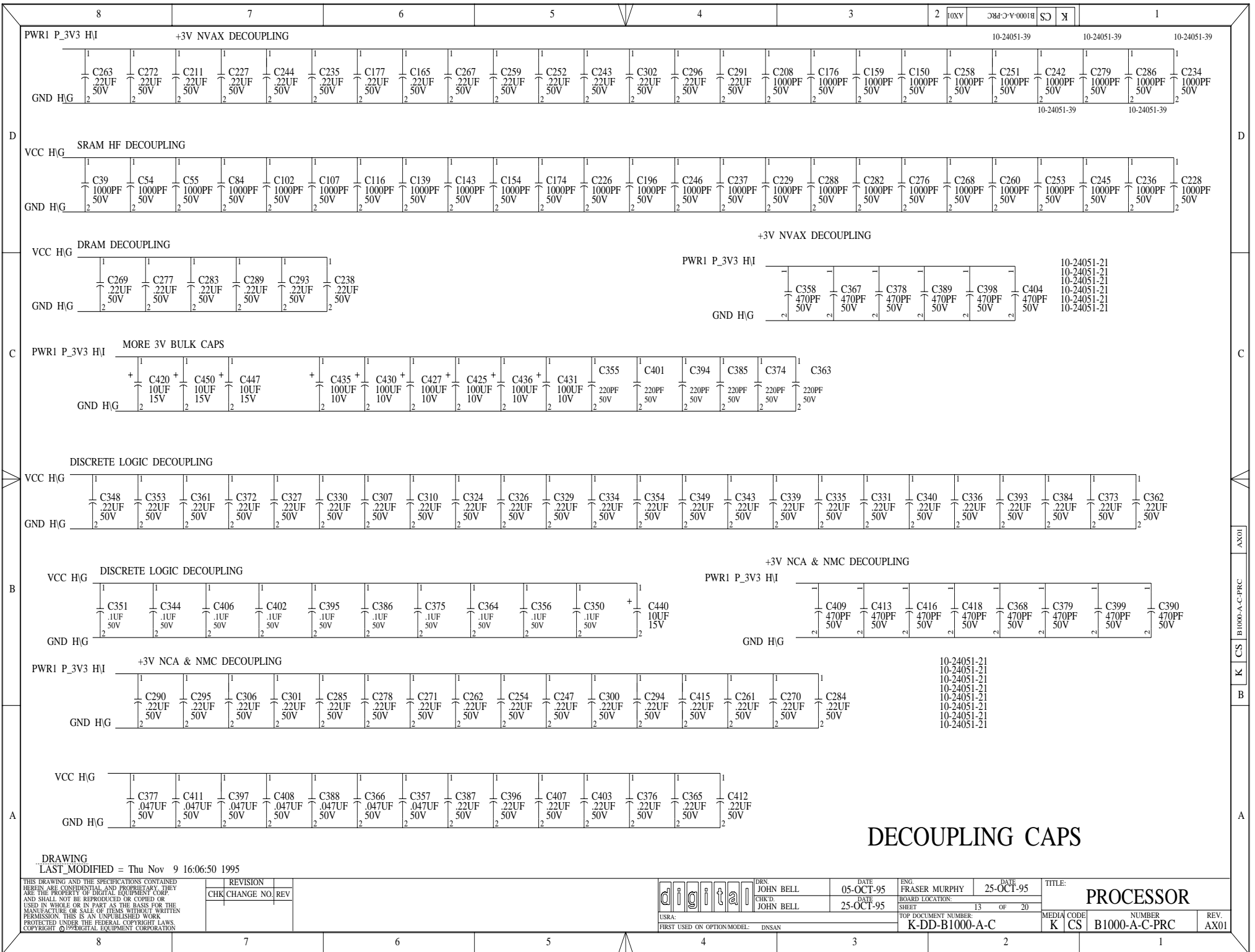


DRAWING
 LAST_MODIFIED = Thu Nov 9 16:06:20 1995

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REVISION	DATE	BY
CHK CHANGE NO. REV		

digital	DRN	DATE	ENG.	DATE	TITLE:
	JOHN BELL	05-OCT-95	FRASER MURPHY	25-OCT-95	PROCESSOR
	CHK D.	DATE	SHEET	BOARD LOCATION:	
	JOHN BELL	25-OCT-95	12 OF 20		
USRA:	TOP DOCUMENT NUMBER:		MEDIA	CODE	NUMBER
FIRST USED ON OPTION MODEL:	K-DD-B1000-A-C		K	CS	B1000-A-C-PRC
	DNSAN				REV. AX01



DECOUPLING CAPS

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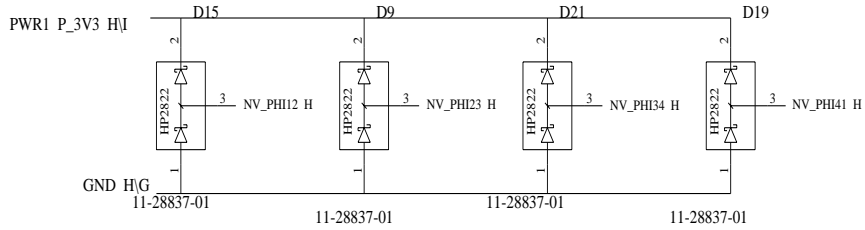
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REVISION	CHK	CHANGE NO.	REV

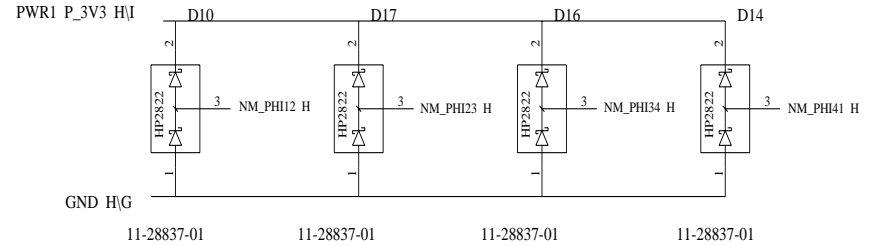
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	CHK'D: JOHN BELL	DATE: 25-OCT-95	BOARD LOCATION:	SHEET: 13 OF 20	PROCESSOR
USRA:	TOP DOCUMENT NUMBER:	K-DD-B1000-A-C		MEDIA CODE:	NUMBER: B1000-A-C-PRC
FIRST USED ON OPTION MODEL: DNSAN				REV:	AX01

AX01 B1000-A-C-PRC K CS B

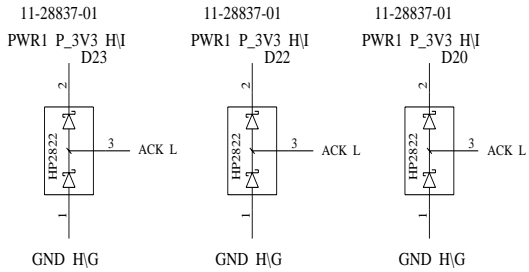
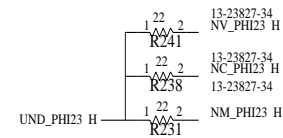
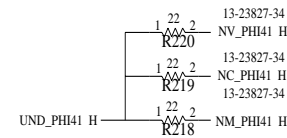
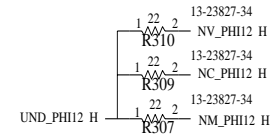
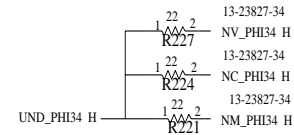
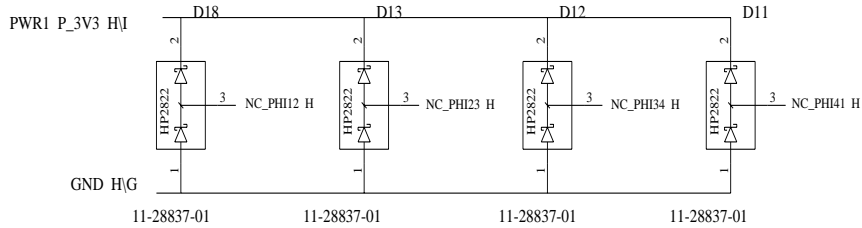
Place beyond the NVAX clock inputs



Place beyond the NMC clock inputs



Place beyond the NCA clock inputs



Place near NVAX Place near NMC Place near NCA

NOTE:

The UND_PHIxx lines must be equal length.
The Nx_PHIxx lines must be equal length

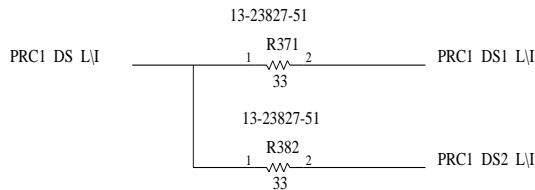
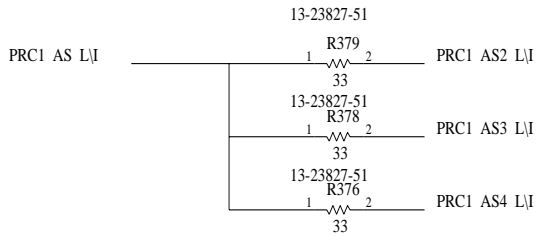
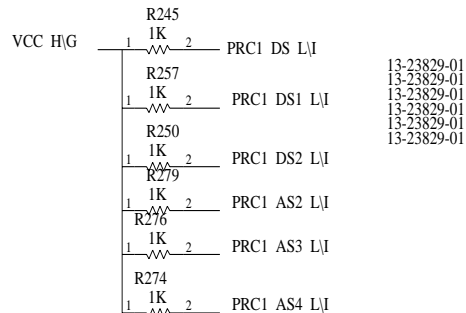
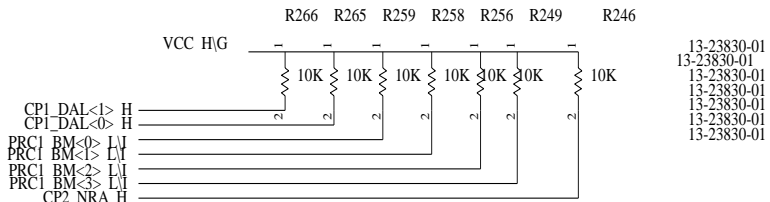
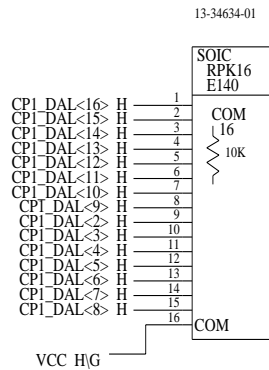
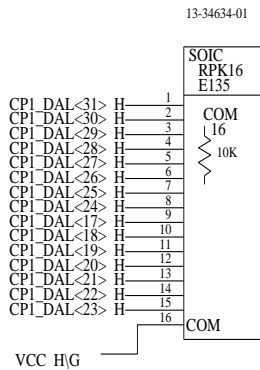
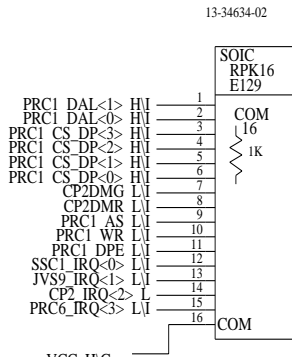
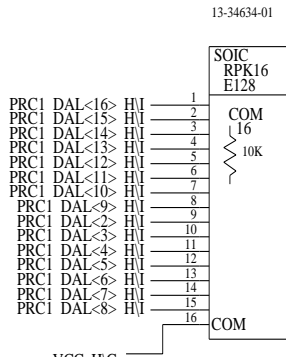
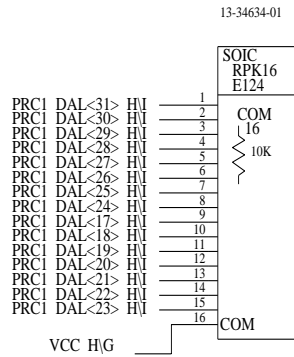
NDAL TERMINATIONS & NDAL CLOCKS

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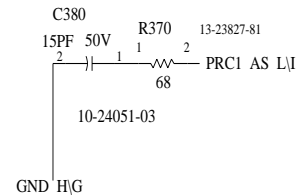
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USRA:	CHK'D.	DATE	BOARD LOCATION:	SHEET	MEDIA
FIRST USED ON OPTION MODEL:	JOHN BELL	25-OCT-95	14	OF 20	CS
DNSAN	TOP DOCUMENT NUMBER:			K-DD-B1000-A-C	NUMBER
					B1000-A-C-PRC
					REV.
					AX01



SSC TERMINATORS



CP BUS Pullup Resistors

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USRA:	CHK'D	DATE	SHEET	BOARD LOCATION:	MEDIA
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DNSAN	TOP DOCUMENT NUMBER:		K-DD-B1000-A-C		NUMBER
					B1000-A-C-PRC
					REV.
					AX01

21-35024-01

Ø
[LOW COST]
[GATE ARR]
DC7238A
E84

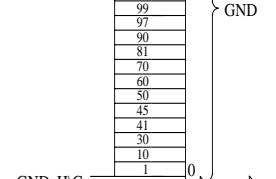
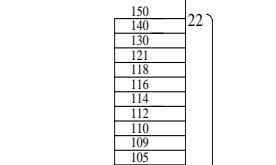
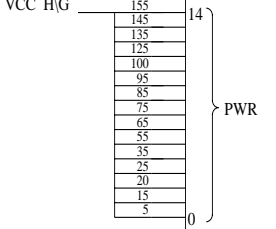
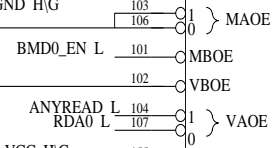
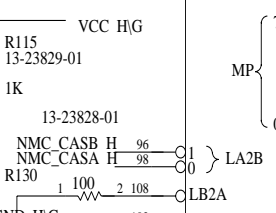
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- MD<30> H 52
- MD<29> H 53
- MD<28> H 54
- MD<27> H 55
- MD<26> H 56
- MD<25> H 57
- MD<24> H 58
- MD<23> H 59
- MD<22> H 60
- MD<21> H 61
- MD<20> H 62
- MD<19> H 63
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- MD<17> H 65
- MD<16> H 66
- MD<15> H 67
- MD<14> H 68
- MD<13> H 69
- MD<12> H 70
- MD<11> H 71
- MD<10> H 72
- MD<9> H 73
- MD<8> H 74
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- MD<5> H 77
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- MD<1> H 81
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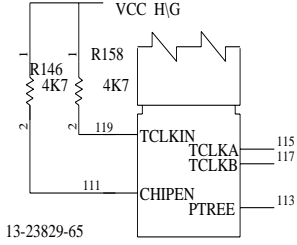


- MD<35> H 91
- MD<34> H 92
- MD<33> H 93
- MD<32> H 94



- 26 SIM_MDA<15> H
- 27 SIM_MDA<14> H
- 28 SIM_MDA<13> H
- 29 SIM_MDA<12> H
- 31 SIM_MDA<11> H
- 32 SIM_MDA<10> H
- 33 SIM_MDA<9> H
- 34 SIM_MDA<8> H
- 36 SIM_MDA<7> H
- 37 SIM_MDA<6> H
- 38 SIM_MDA<5> H
- 39 SIM_MDA<4> H
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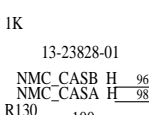
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- 2 SIM_MDB<34> H
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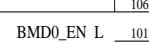
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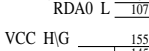
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GND H/G



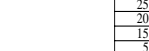
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GND H/G



GND H/G



GND H/G



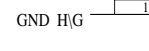
GND H/G



GND H/G



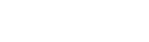
GND H/G



GND H/G



GND H/G



GND H/G

GND H/G

GND H/G

GND H/G

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GND H/G

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	JOHN BELL	05-OCT-95	FRASER MURPHY	25-OCT-95	PROCESSOR
	CHK D.	DATE	BOARD LOCATION:	SHEET	
	JOHN BELL	25-OCT-95		16 OF 20	
USRA:	TOP DOCUMENT NUMBER:		MEDIA	CODE	NUMBER
FIRST USED ON OPTION MODEL:	DNSAN	K-DD-B1000-A-C	K	CS	B1000-A-C-PRC
					REV. AX01

D

C

B

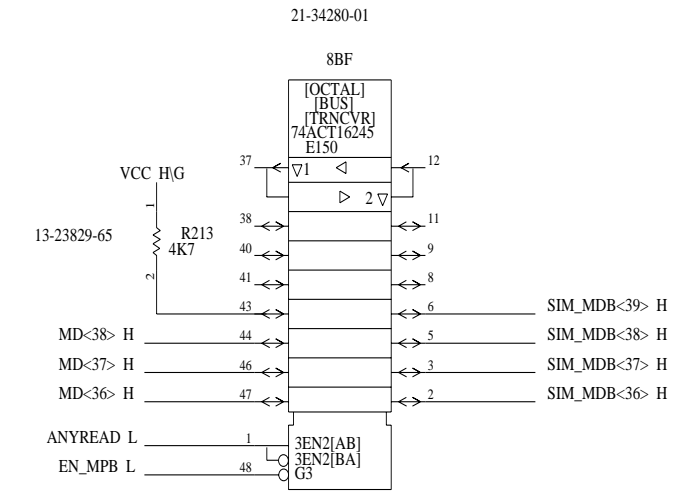
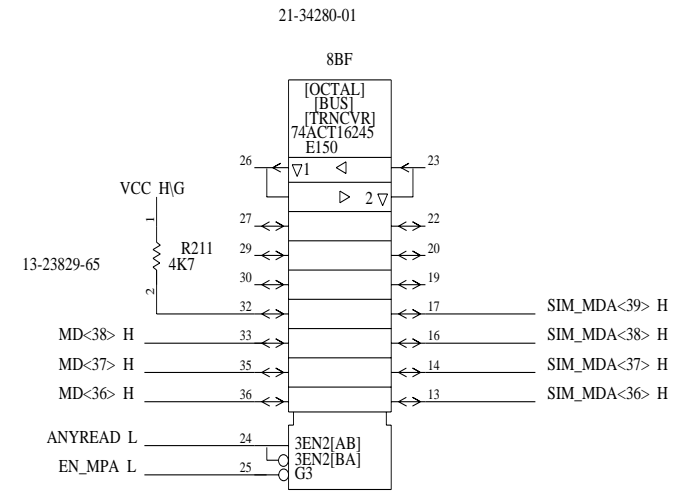
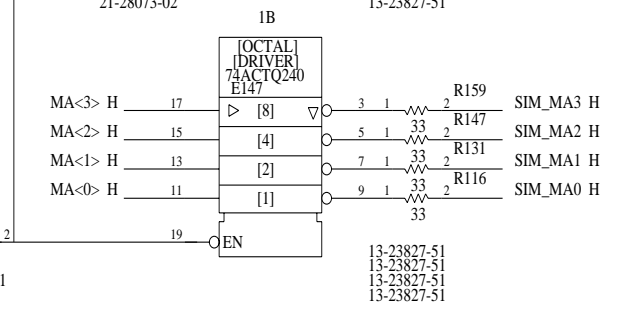
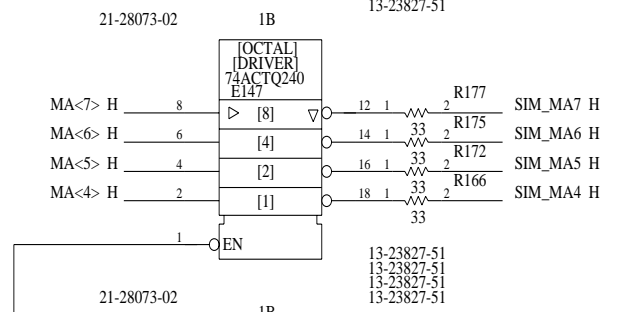
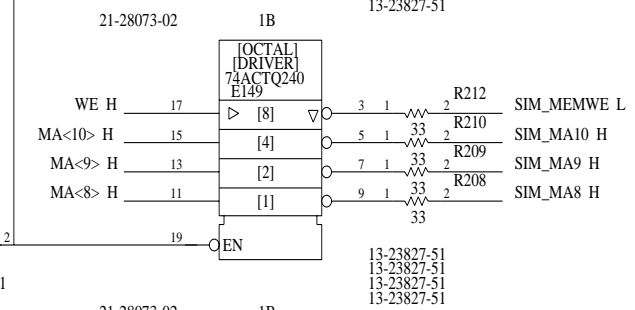
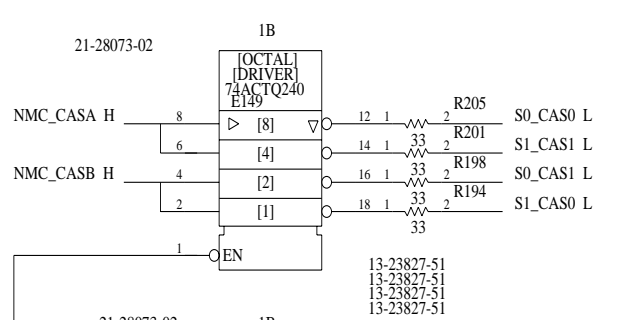
A

D

C

B

A



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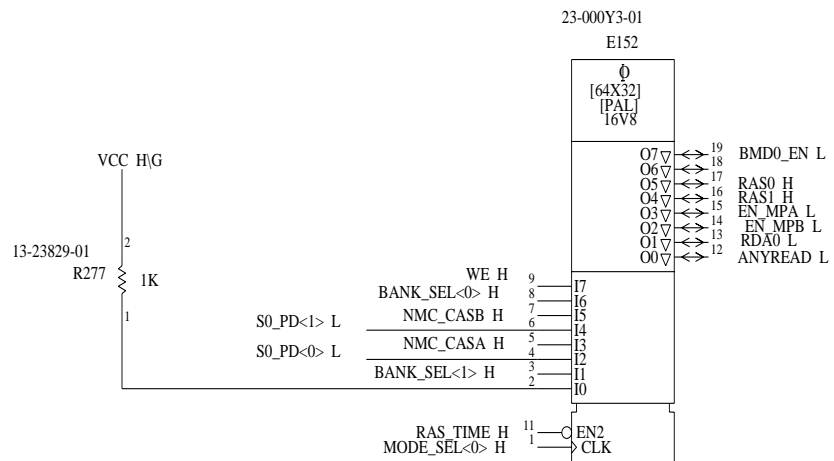
REVISION	CHK	CHANGE NO.	REV

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	JOHN BELL	05-OCT-95	FRASER MURPHY	25-OCT-95	PROCESSOR
USKA:	CHK'D	DATE	BOARD LOCATION:	SHEET	TOP DOCUMENT NUMBER:
FIRST USED ON OPTION MODEL:	JOHN BELL	25-OCT-95	K-DD-B1000-A-C	17 OF 20	K-DD-B1000-A-C
DNSAN					

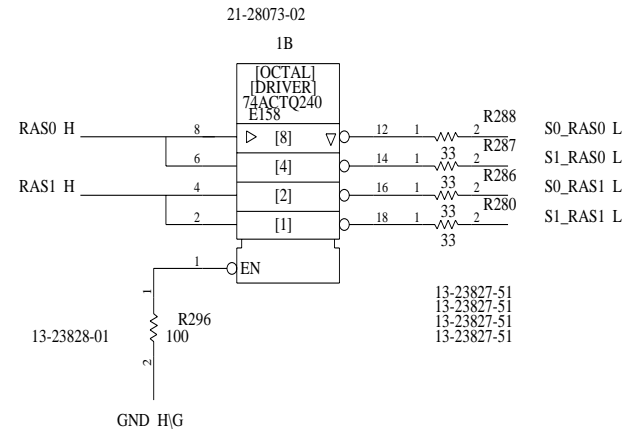
MEDIA	CODE	NUMBER	REV.
K	CS	B1000-A-C-PRC	AX01

AX01
B1000-A-C-PRC
CS
K
B

MEMORY CONTROL PAL



NOTE : PINS 1 & 11 ARE I0 & I9 NOT OEL & CLK



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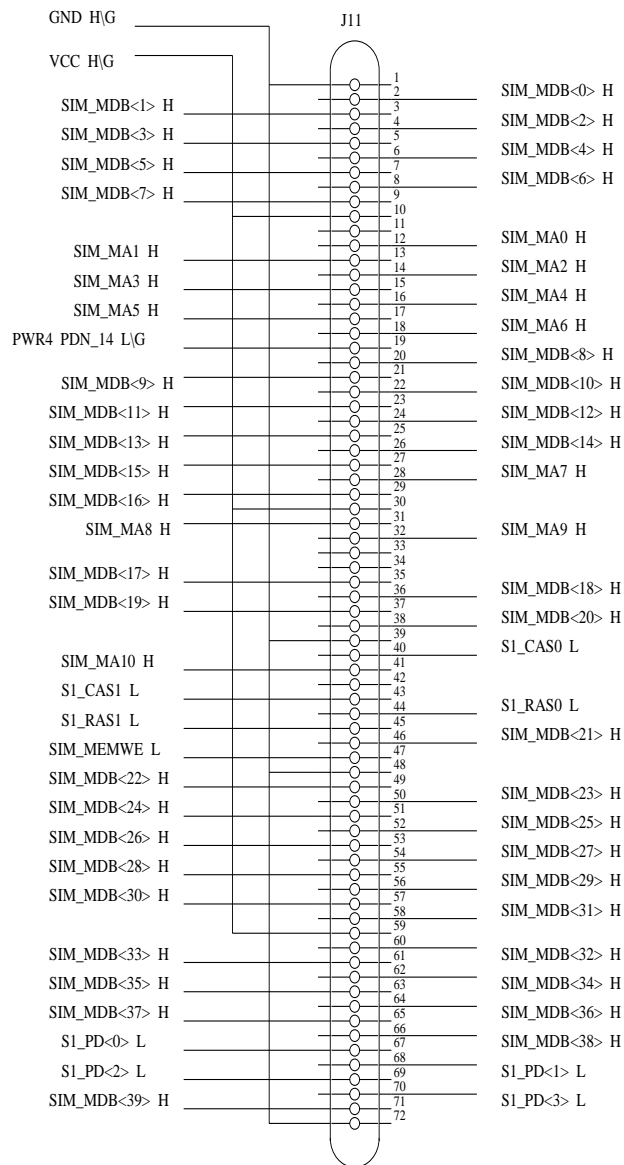
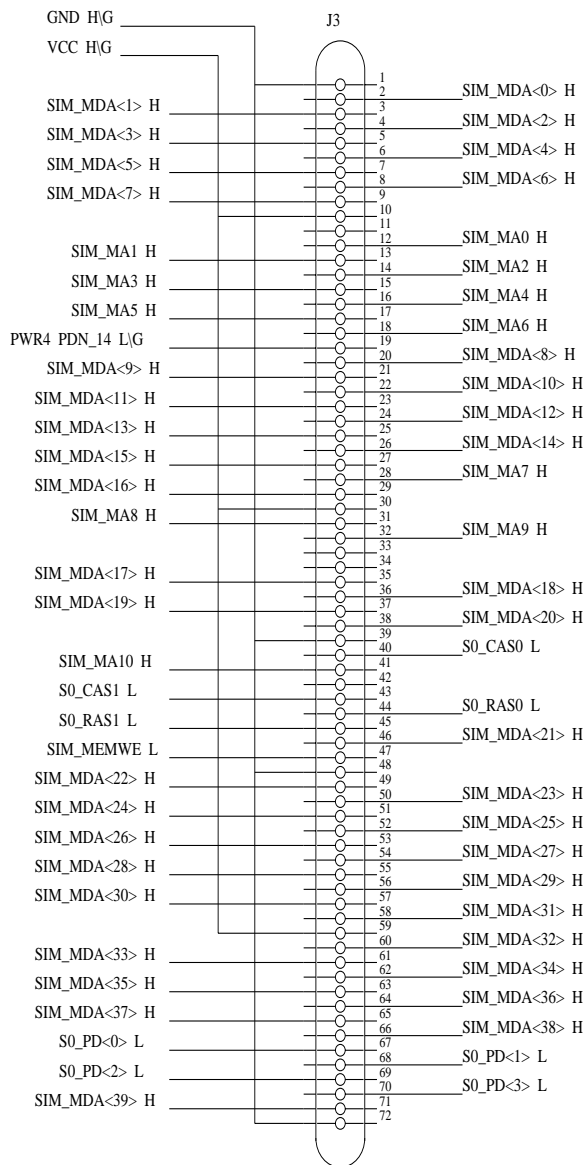
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digital	DRN	DATE	ENG.	DATE	TITLE:
	JOHN BELL	05-OCT-95	FRASER MURPHY	25-OCT-95	PROCESSOR
CHK'D	DATE	BOARD LOCATION:	SHEET	18 OF 20	
JOHN BELL	25-OCT-95				
USRA:	TOP DOCUMENT NUMBER:		MEDIA	CODE	NUMBER
FIRST USED ON OPTION/MODEL:	DNSAN	K-DD-B1000-A-C	K	CS	B1000-A-C-PRC

REV. AX01

12-35432-02

12-35432-02



SIMM CONNECTORS

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	CHK D.	DATE	BOARD LOCATION:	SHEET	
	JOHN BELL	25-OCT-95		19 OF 20	
USRA:	TOP DOCUMENT NUMBER:		MEDIA	CODE	NUMBER
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					REV. AX01

AX01
B1000-A-C-PRC
CS
K
B

D

D

C

C

B

AX01

B1000-A-C-PRC

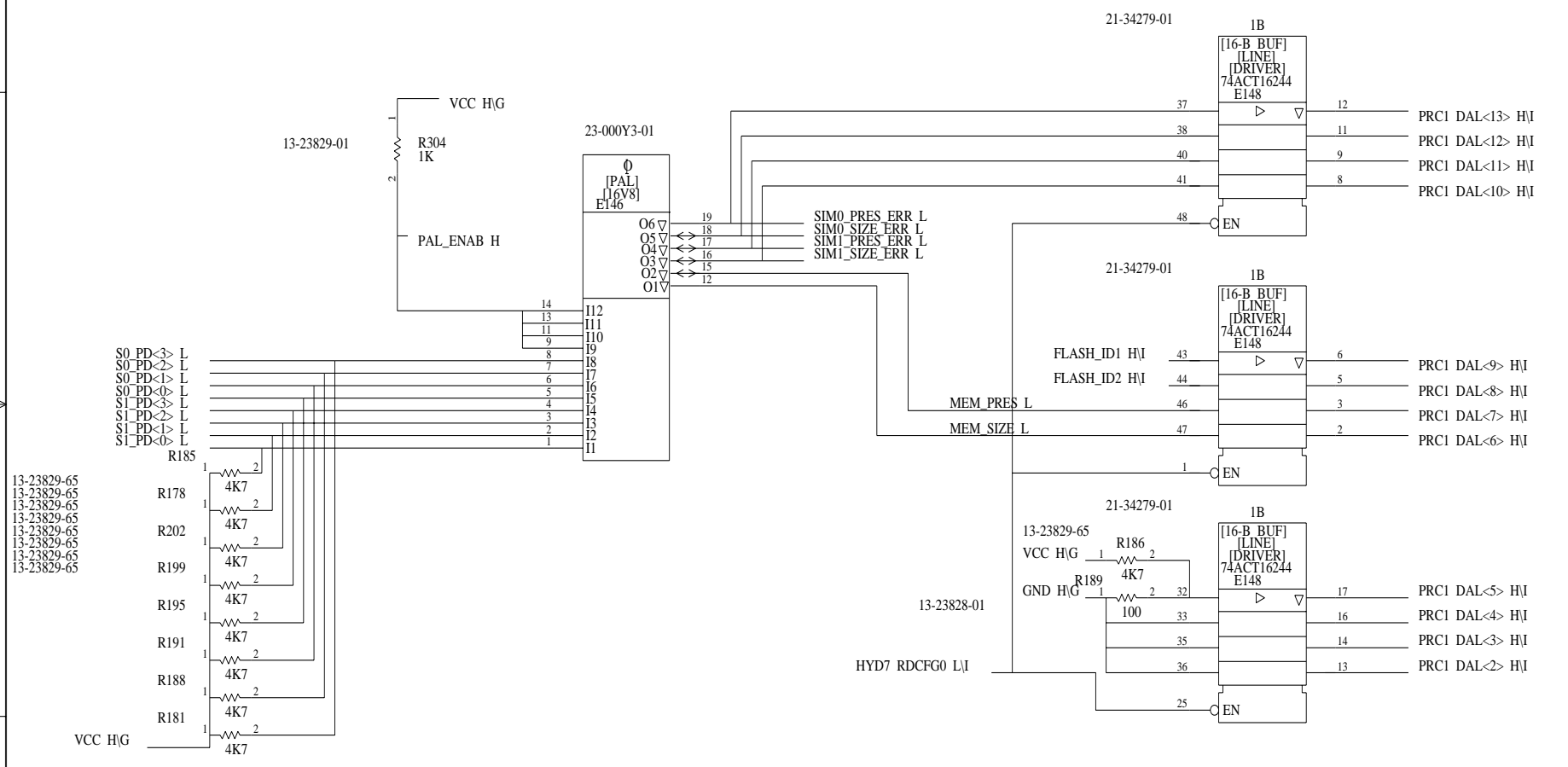
CS

K

B

A

A



Configuration Register

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	JOHN BELL	25-OCT-95		20 OF 20	
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					AX01