DECpc 320sxLP/325sxLP Technical Reference Manual

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FCC Information:

This equipment has been certified to comply with the limits for a Class B computing device, pursuant to Subpart G of Part 15 of FCC Rules. Only peripherals (computer input/output devices, terminals, prints, etc.) certified to comply with the Class B limits may be attached to this computer. Operation with non-certified peripherals is likely to result in interference to radio and TV reception. This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart G of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, you are encouraged to try to correct the interference using one or more of the following methods:

- Re-orient the receiving antenna.
- Relocate the computer or peripheral with respect to the receiver.
- Move the computer or peripheral away from the receiver.
- Plug the computer or peripheral into a different outlet so that they are on different branch circuits than the receiver.

If necessary, you should consult the dealer or an experienced radio/television technician for additional suggestions. You may find the booklet "How to Identify and Resolve Radio/TV Interference Problems" prepared by the Federal Communications Commission helpful. This booklet is available from the U.S. Government Printing Office, Washington D.C. 20402, Stock No. 004-000-00345-4.

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MA 0347 90 CPG DG

Warning:

Shielded cables must be used with this equipment. If you add or replace any cables, the new cables must have shielding capabilities equal to or higher than those provided by the dealer. Modifying or tampering with internal components can cause a malfunction and might invalidate the warranty and void your FCC authorization to operate this equipment.

A

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1

ABOUT THIS MANUAL

This is a Technical Reference Manual provides a comprehensive hardware description of the major components in the DECpc 320sxLP/325sxLP computer. Separate chapters in the manual cover the following topics:

System Overview Chapter 2	Contains system and environmental specifications of the system box.
System Board Chapter 3	Describes major features of the system main logic board.
Central Processing Core Chapter 4	Describes the 80386sx microprocessor
82C386sx Chip Set Chapter 5	Describes operation of the 82C320 system controller/data buffer and the 82C331 ISA bus controller.
82C712 Universal Peripheral Controller Chapter 6	Describes operation of the 82C712 Universal Peripheral Controller II. Information includes Serial & Parallel port descriptions, floppy disk controllers and an Integrated Drive Electronics(IDE) interface description.
8042 Keyboard & Mouse Interface Chapter 7	Describes the operations of the 8042 keyboard and mouse interface.
Video Controller Chapter 8	Describes operation of the OTI VGA Video Controller

Power Supply Chapter 9	Describes the system power supply output specification.
BIOS Interrupt Appendix A	Lists the interrupt service routines available in the system BIOS.
LPS 52/105AT Hard Disk Drives Appendix B	Lists general specifications for the LPS 52/105AT hard disk drives
Floppy Disk Drive (FDD) Appendix C	Describes general specifications for the 3.5", 2MB SONY FDD and the TEAC. 5.25" FDD.

1.1 Conventions

Information that is especially helpful or important is presented as a note, a caution, or a warning:

NOTE: Provides supplementary information of general interest.

CAUTION
Provides information dedicated to avoiding the loss or corruption of data, and/or damage to hardware or equipment.

WARNING
Provides information crucial to preventing personal injury.

1.2 Abbreviations

The following abbreviations are used in this manual:

Kb = kilobit
KB = kilobyte
Mb = megabit
MB = megabyte
Hz = Hertz
MHz = megahertz
ms = millisecond
ns = nanosecond
SIMM = single in-line memory module

1.3 Related Documentation

The following related documents are available as supplements to the information provided in this manual.

Document	Part Number
DECpc 320sxLP/325sxLP User's Guide	EK-DECSX-UG

2

SYSTEM OVERVIEW

This chapter gives information about the technical characteristics of the DECpc 320sxLP/325sxLP. Information includes

- **System Board Specifications**
- **VGA Video Controller Specifications**
- **Environmental Specifications**
- **Physical Dimensions**
- **Power Requirements**
- **System Board Current Requirements**

2.1 System Board Specifications

Table 2-1 lists the system board specifications.

Table 2-1. System Board Specifications

Attribute	Specification
CPU	80386sx
CPU clock speed	20/25 MHz
Master clock speed	40/50 MHz
ISA bus speed	6.67/8/10 MHz
Interrupts	15
Memory addressing	
Physical	16MB
Supported	32MB
ROM BIOS Size	64 KB
DRAM memory	
Speed	80 ns or faster
Type	9-bit SIMM
Standard size	2 MB
Optional sizes	4,6,8,10,12,16,18,20,24,32 MB
Error Protection	Byte parity
System battery	3-year shelf life
Dimensions	8.657 inches by 13 inches
Layers	4

2.2 VGA Video Controller Specifications

Table 2-2 lists the VGA video controller specifications.

Table 2-2. VGA Video Controller Specifications

Attribute	Specification
Processor	OTI-067 microprocessor
Speed	50 MHz
DRAM	512K
Colors	256 from a palette of 256K

2.3 Environmental Specifications

Table 2-3 list the system box environmental specifications.

Table 2-3. Environmental Specifications

Attribute	Specification
Operating temperature	10° to 35°C
Storage temperature	-40°C to 60°C
Operating humidity	20-80% Relative humidity, max wet bulb @33°C
Non-operating humidity	10-90% Relative humidity, max wet bulb @35°C
Altitude	To 10,000 feet maximum
Maximum operating noise	44 dB at operator position
Shock,non-operating	30G, 30 ms, 1/2 sine wave
Vibration, operating 5-500-5 Hz, 1 oct/min sine sweep	0.1G, 1/2 sine wave
Vibration, non-operating 5-300 Hz, 1 oct/min sine sweep	1.19G, 1/2 sine wave

2.4 Physical Dimensions

Table 2-4 lists the physical dimensions of the system box.

Table 2-4. Physical Dimensions

Attribute	Specification
Width	16.14 inches (410 mm)
Height	3.54 inches (90 mm)
Length	15.55 inches (396 mm)
Weight	17.08 lbs (7.75 kg)

2.5 Power Requirements

Table 2-5 lists the power requirements for the system box.

Table 2-5. Power Requirements

Voltage Source	100-120 V ac	220-240 V ac
Maximum Range	88-132 V ac	176-264 V ac
Input Current	3A	1.5A
Frequency Limits	47-63 Hz	47-63 Hz
Power Factor	0.6 min.	0.5 min.
Inrush Current	45A max.	45A max.
Outlet Rating	2A	1A

2.6 System Board Current Requirements

Table 2-6 lists the nominal current requirements for the system board and the parts that obtain power from the system board.

Table 2-6. Current Requirements

Assemblies	+5.0 V dc	-5 V dc	+12.0 V dc	-12.0 V dc
System board with 8 MB of system memory	1.68A	0A	0.1A	0.1A
1.2 MB floppy disk drive	0.46A	0A	0.54A	0A
1.44 MB floppy disk drive	1A	0A	0A	0A
IDE fixed disk drive	0.3A	0A	0.3A	0A
Per Add-on Slot	2A	0.05A	0.5A	0.05A

3

SYSTEM BOARD

This chapter provides an overview of the system main logic board, which includes

- **20MHz or 25MHz 80386sx microprocessor**
- **VLSI 82C386SX Industry Standard Architecture (ISA) chip set**
- **CHIPS 82C712 Universal Peripheral Controller**
- **Keyboard/Mouse Controller**
- **VGA Video Controller**
- **80 ns (or faster) Dynamic Random Access Memory (DRAM)**
- **64 KB of Read-only Memory (ROM)**

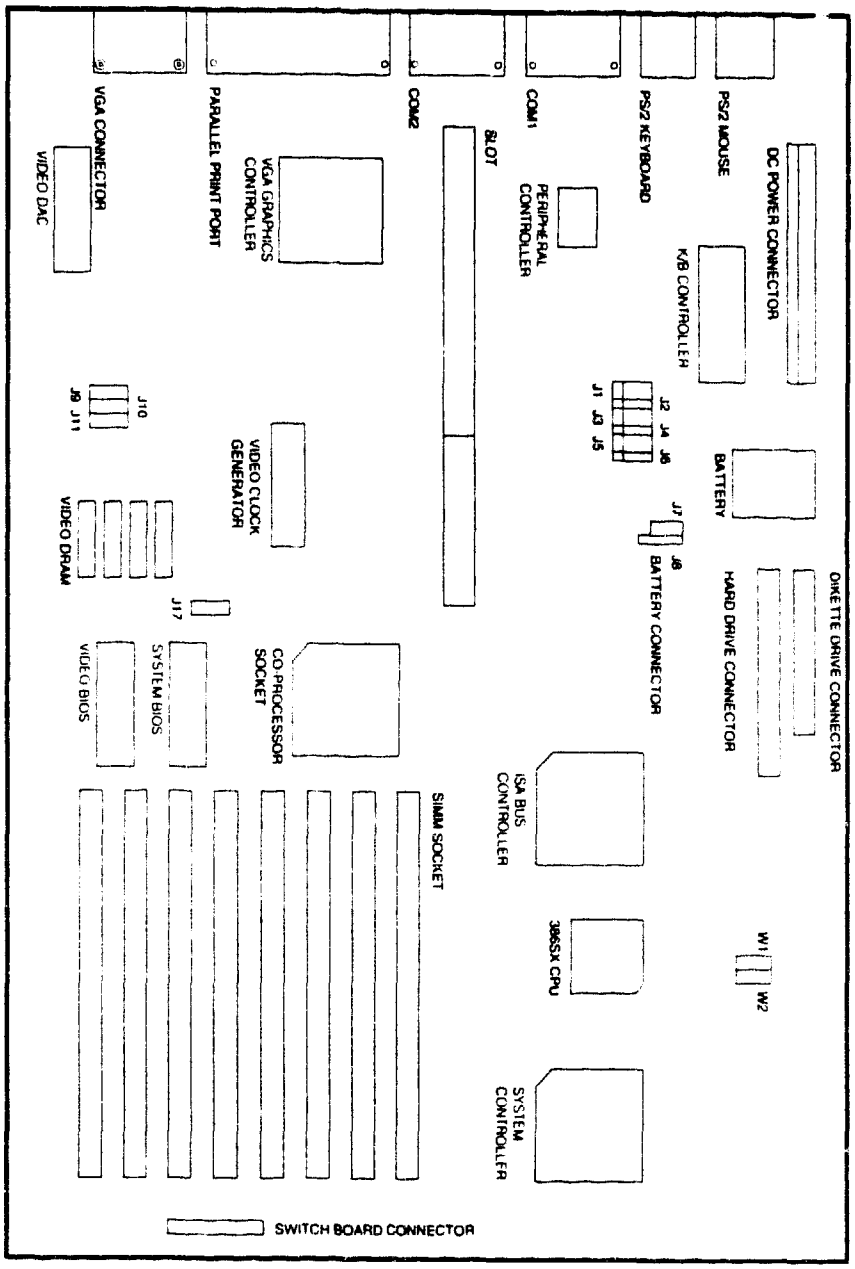


Figure 3-1. System Board Layout

In addition, the system boards support:

- **One 16-bit ISA expansion slot**
- **One 15-pin Video port**
- **Two 9-pin serial ports**
- **One 25-pin parallel**
- **One 34-pin floppy disk controller header**
- **One 48-pin IDE header**
- **6-pin (mini-DIN) keyboard and mouse connectors**
- **Three system status LED indicators**
- **One 115 watt power supply**

The remainder of this chapter provides a brief description of the hardware components and major features for each system board.

3.1 DECpc 320sxLP/325sxLP System Board Features

This section provides detailed descriptions relating to the hardware components and major features of each DECpc 320sxLP/325sxLP system board (see Figure 3-2).

3.1.1 80386SX Microprocessor

The 80386SX microprocessor is a 32-bit CPU with a 16-bit external data bus and a 24-bit external address bus. The 80386SX microprocessor runs at a clock speed of 20/25 MHz, which results in a system speed of 50/40 as per clock cycle.

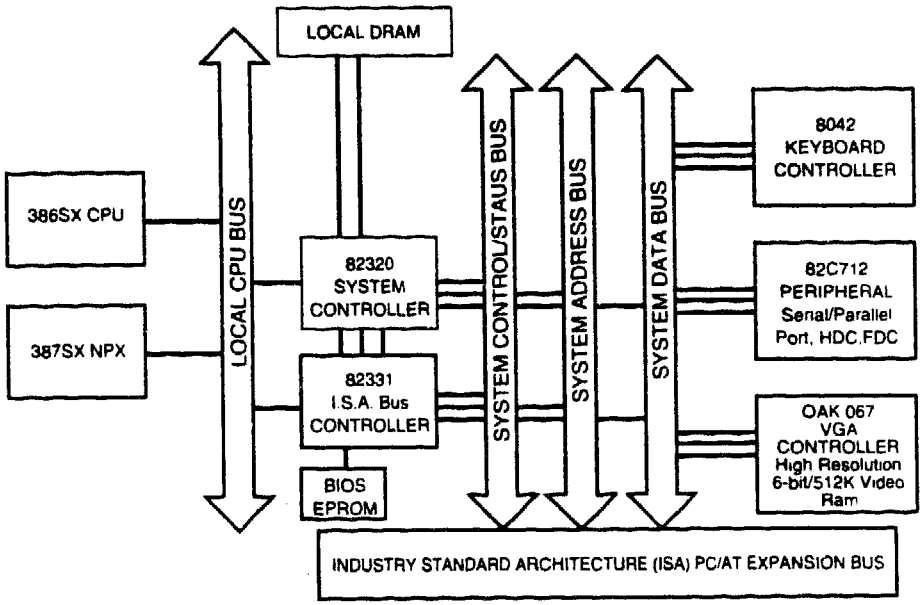


Figure 3-2. DECpc 320sxLP/325sxLP Block Diagram

3.1.2 82C386SX ISA Bus Chip Set

The 82C386SX chip set consists of an 82C331 ISA bus controller and an 82C320 system controller/data buffer. Together, these components are responsible for controlling all addressing and data transmissions to and from the ISA bus.

3.1.3 82C712 Universal Peripheral Controller

The 82C712 provides one printer port, two 16450 UARTs, IDE AT hard disk interface, and floppy disk controller .

3.1.4 OTI-067 Video Graphic Controller

The OTI-067 is a single chip Video Graphics Controller compatible with the IBM VGA standard. It provides a high resolution of 800x600 with 256 colors and 1024x768 with 16 colors.

3.1.5 DRAM

The system supports up to 32MB of system DRAM through the use of eight SIMM sockets located on the main logic board. The SIMM sockets are divided into four banks (designated as bank 0 through bank 3). System memory can be implemented using either 1MB or 4MB SIMMs within each bank. The minimum system memory configuration is 2MB.

3.1.6 ROM

The system board ROM is one 64 KB EPROM. The EPROM contains the system BIOS, a Power-On Self Test (POST), and the Setup Utility. The BIOS initializes the DRAM and loads the operating system. The system BIOS also contains a shadow option. This option, when enabled, increases system performance by placing ROM instructions into high-speed DRAM. POST tests system hardware and the Setup utility allows you to set system configuration parameters.

3.1.7 I/O Ports

There are three I/O ports: one 25-pin parallel printer port and two 9-pin serial (RS232) communication ports.

3.1.8 System Status LED Indicators

The DECpc 320sxLP/325sxLP system provides three system status LED indicators. When on, they indicate power On/Off, Fixed disk activity, and CPU speed.

3.1.9 System Board Configuration Setting

Jumpers can be configured differently to accommodate different system requirements. Table 3-1 defines the jumper settings for the DECpc 320sxLP/325sxLP.

Table 3-1. Configuration Setting

Feature	Description	Jumper Setting
J1: COM2 address selection	Disable	2 & 3 short, 5 & 6 short
	238H	2 & 3 short, 4 & 5 short
	2F8H (default)	1 & 2 short, 4 & 5 short
J2: On board FDC	Enable (default)	1 & 2 short
	Disable	2 & 3 short
J3: COM1 address selection	Disable	2 & 3 short, 5 & 6 short
	338H	2 & 3 short, 4 & 5 short
	3F8H (default)	1 & 2 short, 4 & 5 short
J4: On board IDE	Enable (default)	1 & 2 short
	Disable	2 & 3 short
J5: LPT1 address selection	Disable	2 & 3 short, 5 & 6 short
	378H	1 & 2 short, 5 & 6 short
	3BCH	2 & 3 short, 4 & 5 short
	278H (default)	1 & 2 short, 4 & 5 short
J6: Display adapter Setting	VGA/EGA/MONO (default)	1 & 2 short
	CGA	2 & 3 short
J7: CMOS discharge	Normal (default)	1 & 2 short
	CMOS Discharge	2 & 3 short
J9: Monitor type	Color (default)	1 & 2 short
	Mono	2 & 3 short
J10: Interlaced/ Non-interlaced	Non-interlaced	1 & 2 short
	Interlaced (default)	2 & 3 short
J11: On board VGA	Enable (default)	1 & 2 short
	Disable	2 & 3 short
J17: 387sx coprocessor clock mode select	Sync (default)	1 & 2 short
	Asyn	2 & 3 short
W1: Manufacturing Setting # 1	Co-processor Ready Selection	Reserved
W2: Manufacturing Setting # 2	Pipeline/Non-pipeline	Reserved

4

CENTRAL PROCESSING CORE

The following text describes the 80386SX microprocessor's basic architecture and the two modes of operation. This section concludes with brief descriptions relating to the signals generated by the microprocessor.

The 80386SX microprocessor is a 32-bit CPU with a 16-bit external data bus and a 24-bit external address bus.

The 80386SX microprocessor consists of a Central Processing Unit, a Memory Management Unit, and a Bus Interface (See Figure 4-1).

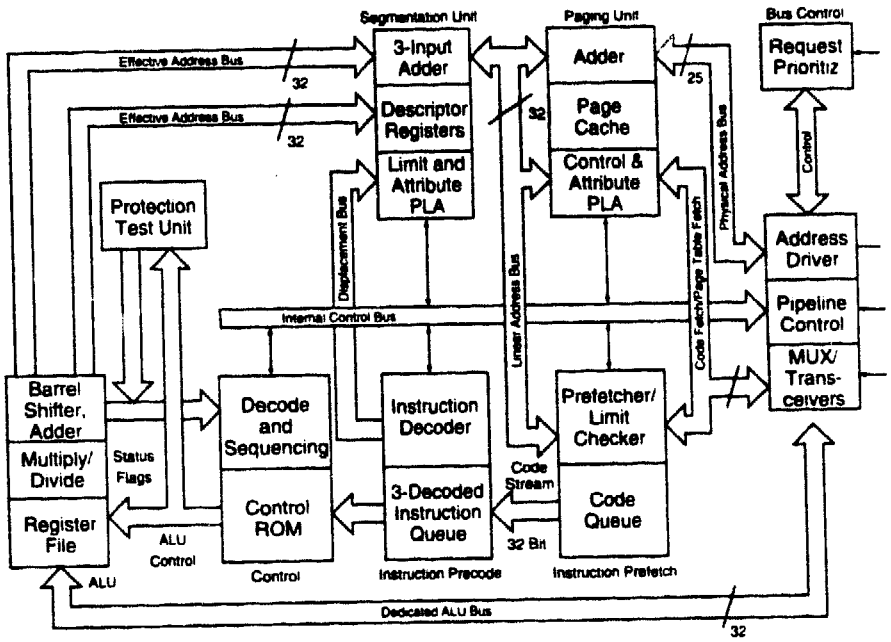


Figure 4-1 80386SX Pipeline 32-bit Microarchitecture

4.1 Central Processing Unit

The Central Processing Unit (CPU) consists of the execution unit and instruction unit. The execution unit contains the eight 32-bit general purpose registers used for both address calculation and data operations. The execution unit also contains a 64-bit barrel shifter that speeds up shift, rotate, multiply, and divide operations. The instruction unit decodes the instruction opcodes and stores them in the decoded instruction queue for immediate use by the execution unit.

4.2 Memory Management Unit

The Memory Management Unit (MMU) consists of a segmentation unit and a paging unit. Segmentation manages the logical address space by providing an extra addressing component that allows the relocation and sharing of code and data. The paging unit operates beneath, and is transparent to, the segmentation process to allow physical address space management.

4.3 Modes of Operation

The 80386SX microprocessor has two modes of operation: real address mode (real mode) and protected virtual address mode (protected mode). In real mode, the 80386SX microprocessor operates as a fast 8086_{M} and sets up the CPU for protected mode operation. Protected mode provides access to the sophisticated memory management paging and privilege capabilities of the microprocessor. In protected mode, software can execute a task switch and enter into a virtual 8086 mode. In this virtual mode 8086 semantics are used and the application program or operating system executes as if running on an 8086 microprocessor.

4.4 Signal Definitions

Table 4-1 lists a signal name for the 80386SX microprocessor.

Table 4-1. 80386SX Signal Name

Pin Number	80386SX Signal Name
1	Do
2	Vss
3	HLDA
4	HOLD
5	Vss
6	-NA
7	-READY
8	Vcc
9	Vcc
10	Vcc
11	Vss
12	Vss
13	Vss
14	Vss
15	CLK2
16	-ADS
17	-BLE
18	A1
19	-BHE
20	NC
21	Vcc
22	Vss
23	M/-IO
24	D/-C
25	W/-R

Table 4-1. (Cont.) 80386SX Signal Name

Pin Number	80386SX Signal Name
26	-LOCK
27	NC
28	-FLT
29	NC
30	NC
31	NC
32	Vcc
33	RESET
34	-BUSY
35	Vss
36	-ERROR
37	PEREQ
38	NMI
39	Vcc
40	INTR
41	Vss
42	Vcc
43	NC
44	NC
45	NC
46	NC
47	NC
48	Vcc
49	Vss
50	Vss

Table 4-1. (Cont.) 80386SX Signal Name

Pin Number	80386SX Signal Name
51	A2
52	A3
53	A4
54	A5
55	A6
56	A7
57	Vcc
58	A8
59	A9
60	A10
61	A11
62	A12
63	Vss
64	A13
65	A14
66	A15
67	Vss
68	Vss
69	Vcc
70	A16
71	Vcc
72	A17
73	A18
74	A19
75	A20

Table 4-1. (Cont.) 80386SX Signal Name

Pin Number	80386SX Signal Name
76	A21
77	Vss
78	Vss
79	A22
80	A23
81	D15
82	D14
83	D13
84	Vcc
85	Vss
86	D12
87	D11
88	D10
89	D9
90	D8
91	Vcc
92	D7
93	D6
94	D5
95	D4
96	D3
97	Vcc
98	Vss
99	D2
100	D1

4.5 Signal Description

A23-A1 (Outputs)
Address Bus: Outputs physical memory or port I/O addresses.

-ADS (Active Low; Output)
Address Status: Indicates that a valid bus cycle definition and address (W/-R, D/-C, M/-IO, -BHE, -BLE, and A23-A1) are being driven at the microprocessor pins.

-BHE, -BLE (Active Low; Outputs)
Byte Enables: Indicate which data bytes of the data bus take part in a bus cycle.

-BUSY (Active Low; Input)
Busy: Signals a busy condition from a processor extension.

CLK2 (Input)
CLK2: Provides the fundamental timing for the microprocessor.

D15-D0 (Inputs/Outputs)
Data Bus: Inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles.

D/-C (Output)
Data/Control: A bus cycle definition pin that distinguishes data cycles, either memory or I/O, from control cycles which are: interrupt acknowledge, halt, and code fetch.

-ERROR (Active Low: Input)
Error: Signals an error condition from a processor extension.

-FLT (Active Low: Input)
Float: An input which forces all bi-directional and output signals, including HLDA, to the three-state condition.

HLDA (Active High; Output)
Bus Hold Acknowledge: Output indicates that the microprocessor has surrendered control of its logical bus to another bus master.

HOLD (Active High; Input)
Bus Hold Request: Input allows another bus master to request control of the local bus.

INTR (Active High; Input)
Interrupt Request: A maskable input that signals the microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

-LOCK (Active Low; Output)
Bus Lock: A bus cycle definition pin that indicates that other system bus masters are not to gain control of the system bus while it is active.

M/-IO (Output)
Memory/IO: A bus cycle definition pin that distinguishes memory cycles from input/output cycles.

-NA (Active Low; Input)
Next Address: Used to request address pipelining.

NC
No Connect: Should always be left unconnected.

NMI (Active High; Input)
Non-Maskable Interrupt Request: A non-maskable input that signals the microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

PEREQ (Active High; Input)
Processor Extension Request: Indicates that the processor has data to be transferred by the microprocessor.

-READY (Active Low; Input)
Bus Ready: Terminates the bus cycle.

RESET (Active High; Input)
Reset: Suspends any operation in progress and places the microprocessor in a known reset state.

Vcc (Active High; Input)
System Power: Provides the +5 V nominal DC supply input.

Vss (Input)
System Ground: Provides the 0 V connection from which all inputs and outputs are measured.

W/-R (Output)
Write/Read: A bus cycle definition pin that distinguishes write cycles from read cycles.

5

82C386SX ISA CHIP SET

The 82C386SX ISA Chip Set contains an 82C320 system controller/data buffer and an 82331 ISA bus controller, (see Figure 5-1). This chapter describes each of these in detail.

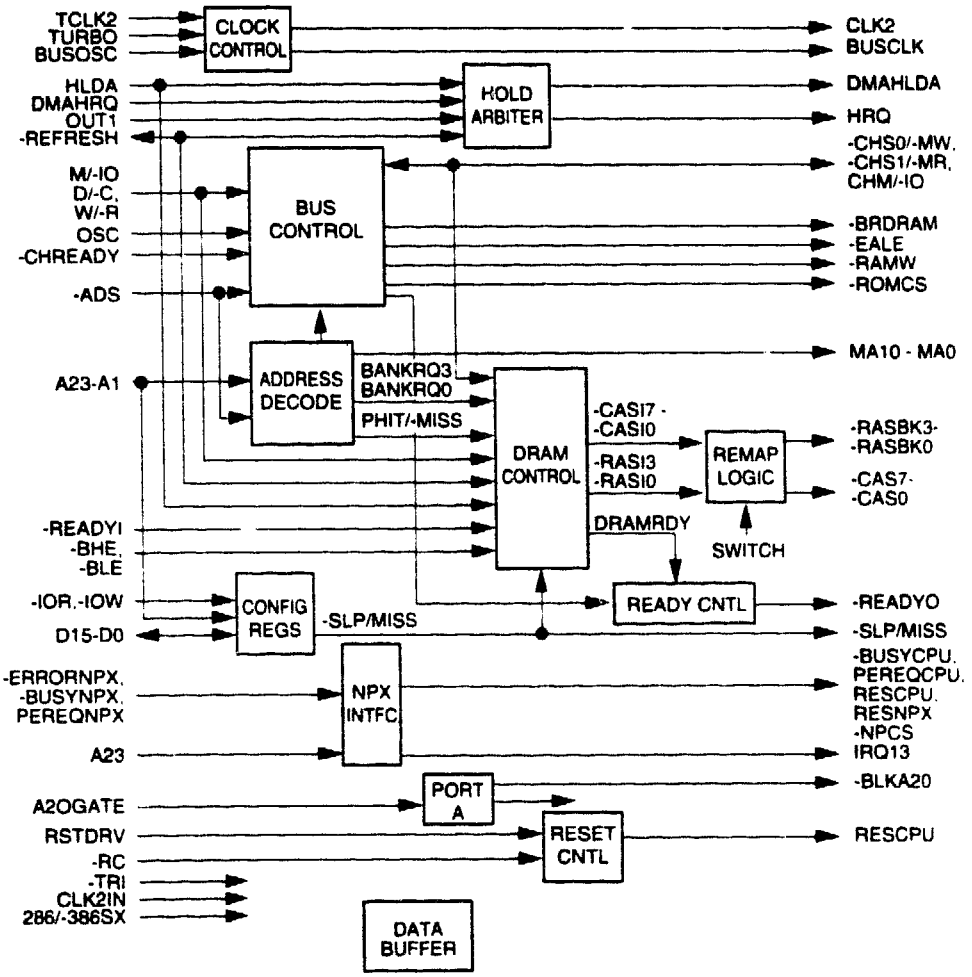


Figure 5-1. 82C386SX Functional Block Diagram

5.1 82C320 System Controller/Data Buffer

The 82C320 system controller provides built-in paged mode operation, two- or four-way interleaving, programmable DRAM timing, system board and ISA slot refresh, full EEMS support, shadowing, and provides the bus clock and signalling interface to the 82C331 ISA bus controller (see Figure 5-2). The I/O address of 82C320 Index Register and Data Port Register is ECh and EDh respectively. Each of the 82C320 Indexed Configuration Registers described in the following sections is accessed first by writing its address to the Index Register at I/O address ECh, then by accessing the data port at I/O address EDh.

The system controller/data buffer consists of the following:

- **A CPU interface**
- **An ISA bus/system controller communication channel**
- **A DRAM support subsystem**
- **I/O control registers**
- **Halt/shutdown detection**
- **Data Buffer**

The following sections describe each of these functions in detail.

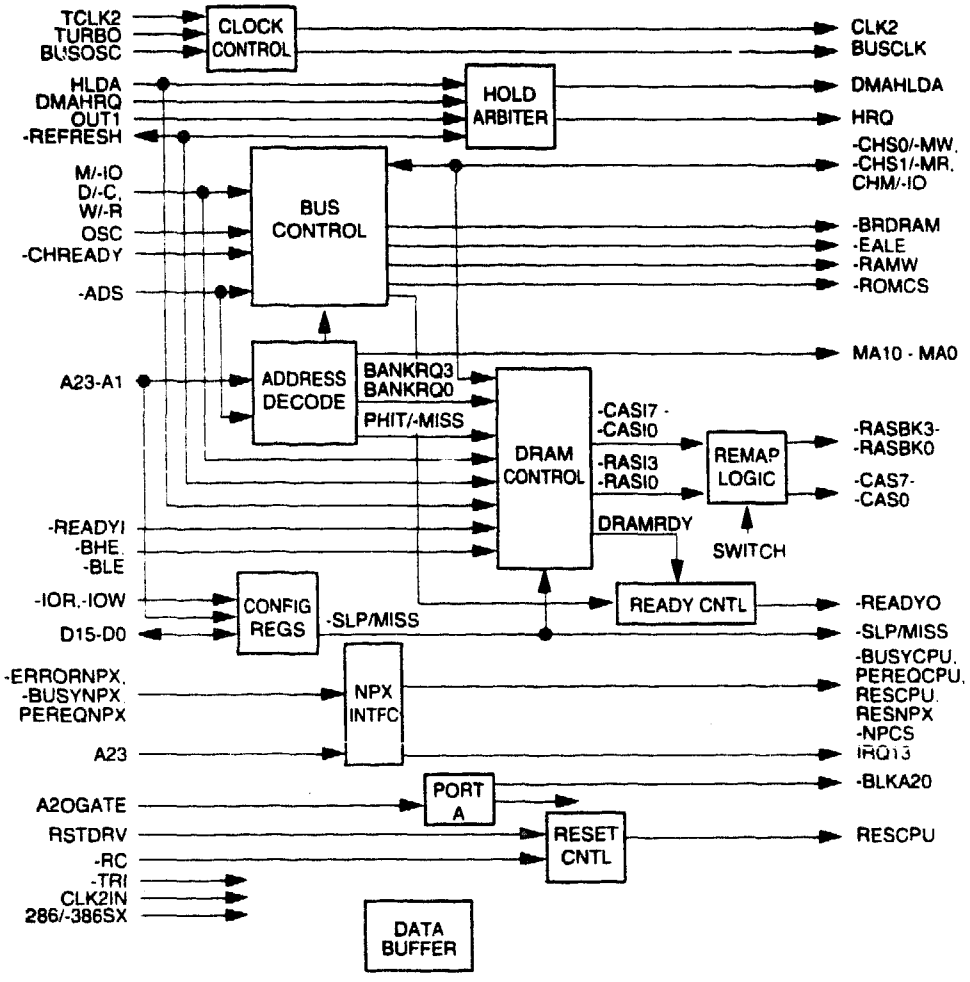


Figure 5-2. 82C320 System Controller Functional Block Diagram

5.1.1 CPU Interface

The VL82C320 handles the top level control interface between the synchronous local and memory data bus and the asynchronous slot data bus. It intercepts the CPU's bus status and address signals, and decodes the bus access. It then decides whether to handle the bus request itself, or send it off to the VL82C331 ISA Bus Controller.

5.1.2 ISA Bus/System Controller Communication Channel

The asynchronous interface to the bus controller is handled by the group of signals listed in Table 5-1. These signals define the type of bus cycle to be run.

Table 5-1. Bus/System Controller Bus Cycle Types

CHM/-IO	-CHS1	-CHS0	Bus Cycle
0	0	0	-INTA
0	0	1	-IOR
0	1	0	-IOW
0	1	1	Reserved
1	0	0	-REFRESH
1	0	1	-MEMR
1	1	0	-MEMW
1	1	1	Reserved

5.1.3 DRAM Support Subsystem

The VL82C320 supports up to 32 Mbyte of DRAM on the system board in four 16-bit banks. Each byte contains its own parity bit for a total of 18 bits per bank. A single bank can consist of 1M or 4M DRAMs.
Both types of DRAM can be mixed between the four memory banks; however, they cannot be mixed within the same memory bank.
The VL82C320 supports four banks by providing four -RASBK signals and eight -CAS signals. This allows direct drive with no external buffering.
Several configuration registers internal to the VL82C320 are used to control the memory map, interleaving, DRAM timing and page mode. These features are discussed in the following sections. Since interleaving requires pairs of banks, various controls described next act on memory in bank pairs. The short hand notation bank A is used when describing something that affects DRAM banks 0 and 1 as a set. Similarly, bank B is used to describe DRAM banks 2 and 3 as a set.

5.1.3.1 Memory Mapping

The memory controller supports the twelve DRAM memory maps listed in Table 5-2. The memory column lists the total amount of DRAM available in each memory map. The RAMMAP (4:0) column indicates the hex value written in bits four through zero from the RAMMAP indexed configuration register (refer to Table 5-3). Each combination listed is addressable in each of the four 16-bit memory banks. Note that memory banks zero through three are referred to as logical banks when internally addressed by the VL82C320. The actual system board memory banks, when accessed internally, might differ depending on the value stored in the indexed configuration register RAMMOV (refer to Table 5-4). In case of a partial or total DRAM bank failure, the remaining functional DRAMs can be switched into an alternate, valid logical memory map by reprogramming RAMMOV and RAMMAP together. Table 5-5 shows the sixteen logical to physical mappings that are available. In the top row of this chart, the numbers 3, 2, 1 and 0 directly under "DRAM BANK MAPPING" refer to the four physical DRAM memory banks. In the sixteen rows beneath, the code that must be programmed into the RAMMOV register bits 4-0 is shown on the left side of the chart. On the right side is shown the logical bank that is mapped to the corresponding physical bank shown in the top row. Figure 5-3 shows an example of upgrading from one 2MB DRAM bank to two 2MB banks. When RAMMOV =00000, the default condition, the logical banks are directed to the same physical bank numbers.

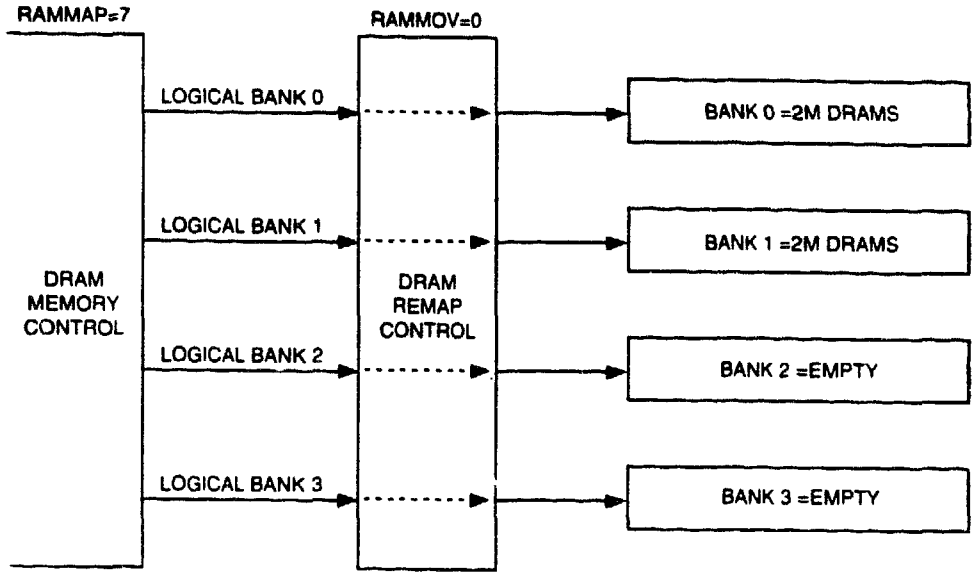


Figure 5-3. DRAM Remap

Table 5-2. DRAM Mapping

Bank 0	Bank 1	Bank 2	Bank 3	Memory MB	RAMMAP (4:0)
1MBx2				2	4
1MBx2	1MBx2			4	7
1MBx2	1MBx2	1MBx2		6	A
1MBx2	1MBx2	1MBx2	1M Bx2	8	B
4MBx2				8	C
1MBx2	4MBx2			10	F
1MBx2	1MBx2	4MBx2		12	10
4MBx2	4MBx2			16	11
4MBx2	4MBx2	1MBx2		18	14
1MBx2	1MBx2	4MBx2	4MBx2	20	15
4MBx2	4MBx2	4MBx2		24	16
4MBx2	4MBx2	4MBx2	4MBx2	32	17

Table 5-3. RAMMAP(03h R/W) Indexed Configuration Register (Default = E0h)

Bit	Function
7 : 5	Always one
4 : 0	DRAM memory map code

Table 5-4. RAMMOV(04h R/W) Indexed Configuration Register (Default = F0h)

Bit	Function
7 : 5	Always one
4 : 0	RAMMOV code

Table 5-5. REMAP Configuration Register Code

RAMMOV Code				DRAM Bank Mapping				
D3	D2	D1	D0	3	2	1	0	Physical DRAM Banks
0	0	0	0	3	2	1	0	
0	0	0	1	3	0	2	1	
0	0	1	0	3	1	2	0	
0	0	1	1	3	0	1	2	
0	1	0	0	3	1	0	2	
0	1	0	1	2	3	0	1	
0	1	1	0	2	1	0	3	
0	1	1	1	2	0	1	3	Logical DRAM Banks
1	0	0	0	1	3	2	0	
1	0	0	1	1	2	3	0	
1	0	1	0	1	0	2	3	
1	0	1	1	0	3	2	1	
1	1	0	0	0	2	3	1	
1	1	0	1	0	2	1	3	
1	1	1	0	0	1	3	2	
1	1	1	1	0	1	2	3	

5.1.3.2 Paged Mode and Interleaving

DRAM operates in paged mode or interleaving. Both options are selected by programming the RAMMAP and RAMSET indexed configuration registers (refer to Tables 5-3 and 5-6, respectively). Paged mode is enabled or disabled for each pair of memory banks independently. Interleaving requires pairs of memory banks. Two-way interleaving is automatically enabled whenever both banks of a pair are populated with like DRAM types. If all four banks are populated with like DRAMs, four-way interleaving automatically occurs when both bank pairs are programmed to interleave on the same bit. If not, two-way interleaving occurs. If the four banks are not populated with like DRAMS, two-way interleaving occurs on pairs that are of the same type. In a machine with three banks populated, the first two banks two-way interleave if they are of the same type. The third does not interleave. Table 5-7 shows the

Table 5-6. RAMSET(05H R/W) Indexed configuration I
(Default = 3Ch)

Bit	Function
7 : 6	DRAM drive current on MA0-MA10 and -RAMW 00 = 150 pF drive (Default) 01 = 300 pF drive 10 = 450 pF drive 11 = 600 pF drive
5	ESTART 0 = Early Start Enable 1 = Early Start Disable (Default)
4	Always one
3	Bank A Page mode 0 = disabled 1 = enabled (Default)
2	Bank B Page mode 0 = disabled 1 = enabled (Default)
1	Bank A interleave 0 = Interleave on bit 1 for all DRAMs (Default) 1 = Interleave on bit 10 for all DRAMs
0	Bank B interleave 0 = Interleave on bit 1 for all DRAMs (Default) 1 = Interleave on bit 10 for all DRAMs

Table 5-7. Automatic Interleave VS. Memory Map

Bank 0	Bank 1	Bank A Address Mode	Bank 2	Bank 3	Bank B Address Mode
Yes	No	Linear	No	No	N/A
Yes	Yes	2-Way Interleave	No	No	N/A
Yes	Yes	2-Way Interleave	Yes	No	Linear
Yes	Yes	2-Way Interleave 0 and 1*	Yes	Yes	2-Way Interleave 2 and 3*

* This is for the case where Banks A and B contain different types of DRAMs. For memory maps 0Bh, and 17h all four banks contain the same DRAM type and four-way interleaving is used if both bank pairs interleave on the same bit.

5.1.3.3 DRAM Timing Parameters

Four configurations registers are used to program the DRAM timing parameters. RASTMA allows programming of RAS ADDSEL delay, tRCD, tRP, and tRAS parameters for banks 0 and 1. RASTMB performs the same functions for banks 2 and 3. CASTMA allows programming of tCST, tCP, tCASR, and tCASW for banks 0 and 1. CASTMB performs the same functions for banks 2 and 3. Refer to Table 5-8 and 5-9 for specific bit allocations. Figures 5-4 and 5-5 show the relationship between these programmable timing signals for page and non-page-mode operation.

Table 5-8. RASTMA(07h R/W) and RASTMB(09h R/W) Configuration Registers (Default = FFh)

Bit	Function
7	RAS address select 0 = 1/2 CLK2 1 = 1 CLK2 (Default)
6	tRCD 0 = 1 CLK2 1 = 2 CLK2s (Default)
5	Always one
4 : 3	tRP 00 = 2 CLK2s 01 = 3 CLK2s 10 = 4 CLK2s 11 = 5 CLK2s (Default)
2 : 0	tRAS 010 = 2 CLK2s 011 = 3 CLK2s 100 = 4 CLK2s 101 = 5 CLK2s 110 = 6 CLK2s 111 = 7 CLK2s (Default)

Table 5-9. CASTMA(08h R/W) and CASTMB (0Ah R/W) Configuration Registers (Default = B7h)

Bit	Function
7 : 6	tCASW 00 = 1 CLK2 01 = 2 CLK2s 10 = 3 CLK2s (Default) 11 = 4 CLK2s
5	tCST 0 = 3 CLK2s 1 = 4 CLK2s (Default)
4 : 3	tCP 00 = 1 CLK2 01 = 2 CLK2s 10 = 3 CLK2s (Default)
2	Always one
1 : 0	tCASR 01 = 2 CLK2s 10 = 3 CLK2s 11 = 4 CLK2s (Default) 00 = 5 CLK2s

5.1.3.4 DRAM Refresh

The VL82C320 performs on-board DRAM refresh and controls both on- and off-board refresh timing in all modes. Refresh may be performed in a coupled mode or decoupled mode. In coupled mode, refresh timing for both system board and slot bus refreshes is performed in a synchronous manner. In decoupled mode, the VL82C320 has complete control over the timing of on-board DRAM refresh and off-board refresh but the timing of each is independent. Configuration register REFCTL is used to program the specific modes (refer to Table 5-10). When set to coupled refresh mode (D7 = 0), the VL82C320 refresh circuitry controls system board refresh and slot bus refresh in a synchronous manner. In that mode, the division specified by bits 2-0 applies to on- and off-board

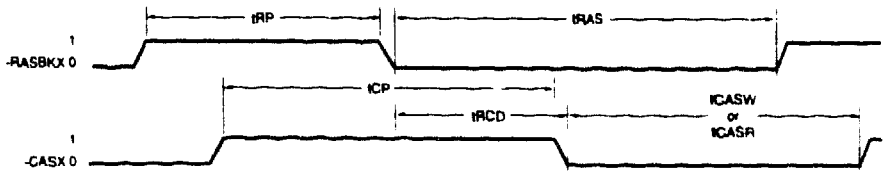


FIGURE 5-4. -RASBK/-CAS TIMING MODEL

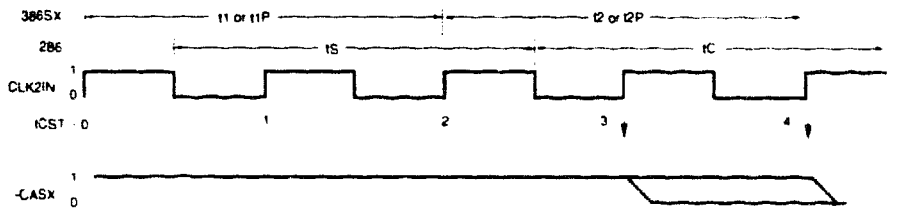


FIGURE5-5. -CAS START TIME(tCST) TIMING MODEL

Note : tCST applies to write cycles only and equals 3 or 4. During read cycles, CAS start time defaults to zero CLK2's for pipelined or two CLK2's for non-pipelined SX or 286 mode. Iff ESTART bit in RAMSET register is programmed inactive (1), then add one to start times just mentioned for reads only. This is the earliest time -CAS can start for read cycles. Actual -CAS start time may be delayed due to -CAS pre-charge or -RASBK to -CAS delay time not yet met.

refresh and bits 6-4 have no effect. Only in decoupled mode (D7 = **1**), do the three bits 6-4 of the VL82C320's REFCTL register apply. In decoupled mode, the VL82C320 refreshes the on-board DRAM independent of the Bus Controller's refresh of the slot bus resident memory. It uses the division rate specified in those bits while the slot bus refresh is performed at the rate specified by the code in bits 2-0.

Table 5-10. REFCTL (05h R/W) Configuration Register (Default = 00h)

Bit	Function
7	Refresh Control 0 = Coupled Refresh (Default) 1 = Decoupled Refresh
6 : 4	Slow refresh (system board) 000 = ÷ 1 (Default) 001 = ÷ 2 010 = ÷ 4 011 = ÷ 8 100 = ÷ 16
3	10/16 I/O 0 = full 16-bit decode is performed (Default) 1 = 10-bit decode is performed
2 : 0	Slow refresh (slots) 000 = ÷ 1 (Default) 001 = ÷ 2 010 = ÷ 4 011 = ÷ 8 100 = ÷ 16

5.1.4 I/O Control Registers

Table 5-11 lists the I/O port addresses for the system controller registers.

Table 5-11. Dedicated I/O Control Registers

Port Address	Function
E8h	EMS index Register
E9h	EMS Active Set
EAh	EMS Data Port Low Byte
EBh	EMS Data Port High Byte
ECh	Configuration Index Register
EDh	Configuration Data Port
EEh	Fast A20
EFh	Fast Reset
F0h	Coprocessor Busy Clear
F1h	Coprocessor Reset
F4h	Slow CPU
F5h	Fast CPU
F8h	Coprocessor
F9h	Configuration Disable
FAh	Coprocessor
FBh	Configuration Enable
FCh	Coprocessor
FEh	Coprocessor

5.1.5 Halt/Shutdown Detection

The system controller detects and acts on 80386SX microprocessor halt and shutdown conditions. The signal levels listed in Table 5-12 determine the existence of halt and shutdown conditions.

Table 5-12. 80386SX Halt/Shutdown Detection

Mode	Signal Levels			
	M/-I0	D/-C	W/-R	A1
Halt	1	0	1	1
Shutdown	1	0	1	0

5.1.6 Data Buffer

The VL82C320 data buffer functions separates the data bus into three buses, D bus, SD bus and the XD bus. The D bus is the CPU's local data bus. The VL82C320 and numeric coprocessor are connected to the D bus. BIOS ROMs are connected to the D Bus (16-bit) or the XD bus (8-bit). The SD bus is the 16-bit slot bus and the XD bus is an 8-bit bus for on-board peripherals such as the VL82C320 registers and the ISA Bus Controller. These buses can be controlled by either the CPU, a DMA controller or a bus master.

5.1.7 Signal Definitions

Table 5-13 lists a signal name for the 82C320 .

Table 5-13. 82C320 Signal Name

Pin Number	82C320 Signal Name
1	VDD
2	CLK2IN
3	-READYI
4	HLDA
5	CLK2
6	-SLP/MISS
7	-READYO
8	HRQ
9	RESCPU
10	-BUSYCPU
11	PEREQCPU
12	D15
13	D14
14	D13
15	D12
16	D11
17	D10
18	D9
19	VSS
20	D8
21	PAR1
22	D7
23	D6
24	D5
25	D4
26	D3
27	D2
28	D1
29	D0
30	PAR0

Table 5-13. (Cont.) 82C320 Signal Name

Pin Number	82C320 Signal Name
31	VSS
32	VDD
33	MA10
34	MA9
35	MA8
36	VSS
37	MA7
38	MA6
39	MA5
40	MA4
41	VDD
42	VSS
43	MA3
44	MA2
45	MA1
46	VSS
47	MA0
48	-RAMW
49	-CAS7
50	-CAS6
51	-CAS5
52	-CAS4
53	-CAS3
54	-CAS2
55	VSS
56	-CAS1
57	-CAS0
58	VDD
59	-RASKB3
60	-RASKB2

Table 5-13. (Cont.) 82C320 Signal Name

Pin Number	82C320 Signal Name
61	-RASKB1
62	-RASKB0
63	-ROMCS
64	-REFRESH
65	RESNPX
66	IRQ13
67	-NPCS
68	PEREQNPX
69	-ERRORNPX
70	-BUSYNPX
71	TCLK2
72	OSC
73	BUSOSC
74	VDD
75	A20GATE
76	TURBO
77	-RC
78	286/-3386SX
79	-TRI
80	-CHREADY
81	VSS
82	VSS
83	DAMHRQ
84	OUT1
85	-IOR
86	-IOW
87	RSTDRV
88	SDLH/-HL
89	-SDSWAP
90	-XDREAD

Table 5-13. (Cont.) 82C320 Signal Name

Pin Number	82C320 Signal Name
91	-LATLO
92	-EALE
93	-CHS0/-MM
94	-CHS1/-MR
95	CHM/-IO
96	-BLKA20
97	BUSCLK
98	DMAHLDA
99	-BRDRAM
100	-PARERRC
101	XD7
102	XD6
103	XD5
104	XD4
105	XD3
106	XD2
107	XD1
108	VSS
109	XD0
110	VDD
111	SD15
112	SD14
113	SD13
114	SD12
115	VSS
116	SD11
117	SD10
118	SD9
119	SD8
120	VSS

Table 5-13. (Cont.) 82C320 Signal Name

Pin Number	82C320 Signal Name
121	VDD
122	SD7
123	SD6
124	SD5
125	SD4
126	VSS
127	SD3
128	SD2
129	SD1
130	SD0
131	VSS
132	A23
133	A22
134	A21
135	A20
136	A19
137	A18
138	A17
139	A16
140	A15
141	A14
142	A13
143	A12
144	A11
145	A10
146	A9
147	A8
148	A7
149	A6
150	A5

Table 5-13. (Cont.) 82C320 Signal Name

Pin Number	82C320 Signal Name
151	A4
152	A3
153	A2
154	A1
155	-BHE
156	-BLE
157	W/-R
158	D/-C
159	M/-IO
160	-ADS

5.1.8 Signal Description

5.1.8.1 CPU Interface Signals

A23-A1 (I-TTL)
Address bits 23 through 1 - When the CPU is bus master and HLDA is active, these signals are driven by the Bus Controller.

-BHE (I-TTL)
Byte High Enable, active low - This signal is driven by the CPU or the Bus Controller. It is used to select the upper byte of a 16-bit wide memory location.

-BLE (I-TTL)
This signal is used to select the lower byte of a 16-bit wide memory location.

W/-R (I-TPU)
This signal is decoded with the remaining control signals to indicate the type of bus cycle requested.

D/-C (I-TPU)
This signal is decoded with the remaining control signals to indicate the type of bus cycle requested.

M/-IO (I-TPU)
Memory active low I/O enable - M/-IO is decoded with the remaining control signals to indicate the type of bus cycle requested.

-ADS (I-TPU)
Address Strobe, active low - This signal is driven by the 386SX as an indicator that the address and control signals are valid. It is used internally to indicate that the address and command are valid and determine the beginning of a bus cycle.

CLK21N (I-CMOS)
This is the main clock input to the VL82C320 and it should be connected to the CLK2 signal that is output by the VL82C320. This signal is used internally to clock the VL82C320 logic.

TCLK2 (I-CMOS)
This input is connected to a crystal oscillator whose frequency is equal to two times the system frequency. The CMOS level is used to generate CLK2 output and optionally, bus clock.

CLK2 (O)
This output signal is CMOS level and generated from TCLK2 signal. It connects the CPU and other on-board logic for synchronization.

-SLP/MISS (IT-OD)
As a "power on reset" default, this signal is an output that is equal to -SLEEP[7]. -SLEEP[1]. When configuration register CTRL[0] = 1, this pin becomes a MISS input for use with a future VLSI product.

-READYO (O)
Ready Out, active low - This signal indicates that the current cycle is complete. It is generated from the internal DRAM controller or the synchronized version of -CHREADY for slot bus accesses. The culmination of these ORed READY signals is sent to the CPU and is also connected to the VL82C320's -READYI input. This signal may be combined externally with other READY sources.

-READYI (I-TTL)
Ready Input, active low - This signal indicates the current bus cycle is complete.

HLDA (I-TTL)
Hold Acknowledge, active high - This signal is issued in response to the HRQ driven by the VL82C320. When HLDA is active, the memory control is generated from -CHS1/-MR and -CHS0/-MW.

HRQ (O)
Hold Request, active high - This signal indicates that a bus master, such as a DMA or AT channel master, is requesting control of the bus. HRQ is a result of the DMAHRQ input or a coupled refresh cycle. It is synchronized to CLK2 and internal clock.

RESCPU (O)
Reset CPU, active high - This signal is issued in response to the control bit for software reset located in the Port A, read from IO port EFh, RC and RSTDRV inputs and in response to VL82C320's detection of a shutdown command. In all cases it is synchronized to CLK2 and internal clock.

-BUSYCPU (O)
Busy CPU, active low - The state of -BUSYNPX is always passed through to -BUSYCPU indicating that the NPX is processing a command. On occurrence of an -ERRORNPX signal, it is latched and held active until occurrence of a write to ports F0h, F1h, or RSTDRV.

PEREQCPU (O)
Processor Extension Request CPU, active high - An output signal generated in response to a PEREQNPX which is issued by the coprocessor to the VL82C320. PEREQCPU is asserted on occurrence of -ERRORNPX after -BUSYNPX has gone inactive. A write to F0h returns control of the PEREQCPU signal to directly follow the PEREQNPX input.

5.1.8.2 On-Board Memory System Interface Signals

-RAMW (O-TTL)
RAM Write, active low - This signal is active during memory write cycles and high at all other times.

MA10-MA0 (O-TTL)
Memory Addresses 10 through 0 - These address bits are the row and column addresses sent to on-board memory. They are buffered and multiplexed versions of the CPU bus addresses.

-RASBK3 - -RASBK0 (O-TTL)
Row Address Strobe, active low - These signals are sent to their respective RAM banks to strobe in the row address buring on-board memory bus cycles. The active period for this signal is fully programmable.

-CAS7 - -CAS0 (O)
Column Address, Strobe, active low - These signals are sent to their respective RAM banks to strobe in the column address during on-board memory bus cycles. There is a -CAS signal for upper and lower bytes of each of the four 16-bit DRAM memory banks. The active period for this signal is completely programmable.

-REFRESH (IC-OD)
Refresh signal, active low - This output is used by the VL82C320 to initiate an off-board DRAM refresh operation in coupled refresh mode. In decoupled mode, the Bus Controller drives refresh active to indicate to the VL82C320 that it has decoded a refresh request command and is initiating an off-board refresh cycle.

-ROMCS (O)
ROM Chip Select - This is the on-board system BIOS ROM chip select.

5.1.8.3 Coprocessor Signals

PEREQNPX (I-TPD)
Coprocessor Extension Request NPX, active high - This input signal is driven by the coprocessor and indicates that it needs transfer of data operands to or from memory. For PC/AT -compatibility, this signal is also gated with the internal ERROR/BUSY control logic before being output to the CPU as PEREQCPU during NPX interrupts.

-ERRORNPX (I-TPU)
Error NPX, active low - An input signal from the coprocessor indicating that an error has occurred in the previous instruction. This signal is internally gated and latched with -BUSYNPX to produce IRQ13.

-BUSYNPX (I-TPU)
Busy NPX, active low - An input signal that is driven by the coprocessor to indicate that it is currently executing a previous instruction and is not ready to accept another. This signal is decoded internally to produce IRQ 13 and to control PEREQCPU.

RESNPX (O)
Reset NPX - This output is connected to the coprocessor reset input. It is triggered through an internally generated system reset or via a write to port F1h. In the case of a system reset, the RESCPU signal is also activated. Write to port F1h only resets the coprocessor. A software FINIT signal must occur after an F1h generated reset in a 386SX system, otherwise, the 387SX is not initialized to the same state that a 287 is placed in by a hardware reset alone. Optionally, the F1 reset may be disabled by setting bit 6 of the MISCSET register to 1.

IRQ13 (O)
Interrupt Request, active high - This output is driven to the Bus Controller to indicate that an error has occurred with in the coprocessor. This signal is a decode of the -BUSYNPX and -ERRORNPX inputs.

-NPCS (O)
Coprocessor Chip Select - Provides decoding of the 287 coprocessor's I/O space. This is the entire F8h to FFh region when Special Features are disabled. When Special Features are enabled, only I/O accesses to F8h, FAh, FCh, and FEh cause -NPCS to be active. This signal is a no connect pin for 387SX operation, and reserved for future use in 386SX systems.

5.1.8.4 Bus Control Signals

-CHREADY (I-CMOS)
Channel Ready, active low - An input issued by the Bus Controller as an indication that the current channel bus cycle is complete. This signal is synchronized internally then combined with READY signals from the coprocessor and DRAM controller to from the final version of READY 0 which is sent to the CPU.

-CHS0/-MW (I-CMOS)
Channel Select 0 or Memory Write, active low - This signal is a de
the CPU's bus control signals and is sent to the Bus Controller. W
combined with -CHS1 and CHM/-IO and decoded, the bus cycle
defined for the Bus Controller. Activation of HLDA reverses this s
become an input from the Bus Controller. It is then a -MEMW sig
the DMA or bus master to access system memory.

-CHS1/-MR (I-CMOS)
Channel Select 1 or Memory Read, active low - This signal is a de
the CPU's bus control signals and is sent to the Bus Controller. W
combined with -CHS0 and CHM/-IO and decoded, the bus cycle
defined for the Bus Controller. Activation of HLDA reverses this s
become an input from the Bus Controller. It is then a -MEMR sign
the DMA or bus master to access system memory.

CHM/-IO (O)
Channel Memory I/O - This signal is a decode of the CPU's bus c
signals and is sent to the Bus Controller. When combined with -C
and CHS1 and decoded, the bus cycle type is defined for the Bu
troller. Activation of HLDA reverses this signal to become an inpu
the Bus Controller. It is then a -MEMR signal for the DMA or bus
access system memory.

-BLKA20 (O)
Block A20, active low - An output driven to the Bus Controller to c
vate address bit 20. It is a decode of the A20DATE signal and Po
indicating the dividing line of the 1 Mbyte memory boundary. Po
may be directly written or set by a read of I/O port EEh.

BUSOSC (I-TTL)
Bus Oscillator - This signal is supplied from an external oscillator
supplied to the Bus Controller when the VL82C320's internal cont
registers are set for asynchronous slot bus mode.

BUSCLK (O)
Bus Clock - This is the source clock used by the Bus Controller to
the slot bus. It is two times the AT bus slock (SYSCLK). It is a pr
mable division from TCLK2 or BUSOSC.

DMAHRQ (I-CMOS)
DMA Hold Request, active high - This signal is an input sent by the Bus Controller. It is internally synchronized by the VL82C320 before used to generate HRQ.

DMAHLDA (O)
DMA Hold Acknowledge - An output sent to the Bus Controller which indicates that the current hold acknowledge is in response to DMAHRQ.

-BRDRAM (O)
Board DRAM, active low - An output to indicate that on-board DRAM is being addressed.

-EALE (O)
Early Address Latch Enable, active low - In 286 mode, this signal is generated internally by decode of the CPU status signals. In 386SX mode, the VL82C320's -ADS input gated directly to the -EALE output.

OUT1 (I-CMOS)
Indicates a refresh request.

5.1.8.5 Peripheral Interface Signals

A20GATE (I-TTL)
Address Bit 20 Enable - An input that is used internally along with Port A bit 1 to determine if A20 is passed through or forced low. It also determines the state of -BLKA20.

TURBO (I-TTL)
Turbo, active high - This input to the VL82C320 determines the speed at whcih the system board operates. It is internally ANDed with a software settable latch. When high, operation is at full speed. When low, CLKw is divided by the value coded in configuration register MISCSET[4:3]. Turbo mode is active only when all TURBO requests are active.

-RC (I-TTL)
Reset Control, active low - The falling edge of this signal causes a RESCPU signal.

5.1.8.6 Bus Interface Signals

OSC (I-TTL)
Oscillator - This is the buffered input of the external 14.318 MHz oscillator.

-IOR (I-TTL)
I/O Read, active low- Indicates that an I/O read cycle is occurring on the bus.

-IOW (I-TTL)
I/O Write, active low - Indicates that an I/O write cycle is occurring on the bus.

RSTDRV (I-TTL)
Reset Drive, active high - This signal is used to reset internal logic and to derive RESCPU, and RESNPX.

SDLH/-HL (I-TTL)
System Data Bus Low to High/High to Low Swap - This signal is used to establish the direction of byte swaps.

-SDSWAP (I-TTL)
System Data Bus Byte Swap Enable - This is the qualifying signal needed for SDLH/-HL.

-XDREAD (I-TTL)
Peripheral Data Bus (XD Bus) Read - This signal determines the direction of the XD bus data flow. When this signal is high, the XD Bus is output enabled.

-LATLO (I-TTL)
SD Bus Low Byte Latch - This signal is needed to latch the SD bus low byte or XD bus to the local data bus until the end of the bus cycle.

D15-D0 (IO-TTL)
CPU Data Bus - This is the data bus directly connected to the CPU. It is also referred to as the local data bus.

SD15-SD0 (IO-TTL)
System Data Bus - This bus connects directly to the slots. It is used to transfer data to/from the slot bus.

XD7-XD0 (IO-TTL)
Peripheral Data Bus - This bus is connected to the Bus Controller and the VL82C320. It is used to transfer data to/from on-board 8-bit peripherals

PAR1,PAR0 (IO-TTL)
Parity Bit Bytes 1 and 0 - These bits are written to memory along with their corresponding bytes during memory write operations. During memory read operations, these bits become inputs and are used along with their respective data bytes to determine if a parity error has occurred.

-PARERROR (O)
Parity Error, active low - This signal is the result of a parity check on all reads from on-board memory.

286/-386SX (I-TPU)
286 or 386SX Mode - Tied high or left open for 286 mode and grounded for use in 386SX based systems.

5.1.8.7 Test Mode Pin

-TRI (I-TPU)
Three-state - This pin is used to drive all outputs to a high impedance state. When -TRI is low, all outputs and bidirectional pins are high impedance.

5.1.8.8 Power and Ground Pins

VDD (PWR)
Power connection, nominally +5 volts. These pins should each have 0.1 uF bypass capacitors.

VSS (GND)
Ground connection, 0 volts.

5.2 82C331 ISA Bus Controller

The 82C331 provides the functions of DMA, page address register, timer, interrupt control, port B logic, slot bus refresh address generation, and real-time clock (see Figure 5-6). The following paragraphs describe each of these subsections in detail.

5.2.1 DMA

The DMA subsection controls DMA transfers between an I/O channel and on- or off-board memory. DMAs can occur over the full 16M range available on the slot bus and the 32M range of system board DRAM and drive the appropriate bus command signals depending on whether the DMA is a memory read or write(see Figure 5-7). The I/O address of 82C331 Index Register and Data Port Register is ECh and EDh respectively. Each of the 82C331 Indexed Configuration Registers described in the following sections is accessed first by writing its address to the Index Register at I/O address ECh, then by accessing the data port at I/O address EDh.

The DMA subsection contains the following:

- **Two 8237-Compatible DMA controllers**
- **Middle address bit latches**
- **DMA controller registers**
- **LS612 Page registers**
- **Address generation**

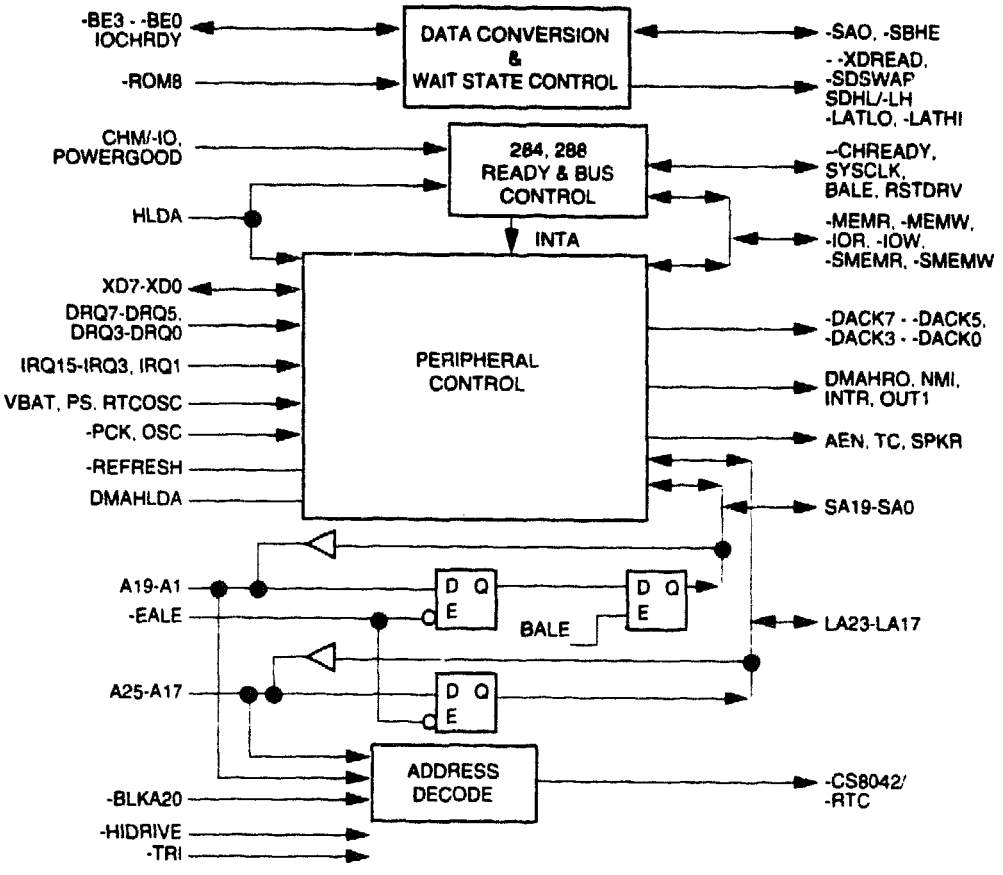


Figure 5-6. 82C331 Functional Block Diagram Subsection

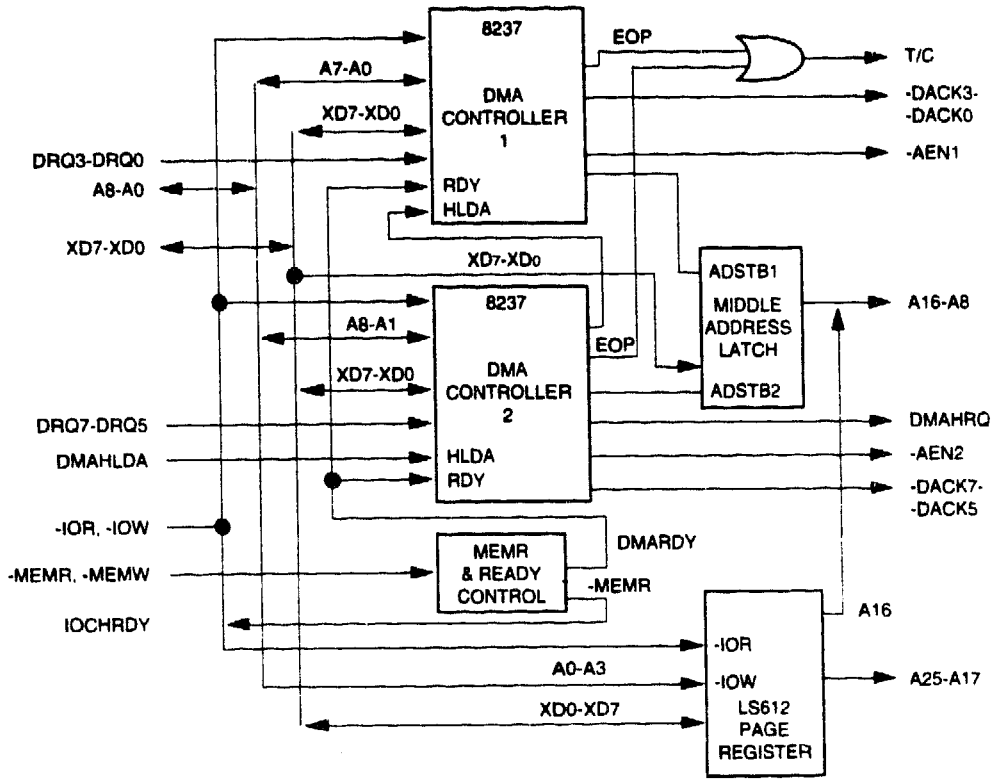


Figure 5-7. DMA Subsection Functional Block Diagram

5.2.1.1 DMA Controllers

The ISA bus controller supports seven DMA channels using two 8237 DMA controller equivalent megacells. The megacells capable of running at SYSCLK or SYSCLK/2 are programmable via indexed configuration register ROMDMA (Refer to Tables 5-14), DMA controller one contains channels zero through three. These channels are used to transfer data between 8-bit peripherals and 8- or 16-bit memory in pages of 64 KB. DMA controller two contains channels four through seven. These channels (except channel four) are used to transfer data between 16-bit I/O adapters and 16-bit memory in pages of 128 KB.

TABLE 5-14. ROMDMA (81h R/W) Indexed Configuration Register (Default = FCh)

Bit	Function
7 : 6	ROM wait states 00 = 3 wait states 01 = 1 wait state 10 = 2 wait state 11 = 3 wait states (Default)
5 : 4	8-bit DMA wait states 00 = 2 DMA clocks 01 = 4 DMA clocks 10 = 3 DMA clocks 11 = 3 DMA clocks (Default)
3 : 2	16-bit DMA wait states 00 = 2 DMA clocks 01 = 4 DMA clocks 10 = 3 DMA clocks 11 = 3 DMA clocks (Default)
1	DMA clock 0 = SYSCLK/2 (Default) 1 = SYSCLK
0	-MEMR timing 0 = -DMAMEMR is active at the same time as in the original design (Default) 1 = the falling edge of -DMAMEMR occurs one DMACLK earlier

5.2.1.2 Middle Address Bit Latches

The middle address bits are latched to an internal 8-bit register when the DMA controller writes a specified value onto an internal bus and by issuing an address strobe. The DMA controller issues the address strobe at the beginning of a DMA cycle and each time the lower 8-bit address increments across an 8-bit subpage boundary during block transfers. The middle DMA address bits register cannot be written to or read from externally and can only be loaded from the address strobe signals

5.2.1.3 DMA Controller Registers

Table 5-15 lists the addresses of all registers that can be read or written to DMA controller one and two.

Table5-15. DMA Controller Read/Write Address

DMA2	DMA1	Function
00C0h	0000h	Channel zero base and current address register
00C2h	0001h	Channel zero base and current word count register
00C4h	0002h	Channel one base and current address register
00C6h	0003h	Channel one base and current word count register
00C8h	0004h	Channel two base and current address register
00CAh	0005h	Channel two base and current word count register
00CCh	0006h	Channel three base and current address register
00CEh	0007h	Channel three base and current word count register
00D0h	0008h	Read status register/write command register
00D2h	0009h	Write request register
00D4h	000Ah	Write single mask register bit
00D6h	000Bh	Write mode register
00D8h	000Ch	Clear byte pointer flip-flop
00DAh	000Dh	Read temporary register/write master clear
00DCh	000Eh	Clear mask register
00DEh	000Fh	Write all mask register bits

5.2.1.4. Page Registers

An extended megacell is used in the ISA bus controller to generate the page registers for each DMA channel. These page registers provide the upper address bits during DMA cycles and are programmed by the 612AXS indexed configuration register(Refer to Table 5-16). Bit 7 enables the extended DMA functions when set to 1 by allowing access to the two required upper address bits, A24 and A25. When bit 7 = 0, the extended functionality is disabled. Any previously stored values for A24 and A25 are disabled and both bits are forced to 0. When bit 7 =1, the extended mode is enabled. A24 and A25 can be set in the memory mapper page register by setting bit 0 of this register to 1 and writing the data to the same address used for the lower page register byte. Resetting bit 0 to 0 allows access to the lower page registers. Bit 6 enables EISA I/O access compatibility when set to 1 by allowing access to the upper DMA page address bits at I/O addresses 4XX where XX = the same address as the lower page register byte. When set to 1, it also enables the extended DMA system and allows the contents of the upper page register's A24 and A25 to be used. Bit 0 allows access via the same I/O addresses to the lower address bits, A16-A23 of the DMA page register when set to 0 or to the upper address bits A24 and A25 when set to 1. The state of this bit has no effect unless bit 7 of this register has been previously set to 1. Tables 5-17 and 5-18 list the available page register options.

Table 5-16. 612AXS(82h R/W) Indexed Configuration Register (Default = 3Eh)

Bit	Function
7	Enable FF
6	4xx enable
5 : 1	Always one
0	FF PTR

Table 5-17. DMA Page Register Option One

Addresses A25:24 (B6 = 1)	Addresses A23:16 (B6 = x)	DMA Channel
0487h	0087h	0
0483h	0083h	1
0481h	0081h	2
0482h	0082h	3
048Bh	008Bh	5
0489h	0089h	6
048Ah	008Ah	7
048Fh	008Fh	-REFRESH

Table 5-18. DMA Page Register Option Two

Addresses A25:24 (B0 =1, B7 =1)	Addresses A23:16 (B0 =0,B7 =1)	DMA Channel
0087h	0087h	0
0083h	0083h	1
0081h	0081h	2
0082h	0082h	3
008Bh	008Bh	5
0089h	0089h	6
008Ah	008Ah	7
008Fh	008Fh	-REFRESH

5.2.1.5 Address Generation

DMA addressing for the ISA slot and system DRAM is made up of upper, middle, and lower address portions. The page registers for each DMA controller generate the upper address portion and must be set up by the 80386SX microprocessor prior to any DMA operation. The DMA controllers generate the middle address portion at the beginning of a DMA operation and each time a DMA address increments or decrements through a block boundary. The DMA controllers also generate the lower address portion during DMA operations. Tables 5-19 and 5-20 list the DMA addressing for the ISA slot and system DRAM.

Table 5-19. DMA Addressing for ISA Slot Access

Page Registers	Middle Address Latches	8237 Megacell	8-Bit DMA	16-Bit DMA
M9				
M8				
M7			LA23	LA23
M6			LA22	LA22
M5			LA21	LA21
M4			S/LA20	S/LA20
M3			S/LA19	S/LA19
M2			S/LA18	S/LA18
M1			S/LA17	S/LA17
M0			SA16	
	D7		SA15	SA16
	D6		SA14	SA15
	D5		SA13	SA14
	D4		SA12	SA13
	D3		SA11	SA12
	D2		SA10	SA11
	D1		SA9	SA10
	D0		SA8	SA9
		A7	SA7	SA8
		A6	SA6	SA7
		A5	SA5	SA6
		A4	SA4	SA5
		A3	SA3	SA4
		A2	SA2	SA3
		A1	SA1	SA2
		A0	SA0	SA1
		VSS		SA0
		-A0	-SBHE	
		VSS		-SBHE

Table 5-20. DMA Addressing for System DRAM Accesses

Page Registers	Middle Address Latches	8237 Megacell	8-Bit DMA	16-Bit DMA
M9				
M8				
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			A16	
	D7		A15	A16
	D6		A14	A15
	D5		A13	A14
	D4		A12	A13
	D3		A11	A12
	D2		A10	A11
	D1		A9	A10
	D0		A8	A9
		A7	A7	A8
		A6	A6	A7
		A5	A5	A6
		A4	S4	A5
		A3	A3	A4
		A2	A2	A3
		A1		A2
		A0		

5.2.2 Interrupt Controller

The interrupt controller consists of two 8259 programmable interrupt controller equivalent megacells with eight interrupt request lines each. The two 8259s are cascaded inside the ISA bus controller with two of the interrupt request inputs connected to internal circuitry. This allows a total of 13 external interrupt requests (see Figure 5-8).

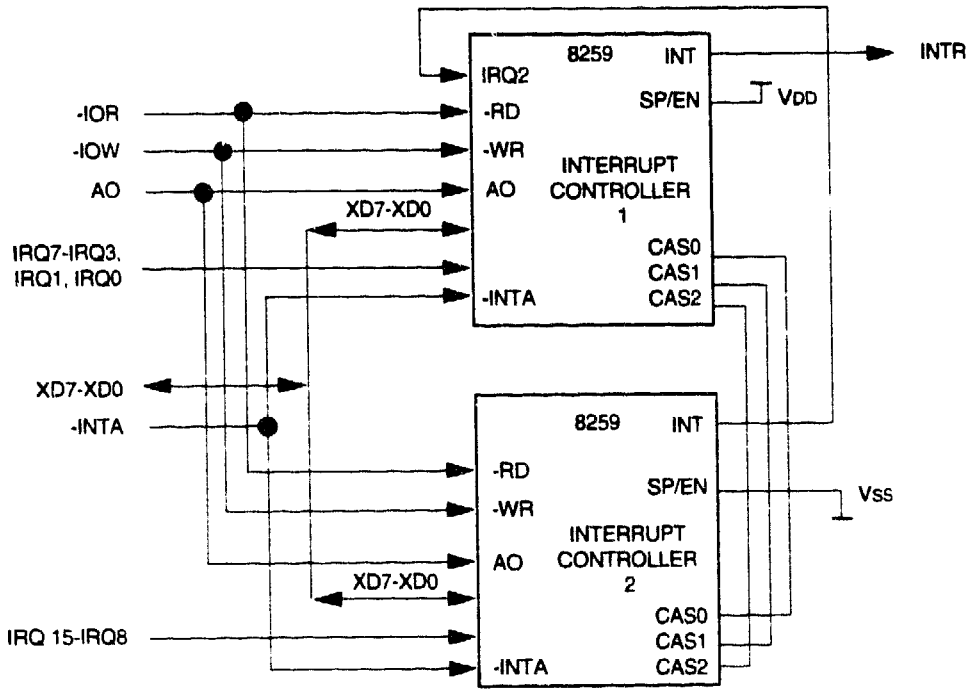


Figure 5-8. Interrupt Controller Block Diagram

5.2.2.1 Interrupt Controller Registers

The internal registers of the 8259 megacells are written to in the same manner as the standard 8259 chip. However, before normal operation begins, each megacell must follow an initialization sequence. The sequence starts by writing Initialization Command Word one (ICW1). Once written, the megacells expect the following sequence: ICW2, ICW3, and ICW4 (if required). Operation Control Words (OCWs) are written any time after initialization (refer to Tables 5-21 and 5-22).

Table 5-21. Interrupt Controller Write Operations

INT1	INT2	XD4	XD3	Register Function
0020h	00A0h	1	x	Write ICW1
0021h	00A1h	x	x	Write ICW2
0021h	00A1h	x	x	Write ICW3
0021h	00A1h	x	x	Write ICW4
0021h	00A1h	x	x	Write OCW1
0020h	00A0h	0	0	Write OCW2
0020h	00A0h	0	1	Write OCW3

Table 5-22. Interrupt Controller Read Operations

INT1	INT2	Register Function
0020h	00A0h	Interrupt Request Register (IRR), In-Service Register (ISR),or Poll Command (PC)
0021h	00A1h	Interrupt Mask Register (IMR)

5.2.2.2 Interrupt Levels

Table 5-23 lists the interrupt levels for the DECpc 320sxLP/325sxLP.

Table 5-23. DECpc 320sxLP/325sxLP System Interrupt Levels

Priority	Interrupt Controller	Interrupt Number	Interrupt Source
1	1	IRQ0	Timer tick
2	1	IRQ1	Keyboard controller
	1	IRQ2	Cascade interrupt
3	2	IRQ8	Real-time clock (RTC)
4	2	IRQ9	Reserved
5	2	IRQ10	Reserved
6	2	IRQ11	Reserved
7	2	IRQ12	Mouse interrupt
8	2	IRQ13	Numeric coprocessor
9	2	IRQ14	Hard disk drive
10	2	IRQ15	Reserved
11	1	IRQ3	COM2
12	1	IRQ4	COM1
13	1	IRQ5	Reserved
14	1	IRQ6	Floppy disk drive
15	1	IRQ7	LPT1

5.2.3 Counter/Timer

This timer subsection consists of one 8254 programmable counter/timer equivalent megacell with three internal independent counters. The clocks for each of the internal counters are tied to a 14.318 MHz oscillator through a divide-by-twelve counter. The gate inputs of counters zero and one are tied high to enable them at all times. The gate input of counter two is tied to bit zero of the port B register inside the ISA bus controller (see Figure 5-9).

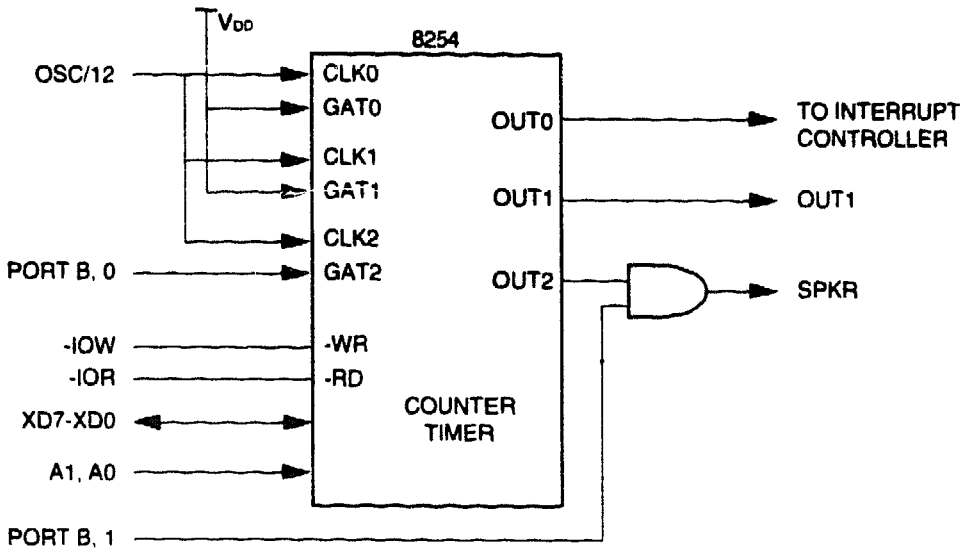


Figure 5-9. Counter/Timer Functional Block Diagram

5.2.3.1 Counter/Timer Outputs

The timer consists of one 8254 counter/timer megacell (see Figure 5-9). One of the outputs is directly available at an external pin. The output of counter zero is connected to input IRQ0 at interrupt controller one. The output of counter one is directly connected to pin OUT1. The output of one counter is tied to one of the inputs of an AND gate; the other AND gate input is connected to bit-one of the port B register inside the ISA bus controller. Table 5-24 lists the addressing for each of the counter/timer's internal registers.

Table 5-24. Counter/Timer Register Addressing

Address	-IOR	-IOW	Register Function
0040h	1	0	Write initial count to counter
0040h	0	1	Read count/status from counter zero
0041h	1	0	Write initial count to counter one
0041h	0	1	Read count/status from counter one
0042h	1	0	Write initial count to counter two
0042h	0	1	Read count/status from counter two
0043h	1	0	Write control word
0043h	0	1	No operation

5.2.3.2 Real-Time Clock

The Real Time Clock (RTC) contains a 146818A RTC equivalent megacell. This megacell consists of 10 RAM bytes (for the time, calendar, and alarm data), four control and status bytes, and 114 general purpose RAM bytes (refer to Table 5-25).

Table 5-25. Real Time Clock Address Map

Address	Function	Range
-7Fh	User RAM (Standby)	
0Dh	RTC Register D	(Readonly)
0Ch	RTC Register C	(Read-only)
0Bh	RTC Register B	(Read/Write)
0Ah	RTC Register A	(Read/Write)
09h	Year	0-99
08h	Month	1-12
07h	Date of Month	1-31
06h	Day of Week	1-7
05h	Hours (Alarm)	0-23
04h	Hours (Time)	0-23;24 Hour Mode
04h	Hours (Time)	1-12;12 Hour Mode
03h	Minutes (Alarm)	0-59
02h	Minutes (Time)	0-59
01h	Seconds (Alarm)	0-59
00h	Seconds (Time)	0-59

5.2.3.3 Time-Of-Day Registers

The contents of the time-of-day registers can be binary or BCD. The addressing for these registers are listed in Table 5-26.

Table 5-26. Time-of-Day Register Addressing

Address	BCD Mode	Binary Mode	Function/Time
09	99:0	63:0h	Year
08	12:1	0C:1h	Month
07	31:1	1F:1h	Date
06	7:1	7:1h	Day-of-week
05	12:1	0C:01h	Hours alarm (AM)
05	92:81	8C:81h	Hours alarm (PM)
04	12:1	0C:01h	Hours (AM)
04	92:81	8C:81h	Hours (PM)
03	59:0	3B:00h	Minutes alarm
02	59:0	3B:00h	Minutes
01	59:0	3B:00h	Seconds alarm
00	59:0	3B:00h	Seconds

5.2.4 Control Registers

The 146818 megacell contains four control registers: A,B,C, and D. All four registers are accessible by the 80386SX microprocessor and are fully accessible during update cycles (refer to Table 5-25).

All 128 bytes can be directly read and written by the 80386SX microprocessor except for the following:

- **Registers C and D (read-only)**
- **Bit seven of register A (read-only)**

5.2.4.1 Control Register A

This register contains control bits for selecting periodic interrupts, input divisors, and an update-in-progress status bit. Refer to Table 5-27 for control register A bit assignments.

Table 5-27. Control Register A Bit Assignments

Bit	Description	Abbreviation
7	Update in progress	UIP (Read-only)
6	Divisor bit two	DV2
5	Divisor bit one	DV1
4	Divisor bit zero	DV0
3	Rate select bit three	RS3
2	Rate select bit two	RS2
1	Rate select bit one	RS1
0	Rate select bit zero	RS0

5.2.4.2 Control Register B

This register contains command bits to control various modes of operation and interrupt enables for the RTC. Refer to Table 5-28 for control register B bit assignments.

Table 5-28. Control Register B Bit Assignments

Bit	Description	Abbreviation
7	Set command	SET
6	Periodic interrupt enable	PIE
5	Alarm interrupt enable	AIE
4	Update end interrupt enable	UIE
3	Reserved	
2	Data mode (binary or BCD)	DM
1	24/12 mode	24/12
0	Daylight savings enable	DSE

5.2.4.3 Control Register C

This register contains status information relating to interrupts and the internal operation of the RTC. Refer to Table 5-29 for control register C bit assignments.

Table 5-29. Control Register C Bit Assignments

Bit	Description	Abbreviation
7	IRQ pending flag	IRQF
6	Periodic interrupt flag	PF
5	Alarm interrupt flag	AF
4	Update ended flag	UF
3 : 0	Reserved (read as 0)	

5.2.4.4 Control Register D

This register contains a bit indicating the status of the on-chip standby RAM. Refer to Table 5-30 for control register D bit assignments

Table 5-30. Control Register D Bit Assignments

Bit	Description	Abbreviation
7	Valid RAM data and time	VRT
6 : 0	Not used (read as 0)	

.2.5 Signal Definitions

Table 5-31 lists a signal name for the 82C331.

Table 5-31. 82C331 Signal Name

Pin Number	82C331 Signal Name
1	SA6
2	-DACK2
3	SA5
4	T/C
5	SA4
6	BALE
7	SA3
8	SA2
9	OSC
10	VSS
11	SA1
12	SA0
13	-MEMCS16
14	-SBHE
15	-IOCS16
16	LA23
17	IRQ10
18	LA22
19	VDD
20	VSS

Table 5-31.(Cont.) 82C331 Signal Name

Pin Number	82C331 Signal Name
21	IRQ11
22	LA21
23	IRQ12
24	LA20
25	IRQ15
26	LA19
27	IRQ14
28	LA18
29	-DACK0
30	VSS
31	LA17
32	DRQ0
33	-MEMR
34	-DACK5
35	-MEMW
36	DRQ5
37	-DACK6
38	DRQ6
39	-DACK7
40	VSS
41	DRQ7
42	-MASTER
43	A25
44	A24
45	A23
46	A22
47	A21
48	A20
49	A19
50	A18

Table 5-31.(Cont.) 82C331 Signal Name

Pin Number	82C331 Signal Name
51	A17
52	A16
53	A15
54	A14
55	A13
56	A12
57	A11
58	A10
59	VDD
60	VSS
61	A9
62	A8
63	A7
64	A6
65	A5
66	A4
67	A3
68	A2
69	-BE3
70	A1
71	-BHE
72	A0
73	(C286)-386DX
74	HLDA
75	INTR
76	NMI
77	-CHS0/-MW
78	-CHS1/-MR
79	VDD
80	VSS

Table 5-31.(Cont.) 82C331 Signal Name

Pin Number	82C331 Signal Name
81	VSS
82	CHM/-IO
83	-EALE
84	-BRDRAM
85	-CHREADY
86	BUSCLK
87	-BLKA20
88	DMAHLDA
89	DMAHRQ
90	OUT1
91	XD7
92	XD6
93	VSS
94	XD5
95	XD4
96	XD3
97	XD2
98	XD1
99	XD0
100	VDD
101	-SDSWAP
102	SDLH/-HL
103	-XDREAD
104	-LATLO
105	-LATHI
106	VSS
107	SPKR
108	-CS8042/-RTC
109	IRQ1
110	IRQ13

Table 5-31.(Cont.) 82C331 Signal Name

Pin Number	82C331 Signal Name
111	-PCK
112	-ROM8
113	-HIDRIVE
114	-TRI
115	POWERGOOD
116	VBAT
117	PS/-RCLR
118	XTALIN
119	XTALOUT
120	VSS
121	-IOCHK
122	RSTDRV
123	IRQ9
124	DRQ2
125	-WS0
126	IOCHRDY
127	-SMEMW
128	AEN
129	-SMEMR
130	VSS
131	SA19
132	-IOW
133	SA18
134	-IOR
135	SA17
136	-DACK3
137	SA16
138	DRQ3
139	VDD
140	VSS

Table 5-31.(Cont.) 82C331 Signal Name

Pin Number	82C331 Signal Name
141	SA15
142	-DACK1
143	SA14
144	DRQ1
145	SA13
146	-REFRESH
147	SA12
148	SYSCLK
149	SA11
150	VSS
151	IRQ7
152	SA10
153	IRQ6
154	SA9
155	IRQ5
156	SA8
157	IRQ4
158	SA7
159	IRQ3
160	VSS

.2.6 Signal Description

.2.6.1 CPU Interface

A25, A24 (O-TS)
Address bus- These pins are outputs during DMA, master, or standard refresh modes. They are high impedance at all other times. A25 and A24 are driven from the altermate 612 registers during DMA and refresh cycles and are driven low during master cycles.

A23-A2 (IO-TTL)
Address bus- These pins are outputs during DMA, master, or standard refresh modes. They are inputs at all other times. As inputs, they are passed to the SA and LA buses and A15-A2 are used to address I/O registers internal to the bus control chip. As outputs, they are driven from different sources depending on which mode the VL82C331 is in. While in refresh mode, these pins are driven from the 612 and refresh address counter. While in DMA mode, they are driven from the 612 and DMA controller subsection. If the VL82C331 is in master mode, the pins A23-A17 are driven from the inputs LA23-LA17 and the pins A16-A2 are driven from the inputs SA16-SA2.

-BE3 (IO-TPU)
Byte Enable 3, active low- This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other byte enable signals to generate SA1, SA0 and-SBHE. As an output in 386DX mode SA1,SA0, and-SBHE are used to determine the value of-BE3. This pin should be left unconnected when using this part in 286/386SX mode.

A1 (IO-TTL)
This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. It is interpreted as address A1 and passed to SA1. As an output it is driven from the SA1 input.

-BHE (IO-TTL)
This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. It is interpreted as -BHE and passed to -SBHE. As an output it is driven from the -SBHE input.

A0 (IO-TTL)
This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. It is interpreted as A0 and passed to SA0. As an output it is driven from the SA0 input.

(C286)-386DX (I-TPU)
CPU is 286/386SX or 386DX- This pin defines the type of address bus to which the bus controller chip is interfaced. If the pin is tied high, the address bus is assumed to be emulating 286/386SX signals. In this mode, A25, A24, and -BE3 would be left unconnected. The pins -BE2 (A1), -BH1 (-BHE) and -BE0 (A0) would take on the 286/386SX functions. If the pin is tied low, A25, A24 can be used to generate up to 64 Mbyte addressing for DMA, and the byte enable pins will take on the normal 386DX addressing functions. This pin has an internal pull-up to cause the chip to default to 286/386SX mode if left unconnected. This pin is a hard wiring option and must not be changed dynamically during operation. When strapped for 286/386SX mode, the VL82C331 is assumed to be interfaced to the VL82C320 System Controller which in turn may be strapped for 286 or 386SX operation.

HLDA (I-TTL)
Hold Acknowledge- This is the hold acknowledge pin directly from the CPU. It is used to control direction on address and command pins. When HLDA is low, the VL82C331 is defined as being in the CPU mode. In the CPU mode, the local address bus (A bus) pins are inputs. The system address bus (SA and LA) pins along with the command pins (-MEMR, -MEMW, -IOR and -IOW) are outputs. When HLDA is high, the VL82C331 can be in DMA, refresh, or master modes. In both DMA and refresh modes, the commands and all address buses (A, SA and LA) are outputs. In master mode, the commands and system address bus (SA and LA) pins are inputs and the local address bus (A bus) pins are outputs. The SA bus is passed directly to the A bus except bits 17,18, and 19 are ignored. LA23-LA17 is passed directly to A23-A17.

INTR (O)
Interrupt Request - INTR is used to interrupt the CPU and is generated by the 8259 megacells any time a valid interrupt request input is received.

NMI (O)
Non-Maskable interrupt- This output is used to drive the NMI input to the CPU. This signal is asserted by either a parity error (indicated by -PCK being asserted after the ENP ARCK bit in Port B has been asserted), or an I/O channel error (indicated by -IOCHCK being asserted after the ENIOCK bit in Port B has been asserted). The NMI output is enabled by writing a 0 to bit D7 of I/O port 70h. NMI is disabled on reset.

5.2.6.2 System Controller Interface

-CHS0/-MW (IO-TTL)
Channel Status 0 or active low Memory Write - This input is used along with -CHS1 and CHM/-IO to determine what type of bus cycle the Bus Controller is to perform. This input has the same meaning and timing requirements as the S0 signal for a 286 microprocessor. -CHS0 going active indicates a write cycle unless -CHS1 is also active. When both status inputs are active it indicates an interrupt acknowledge cycle. This input is synchronized to the BUSCLK input. Activation of CPUHLDA reverses this signal to become an output to the System Controller. It is then a -MEMW signal for DMA or bus master access to system memory.

-CHS1/-MR (IO-TTL)
Channel Status 1 or active low Memory Read - This input is used along with -CHS0 and CHM/-IO to determine the bus cycle type. This input has the same meaning and timing requirements as the S1 signal for a 286 microprocessor. -CHS1 going active indicates a read cycle unless -CHS0 is also active. When both status inputs are active it indicates an interrupt acknowledge cycle. This input is synchronized to the BUSCLK input. Activation of CPUHLDA reverses this signal to become an output to the System Controller. It is then a -MEMR signal for DMA or bus master access to system memory.

CHM/-IO (I-TTL)
Channel Memory or active low I/O select - This input is used along with -CHS0 and -CHS1 to determine the bus cycle type. This input has the same meaning and timing requirements as the M/-IO signal for a 286/386SX microprocessor. CHM/-IO is sampled anytime -CHS0 or -CHS1 is active. If sampled high, it indicates a memory read or write cycle. If sampled low, an I/O read or write cycle should be executed. This input is synchronized to the BUSCLK input.

-EALE (I-TPU)
Early Address Latch Enable, active low - This input is used to latch the A23-A2 and Byte Enable signals. The latches are open when -EALE is low and hold their value when -EALE is high. The latched addresses are fed directly to the LA23-LA17 bus to provide more address setup time on the bus before a command goes active. The lower latched addresses are latched again with an internal ALE signal as soon as -CHS0 or -CHS1 is sampled active and fed to the SA19-SA0 and -SBHE outputs. In a 386DX system, this input is connected directly to the -ADS output from the CPU. In a 286/386SX system, this input is connected to the -EALE output from the VL82C320 System Controller.

-BRDRAM (I-TTL)
On-board DRAM, active low- An input from the System Controller indicating that the on-board DRAM is being addressed.

-CHREADY (O)
Channel Ready, active low- This output is maintained in the active state when no bus accesses are active. This indicates that the VL82C331 is ready to accept a new command. During normal bus accessed, -CHREADY is negated as soon as a valid bus requested is sampled on the -CHS0 and -CHS1 inputs. It is asserted again to indicate that the VL82C331 is ready to complete the current cycle. The bus command signals are then terminated on the next falling edge of the BUSCLK input.

BUSCLK (I-CMOS)
Bus Clock- This is the main clock input for the VL82C331. It runs at twice the frequency desired for the SYSCLK output. All inputs are synchronous with the falling edge of this input.

-BLKA20 (I-TTL)
Block A20, active low - This input is used while CPUHLDA is low to force the LA20 outputs low anytime it is active. When -BLKA20 is negated LA20 is generated from A20.

DMAHRQ (O)
Hold Request - This output is generated by the DMA controller any time a valid DMA request is received. It is connected to the DMAHRQ pin on the System Controller.

CMAHLDA (I-TTL)
DMA Hold Acknowledge - An input from the System Controller which indicates that the current hold acknowledge state is for the DMA controller or other bus master.

OUT1 (O)
Output 1-Indicates a refresh request to the System Controller. This is the 15 µsec output of timer channel 1.

5.2.6.3 ROM Interface

-ROM8 (I-TPU)
8/16 bit ROM select - This input indicates the width of the ROM BIOS. If -ROM8 is low, the VL82C331 chip generates 8-to 16-bit conversions for ROM accesses. Data buffer controls are generated assuming the ROM is on the MD bus. If -ROM8 is high, data buffer controls are generated assuming 16-bit wide ROMs are on the MD bus.

5.2.6.4 Bus Interface

-IOR (IO-TTL)
I/O Read, active low - This signal is an input when CPUHLDA is high and -MASTER is low. It is an output at all other times. When CPUHLDA is low, -IOR is driven from the 288 bus controller megacell. When CPUHLDA is high and -MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an extrnal 10K ohm pull-up resistor.

-IOW (IO-TTL)
I/O Write, active low - This signal is an input when CPUHLDA is high and -MASTER is low. It is an output at all other times. When CPUHLDA is low, -IOW is driven from the 288 bus controller megacell. When CPUHLDA is high and -MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an external 10K ohm pull-up resistor.

-MEMR (IO-TTL)
Memory Read, active low - This signal is an input when CPUHLDA is high and -MASTER is low. It is an output at all other times. When CPUHLDA is low, -MEMR is driven from the 288 bus controller megacell. When CPUHLDA is high and -MASTER is high, it is driven by the 8237 DMA controller megacells. This signal does not puise low for DMA address above 16 Mbytes. DMA above 16 Mbytes is only performed to the system board, never to the slot bus. This pin requires an external 10K ohm pull-up resistor.

-MEMW (IO-TTL)
Memory Write, active low - This signal is an input when CPUHLDA is high and -MASTER is low. It is an output at all other times. When CPUHLDA is low, -MEMW is driven from the 288 bus controller megacell. When CPUHLDA is high and -MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an external 10K ohm pull-up resistor.

-SMEMR (O-TS)
Memory Read, active low - -SMEMR is asserted on memory read cycles to addresses below 1 Mbyte and all refresh cycles. It is three stated for all addresses above 1 Mbyte. This pin requires an external 10K ohm pull-up resistor.

-SMEMW (O-TS)
Memory Write, active low - -SMEMW is asserted on memory write cycles to addresses below 1 Mbyte. It is three stated for all addresses above 1 Mbyte. This pin requires an external 10K ohm pull-up resistor.

LA23-LA17 (IO-TTL)
Latchable Address bus - This bus is an input when CPUHLDA is high and -MASTER is low. It is an output bus at all other times. When CPUHLDA is low, the LA bus is driven by the latched values from the A bus. When CPULDA is high and -MASTER is high, the LA bus is driven by the 612 memory mapper for DMA cycles and normal refresh. The LA bus is latched internally with the -EALE input.

SA19-SA17 (O-TS)
System Address bus - This bus is three stated when CPUHLDA is high and -MASTER is low. It is an output bus at all other times. When CPUHLDA is low, the SA bus is driven by the latched values from the A bus. When CPUHLDA is high and -MASTER is high, the SA bus is driven by the 8237 DMA controller megacells or refresh address generator. The SA bus will become valid in the middle of the status cycle generated by the -CHS0 and -CHS1 inputs. They are latched with an internally generated ALE signal.

SA16-SA0 (IO-TTL)
System Address bus - This bus an input when CPUHLDA is high and -MASTER is low. It is an output bus at all other times. When CPUHLDA is low, the SA bus is driven by the latched values from the A bus. When CPUHLDA is high and -MASTER is high, the SA bus is driven by the 8237 DMA controller megacells or refresh address generator. The SA bus will become valid in the middle of the status cycle generated by the -CHS0 and -CHS1 inputs. They are latched with an internally generated ALE signal.

-SBHE (IO-TTL)
System Byte High Enable, active low - This pin is controlled the same way as the SA bus. It is generated from a decode of the -BE inputs in CPU mode. It is forced low for 16-bit DMA cycles and forced the opposite value of SA0 for 8-bit DMA cycles.

-REFRESH (IT-OD)
Refresh signal, active low - This I/O signal is pulled low whenever a decoupled refresh command is received from the System Controller. It is used as an input to sense refresh requests from external sources such as the System Controller for coupled refresh cycles or bus masters. It is used internally to clock the refresh address counter and select a location in the memory mapper which drives A23-A17. -REFRESH is an open drain output capable of sinking 24 mA.

SYSCLK (O)
System Clock - This output is half the frequency of the BUSCLK input. The bus control outputs BALE and the -IOR, -IOW, -MEMR and -MEMW are synchronized to SYSCLK.

OSC (I-TTL)
Oscillator - This is the buffered input of the external 14.318 MHz oscillator.

RSTDRV (O)
Reset Drive, active high - This output is a system reset generated from the POWERGOOD input. RSTDRV is synchronized to the BUSCLK input.

BALE (O)
Buffered Address Latch Enable, active high - A pulse which is generated at the beginning of any bus cycle initiated from the CPU. BALE is forced high anytime CPUHLDA is high.

AEN (O)
Address Enable - This output goes high anytime the inputs CPUHLDA and -MASTER are both high.

T/C (O)
Terminal Count - This output indicates that one of the DMA channels terminal count has been reached. This signal directly drives the system bus.

-DACK7 - -DACK5, -DACK3 - -DACK0 (O)
DMA Acknowledge, active low - These outputs are the acknowledge signals for the corresponding DMA requests. The active polarity of these lines is set active low on reset. Since the 8237 megacells are internally cascaded together, the polarity of the -DACK signals must not be changed. This signal directly drives the system bus.

DRQ7-DRQ5,DRQ3-DRQ0 (I-TSPU)
DMA Request - These asynchronous inputs are used by an external device to indicate when they need service from the internal DMA controllers. DRQ0-DRQ3 are used for transfers from 8-bit I/O adapters to/from system memory. DRQ5-DRQ7 are used for transfers from 16-bit I/O adapters to/from system memory. DRQ4 is not available externally as it is used to cascade the two DMA controllers together.

IRQ15-IRQ9,IRQ7-IRQ3,IRQ1 (I-TTL)
Interrupt Request - These are the asynchronous interrupt request inputs for the 8259 megacells. IRQ0 and IRQ2 are not available as external inputs to the chip, but are used internally. IRQ0 is connected to the output of the 8254 counter 0. IRQ2 is used to cascade the two 8259 megacells together. All IRQ input pins are active high.

-MASTER (I-TTL)
Master, active low - This input is used by an external device to disable the internal DMA controllers and get access to the system bus. When asserted it indicates that an external bus master has control of the bus.

-MEMCS16 (I-TTL)
Memory Chip Select 16 bit - This input is used to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the Sytem Controller requests a 16-bit memory cycle and -MEMCS16 is sampled high.

-IOCS16 (I-TTL)
I/O Chip Select 16 bit - This input is used to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the System Controller requests a 16-bit I/O cycle and -IOCS16 is sampled high.

-IOCHK (I-TTL)
I/O Channel Check, active low - This input is used to indicate that an error has taken place on the I/O bus. If I/O checking is enabled, an -IOCHK assertion by a peripheral device generates an NMI to the processor. The state of the -IOCHK signal is read as data bit D6 of the Port B register.

IOCHRDY (I-TTL)
I/O Channel Ready - This input is pulled low in order to extend the read or write cycles of any bus access initiated by the CPU, DMA controllers or refresh controller. The default number of wait states for cycles initiatede by the CPU are four wait states for 8-bit peripherals, one wait state for 16-bit peripherals and three wait states for ROM cycles. One DMA wait state is inserted as the default for all DMA cycles. Any peripheral that cannot present read data, or strobe-in write data in this amount of time must use -IOCHRDY to extend these cycles.

-WS0 (I-TTL)
Wait State 0, active low - This input is pulled low by a peripheral on the S bus to terminate a CPU controlled bus cycle earlier than the default values defined internally on the chip.

POWERGOOD (I-TSPU)
System power on reset - This input signals that power to the board is stable. A schmitt-trigger input is used. This allows the input to be connected directly to an RC network.

5.2.6.5 Peripheral Interface

8042/-RTC (O)
Chip Select for 8042, active low - This output is active any time an SA address is decoded at 60h or 64h. It is intended to be connected to the chip select of the keyboard controller. If BUSCTL[6]=1, this pin is also active for RTC accesses at 70h and 71h. This is for use when the internal RTC is disabled and an external RTC is used.

XTALIN (I-CMOS)
Crystal Input - An internal oscillator input for the real time clock cry
requires a 32.768 KHz external crystal or stand-alone oscillator.

XTALOUT (O)
Crystal Output- An internal oscillator output for the real time clock
See XTALIN. This pin is a no connect when an external oscillator i

PS/-RCLR/-IRQ8 (I-TSPU)
Power Sense, active high - Used to reset the status of the Valid RA
Time (VRT) bit. This bit is used to indicate that the power has faile
that the contents of the RTC may not be valid. This pin is connect
external RC network. When BUSCTL[6]=1, this pin becomes -IRQ
for use with an external RTC.

VBAT (I)
Voltage Battery - Connected to the RTC hold-up battery.

SPKR (O)
Speaker - This output drives an externally buffered speaker. This
created by gating the output of timer 2. Bit 1 of Port B, 61H, is us
enable the speaker output, and bit 0 is used to gate the output of
timer.

5.2.6.6 Data Buffer Interface

XD7-XD0 (IO-TTL)
Periipheral data bus - The bidirectional X data bus outputs data o
INTA cycle or I/O read cycle to any valid address within the VL82
is configured as an input at all other times.

-SDSWAP (O)
System Data Swap, active low during some 8-bit accesses - It inc
that the data on the SD bus must be swapped from low byte to hi
or vice versa depending on the state of the SDLH/-HL pin. -SDSV
active for 8-bit DMA cycles when an odd address access occurs
more than one byte wide. For non-DMA accesses, -SDSWAP is a
any bus cycle to an 8-bit peripheral that is addressing the odd by

SDLH/-HL (O)
System Data Low to High, or High to Low - This signal is used to determine which direction data bytes must be swapped when -SDSWAP is active. When SDLH/-HL is high, it indicates that data on the low byte must be transferred to the high byte. When SALH/HL is low, it indicates that data on the high byte must be transferred to the low byte. SDLH/-HL is low for 8-bit DMA memory read cycles. For non-DMA accesses, SDLH/HL is low for any memory write or I/O write when -SBHE is low. SDLH/-HL is high at all other times.

-XDREAD (O)
Peripheral Data Read - This output is active low any time an INTA cycle occurs or an I/O read occurs to the address space from 0000h to 00F7h, which is defined as being resident on the peripheral bus.

-LATLO (O)
Latch Low byte - This output is generated for all I/O read and memory read bus accesses to the low byte. It is active with the same timing as the read command and returns high at the same time as the read command. This signal latches the data into the data buffer chip so that it acn be presented to the CPU at a later time. This step is required due to the asynchronous interface between the System Controller and VL82C331.

-LATHI (O)
Latch High byte - This output is generated for all I/O read and memory read bus accesses to the high byte. It is active with the same timing as the read command and returns high at the same time as the read command. This signal latches the data into the data buffer chip so that it can be presented to the CPU at a later time. This step is required due to the asynchronous interface between the System Controller and VL82C331.

-PCK (I-TPU)
Parity Check input, active low with pull-up - Indicates that a parity error has occurred in the on-board memory array. Assertion of this signal (if enabled) generates an NMI to the processor. The state of the -PCK signal is read as data bit D7 of the Port B register.

-HIDRIVE (I-TPU)
High Drive Enable - This pin is a wire strap option. When this input is low, all bus drivers defined with an IOL spec of 24 mA will sink the full 24 mA of current. When this input is high, all pins defined as 24 mA have the output low drive capability cut in half to 12 mA.

5.2.6.7 Test Mode Pin

-TRI (I-TPU)
Three-state - This pin is used to control the three-state drive of all outputs and bidirectional pins on the chip. If this pin is pulled low, all pins on the chip except XTALOUT are in a high impedance mode. This is useful during system test when test equipment or other chips drive the signals or for hardware fault tolerant applications. -TRI has an internal pull-up.

5.2.6.8 Power and Ground Pins

VDD (PWR)
Power connection, nominally +5 volts. These pins should each have 0.1 uF bypass capacitors.

VSS (GND)
Ground connection, 0 volts.

6

82C712 UNIVERSAL PERIPHERAL CONTROLLER II

The 82C712 Universal Peripheral Controller II (UPCII) is a 100-pin integrated chip. Its primary function is to provide peripheral support for the DECpc 320sxLP/325sxLP system (see Figure 6-1). Supported peripherals include:

- **Two 16450 UARTs (COM1 and COM2)**
- **One parallel port (LPT1)**
- **Integrated Drive Electronics (IDE) AT hard disk interface**
- **Floppy disk controller**

6.1 Serial Communications Ports

The peripheral controller contains two software-compatible 16450 UARTs designated as COM1 and COM2.

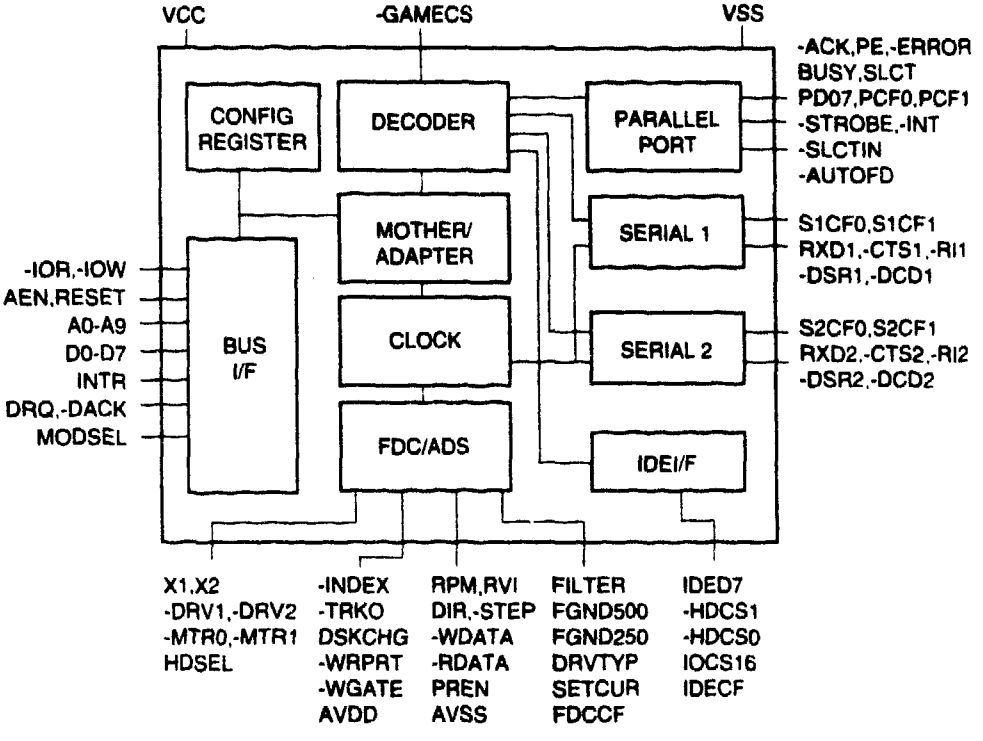


Figure 6-1. 82C712 Block Diagrem

6.1.1 Serial Communications Ports Registers

Addressing of the accessible UART registers is shown in Table 6-1. The base address of all registers is determined during the configuration sequence (see section 6.5 "82C712 Configuration"). UART registers are located at sequentially increasing addresses above this base address.

The following registers used by the serial Communication ports:

- **Received Buffer Register**
- **Transmit Buffer Register**
- **Interrupt Enable Register**
- **Interrupt Flag Register**
- **Byte Format Register**
- **Modem Control Register**
- **Line Status Register**
- **Modem Status Register**
- **Scratch Pad Register**
- **Divisor LSB**
- **Divisor MSB**

Table 6-1. Addressing of UART Registers

Offset	DRAB	I/O Function	Register
0h	0	Read	Received Buffer Register
0h	0	Write	Transmit Buffer Register
1h	0	Read/Write	Interrupt Enable Register
2h	x	Read/Write	Interrupt Flag Register
3h	x	Read/Write	Byte Format Register
4h	x	Read/Write	Modem Control Register
5h	x	Read	Line Status Register
6h	x	Read/Write	Modem Status Register
7h	x	Read/Write	Scratch Pad Register
0h	1	Read/Write	Divisor LSB
1h	1	Read/Write	Divisor MSB

Where:
x = Don't Care
DRAB = Divisor Register Address Bit (Bit 7 of Byte Format Register)

6.1.1.1 Receive Buffer (RB) Offset = 0h, Read only, DRAB = 0

This register holds the incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Double buffering is supported by the 82C712. This scheme uses an additional shift register (the Receive Shift Register; not user accessible) to assemble the incoming byte before it is loaded into the Receive Buffer. Refer to Table 6-2 for bit assignment.

Table 6-2. Receiver Buffer Register Bit Assignment

Bit	Function
7 : 0	Data bit 7 : 0

6.1.1.2 Transmit Buffer (TB) Offset=oh Write only, DRAB=0

This register holds the data byte to be sent. Bit 0 is the least significant bit, which is transmitted and received first. Double buffering is supported by the 82C712. This scheme uses a shift register (the Transmit Shift Register; not user accessible) which is loaded from the Transmit Buffer. The transmitted byte is then shifted out of the Transmit Shift Register to the TXD pin. Refer to Table 6-3 for bit assignment.

Table 6-3. Transmit Buffer Register Bit Assignment

Bit	Function
7 : 0	Data bit 7 : 0

6.1.1.3 Interrupt Enable Register (IER) Offset=1h, Read/Write, DRAB = 0

The low order 4 bit of this register control the enabling of each of the four possible types of interrupts. Setting a bit to a logic 1 enables the corresponding interrupt. It is possible to enable all, none, or some of the interrupt sources. Disabling all interrupts means that the interrupt flag register content is not valid and that none of the interrupt signals output by the 82C712 can be triggered by a UART. All other portions of the UART are unaffected by the disabling of interrupts. Refer to Table 6-4 for bit assignment.

Table 6-4. Interrupt Enable Register Bit Assignment

Bit	Function
7 : 4	Always Zero
3	A logic 1 here causes an interrupt when one of the bits in the MODEM Status register changes state
2	A logic 1 here causes an interrupt when an error (Overrun, Parity, Framing or Break) has been encountered. The line Status register must be read to determine the type of error.
1	A logic 1 here causes an interrupt when the Transmit Buffer is empty
0	A logic 1 here causes an interrupt when the Receive Buffer contains valid data

6.1.1.4 Interrupt Flag Register (IFR) Offset = 2h Read/Write, DRAB = X

When accessed, this register reports the highest pending interrupt. By reading it, the CPU can determine the source of the interrupt and can act accordingly. The Interrupt Flag Register (IFR) records the highest pending interrupt in bits 0 through 2. Other interrupts are temporarily disregarded (they are internally saved by the 82C712) until the highest priority one is serviced. Four levels of prioritized interrupts exist. In descending order of priority they are: 1. Line Status (highest priority); 2. Receive Buffer full; 3. Transmit Buffer empty; 4. MODEM Status (lowest priority). Refer to Table 6-5 for bit assignment. Refer to Table 6-6 for UART interrupt specification.

Table 6-5. Interrupt Flag Register Bit Assignment

Bit	Function
7 : 3	Always Zero
2 : 1	Interrupt ID bit 2 : 1
0	Zero if interrupt pending

Table 6-6. UART Interrupt Specifications

Bit 2	Bit 1	Bit 0	Priority	Type	Source	Servicing The Interrupt
0	0	1		NO INTERRUPT PENDING		
1	1	0	Highest	Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Read Line Status Register
1	0	0	Second	Receive Buffer Full	Receive Data	Read Receive
0	1	0	Third	Transmit Buffer Empty	Transmit Buffer	Read IFR or Write transmit buffer
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Carrier Detect	Read MODEM Status Register

6.1.1.5 Byte Format Register (BFR) Offset = 3h, Read/Write, DRAB = X

This read/write register contains format information for the serial line. Since it can be read, a separate copy of its content need not be kept in system memory. Refer to Table 6-7 for bit assignment.

Table 6-7. Byte Format Register Bit Assignment

Bit	Function
7	Divisor Register Address Bit (DRAB) 0 = access to all other internal UART registers 1 = access to the Divisor Registers
6	Set break 0 = set break 1 = clear break
5	Stick parity 0 = sum is used to determined parity 1 = force parity bit
4	Even parity select 0 = odd parity 1 = even parity
3	Parity enable 0 = disable parity generation and checking 1 = enable parity generation and checking
2	No. of stop bits 0 = 1 stop bits 1 = 1 1/2 stop bits (5 Bits Word Length) 1 = 2 stop bits (6 Bits Word Length) 1 = 2 stop bits (7 Bits Word Length) 1 = 2 stop bits (8 Bits Word Length)
1 : 0	Word length 0 0 = 5 Bits Word Length 1 0 = 6 Bits Word Length 0 1 = 7 Bits Word Length 1 1 = 8 Bits Word Length

6.1.1.6 Modem Control Register (MCR) Offset = 4h, Read/Write, DRAB = X

This byte-wide register is used to manage the connection to an external MODEM or data set. Refer to Table 6-8 for bit assignment.

Table 6-8. Modem Control Register Bit Assignment

Bit	Function
7 : 5	Always Zero
4	Loopback
3	This bit is used to enable an interrupt (OUT2 pin of UART). When OUT2=0 (default), the serial interrupt is forced into high impedance. When OUT2=1 the serial interrupt output is enabled.
2	This bit is used to control the OUT1 bit. It does not have an output pin associated with this bit. It can be read or written by CPU.
1	Request to send 0 = force -RTS to inactive state 1 = force -RTS to active state
0	Data terminal ready 0 = force -DTR to inactive state 1 = force -DTR to active state

6.1.1.7 Line Status Register (LSR) Offset = 5h, Read Only, DRAB = X

This byte-wide register supplies serial link status information to the CPU. A Receive Line Status interrupt is caused by one of the conditions flagged by Bits 1 through 4 of this register. It is read only. Writes to it are used at the factory for testing purposes and are not recommended. Refer to Table 6-9 for bit assignment.

Table 6-9. Line Status Register Bit Assignment

Bit	Function
7	Always Zero
6	Transmitter empty 0 = transmit buffer and transmit shif register not empty 1 = transmit buffer and transmit shif register empty
5	Transmit buffer empty 0 = write to transmit buffer 1 = character is loaded from the transmit buffer into the transmit shift register
4	Break interrupt 0 = reading LSR 1 = break interrupt
3	Framing error 0 = reading LSR 1 = no stop bit
2	Parity error 0 = reading LSR 1 = parity error detected
1	Overrun error 0 = CPU read LSR 1 = overrun occurs
0	Data ready 0 = reading the receive buffer 1 = character has been transferred from the receive shift register to the receive buffer

6.1.1.8 MODEM Status Register (MSR) Offset = 6h, Read/Write, DRAB = X

This byte-wide register holds the current value of the MODEM control lines. It also sets a bit (to a logic 1) each time one of these control lines changes state. Reading the MSR resets all of the Change bits to 0. a MODEM Status Interrupt is generated (if it is enabled) when Bit 0, 1, 2 or 3 is set to a 1. Refer to Table 6-10 for bit assignment.

Table 6-10. Modem Status Register Bit Assignment

Bit	Function
7	Data carrier detect; It is the complement of the -DCD pin. In diagnostic loopback mode, it is controlled by Bit 3 of the MCR.
6	Ring indicator; It is the complement of the -RI pin. In diagnostic loopback mode, it is controlled by Bit 2 of the MCR.
5	Data set ready; It is the complement of the -DSR pin. When in diagnostic loopback mode, this bit is identical to the -DTR bit in the MCR.
4	Clear to send; It is the complement of the -CTS pin. When in diagnostic loopback mode, this bit is identical to the -RTS bit in the MODEM Control Register (MCR).
3	Delta data carrier detect; It is set to a 1 if the -DCD line has changed state since the last time the MSR was read.
2	Trailing edge ring indicator; It is set to a 1 if the -RI line has changed from a logic 0 to a logic 1 since the last time the MSR was read.
1	Delta data set ready; It is set to a 1 if the -DSR line has changed state since the last time the MSR was read.
0	Delta clear to send; It is set to a 1 if the -CTS line has changed state since the last time the MSR was read.

6.1.1.9 Scratchpad Register Offset = 7h, Read/Write, DRAB = X

This byte-wide register has no effect on the UART within which it is located. It can be used for any purpose by the programmer.

6.1.1.10 Effects of Hardware Reset

Table 6-11 details the effect of a hardware RESET on the UART located in a 82C712.

Table 6-11. Hardware Reset on the 82C712 UART

Register	Cause of Reset	Reset State
Interrupt Enable Register	Hardware RESET	All bits = logic 0
Interrupt Flag Register	Hardware RESET	Bit 0 = logic 1 Other bits = logic 0
Byte Format Register	Hardware RESET	All bits = logic 0
MODEM Control Register	Hardware RESET	All bits = logic 0
Line Status Register	Hardware RESET	Bits 5,6 = logic 1 Other bits = logic 0
MODEM Status Register	Hardware RESET	Bits 0-3 = logic 1 Bits 4-7 = Input Signal
Receive Line Status Interrupt	Hardware RESET or Read LSR	logic 0 (low)
Receive Buffer Full Interrupt	Hardware RESET or Read RB	logic 0 (low)
Transmit Buffer Empty Interrupt	Hardware RESET or Read TB	logic 0 (low)
MODEM Status Interrupt	Hardware RESET or Read MSR	logic 0 (low)

6.1.2 Baud Rate Generation

The UART contains a programmable Baud Generator. The 24 MHz crystal oscillator frequency input is divided by 13 to provide a frequency of 1.8462 MHz. This is sent to the Baud Rate Generator and divided by the divisor for the UART. The output frequency of the Baud Rate Generator is 16 x the baud rate. Table 6-12 lists decimal divisors to use with a crystal frequency of 24 MHz.

Table 6-12. Divisors, Baud Rates and Clock Frequencies

	1.8462 MHz Clock	
Divisor **Baud Rate**	**Decimal Divisor for 16 X Clock**	**Percent Error (Note)**
50	2304	0.001
75	1536	
110	1047	
134.5	857	0.004
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.005
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	0.030
115200	1	

NOTE : The percent error for all Baud Rates, except where indicated otherwise, is 0.002%.

6.1.3 Serial Communications Header

The COM1 and COM2 provide the serial communications channels for the DECpc 320sxLP/325sxLP system. Table 6-13 lists the pinouts for COM1 and COM2.

Table 6-13. Serial Communications Connector Pinouts

Pin No.	Function
1	Data carrier detect
2	Receive data
3	Transmit data
4	Data terminal ready
5	Ground
6	Data set ready
7	Request to send
8	Clear to send
9	Ring indicator

6.2 Parallel Printer Port

The parallel printer port contains the functionality of a 16C452 printer port. The parallel printer port uses the following registers

- **Data Latch - Port A**
- **Printer Status - Port B**
- **Printer Control - Port C**

6.2.1 Data Latch Register

This read/write register is located at an offset of 00h from the base address of the parallel port. Data written to this register is transmitted to the printer. Data read from this port is the data which is on the connector.

6.2.2 Printer Status Register

This read-only register is located at an offset of 01h from the base address of the parallel port. This register contains real-time status for the LPT connector pins (Refer to Table 6-14).

Table 6-14. LPT Port Status Bit Assignments

Bit	Function
7	The state of the BUSY input pin 0 = the printer is busy and cannot accept data 1 = the printer is ready to accept data.
6	The state of the -ACK input pin 0 = the printer has received a character and is ready to accept another. 1 = it is still reading the last character sent or data has not been received.
5	The state of the PE input pin 0 = the presence of paper. 1 = a paper end condition.
4	The state of the SLCT input pin 0 = printer is not selected. 1 = printer is online.
3	The inverted state of the -ERROR input pin 0 = an error condition has been detected 1 = no errors.
2 : 0	Reserved

6.2.3 Printer Control Register

This read/write register is located at an offset of 02h from the base address of the parallel port. This register controls the printer control lines driven from the port (Refer to Table 6-15).

Table 6-15. LPT Port Control Bit Assignments

Bit	Function
7 : 5	Reserved
4	IRQEN; used to enable or disable interrupts resulting from the printer -ACK signal. 0 = IRQ is disabled 1 = generates interrupts when ACK changes from active to inactive
3	-SLCTIN; used to drive the -SLCTIN output pin. 0 = the printer is not selected 1 = selects the printer
2	-INIT; used to control the -INIT output pin. 0 = initializes the printer
1	-AUTOFD; used to control the -AUTOFD output pin. 0 = no autofeed 1 = causes the printer to generate a line feed after each line is printed
0	-STROBE; used to control the -STROBE output pin. 0 = no strobe 1 = generates the active low pulse(0.5 µs pulse minimum) which is required to clock data into the printer

6.2.4 Parallel Printer Port Header

Header LPT1 provides the parallel printer port channel for the DCEpc 320sxLP/325sxLp. Table 6-16 lists header pinouts.

Table 6-16. Parallel Printer Connector Pinouts

Pin No.	Signal	Function
1	-STROBE	Strobe
2 : 9	PD0-PD7	Printer data bit zero-seven
10	-ACK	Acknowledge
11	BUSY	Busy
12	PE	Paper end
13	SLCT	Select
14	-AUTOFD	Auto feed
15	-ERROR	Error
16	-INIT	Initialize printer
17	-SLCTIN	Select input

6.3 Integrated Drive Electronics Interface

THE 82C712 provides the control signals for the IDE interface and the IDE buffers as Table 6-17.

Table 6-17. IDE Control Signal

Signal	Function
-HDCS0	Primary Hard Disk Chip Select used to access the Task File Registers decodes 1F0h-1F7h
-HDCS1	Secondary Hard Disk Chip Select, decodes 3F6h-3F7h
-IOCS16	When active it indicates 16 bit I/O transfer
-IDED7	D7 of the IDE interface should be connected to this pin

6.3.1 Hard Disk Registers

Twelve hard disk registers control IDE operations. They are accessed between addresses 1F0h-1F7h, 3F6h and 3F7h. Table 6-18 lists the IDE register I/O addresses, specifies the I/O function required to access the registers. The following registers control IDE operations in AT mode:

- **Data Register**
- **Error Register**
- **Write Compensation Register**
- **Sector Count Register**
- **Sector Number Register**
- **Cylinder Number Register**
- **Drive/Head Register**
- **Status Register**
- **Command Register**
- **Fixed Disk Register**
- **Digital Input Register**

Table 6-18. IDE Register Address Map

Address	I/O Function	Register
1F0h	Read/Write	Data Register
1F1h	Read	Error Register
1F1h	Write	Write Compensation Register
1F2h	Read/Write	Sector count Register
1F3h	Read/Write	Sector Number Register
1F4h	Read/Write	Cylinder Number Register(Low Byte)
1F5h	Read/Write	Cylinder Number Register(High Byte)
1F6h	Read/Write	Drive/Head Register
1F7h	Read	Status Register
1F7h	Write	Command Register
3F6h	Write	Fixed Disk Register
3F7h	Read	Digital Input Register

3.3.1.1 Data Register

Read and Write to sector buffer. Accessed only when Read or Write command is executed.

3.3.1.2 Error Register

This register contains the status of the last executed command Refer to Table 6-19 for bit assignment.

Table 6-19. Error Register Bit assignments

Bit	Function
7	Set 1 if bad block detect.
6	Set 1 if Data ECC error.
5	Not used.
4	Set 1 if ID is not found.
3	Not used.
2	Set 1 if command is aborted.
1	Set 1 if track 0 is error.
0	Set 1 if Data Address Mark not found.

6.3.1.3 Write Compensation Register

This register contains the starting cylinder value divided by 4.

6.3.1.4 Sector Count Register

This register contains the number of sectors during a Verify, Read, Write or Format command. Note that a 0 value means 256 sector transfer.

6.3.1.5 Sector Number Register

This register contains the target's logical sector number of Read, Write and Verify command.

6.3.1.6 Cylinder Number Register (1F4h = Low Byte, 1F5h = High Byte)

These registers contain LSB and MSB of the first cylinder number where the disk is to be accessed for Read, Write, Seek and Verify command.

6.3.1.7 Drive/Head Register

Table 6-20. Drive/Head Register

Bit	Function
7	Set to 1
6	Set to 0
5	Set to 1
4	Drive select. 0 = Primary 1 = Secondary
3 : 0	head number (bit 3:MSB and bit 0:LSB)

6.3.1.8 Status Register

This register contains the status of the drive. Refer to Table 6-21 for bit assignments .

Table 6-21. Status Register Bit Assignments

Bit	Function
7	Set to 1 if the drive is busy.
6	Set to 1 if the drive is ready to accept command.
5	Set to 1 if write fault condition occurred.
4	Set to 1 if seek command is completed.
3	Set to 1 if drive is ready to transfer data.
2	Set to 1 if data correction is successful.
1	Set to 1 if index mark is detected.
0	Set to 1 if error occur from last command.

6.3.1.9 Command Register

This register contains command op code for fixed disk operation.

6.3.1.10 Fixed Disk Register

Table 6-22. Fixed Disk Register Bit Assignments

Bit	Function
7 : 4	Not Used
3	HEAD3EN
2	RESET 0 = Normal operation (Default) 1 = Generate reset to HDC
1	-IRQEN 0 = Enabled interrupt 1 = Disable interrupt (Default)
0	Reserved

6.3.1.11 Digital Input Register Definition

Table 6-23. Digital Input Register Definition Bit Assignments

Bit	Function
7	Diskette Change
6	Write Gate (HDC)
5	Head Select 3/Reduced Write Current (HDC)
4	Head Select 2 (HDC)
3	Head Select 1 (HDC)
2	Head Select 0 (HDC)
1	Drive Select 1 (HDC)
0	Drive Select 0 (HDC)

6.4 Floppy Disk Controller (FDC)

The 82C712 contains a fully compatible NECμPD72065B Floppy Disk Controller (FDC), an on-chip precision Analog Data Separator (ADS). The XT/AT bus interface circuitry is completely integrated with the 82C712 and requires no external logic when interfaced with the XT/AT bus. The licensed 765 core guarantees the compatibility. The on-chip Data Separator supports 250/300/500 Kb/s and 1Mb/s. Depending on the selected data rate, up to 3 external filters are automatically switched.

6.4.1 Floppy Disk Register

Five general registers control FDC operations. They are accessed at addresses 3F2h,3F4h,3F5h, and 3F7h. Table 6-24 lists the FDC register I/O addresses, specifies the I/O function required to access the registers. The following registers control FDC operations in AT mode:

- **Digital Output Register**
- **Main Status Register**
- **Data Register**
- **Digital Input Register**
- **Configuration Control Register**

Table 6-24. FDC Register Address Map

Address	I/O Function	Register
3F2h	Write	Digital Output Register
3F4h	Read	Main Status Register
3F5h	Read/write	Data Register
3F7h	Read	Digital Input Register
3F7h	Write	Configuration Control Register

3.4.1.1 Digital Output Register (Drive Control Register)

This writer register contains the motor enable bits, a DMA gate bit, a reset bit, and drive selection bits. Refer to Table 6-25 for bit assignments. Refer to Table 6-26 for drive/motor selection.

Table 6-25. Digital Output Register Bit Assignments

Bit	Function
7 : 4	Motor enable 3 : 0
3	enable DMA (DRQ and -DACK) and interrupt (IRQ)
2	Reset floppy controller
1 : 0	Drive select 1 : 0

Table 6-26. Drive/Motor selection

b7	b6	b5	b4	b1	b0	Driver
			1	0	0	0
		1		0	1	1
	1			1	0	2
1				1	1	3

6.4.1.2 Main Status Register

This read only register controls the data input and output mod
passes ready information to the 80386SX. Refer to Table 6-27
assignments.

Table 6-27. Main Status Register Bit Assignment

Bit	Function
7	Request for master; This bit indicates that the d is ready to send or receive data to or from the C bits DIO and RQM should be used to perform t handshaking function of "ready" and "direction CPU.
6	Data Direction (DIO); This bit indicates the dire transfer between the FDC and the data register then data is transferred from the data register t DIO=0, then transfer is from the CPU to the dat
5	Execution Mode (EXM); This bit is set only whe execution phase is in the non DMA mode. Whe goes low, the execution phase has ended and phase has begun. This bit operates only in the mode.
4	Command in process; Set high when the Read command is in progress. The FDC will not acce command.
3	Drive 3 Seeking; Set high when drive 3 is in the The FDC will not accept any other command.
2	Drive 2 Seeking; Set high when drive 2 is in the The FDC will not accept any other command.

Table 6-27. (Cont.) Main Status Register Bit Assignments

Bit	Function
1	Drive 1 Seeking; Set high when drive 1 is in the Seek mode. The FDC will not accept any other command.
0	Drive 0 Seeking; Set high when drive 0 is in the Seek mode. The FDC will not accept any other command.

6.4.1.3 Data Register

This read/write register is also the FIFO. All data and command information passes through the data register.

6.4.1.4 Digital Input Register

This read only register senses the state of the DSKCHG at bit 7. All other bits are tristated.

6.4.1.5 Configuration Control Register (Data Rate Register)

This write only register sets the data rate. Refer to Table 6-28 for bit assignments. Refer to Table 6-29 for data rate selection.

Table 6-28. Configuration Control Register Bit Assignments

Bit	Function
7 : 2	Reserved
1 : 0	Data rate selection 1 : 0

Table 6-29. Data Rate and Precompensation Programming Values

D1 **	D0 **	DRVTYP Pin	Data Rate MFM (Kb/s)	Normal Precomp* (ns)	Alternate Precomp* (ns)	FGND pin Enabled	RPM/LC Pin Level
0	0	x	500	125	125	FGND500	High
0	1	0	250	125	250	FGND250	Low
0	1	1	300	208	208	FGND250	Low
1	0	0	250	125	250	FGND250	Low
1	0	1	250	125	250	FGND250	Low
1	1	0	1000	63	83	None	High
1	1	1	1000	83	83	None	Low

* Normal values when PUMP/PREN pin set low;
Alternate values when PUMP/PREN pin set high.

** D0 and D1 are Data Rate Control Bits.

6.5 82C712 Configuration

The 82C712 is configured by hardware. Two serial ports, parallel port, IDE AT and FDC are available in this mode. Also, IRQ is active high only. The port addresses and enabling/disabling are determined by the jumper selects. (Refer to Table 6-30 through 6-34)

Table 6-30. Parallel Port Address Select

PCF1	PCF0	Function	
0	0	Disabled	
0	1	LPTA	3BCh
1	0	LPTB	378h
1	1	LPTC	278h

Table 6-31. Primary Serial Port Address Select

S1CF1	S1CF0	Function	
0	0	Disabled	
0	1	COM3	338h
1	0	COM2	2F8h
1	1	COM1	3F8h

Table 6-32. Secondary Serial Port Address Select

S1CF1	S1CF0	Function	
0	0	Disabled	
0	1	COM4	238h
1	0	COM1	3F8h
1	1	COM2	2F8h

Table 6-33. IDE Control

IDECF	Function
0	IDE Disabled
1	IDE Enabled

Table 6-34. FDC Control

FDCCF	Function
0	FDC Disabled
1	FDC Enabled

6.6 Signal Definitions

Table 6-35 lists a signal name for the 82C712.

Table 6-35. 82C712 Signal Name

Pin Number	82C712 Signal Name
1	RPM/LC
2	-MTR0
3	-DRV1
4	-DRV0
5	-MTR1
6	VSS
7	DIR
8	-STEP
9	-WDATA
10	-WGATE
11	HDSEL
12	-INDEX
13	-TRK0
14	-WRTPRT
15	VCC
16	-RDATA
17	DSKCHG
18	PREN
19	DRVTYP
20	X1/CLK
21	X2
22	IDED7
23	S1CF1
24	S1CF0
25	-HDCS0

Table 6-35.(Cont.) 82C712 Signal Name

Pin Number	82C712 Signal Name
26	-HDCS1
27	-IOCS16
28	A0
29	A1
30	A2
31	A3
32	A4
33	A5
34	A6
35	TC
36	-DACK
37	SSPIRQ
38	PSPIRQ
39	PINTR
40	FINTR
41	A7
42	A8
43	A9
44	-IOR
45	IOW
46	AEN
47	VSS
48	D0
49	D1
50	D2

Table 6-35.(Cont.) 82C712 Signal Name

Pin Number	82C712 Signal Name
51	D3
52	FDRQ
53	D4
54	D5
55	D6
56	D7
57	RESET
58	-GAMECS
59	SLCT
60	PE
61	BUSY
62	-ACK
63	PD7
64	PD6
65	PD5
66	PD4
67	VSS
68	PD3
69	PD2
70	PD1
71	PD0
72	VCC
73	-SLCTIN
74	-INIT
75	-ERROR

Table 6-35.(Cont.) 82C712 Signal Name

Pin Number	82C712 Signal Name
76	-AUTOFD
77	-STROBE
78	RXD1
79	PCF0
80	-DSR1
81	PCF1
82	-CTS1
83	IDECF
84	RI1
85	-DCD1
86	R12
87	-DCD2
88	RXD2
89	FDCCF
90	-DSR2
91	S2CF0
92	-CTS2
93	S2CF1
94	FGND500
95	FGND250
96	FILTER
97	RVI
98	AVSS
99	SETCUR
100	AVCC

6.7 Signal Description

6.7.1 Host Interface

PSPIRQ (Primary Serial Port Interrupt)
PSPIRQ is a source of Primary Serial Port (PSP) interrupt. Externally, it should be connected to either IRQ3 or IRQ4 via jumpers.

SSPIRQ(Secondary Serial Port Interrupt)
SSPIRQ is a source of Secondary Serial Port (SSP) interrupt. Externally, it should be connected to either IRQ3 or IRQ4 via jumpers.

FINTR (Floppy Controller Interrupt Request, T)
Floppy Controller Interrupt Request (programmable polarity), 24 mA driver. This interrupt is enabled/disabled via bit 3 of the Drive Control Register. The active output is used to get the attention of the CPU. The required action depends on the current function of the controller.

PINTR (Parallel Port Interrupt Request, T)
Parallel Port Interrupt Request (programmable polarity), 24 mA driver. The interrupt is enabled/disabled via bit 4 of the Parallel Control Register. If enabled, the interrupt is generated following the -ACK signal input.

A0-A9 (I/O Address, I)
Host address bit 0-9. These address bits are latched internally at the beginning of -IOR or -IOW.

AEN (Address Enable, I)
Active high Address Enable indicates DMA activity. Normally, this signal is used with A0-A9, -IOW, -IOR to decode I/O address ports.

-IOR (I/O Read, I)
Active low I/O read from host.

-IOW (I/O Write, I)
Active low I/O write from host.

RESET (Master Reset, IS)
Active high Reset from host (Schmitt-trigger input). RESET has to be valid for a minimum of 500 nanosecond. The effect of hardware reset is shown in the functional description of each port. The configuration registers are not affected. They come up in the default condition only on power up. The falling edge of RESET will latch the jumper configuration. The jumper select pin must be valid prior to this edge.

D0-D7 (Data Bus, I/OH)
Host data bus, 24 mA driver. This bi-directional data bus is used to transfer information between the CPU and the 82C712.

-DACK (DMA Acknowledge, I)
Active low input to acknowledge the DMA request. This signal normally is used to enable DMA read or write.

FDRQ (FDC DMA Request, OH)
Active high DMA request output signal to the host, 24 mA driver.

TC (Terminal Count, I)
Active high input signal indicates termination of DMA transfer, qualified by -DACK before use on chip.

5.7.2 Parallel Port Controller

PD0-PD7 (Port Data, I/OH)
The bi-directional parallel data bus is used to transfer information between CPU and peripherals. These signals have high current drive and capable of sinking 24 mA @0.5V.

-STROBE (Data Strobe, OC)
This active low output indicates to the peripheral that the data at the parallel port is valid. This pin has high current drive and is capable of sinking 24 mA @0.5V.

-SLCTIN (Select Input, OC)
This active low output selects the printer when it is low. This pin has high current drive and is capable of sinking 24 mA @0.5V.

-INIT (Initialize, OC)
This active low output initialized (resets) the printer when it is low. This pin has high current drive and is capable of sinking 24 mA @0.5V.

-AUTOFD (Automatic Feed, OC)
When this output is low the printer automatically adds one line feed after each line is printed. This pin has high current drive and is capable of sinking 24 mA @0.5V.

-ACK (Acknowledge, I)
Active low Acknowledge input. Low indicates that data has been received and the printer is ready to accept more data.

BUSY (Printer Busy, I)
Active high Busy input. The high input signal indicates the printer can not accept additional data.

PE (Paper End, I)
Active high Paper End input. The high input signal indicates the printer is out of paper.

SLCT (Select, I)
Active high device Select input. The input is set high by the printer when it is selected.

-ERROR (Error, I)
Active low Error input. This input is set low by the printer when it detects the error.

PCF0 (I)
Parallel Port Configuration Control 0 in 82C712. Input during hardware RESET to select address for parallel port. (NOTE 1)

PCF1 (I)
Parallel Port Configuration Control 1 in 82C712. input during hardware RESET to select address for parallel port. (NOTE 1)

.7.3 Serial Port Interface

-CTS1, -CTS2 (Clear to Send, I)
Active low Clear to Send inputs for Primary and Secondary serial ports. Handshake signal which notifies the UART that the MODEM is ready to receive data. The CPU can monitor the status of -CTS signal by reading bit 4 of Modem Status Register (MSR). A -CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of interrupt Enable Register is set, the interrupt is generated when -CTS changes state. The -CTS signal has no effect on the transmitter. Note:Bit 4 of MSR is the complement of -CTS.

-DSR1, -DSR2 (Data Set Ready, I)
Active low Data Set Ready inputs for Primary and Secondary serial ports Handshake signal which notifies the UART that the MODEM is ready to establish the communication link. The CPU can monitor the status of -DSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when -DSR changes state. Note: Bit 5 of MSR is the complement of -DSR.

-DCD1, -DCD2 (Data Carrier Detect, I)
Active low Data Carrier Detect input for Primary and Secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the MODEM. The CPU and monitor the status of -DCD signal by reading bit 7 of Modem Status Register (MSR). A -DCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when -DCD changes state. Note: Bit 7 of MSR is the complement of -DCD.

-RI1, -RI2 (Ring Indicator, I)
Active low Ring Indicator input for Primary and Secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the MODEM. The CPU can monitor the status of RI signal by reading bit 6 of Modem Status Register (MSR). A -RI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when -RI changes state. Note: Bit 6 of MSR is the complement of -RI.

RXD1, RXD2 (Receive Data, I)
Active high receive serial data input from communication link.

S1CF0 (I)
Primary Serial configuration 0 in 82C712 . Input during hardware RESET to select address for secondary serial port. (NOTE 1)

S1CF1 (I)
Primary Serial configuration 1 in 82C712 . Input during hardware RESET to select address for secondary serial port. (NOTE 1)

S2CF0 (I)
Secondary Serial Port Configuration Control 0 in 82C712. input during hardware RESET to select address for secondary serial port. (NOTE 1)

S2CF1 (I)
Secondary Serial Port Configuration Control 1 in 82C712. input during hardware RESET to select address for secondary serial port. (NOTE 1)

6.7.4 IDE Interface

-IOCS16 (16 bit I/O Indication, I)
Active low 16 bit I/O indication while in the AT hard disk node. The hard disk interface generates IOCS16 to inform the host and the 82C712 that 16 bit I/O transfers are about to begin. IOCS16 is active only when transferring data words in AT mode. Low = 16 bit, high = 8 bit (AT mode)

IDED7 (IDE Data Bit 7, I/OH)
IDE Data Bit 7 while in the AT hard disk mode. IDED7 transfers data at I/O addresses 1F0h-1F7h (R/W), 3F6h (R/W), 3F7h(W). IDED7 should be connected to the IDE data bit 7. Normally, the 82C712 functions as a buffer, transferring data bit 7 between the IDE device and the host. During read of I/O address 3F7h, IDED7 is FDC Disk Change bit 7. In the XT hard disk mode, IDE7 is no used.

-HDCS0 (Hard Disk Chip Select 0, OH)
Active low Hard Disk Chip Select 0 for IDE interface in either AT/XT hard disk modes. This decodes the address space 1F0h-1F7h (default) if configured in At mode (CR#00h<1> = 1) or 320h-323h if configured in XT mode (CR#00h<1> =0).

-HDCS1 (Hard Disk Chip Select 1, OH)
Active low Hard Disk Chip Select 1 for IDE interface, in either AT/XT hard disk modes. This decodes the address space 3F6h-3F7h.

IDECF (I)
IDE configuration control in 82C712. Input during hardware RESET to enable/disable IDE. (NOTE 1)

5.7.5 Floppy Interface

-RDATA (Read Data, IS)
The active low signal reads raw data from the disk. This is a Schmitt input.

-WDATA (Write Data, OD)
This active low signal writes precompensated serial data to the selected drive. This is a high open current drain output and is not gated internally with the write gate.

-DRV0,1 (Drive, OD)
These active open drain outputs select drives 0-3. Two drives can be supported directly. An external decoder (2 to 4) is needed to select four drives.

DSKCHG (Disk Change, IS)
This Diskette Change signal notifies the FDC that the disk drive door has been opened. This Schmitt latched input is inverted and read via bit 7 of I/O address 3F7h.

-WGATE (Write Gate, OD)
This active low open drain signal enables the head to write onto the disk.

DIR (Direction, OD)
This open drain output signal controls the head movement direction. (Low = Step in; High = Step out)

-STEP (OD)
This active low output signal supplies the step pulse, at a programmable rate, to move the head for seek operation.

HDSEL (Head Select, OD)
This open drain output selects the head on the selected drive. (Low = side 0; High = side 1)

-TRK0 (Track 0, IS)
This active low Schmitt input indicates that the head is in track 0 of the selected drive.

-WRPRT (Write Protect, IS)
This active low Schmitt input indicates that the disk is write-protected. Any Write command is ignored.

-INDEX (IS)
This active low Schmitt input indicates the beginning of a track.

-MTR0,1 (Motor, OD)
This active low open drain output selects motor drivers 0-3. Two drivers are supported directly. An external decoder (2 to 4) is needed to select four motor drivers. The motor enable bits are software controllable via the Digital Output Register (DOR).

FILTER (I/O)
This signal is the output of the charge pump and the input to the VCO. PLL filter circuitry is connected to this pin (FGND250, FGND500 and analog ground).

FGND500 (Filter Ground 500 Kb/s, OL)
This low impedance output signal is connected to 500 Kb/s (MFM) PLL filter circuitry.

FGND250 (Filter Ground 250 Kb/s, OL)
This low impedance output signal is connected to 250 Kb/s (MFM) PLL filter circuitry.

PREN (Precompensation Enable, I)
This input selects precompensation mode: Low = Normal, High = Alternate. Precompensation values (shown in Floppy section) depend on the selected data rate and precompensate mode.

DRVTYP (Drive Type, I)
When this input is low, the dual speed spindle motor driver is used. If 300Kb/s is selected via Data Rate register, the PLL actually runs at 250Kb/s. When this input is high (standard AT), the single speed spindle motor driver is used. The PLL runs at 300Kb/s when data rate is selected at 300Kb/s.

SETCUR (Set Current, I)
This signal is connected to the Analog ground via an external resistor to set the charge pump current for PLL filter.

RPM/LC (Revolutions per Minute/Low current, OD)
Depending on DRVTYP input, this open drain output signal can function in two modes:

1. When DRVTYP is LOW (dual speed spindle), this output selects either 300RPM or 360RPM. This output is low when 250/300Kb/s is selected and high when 500Kb/s selected.

2. When DRVTYP is HIGH (single speed spindle), the output goes high when 500Kb/s is selected (high density media). It is also used to indicate when to reduce write current.

RV1 (I)
An external resistor connects this pin to Analog ground for PLL filter.

FDCCF (I)
FDC Configuration control in 82C712. Input during hardware RESET to enable/disable FDC. (NOTE 1)

6.7.6 Power and Ground

Vcc (2) (Power)
+5VDC Digital supply.

X1/CLK (Crystal Clock)
The external connection for series resonant 24 MHz crystal input. ACMOS compatible oscillator is required if a crystal is not used.

X2 (Crystal, O)
24 MHz crystal. If an external clock is used, this pin should not be connected.

-GAMECS (GAMECS, O)
It will be low when I/O address 201h is selected.

Vss (Ground)
0V Reference for the FDC digital, CPU interface, serial ports, parallel port, and disk interface output drive circuitry, respectively.

AVcc (Analog Power)
Analog +5VDC for the PLL.

AVss (Analog Ground)
Analog Ground for the PLL.

Buffer Types:

I = TTL input	OD = High current open drain output
IS = Schmitt-trigger input	OL = Low current open drain output
O = TTL output	T = Tri-state TTL output, 24 mA
OH = High current TTL output	Oclk = Clock Input
OC = Open Drain	

NOTE 1 : The external 27K ohm resistor is used to pull these pins to the required signal levels.

7

8042 KEYBOARD/MOUSE CONTROLLER

The Keyboard/Mouse controller ROM contains the program required to support the PS/2 command set and 128 bytes of conversion code. Serial I/O is handled with receiver/transmitter hardware implementations that depend on an 8-bit timer for time-out detection.

7.1 Command Invocation

The system writes commands to Port 64h and the data associated with the command to Port 60h. The system reads all keyboard and mouse data at Port 60h. The system reads the 8042 status at Port 64h. Keyboard commands and data are written to Port 60h. Mouse commands are written to Port 60h after the Write mouse (0D4h) command. The mouse data follows the same procedure. The 8042 Status Register (read of Port 64h) indicates if the 8042 is ready to accept another command or if data is ready from the last command. The system can only send data or a command to the 8042 if the IBF (Input Buffer Full, bit 1 of the Status Register) flag is false. The data is only valid from the 8042 if the OBF (Output Buffer Full, bit 0 of the Status Register) flag is true. Before issuing a command to return data, the OBF and IBF should be false. After waiting for the OBF flag to go true, the data is read from Port 60h.

7.2 Status Register

The status register is an eight bit read only register accessed via Port 64h. An IN on Port 64h provides the status shown in Table 7-1.

Table 7-1. Status Register

Bit	Function
7	Receive parity error 0 = normal 1 = parity error
6	General time-out 0 = normal 1 = time-out occurred
5	Mouse Output Buffer Full 0 = empty 1 = full
4	Keyboard enable 0 = disabled 1 = enabled
3	Command/data (F1) 0 = data or idle 1 = command or active
2	System flag (F0) Value = value of the system flag (bit2) in the Keyboard Controller Command Byte
1	Input buffer full (IBF) 0 = empty 1 = full
0	Output buffer full (OBF) 0 = empty 1 = full

7.3 Standard Commands

The Keyboard/Mouse Controller supports a Standard Command Set described in Table 7-2.

Table 7-2. Standard Command Set

ADDRESS	DESCRIPTION
C0h-1Fh	Read the contents of the designated RAM locations (20h-3Fh) and send it to the system.
20h-3Fh	Read from RAM
40h-5Fh	Get a byte of data from system and write into one of locations (20h-3Fh)
60h-7Fh	Write to RAM
A4h	Test Password Returns 0FAh if password is loaded. Returns 0F1h if password is not loaded.
A5h	Load Password Loads Password until a '0' is received from the system.
A5h	Enable Password Enables the checking of keystrokes for a match with the password.
A7h	Disable Mouse
A8h	Enable Mouse
A9h	Test Mouse Clock and Data

Table 7-2.(Cont.) Standard Command Set

ADDRESS	DESCRIPTION
AAh	8051 Self Test Returns 55h if successful self test.
ABh	Test Keyboard Clock and Data lines.
ACh	The Diagnostic Dump is not implemented
ADh	Disable Keyboard
AEh	Enable Keyboard
Coh	Emulate reading the input port (P1) and send data to the system
C1h	Continuously puts the lower four bits of Port 1 into the STATUS register.
C2h	Continuously puts the upper four bits of Port 1 into the STATUS register.
D0h	Send Port 2 value to the system (emulates data since there's no real P2)
D1h	Only set/reset GateA20 line based on the system data bit 1.
D2h	Send data back to the system as if it came from the keyboard.
D3h	Send data back to the system as if it came from the mouse.
D4h	Output next received byte of data from system to the mouse.
E0h	Reports the state of the test inputs.
FXh	Pulse only P2.0 (the reset line) low for 6us if Command byte is even.

7.4 Extended Commands

The Keyboard/Mouse Controller supports an extended command set described in Table 7-3.

Table 7-3. Extended Command Set

ADDRESS	DESCRIPTION
B8h	Setup Phoenix extended memory access INDEX
B9h	Get current Phoenix extended memory access INDEX
BAh	Get current Phoenix extended memory referenced by INDEX
BBh	Write Phoenix extended memory referenced by INDEX
BCh/BDh	Read/Write RAM @VPointer
C7h	Sets Port 1 bits corresponding bits to system data bits that are set.
C8h	Clears Port 1 bits corresponding bits to system data bits that are set.
C9h	Sets Port 2 bits corresponding bits to system data bits that are set.
CAh	Clears Port 2 bits corresponding bits to system data bits that are set.
D3h/D4h	Set/Clear Fast GateA20 Acknowledge (0FAh) is sent to the system upon completion of the command.
D5h	Read Phoenix Version Number (2 bytes).
D6h	Read Version Information (2 bytes)

Table 7-3.(Cont.) Extended Command Set

ADDRESS	DESCRIPTION
D7h	Read Model number (2 bytes) and then read the customer's model number (1 byte).
D8h/D9h	Set/Clear Fast GateA20 Acknowledge (0FAh) is sent to the system upon completion of the command.
EXh	The Phoenix extended Odd EXh commands sets P2.1,2 or 3 based on command bits 1,2 and 3. Even EXh commands clears P2.1,2 or 3 based on command bits 1,2 and 3.

7.5 Keyboard Controller Command Byte

The internal status is defined by the Keyboard Controller Command Byte (KCCB). The KCCB resides in RAM at location 20h. The KCCB can be read/written with the special commands listed in Table 7-4.

NOTE: The KCCB is read with a 20h command and written with a 60h command.

Table 7-4. Keyboard Controller Command Byte

Bit	Function
7	Reserved (always zero)
6	Keycode conversion 0 = Scan Code no conversion 1 = Scan Code conversion enabled
5	Disable Mouse 0 = enabled 1 = disabled
4	Disable Keyboard 0 = enabled 1 = disabled
3	Reserved (always zero)
2	System flag 0 = hot reset did not occur 1 = hot reset occurred
1	Enable Mouse OBF interrupt 0 = disabled 1 = enabled
0	Enable Keyboard OBF interrupt 0 = disabled 1 = enabled

7.6 Keyboard Commands

Any command/data written to Port 60h is automatically transmitted to the keyboard by the 8042 if 8042 is not in a waiting for data mode. Refer to Table 7-5 for Keyboard Commands.

Table 7-5. Keyboard Commands

COMMAND	DESCRIPTION
EDh	Set LEDs
EEh	Echo
EFh	Invalid command
F0h	Select alternate scan code set
F1h	Invalid command
F2h	Read ID bytes
F3h	Set typematic delay and rate
F4h	Enable keyboard
F5h	Disable keyboard and set defaults
F6h	Set defaults
F7h	Set all keys typematic
F8h	Set all keys make/break
F9h	Set all keys make only
FAh	Set all keys typematic/make/break
FBh	Set key type typematic
FCh	Set key type make/break
FDh	Set key type make only
FEh	Resend the last transmission
FFh	BAT, Reset the defaults and buffers

NOTE: Commands F7 through FD are normally used for Character Set 3.

'.7 Mouse Commands

The mouse command sequence is as follows:

1. Write an 8042 command D4h (Write Mouse) to Port 64h.
2. Write command/data to Port 60h.

Refer to Table 7-6 for Mouse Commands.

Table 7-6. Mouse Commands

COMMAND	DESCRIPTION
E6h	Reset Scaling
E7h	Set Scaling
E8h	Set Resolution
E9h	Status Request
EAh	Set Stream Mode
EBh	Read Data
ECh	Reset Wrap Mode
EDh	Invalid Command
EEh	Set Wrap Mode
EFh	Invalid Command
FOh	Set Remote Mode
F1h	Invalid Command
F2h	Read Device Type
F3h	Set Sampling Rate
F4h	Enable Mouse
F5h	Disable Mouse
F6h	Set Default Values
F7h - FDh	Reserved
FEh	Resend
FFh	Reset

8

VGA VIDEO CONTROLLER

The DECpc 320sxLP/325sxLP system board contains an Extended High Resolution Video Controller. Figure 8-1 shows the major VGA Video controller hardware components. Components include

- **OTI-067 VGA Graphics Controller**
- **OTI-066 Video DAC**
- **OTI-069 Video Pixel Clock Generator**
- **Video BIOS EPROM**
- **Video RAM**

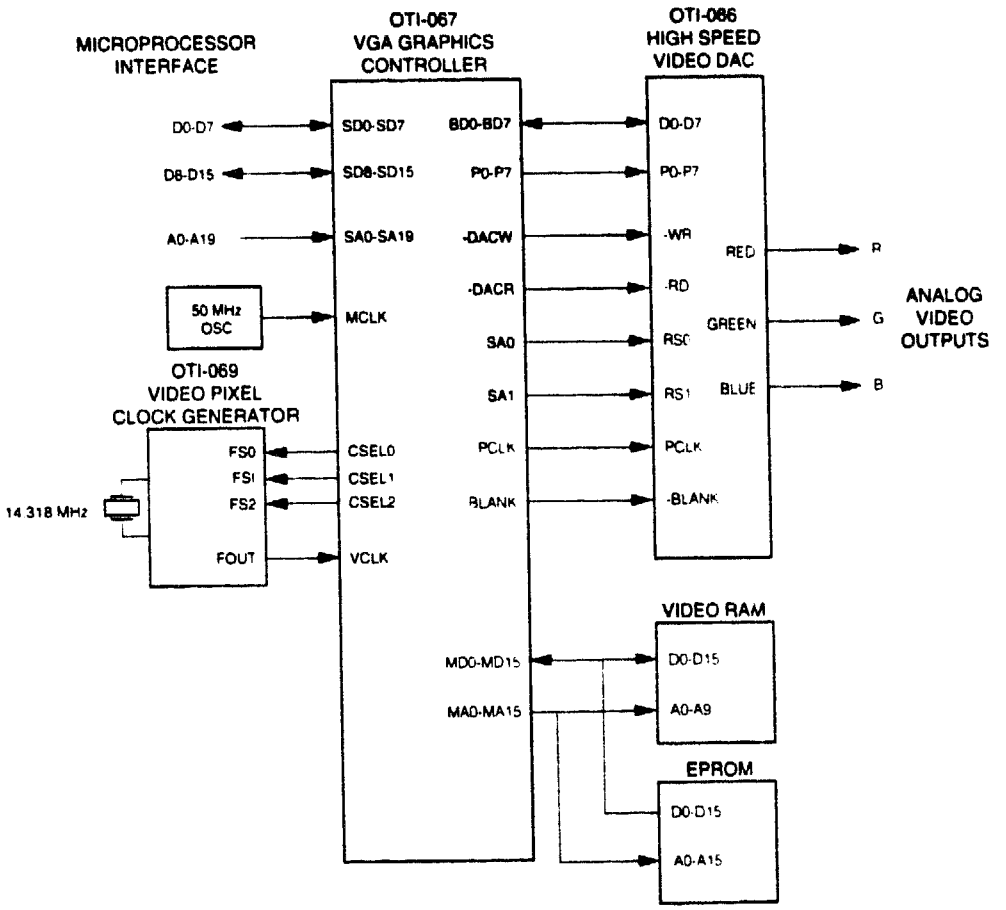


Figure 8-1. Video Controller Block Diagram

3.1 OTI-067 VGA Graphics Controller

The OTI-067 is a highly integrated, single chip Video Graphics Controller. Figure 8-2 shows a block diagram of the OTI-067. The following sections briefly describe the following major components.

- **CRT Controller (CRTC)**
- **Attribute Controller**
- **Graphics Controller**
- **Sequencer**
- **Memory Buffer**
- **Bus Interface**

3.1.1 CRT Controller

The CRTC generates horizontal and vertical timing signals, addresses for the dynamic RAM display buffer, and cursor and underline timing signals.

3.1.2 Attribute Controller

The attribute controller receives video memory data from the graphics controller and formats the data for display on the CRT. The attribute controller also controls blinking, underlining, cursor insertion, and pixel (bit) panning.

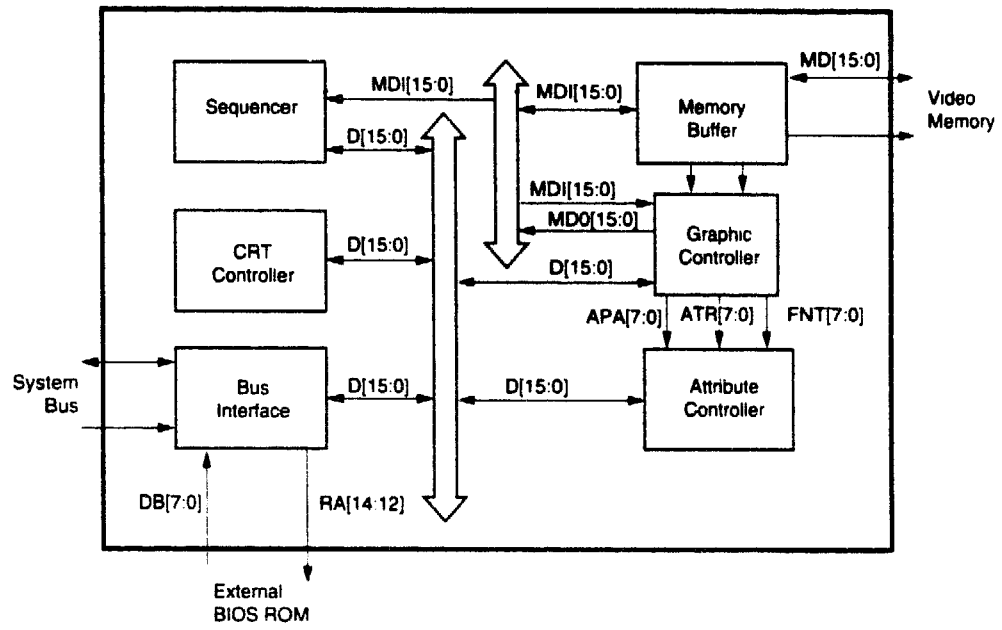


Figure 8-2. OTI-067 Block Diagram

3.1.3 Graphics Controller

The graphics controller handles the data flow between the display memory and the attribute controller during the active display period. Further it supports data flow between the host processor and the display memory. During the active display time, memory data is fetched from memory to fill the FIFO which is then used to supply data to the attribute controller as required. In APA (All-Points-Addressable) modes, sometimes referred to as graphics mode, parallel memory data is converted to serial bit-plane data before sending it to the attribute controller. In A/N modes, sometimes referred to as Alphanumeric mode, the parallel memory data is sent to the attribute controller without conversion. During video memory read or write operations, the graphics controller can perform logical operations on the parallel memory data.

8.1.4 Sequencer

The sequencer generates basic DRAM timing signals and all clock and reset signals. It also arbitrates access to video memory between the system microprocessor and the CRTC during active display intervals by inserting system microprocessor memory cycles between display memory cycles, and provides memory mapping of the video memory. Map mask registers can be used to protect entire memory maps from being altered.

8.1.5 Memory Buffer (FIFO)

The memory buffer or FIFO (First-In-First-Out) provides an interface between video memory and the Graphics Controller during active display time, which improves the system microprocessor video memory access bandwidth.

8.1.6 Bus Interface

The bus interface decodes memory addresses and I/O addresses to the video memory or VGA registers, generates all handshake signals to the system microprocessor, controls the backward-compatible logic (NMI), and controls the internal data bus.

8.2 OTI-066 Video DAC

The OTI-066 is a monolithic triple 6-bit video digital to analog converter (DAC) with 256 x 18 color palette for high-speed video applications. With this color palette, 256 color combinations out of 256K possible colors can be selected for display. A pixel mask is incorporated to allow for fast update of video information in a single cycle. The DAC on chip is capable of driving 75Ω or 37.5Ω standard loads at pixel rates of 65 MHz. All microprocessor interface I/O are TTL-compatible. Figure 8-3 shows a block diagram of the OTI-066 Video DAC.

An 8-bit value read on the Pixel Address inputs is used as a read address for the look-up table. This data is partitioned as three fields of 6 bits. Each field is applied to the inputs of a 6-bit DAC. An externally generated blank signal can be input to the OTI-066. This signal acts on all three of the analog outputs. The -BLANK signal is delayed internally so that it appears at the analog outputs with the correct relationship to the pixel stream. The contents of the look-up table are accessed via an 8-bit wide interface to the OTI-067. The use of an internal synchronizing circuit allows color value accesses to be totally asynchronous to the video path. A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the color look-up table to facilitate such operations as animation and flashing objects. The pixel mask register is directly in the pixel stream, thus operations on the contents of the mask register should be synchronized to the pixel stream. Pixel address and -BLANK inputs are sampled on the rising edge of the Pixel Clock. Their effect appears at the analog outputs after three further rising edges of the Pixel Clock (see Figure 8-4).

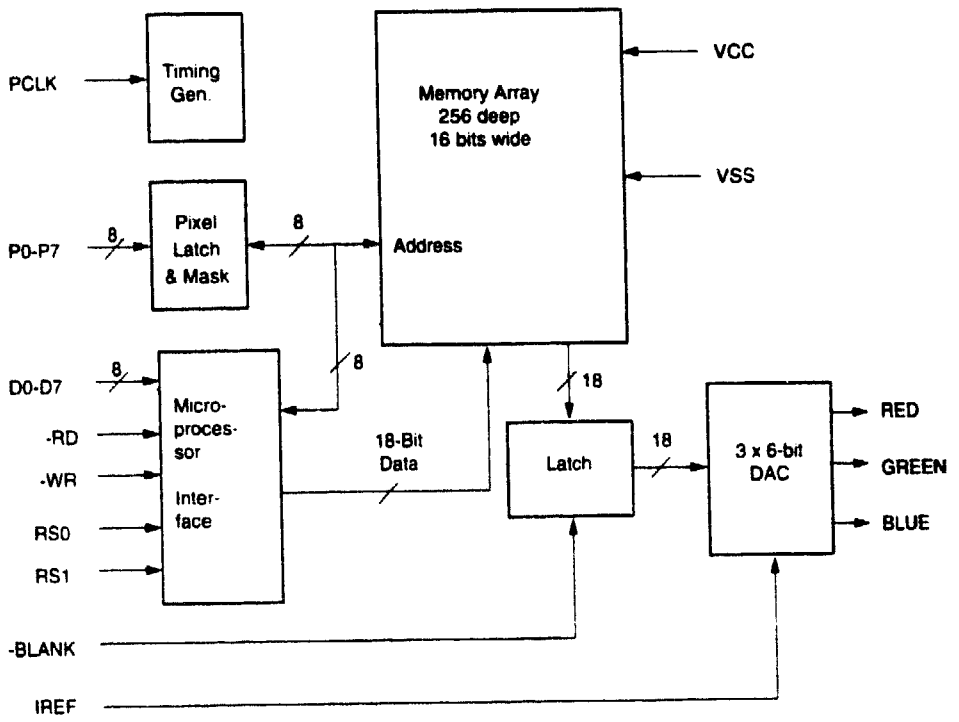


Figure 8-3. OTI-066 Block Diagram

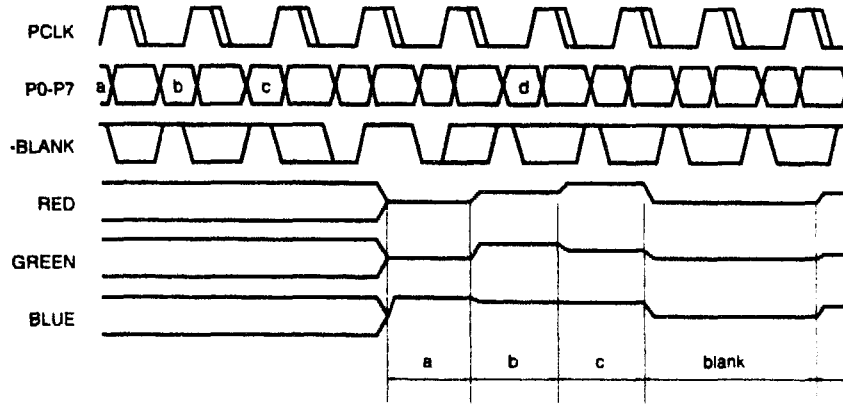


Figure 8-4 Video Path timing model

8.2.1 Analog Outputs

The outputs of the DACs are designed to be capable of producing 0.7-volt peak white amplitude with an IREF of 8.88 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output loading ($R_{effective}$) of 37.5Ω. The -BLANK input to the OTI-066 acts on all three of the analog outputs. When the -BLANK input is low, a binary zero is applied to the inputs of the DACs. The expression for calculating IREF with various peak white voltage/output loading combinations is:

$$IREF = \frac{V_{peak\ white}}{2.058 \times R_{effective}}$$

Note that for all values of IREF and output loading,

$$V_{BLACKLEVEL} = 0$$

8.2.2 Microprocessor Interface

There are three microprocessor interface registers accessed using RS0 and RS1 that control addressing, color value, and pixel masking features (Refer to Table 8-1).

Table 8-1. Microprocessor Interface Registers

RS1	RS0	Size (Bits)	Register
0	0	8	Address (write mode)
1	1	8	Address (read mode)
0	1	18	Color Value
1	0	8	Pixel Mask

8.2.2.1 Write-mode Address Register

To set a new color definition, a value specifying a location in the color look-up table is first written to the Write-mode Address register (RS0=0, RS1=0). The values for the red, green, and blue intensities are then written in succession to the Color Value register. After blue data is written to the Color Value register, the new color definition is transferred to the color look-up table. The Address register is automatically incremented. Since the Address register increments after each new color definition has been transferred from the Color Value register to the color look-up table, it is simple to write a set of consecutive locations with new color definitions. First, the start address of the set of locations is written to the write mode Address register. Then, the color definitions for each location are written sequentially to the Color Value register.

8.2.2.2 Read-mode Address Register

To read a color definition, a value specifying the location in the look-up table to be read is written to the Read-mode Address register. After this value has been written, the contents of the location specified are copied to the Color Value register. The Address register is automatically incremented. The red, green, and blue intensity values can be read by a sequence of three reads from the Color Value register. After the blue value has been read, the location in the look-up table currently specified by the Address register is copied to the Color Value register and then sequentially reading the color definitions for each location in the set Whenever the Address register is updated, any furnished color definition read or write is aborted and a new one may be begin.

3.2.2.3 Color Value Register

The Color Value register is internally an 18-bit wide register used as a buffer between the microprocessor interface and the color look-up table. A value can be read from or written to this register by a sequence of three-byte transfers at this register address. When a byte is written, only the least significant six bits (D0-D5) are used. When a byte is read, only the least significant six bits contain information. The most significant two bits will be zero. The sequence of data transfer is RED, GREEN, then BLUE. After writing three values to this register, its contents are written to the location in the color look-up table specified by the Address register. The Address register then increments. After reading three values from this register, the contents of the location in the color look-up table specified by the Address register are copied into the Color Value register. The Address register then increments. Each transfer between the Color Value register and the color look-up table replaces the normal pixel mapping operation of the OTI-066 for a single pixel.

3.2.2.4 Pixel Mask Register

The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0-P7). A '1' in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered. A '0' sets the corresponding bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the look-up table is being accessed through that same interface.

8.2.2.5 Microprocessor Interface Timing Specifications

Table 8-2 shows the microprocessor interface timing specifications. See Figure 8-5 through 8-13 for the timing models.

Table 8-2. Microprocessor Interface Timing Specifications

Symbol	Parameter	Max.	Min	Units	Notes
tWLWH	-WR pulse width low		50	nS	
tRLRH	-RD pulse width low		50	nS	
tSVWL	Register select set-up time		10	nS	
tSVRL	Register select set-up time		10	nS	
tWLSX	Register select hold time		10	nS	
tRLSX	Register select hold time		10	nS	
tDVWH	Write data set-up time	15	10	nS	
tWHDX	Write data hold time	15	10	nS	
tRLQX	Output turn-on delay	5	5	nS	
tRLQV	Read enable access time	40		nS	
tRHQX	Output hold time		5	nS	
tRHQZ	Output turn-off delay	20		nS	1
tWHWL1	Successive write interval		4τ	ns	3
tWHRL1	Write followed by read interval		4τ	nS	3
tRHRL1	Successive read interval		4τ	nS	3
tRHWL1	Read followed by write interval		4τ	nS	3
tWHWL2	Write after color write		4τ	nS	2, 3
tWHRL2	Read after color write		4τ	nS	2, 3
tRHRL2	Read after color read		7τ	nS	2, 3
tRHWL2	Write after color read		7τ	nS	2, 3
tWHRL3	Read after read address write		7τ	nS	2, 3
	Write/Read enable transition time	50		nS	

NOTES:

1. **Measure 200 mV from steady state output voltage.**

2. **This parameter allows for synchronization between operations on the microprocessor interface and the pixel stream being processed by the color look-up table.**

3. **τ = PCLK period (tCHCH)**

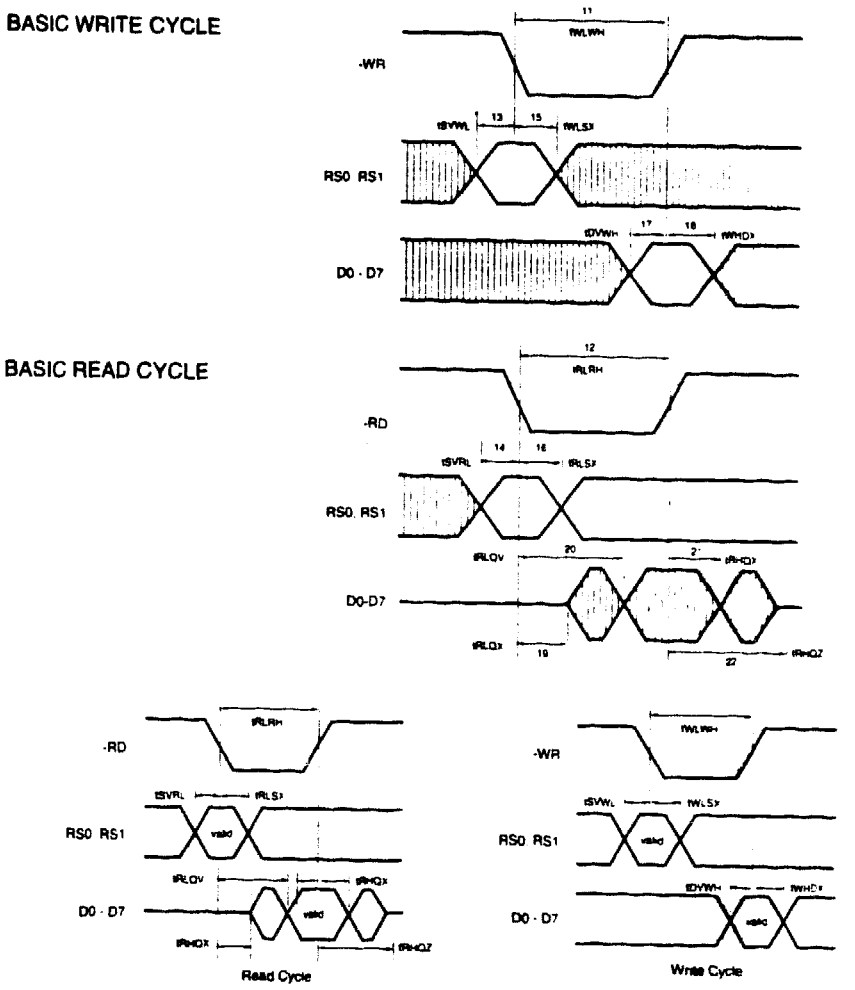


Figure 8-5. Microprocessor Interface Timing Model I

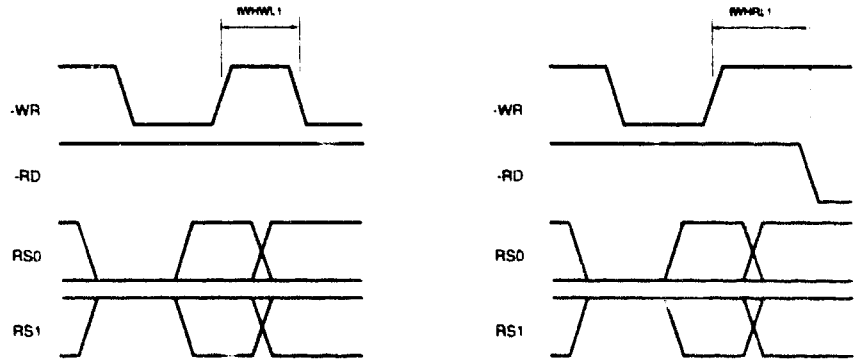


Figure 8-6. Microprocessor Interface Timing Model II

Read from:
a) pixel mask register
b) pixel address register (read mode)
c) pedel address register (write mode)

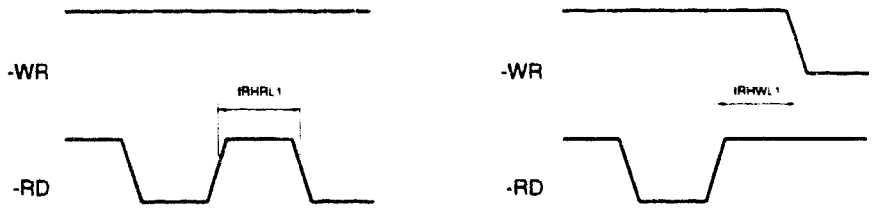


Figure 8-7. Microprocessor Interface Timing Model III

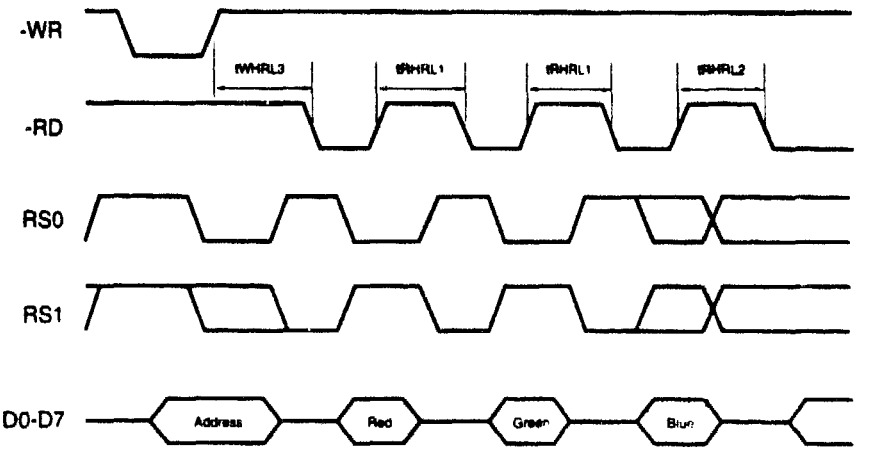


Figure 8-8. Microprocessor Interface Timing Model IV

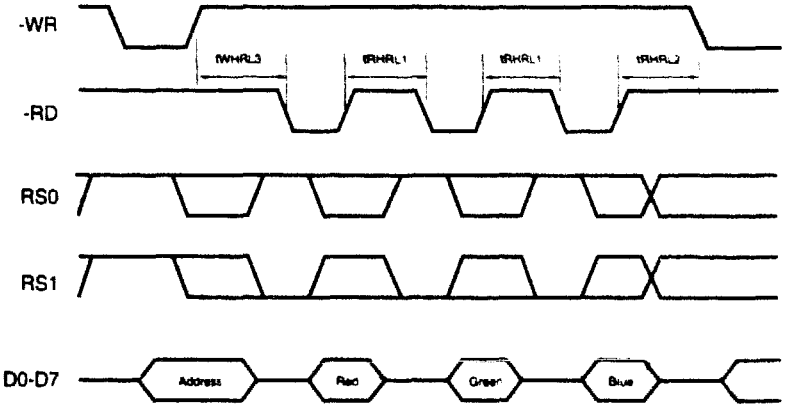


Figure 8-9. Microprocessor Interface Timing Model V

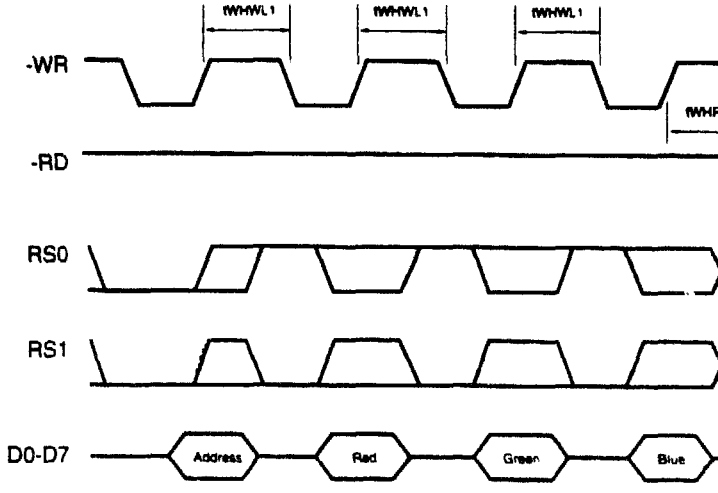


Figure 8-10. Microprocessor Interface Timing Mod

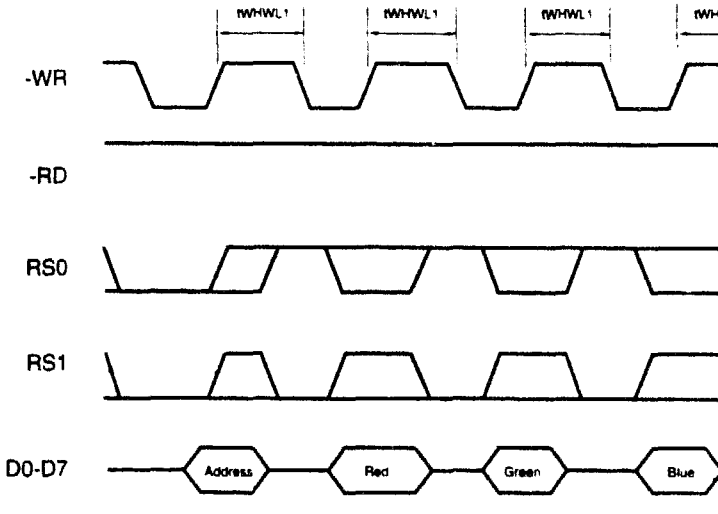
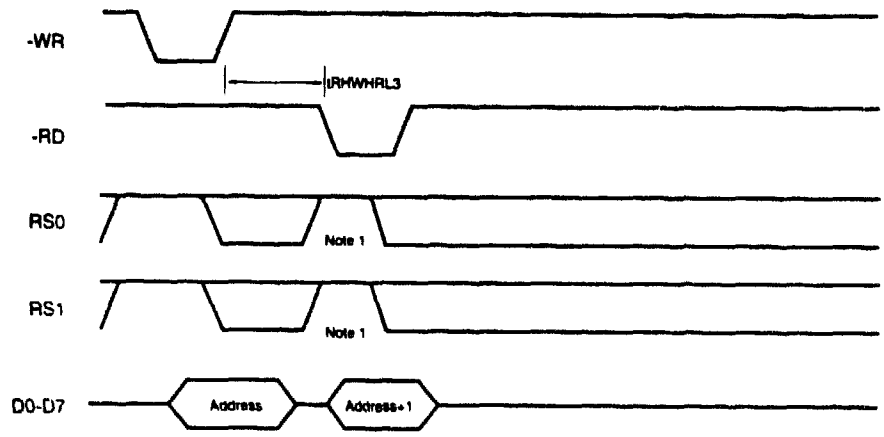
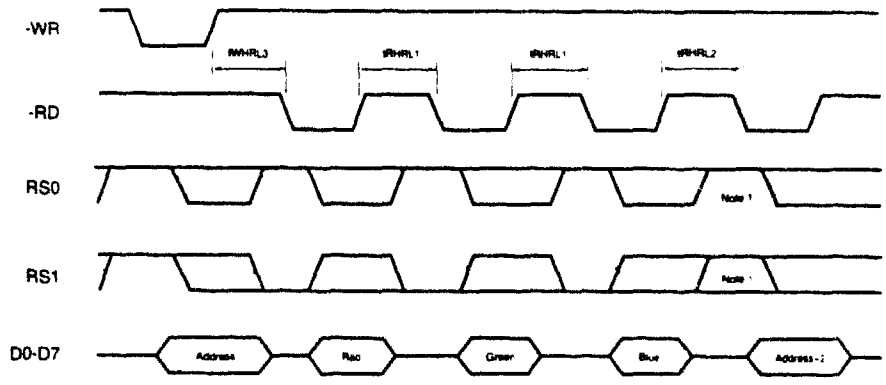


Figure 8-11. Microprocessor Interface Timing Mod



Note 1: The timing for reading from address 0,0 is identical to that for reading from address 1,1

Figure 8-12. Microprocessor Interface Timing Model VIII



Note 1 The timing for reading from address 0,0 is identical to that for reading from address 1,1

Figure 8-13. Microprocessor Interface Timing Model IX

8.3 OTI-069 Video Pixel Clock Generator

The OTI-069 Pixel Clock Generator is an integrated circuit specifically designed for generating the video pixel frequencies required by OTI-067. Phase-locked-loop circuitry permits rapid, glitch-free transitions between clock frequencies. A 14.31818 MHz series-resonant crystal with no additional external components is all that is required for generating the video pixel frequencies. A 6 MHz bandwidth CMOS op-amp, included in the device, permits fast frequency acquisition and decreases phase jitter and susceptibility to externally generated noise. Figure 8-14 shows a block diagram of the OTI-069 Video Pixel Clock Generator.

On-Chip features include:

- **Advanced PLL-low phase jitter**
- **High frequency operation for extended video modes**
- **Fast acquisition of selected frequencies**

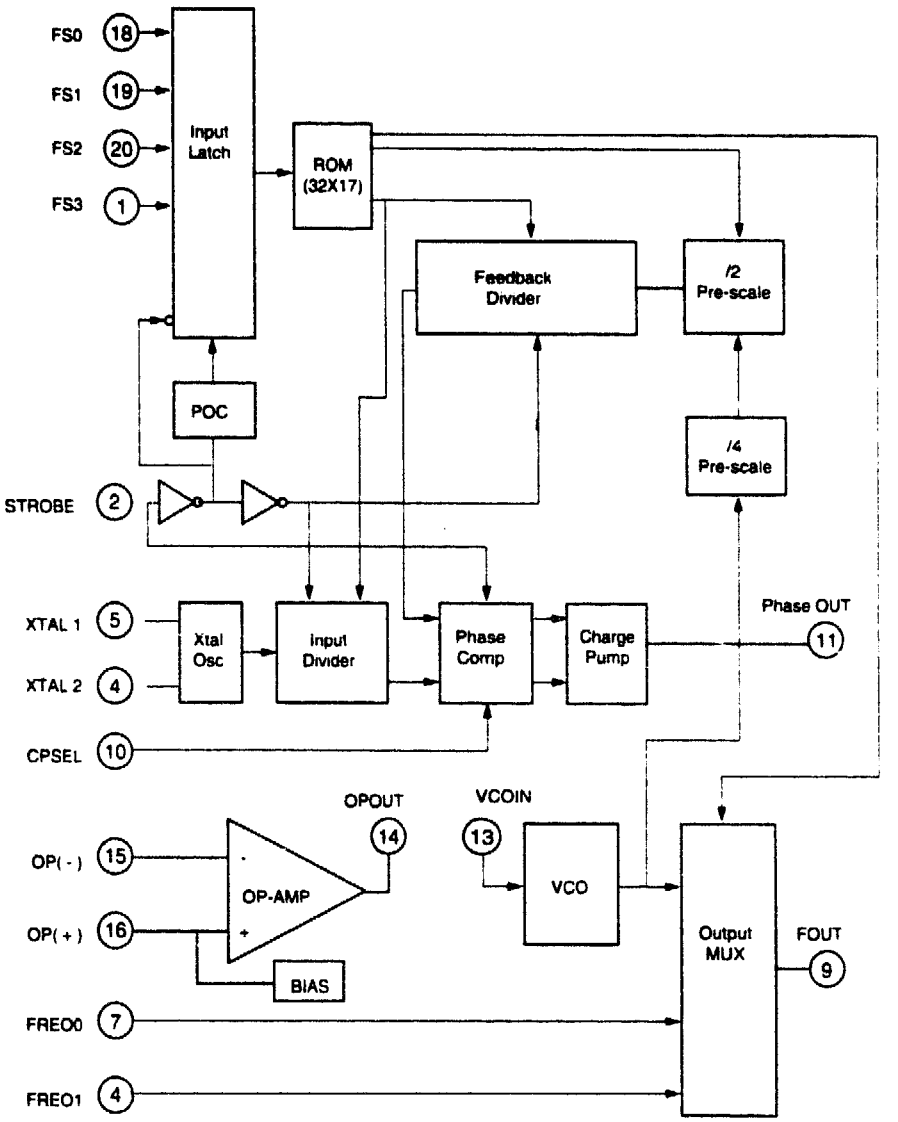


Figure 8-14. OTI-069 Video Pixel Clock Generator Block Diagram

8.4 Video BIOS EPROM

The OTI-067 provides the necessary control and decodes to support a 16 or 8 bit BIOS ROM data path. In 8-bit BIOS ROM mode, the video memory and I/O space is still accessed in 16-bit mode. If set for 16-bit BIOS ROM mode, the internal circuitry will automatically detect whether the adapter is interfaced to an 8 or 16 bit PC bus. Upon Power-up reset, the ROM paging feature is enabled by reading the preset configuration into the configuration register.

8.5 Video RAM

The OTI-067 supports 256Kx4 DRAM in all modes. It supports 512 KBytes of DRAM by using four 256Kx4 DRAM chips. The OTI-067 provides all the necessary control signals and address/data lines to access the video memory in page mode. For a 45 MHz memory clock, DRAMS with an access speed of 80 ns are required, 70ns DRAMs are required for a 50 MHz memory clock. In extended modes with 256 colors, the video memory is organized in a packed pixel mode; 1 byte from 1 plane as a pixel. This requires programming of an OTI extended register. For 16 color extended modes, the video memory is organized as planar mode (1 bit from each of 4 planes).

8-6 VGA Compatible Registers

The following sections describe the VGA Compatible registers. Table 8-3 lists the register I/O address the I/O function required to access the register.

Table 8-3. VGA Compatible Register Address Map

Address		I/O Function	Register	Index
Mono Port	**Color Port**			
3CCh/3C2h	3CCh/3C2h	Read/Write	Miscellaneous Output	-
3C2h	3C2h	Read	Input Status 0	-
3BAh	3DAh	Read	Input Status 1	-
3CAh/3BAh	3CAh/3BAh	Read/Write	Feature Control	-
3C7h	3C7h	Read	DAC	-
3C4h	3C4h	Read/Write	Sequencer Address	-
3C5h	3C5h	Read/Write	Reset	00h
3C5h	3C5h	Read/Write	Clocking Mode	01h
3C5h	3C5h	Read/Write	MAP Mask	02h
3C5h	3C5h	Read/Write	Character Map Select	03h
3C5h	3C5h	Read/Write	Memory Mode	04h
3CEh	3CEh	Read/Write	Graphics Address	-
3CFh	3CFh	Read/Write	Set/Reset	00h
3CFh	3CFh	Read/Write	Enable Set/Reset	01h
3CFh	3CFh	Read/Write	Color Compare	02h
3CFh	3CFh	Read/Write	Data Rotate	03h
3CFh	3CFh	Read/Write	Read Map Select	04h
3CFh	3CFh	Read/Write	Graphics Mode	05h
3CFh	3CFh	Read/Write	Graphics Misc	06h
3CFh	3CFh	Read/Write	Color Don't Care	07h
3CFh	3CFh	Read/Write	Bit Mask	08h

Table 8-3. (Cont.) VGA Compatible Register Address Map

Address		I/O Function	Register	Index
Mono Port	Color Port			
3C0h	3C0h	Read/Write	Attribute Address	-
3C0h	3C0h	Read/Write	Color Palette Register 0-15	00-0Fh
3C0h	3C0h	Read/Write	Mode Control	10h
3C0h	3C0h	Read/Write	Overscan Color	11h
3C0h	3C0h	Read/Write	Color Plane Enable	12h
3C0h	3C0h	Read/Write	Horizontal Pixel Panning	13h
3C0h	3C0h	Read/Write	Color Select	14h
3B4h	3D4h	Read/Write	CRTC Address	-
3B5h	3D5h	Read/Write	Horizontal Total	00h
3B5h	3D5h	Read/Write	Horizontal Display Enable End	01h
3B5h	3D5h	Read/Write	Start Horizontal Blanking	02h
3B5h	3D5h	Read/Write	End Horizontal Blanking	03h
3B5h	3D5h	Read/Write	Start Horizontal Retrace Pulse	04h
3B5h	3D5h	Read/Write	End Horizontal Retrace	05h
3B5h	3D5h	Read/Write	Vertical Total	06h
3B5h	3D5h	Read/Write	Overflow	07h
3B5h	3D5h	Read/Write	Preset Row Scan	08h
3B5h	3D5h	Read/Write	Maximum Scan Line	09h
3B5h	3D5h	Read/Write	Cursor Start	0Ah
3B5h	3D5h	Read/Write	Cursor End	0Bh
3B5h	3D5h	Read/Write	Start Address High	0Ch
3B5h	3D5h	Read/Write	Start Address Low	0Dh
3B5h	3D5h	Read/Write	Cursor Location High	0Eh
3B5h	3D5h	Read/Write	Cursor Location Low	0Fh
3B5h	3D5h	Write	Vertical Retrace Start	10h
3B5h	3D5h	Write	Vertical Retrace End	11h

Table 8-3. (Cont.) VGA Compatible Register Address Map

Address		I/O Function	Register	Index
Mono Port	Color Port			
3B5h	3D5h	Read/Write	Vertical Display Enable End	12h
3B5h	3D5h	Read/Write	Offset	13h
3B5h	3D5h	Read/Write	Underline Location	14h
3B5h	3D5h	Read/Write	Start Vertical Blanking	15h
3B5h	3D5h	Read/Write	End Vertical Blanking	16h
3B5h	3D5h	Read/Write	CRTC Mode Control	17h
3B5h	3D5h	Read/Write	Line Compare	18h
3B5h	3D5h	Read	Readback CRT Latches	22h

8.6.1 General Registers

General registers control miscellaneous output, input status, feature, DAC operations in VGA compatible mode. The bit definitions for these registers are listed in Table 8-4 through 8-8.

8.6.1.1 Miscellaneous Output Register

Table 8-4. Miscellaneous Output Register Bit Assignment

Bit	Function
7	Vertical Sync Polarity 0 = Positive Vertical Retrace 1 = Negative Vertical Retrace
6	Horizontal Sync Polarity 0 = Positive Vertical Retrace 1 = Negative Vertical Retrace
5	Page Bit For Odd/Even 0 = Low 64K page of memory 1 = High 64K page of memory
4	0 = Reserved
3:2	Clock Select - These two bits, CSEL0 and CSEL1, are used with 3DF index D bit 5 as follows:

CSEL2	CSEL1	CSEL0	CLOCK
0	0	0	25.175 Mhz
0	0	1	28.322 Mhz
0	1	0	65 Mhz
0	1	1	44.9 Mhz
1	0	0	14.161Mhz (derived from 28.322)
1	0	1	18 Mhz (derived from 36 Mhz)
1	1	0	40 Mhz
1	1	1	36 Mhz

Table 8-4. (Cont.) Miscellaneous Output Register Bit Assignment

Bit	Function
1	Enable RAM 0 = Disable Video RAM address decode from the system microprocessor 1 = Enable Video RAM to the system microprocessor
0	Input/Output Address Select 0 = Monochrome emulation with CRTC addresses set to 3Bxh, Input Status 1 register set to 3BAh 1 = Color emulation with CRTC addresses set to 3Dxh, Input Status 1 register set to 3DAh

8.6.1.2 Input Status 0 Register

Table 8-5. Input Status 0 Register Bit Assignment

Bit	Function
7	CRT Interrupt 0 = Vertical retrace interrupt is pending 1 = Vertical retrace interrupt is cleared
6:5	Reserved
4	Switch Sense 0 = Selected sense switch is off or 0 1 = Vertical retrace interrupt is on or 1
3:0	Reserved

8.6.1.3 Input Status 1 Register

Table 8-6. Input Status 1 Register Bit Assignment

Bit	Function
7:6	Reserved
5:4	Diagnostic Usage - Reports the status of two of the eight VGA attribute controller outputs. The values set into the Video Status MUX field of the Color Plane Enable Register determine which colors are input to these two diagnostic bits.

Color Plane Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

3	Vertical Retrace 0 = Video information is being displayed 1 = A vertical retrace interval is in progress
2:1	Reserved
0	Display Enable 0 = The display of video data is enabled 1 = The display is in horizontal or vertical retrace mode

8.6.1.4 Feature Control Register

Table 8-7. Feature Control Register Bit Assignment

Bit	Function
7:4	Reserved
3	Vertical Sync Select 0 = This bit should always be set to 0 to enable normal vertical sync output to the monitor 1 = The vertical sync output is the logical OR of vertical sync and vertical display enable
2:0	Reserved

8.6.1.5 DAC Registers

Table 8-8. DAC Registers Address Map

Port	Read/Write	Register
3C6h	Read/Write	PEL Mask
3C7h	Read	DAC State Register
3C7h	Write	PEL Address (Read Mode)
3C8h	Read/Write	PEL Address (Write Mode)
3C9h	Read/Write	PEL Data Register

8.6.2 Sequencer Registers

Sequencer registers control sequencer address reset, clocking
plane mask, character map select and memory mode operation
compatible mode. The bit definitions for these registers are liste
8-9 through 8-15.

8.6.2.1 Sequencer Address Register

This register is a pointer register located at address 3C4h. It is
with a binary value that points to the Sequencer Data register wh
is to be written. This value is referred to as the index.

Table 8-9. Sequencer Address Register Bit Assignme

Bit	Function
7:3	Reserved
2:0	Sequencer Address - A binary value pointing to th where data is to be read or written.

.6.2.2 Reset Register

This is a read/write register pointed to when the value in the Sequencer Address register is 00h .

Table 8-10. Reset Register Bit Assignment

Bit	Function
7:2	Reserved
1	Synchronous Reset 0 = Synchronous clear and halt the sequencer 1 = Bit 1 and 0 must be 1 to allow the sequencer to operate
0	Asynchronous Reset 0 = Asynchronous clear and halt the sequencer. This may cause data loss in the dynamic RAMs 1 = Bit 1 and 0 must be 1 to allow the sequencer to operate

8.6.2.3 Clocking Mode Register

This is a read/write register pointed to when the value in the Sequencer Address register is 01h .

Table 8-11. Clocking Mode Register Bit Assignment

Bit	Function
7:6	Reserved
5	Screen Off 0 = Normal screen operation 1 = Turns off the video screen and assigns the maximum memory bandwidth to the system CPU
4	Shift 4 0 = The video serializers are reloaded every character clock 1 = The serializers are loaded every fourth character clock. This is useful when 32 bits are fetched per cycle and chained together in the shift registers
3	Dot Clock 0 = Select normal dot clocks derived from the sequencer master clock input 1 = The master clock will be divided by 2 to generate the dot clock. This is used for 320 and 360 horizontal PEL modes
2	Shift Load 0 = If bit 4 is set to 0, also, the video serializers are reloaded every character clock 1 = The video serializers are reloaded every other character clock, this mode is useful when 16 bits are fetched per cycle and chained together in the shift load registers
1	Reserved

Table 8-11. (Cont.) Clocking Mode Register Bit Assignment

Bit	Function
0	8/9 dot Clocks - The 9 dot mode is for Alphanumeric modes only. The ninth dot equals the eighth dot for ASCII codes C0 through DF hex. Also, see the Line Graphics Character Code bit in the Attribute Mode Control register section. 0 = Directs the sequencer to generate nine dot wide character clocks 1 = Generate eight dot wide character clocks

8.6.2.4 MAP Mask Register

This is read/write register pointed to when the value in the Sequencer Address register is 02h.

Table 8-12. Map Mask Register Bit Assignment

Bit	Function
7:4	Reserved
3:0	Map Mask - For odd/even modes, maps 0 and 1, and maps 2 ad 3 should have the same map mask value. When chain 4 mode is selected, all maps should be enabled. This is a read-modify-write operation. 0 = Disable memory write to the corresponding map 1 = Enables the system to write to the corresponding map. If all four bits are set to 1, the system CPU can perform a 32-bit operation with only one memory cycle

8.6.2.5 Character Map Select Register

This is a read/write register pointed to when the value in the Sequencer Address register is 03h.

Table 8-13. Character Map Select Register Bit Assignment

Bit	Function
7:6	Reserved
5	Character Map Select High Bit A
4	Character Map Select High Bit B
3:2	Character Map Select A

Bit 5	Bit 3	Bit 2	Map	Table Location
0	0	0	0	1st 8k of Map 2
0	0	1	1	3rd 8k of Map 2
0	1	0	2	5th 8k of Map 2
0	1	1	3	7th 8k of Map 2
1	0	0	4	2nd 8k of Map 2
1	0	1	5	4th 8k of Map 2
1	1	0	6	6th 8k of Map 2
1	1	1	7	8th 8k of Map 2

1:0 Character Map Select B

Bit 4	Bit 1	Bit 0	Map	Table Location
0	0	0	0	1st 8k of Map 2
0	0	1	1	3rd 8k of Map 2
0	1	0	2	5th 8k of Map 2
0	1	1	3	7th 8k of Map 2
1	0	0	4	2nd 8k of Map 2
1	0	1	5	4th 8k of Map 2
1	1	0	6	6th 8k of Map 2
1	1	1	7	8th 8k of Map 2

.6.2.6 Memory Mode Register

This is a read/write register pointed to when the value in the Sequencer Address register is 04h.

Table 8-14. Memory Mode Register Bit Assignment

Bit	Function
7:4	Reserved
3	Chain 4 0 = If bit 2 is set to 1, this bit enables the system CPU to address data sequentially within a bit map by use of the Map Mask register 1 = Causes two low-order address bits to select the map that will be accessed as follows: **A1** **A0** **Map Selected** 0 0 0 0 1 1 1 0 2 1 1 3
2	Odd/Even 0 = Directs even CPU addresses to access maps 0 and 2, and odd CPU addresses to access maps 1 and 3 1 = If bit 3 is set to 0, this bit causes system CPU Addresses to sequentially address data within a bit map
1	Extended Memory 0 = No extended memory present. Display memory is less than 64 Kbytes 1 = Extended memory is present. Display memory is greater than 64 Kbytes. If set to 1 the VGA is permitted to use the 256k bytes of video memory. This also enables character map selection
0	Reserved

8.6.3 Graphics Controller Registers

Graphics Controller registers control graphics set/rest, color compare, data rotate, read map select, and bit mask operations in VGA compatible mode. The bit definitions for these registers are listed in Table 8-15 through 8-24.

8.6.3.1 Graphics Address Register

Table 8-15. Graphics Address Register Bit Assignment

Bit	Function
7:4	Reserved
3:0	Graphics Address Bits - These bits are used to point to the other registers in the graphics section.

8.6.3.2 Set/Reset Register

Table 8-16. Set/Rest Register Bit Assignment

Bit	Function
7:4	Reserved
3:0	This field represents the value written to all 8 bit of the respective memory map when the system CPU does a memory write with write mode 0 selected and Set/Reset mode is enabled for the corresponding map. However, in write mode 3, enable Set/Reset register has no effect.

.6.3.3 Enable Set/Reset Register

Table 8-17. Enable Set/Reset Register Bit Assignment

Bit	Function
7:4	Reserved
3:0	Enable Set/Reset 0 = If write mode is 0 and Set/Reset is not enabled on a map, that map is written with the value of the system CPU 1 = If write mode is 0 and Set/Reset is enabled on a map, the respective memory is written with the value of the Set/Reset register

6.3.4 Color Compare Register

Table 8-18. Color Compare Register Bit Assignment

Bit	Function
7:4	Reserved
3:0	4-bit color value to be compared

8.6.3.5 Data Rotate Register

Table 8-19. Data Rotate Register Bit Assignment

Bit	Function
7:5	Reserved
4:3	Function Select **Bit 4** **Bit 3** **Function** 0 0 Data unmodified 0 1 Data ANDed with latch data 1 0 Data ORed with latch data 1 1 Data XORed with latch data
2:0	Rotate Count - This field represents a binary encoded value of the number of positions to right-rotate the system CPU data bus during system CPU memory writes. This rotation occurs before any other logical operation on the data takes place. This operation is done when write mode is 0. To write non-rotated data the system CPU must select a count of 0.

8.6.3.6 Read Map Select Register

Table 8-20. Read Map Select Register Bit Assignment

Bit	Function
7:2	Reserved
1:0	Map Select - This field represents a binary encoded value of the memory map number from which the system CPU reads data. This register has no effect on the color compare read mode. In odd/even modes the value may be 00 or 01 (10 or 11) for chained maps 0,1 (2,3).

8.6.3.7 Graphics Mode Register

Table 8-21. Graphics Mode Register Bit Assignment

Bit	Function
7	Reserved
6	256 Color Mode 0 = Allows bit 5 to control the loading of the Shift registers 1 = Causes the Shift register to be loaded in a manner that supports the 256-color mode
5	Shift Register
4	Odd/Even 0 = Normal VGA mode 1 = Selects the odd/even addressing mode used to emulate the IBM CGA compatible modes
3	Read Type 0 = The system microprocessor reads data from the memory map selected by the Read Map Select register. Read Map Select register has no effect if bit 3 of the Sequencer Memory Mode register equals 1. Bit 0 of the Read Map Select register has no effect if bit 4 of the Graphic Mode register equals 1. 1 = The system microprocessor reads the results of the comparison of the 4 memory maps and the Color Compare register.
2	Reserved

Table 8-21. (Cont.) Graphics Mode Register Bit Assignment

Bit	Function		
1:0	Write Mode		
	Bit 1	**Bit 0**	**Function**
	0	0	Each memory map is written with the system CPU data rotated by the number of counts in the Rotated register, unless Set/Reset is enabled for the map. Maps for which Set/Reset is enabled are written with 8-bits of the value contained in the Set/Reset register for that map.
	0	1	Each memory map is written with the contents of the system CPU latches. These latches are loaded by a system CPU Read operation.
	1	0	Memory map n (0-3) is filled with 8-bits of the value of data bit n.
	1	1	Each map is written with 8-bits of the value contained in the Set/Reset register for that map (Enable Set/Reset register has no effect). Rotated system CPU data is ANDed with the Bit Mask register data to form an 8-bit value that performs the same function as the Bit Mask register does in write modes 0 and 2

8.6.3.8 Miscellaneous Register

Table 8-22. Miscellaneous Register Bit Assignment

Bit	Function
7:4	Reserved
3:2	Memory Map **Bit 3** **Bit 2** **Function** 0 0 Hex A0000 for 128K bytes 0 1 Hex A0000 for 64K bytes 1 0 Hex B0000 for 32K bytes 1 1 Hex B8000 for 32K bytes
1	Odd/Even 0 = Standard VGA addressing 1 = Replace system CPU address bit 0 with a higher-order address bit and select odd/even maps with odd/even values of the system CPU A0 bit, respectively
0	Graphics Mode 0 = Selects text mode operation 1 = Selects graphics mode. When this mode is selected, the character generator address latches are disabled

8.6.3.9 Color Don't Care Register

Table 8-23. Color Don't Care Register Bit Assignment

Bit	Function
7:4	Reserved
3	Map 3 0 = Don't participate in the color compare cycle 1 = Participate in the color compare cycle
2	Map 2 0 = Don't participate in the color compare cycle 1 = Participate in the color compare cycle
1	Map 1 0 = Don't participate in the color compare cycle 1 = Participate in the color compare cycle
0	Map 0 0 = Don't participate in the color compare cycle 1 = Participate in the color compare cycle

8.6.3.10 Bit Mask Register

Table 8-24. Bit Mask Register Bit Assignment

Bit	Function
7:0	Bit Mask 0 = Any bit set to 0 causes the corresponding bit n in each map to be immune to change, provided that the location being written was the last location read by the system CPU 1 = Bits set to 1 allow unimpeded writes to the corresponding bits in the maps

8.6.4 Attribute Controller Registers

Attribute Controller registers control color palette, overscan, color plane enable, horizontal pixel panning and color select operations in VGA compatible mode. The bit definitions for these registers are listed in Table 8-25 through 8-31.

8.6.4.1 Attribute Address Register

Table 8-25. Attribute Address Register Bit Assignment

Bit	Function
7:6	Reserved
5	Palette Address Source
4:0	Attribute Address

8.6.4.2 Palette Registers 0 - 15

Table 8-26. Palette Registers 0-15 Bit Assignment

Bit	Function
7:6	Reserved
5:0	Palette

8.6.4.3 Attribute Mode Control Register

Table 8-27. Attribute Mode Control Register Bit Assig

Bit	Function
7	P5,P4 Select 0 = P5 and P4 are the outputs of the Palette reg 1 = P5 and P4 are bits 1 and 0 of the Color Sel
6	PEL Width 0 = All modes except for mode 13 hex 1 = The video pipeline is sampled so that 8-bit able to select a color in the 256-color mod
5	PEL Panning Compatibility 0 = Line compare has no effect on the output c Panning register 1 = A successful line compare in the CRT cont the output of the PEL Panning registers to +VSYNC occurs, at which time the output programmed value. This bit allows a selec the screen to be panned
4	Reserved
3	Enable Blink/Select Background Intensity 0 = Selects the background intensity of the att which was available on the Monochrome a adapters 1 = Enables the blink attribute in text modes a graphics modes

Table 8-27. (Cont.) Attribute Mode Control Register Bit Assignment

Bit	Function
2	Enable line Graphics Character Codes 0 = The ninth dot will be the same as the background 1 = Enables the special line graphics character codes for Monochrome emulation mode. When enabled, this bit forces the ninth dot of a line graphic character to be identical to the eighth dot of the character. The line graphics character modes for the Monochrome emulation mode are C0 hex through DF hex. For character fonts that do not use the line graphics character codes this range, bit 2 should be set to 0. Otherwise, unwanted video information will be displayed on the CRT screen
1	Mono Emulation 0 = Color emulation mode is set 1 = Monochrome emulation mode is set
0	Graphics/Alphanumeric Mode 0 = Selects alphanumeric mode 1 = Selects graphics mode

8.6.4.4 Overscan Color Register

Table 8-28. Overscan Color Register Bit Assignment

Bit	Function
7:0	Overscan Color

8.6.4.5 Color Plane Enable Register

Table 8-29. Color Plane Enable Register Bit Assignme

Bit	Function			
7:6	Reserved			
5:4	Video Status MUX			
	Color Plane Register		**Input Status Register**	
	Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
	0	0	P2	P0
	0	1	P5	P4
	1	0	P3	P1
	1	1	P7	P6
3:0	Enable Color Plane			

3.6.4.6 Horizontal PEL Panning Register

Table 8-30. Horizontal PEL Panning Register Bit Assignment

Bit	Function
7:4	Reserved
3:0	Horizontal PEL Panning - This register selects the number of picture elements (PELs) to shift the video data horizontally to the left. PEL panning is available in both graphics and text modes. In monochrome emulation text modes and modes 0+, 1+, 2+, 3+, the image can be shifted a maximum of 8 PELs. Mode 13 allows a maximum shift of 3 PELs. Programming 1,3,5, or 7 into the PEL Panning register during mode 13 will cause a color change on the display. All other modes, the image can be shifted a maximum of 7 PELs. The sequence for shifting the image is as follows:

PEL Panning Register Value	Number of PELs Shifted to the left 0+,1+,2+,3+,7,7+	All Other modes	Mode 13
0	1	0	0
1	2	1	-
2	3	2	1
3	4	3	-
4	5	4	2
5	6	5	-
6	7	6	3
7	8	7	-
8	0	-	-

8.6.4.7 Color Select Register

Table 8-31. Color Select Register Bit Assignment

Bit	Function
7:4	Reserved
3:2	S_color 7,6
1:0	S_color 5,4

8.6.5 CRT Controller Registers

8.6.5.1 CRT Controller Address Register

This register is a pointer register located at 3B4h for Monochrome emulation modes or 3D4h for Color emulation modes depending on bit 0 of the Miscellaneous output register at address 3C2h. The CRT Controller Addresses register is loaded with a binary value, or index, that points to the CRT Controller Data register where data is to be written. All CRT controller registers are read/write registers.

Table 8-32. CRT Controller Address Register Bit Assignment

Bit	Function
7:6	Reserved
5	Test
4:0	CRT Controller Address

.6.5.2 Horizontal Total Register

Table 8-33. Horizontal Total Register Bit Assignment

Bit	Function
7:0	Horizontal Total

.6.5.3 Horizontal Display Enable End Register

Table 8-34. Horizontal Display Enable End Register Bit Assignment

Bit	Function
7:0	Horizontal Display Enable End

.6.5.4 Start Horizontal Blanking Register

Table 8-35. Start Horizontal Blanking Register Bit Assignment

Bit	Function
7:0	Start Horizontal Blanking

8.6.5.5 End Horizontal Blanking Register

This register determines when the horizontal blanking output signal becomes inactive.

Table 8-36. End Horizontal Blanking Register Bit Assignment

Bit	Function		
7	Test		
6:5	Display Enable		
	Bit 6	**Bit 5**	**Skew**
	0	0	Zero character clock skew
	0	1	One character clock skew
	1	0	Two character clock skew
	1	1	Three character clock skew
4:0	End Horizontal Blanking		

8.6.5.6 Start Horizontal Retrace Pulse Register

Table 8-37. Start Horizontal Retrace Pulse Register Bit Assignment

Bit	Function
7:0	Start Horizontal Retrace Pulse

.6.5.7 End Horizontal Retrace Register

This register specifies the character position at which the Horizontal Retrace Pulse becomes inactive.

Table 8-38. End Horizontal Retrace Register Bit Assignment

Bit	Function		
7	End Horizontal Blanking		
6:5	Horizontal Retrace Delay		
	Bit 6	**Bit 5**	**Amount of Skew**
	0	0	Zero skew
	0	1	One skew
	1	0	Two skew
	1	1	Three skew
4:0	End Horizontal Retrace		

6.5.8 Vertical Total Register

Table 8-39. Vertical Total Register Bit Assignment

Bit	Function
7:0	Vertical Total

8.6.5.9 CRT Controller Overflow Register

Table 8-40. CRT Controller Overflow Register Bit Assignment

Bit	Function
7	Vertical Retracer Start
6	Vertical Display Enable END
5	Vertical Total
4	Line Compare
3	Start Vertical Blank
2	Vertical Retrace Start
1	Vertical Display
0	Vertical Total

8.6.5.10 Preset Row Scan Register

Table 8-41. Preset Row Scan Register Bit Assignment

Bit	Function
7	Reserved
6:5	Byte Panning Control
4:0	Preset Row Scan (PEL Scrolling)

8.6.5.11 Maximum Scan Line Register

Table 8-42. Maximum Scan Line Register Bit Assignment

Bit	Function
7	200 to 400 Line conversion
6	Line Compare
5	Start Vertical Blank
4:0	Maximum Scan Line

8.6.5.12 Cursor Start Register

Table 8-43. Cursor Start Register Bit Assignment

Bit	Function
7:6	Reserved
5	Cursor Off 0 = Turns on the cursor 1 = Turns off the cursor
4:0	Cursor Start

8.6.5.13 Cursor End Register

Table 8-44. Cursor End Register Bit Assignment

Bit	Function		
7	Reserved		
6:5	Cursor Skew		
	Bit 6	**Bit 5**	**Function**
	0	0	Zero-character clock skew
	0	1	One-character clock skew
	1	0	Two-character clock skew
	1	1	Three-character clock skew
4:0	Cursor End		

8.6.5.14 Start Address High Register

Table 8-45. Start Address High Register Bit Assignment

Bit	Function
7:0	Start Address High

8.6.5.15 Start Address Low Register

Table 8-46. Start Address Low Register Bit Assignment

Bit	Function
7:0	Start Address Low

3.6.5.16 Cursor Location High Register

Table 8-47. Cursor Location High Register Bit Assignment

Bit	Function
7:0	Cursor High

3.6.5.17 Cursor Location Low Register

Table 8-48. Cursor Location Low Register Bit Assignment

Bit	Function
7:0	Cursor Low

3.6.5.18 Vertical Retrace Start Register

Table 8-49. Vertical Retrace Start Register Bit Assignment

Bit	Function
7:0	Vertical Retrace Start

8.6.5.19 Vertical Retrace End Register

Table 8-50. Vertical Retrace End Register Bit Assignment

Bit	Function
7	Protect R0-7 0 = Enables writing to CRTC registers 0-7 1 = Disables writing to CRTC registers 0-7. The line compare bit 4 in register 07 hex is not protected
6	Select 5 Refresh Cycles 0 = Selects three refresh cycles. The BIOS sets this bit to 0 during a mode set, a reset, or power on 1 = Selects five refresh cycles per horizontal line. This allow the use of the VGA chip with slow sweep rate displays (15.75 kHz)
5	Enable Vertical Interrupt 0 = Enables a vertical retrace interrupt (on IRQ2) This interrupt level may be shared so the Input Status register 0, bit 7 should be checked to find out is the VGA caused the interrupt to occur 1 = Disable the vertical retrace interrupt
4	Clear Vertical Interrupt 0 = Clears the vertical retrace interrupt flip-flop 1 = Allows the vertical interrupt to be set at the start of the next vertical retrace interval
3:0	Vertical Retrace End

8.6.5.20 Vertical Display Enable End Register

Table 8-51. Vertical Display Enable End Register Bit Assignment

Bit	Function
7:0	Vertical Display Enable End

8.6.5.21 Offset Register

Table 8-52. Offset Register Bit Assignment

Bit	Function
7:0	Offset

8.6.5.22 Underline Location Register

Table 8-53. Underline Location Register Bit Assignment

Bit	Function
7	Reserved
6	Doubleword Mode 0 = Normal word addressing mode 1 = Memory addresses are doubleword addresses
5	Count By 4 0 = Normal clocking 1 = The memory address counter is clocked with the character clock divided by 4
4:0	Underline Location

8.6 5.23 Start Vertical Blanking Register

Table 8-54. Start Vertical Blanking Register Bit Assignment

Bit	Function
7:0	Start Vertical blank

8.6.5.24 End Vertical Blanking Register

Table 8-55. End Vertical Blanking Register Bit Assignment

Bit	Function
7:0	End Vertical Blank

8.6.5.25 CRTC Mode Control Register

Table 8-56. CRTC Mode Control Register Bit Assignment

Bit	Function
7	Hardware Reset 0 = Forces horizontal and vertical retrace to clear 1 = Forces horizontal and vertical retrace to be enabled
6	Word Mode or Byte Mode 0 = The word mode shifts all memory address counter bits down one bit, and the most-significant bit of the counter appears on the least-significant bit of the memory address outputs 1 = Selects the byte address mode
5	Address Wrap 0 = Selects MA13. This is selected in applications where only 64K memory is present 1 = Selects MA15. This should be selected in odd/even mode since 256K of video memory is installed on the system board
4	Reserved
3	Count By Two 0 = The memory address counter is clocked with the character clock input 1 = Clocks the memory address counter with the character clock input divided by 2

Table 8-56. (Cont.) CRTC Mode Control Register Bit Assignment

Bit	Function
2	Horizontal Retrace Select 0 = Selects normal horizontal retrace as the clock that controls the vertical timing counter 1 = Selects horizontal retrace divided by 2 as the clock that controls the vertical timing counter. Therefore, the vertical resolution is doubled to 2048 horizontal scan lines
1	Select Row Scan Counter 0 = Selects row scan counter bit 1 for CRT memory address bit MA14 1 = Selects MA14 counter bit for CRT memory address bit MA14
0	Compatibility Mode Support 0 = Row scan address bit 0 is substituted for memory address bit 13 during active display time 1 = Enables memory address bit 13 to appear on the memory address output bit 13 of the CRT controller

8.6.5.26 Line Compare Register

Table 8-57. Line Compare Register Bit Assignment

Bit	Function
7:0	Line Compare

8.7 Extended Registers

There are fourteen extended registers that occupy two I/O ports at address 3DEh and 3DFh. Table 8-58 list the register I/O address, the I/O function, index and bits. The bit definitions for these registers are listed in Table 8-59 through 8-70.

Table 8-58. Extended Register Address Map

Port	I/O Function	Register	Index	Bits
3DEh	Read/Write	Extension Address Register	-	5
3DFh	Read/Write	Scratch Register 1	9	8
3DFh	Read/Write	Scratch Register 2	A	8
3DFh	Read/Write	Scratch Register 3	B	8
3DFh	Read/Write	CRT Control Register	C	8
3DFh	Read/Write	OTI Miscellaneous Register	D	7
3DFh	Read/Write	Backward Compatibility Register	E	8
3DFh	Read	NMI Data Cache Register	F	8
3DFh	Read	DIP Switch Read	10	6
3DFh	Read/Write	Segment Register	11	6
3DFh	Read	Configuration Register	12	3
3DFh	Read/Write	Bus Control Register	13	5
3DFh	Read/Write	OTI Overflow Register	14	8
3DFh	Read/Write	HSYNC/2 Start Register	15	8

8.7.1 Extension Address Register

Table 8-59. Extension Address Register Bit Assignment

Bit	Function
4:0	5-bit index pointer to the extension data registers

8.7.2 Scratch Registers 1-3

Table 8-60. Scratch Registers 1-3 Bit Assignment

Bit	Function
7:0	8 scratch bits

3.7.3 CRT Control Register

Table 8-61. CRT Control Register Bit Assignment

Bit	Function
7	In CGA/Hercules emulation mode
6	Vertical SYNC test
5	Attribute test
4	A logic 1 selects 64 internal latches for fully 16 bit operation
3	I/O write test
2	When set to 1, the Maximum Scan Line register bit 0 to 4 are write protected
1	When set to 1, the following registers in CRT Controller area are write protected
0	When set to 1, the following registers in CRT Controller area are write protected

8.7.4 OTI Miscellaneous Register

Table 8-62. OTI Miscellaneous Register Bit Assignment

Bit	Function
7	DRAM configuration
6	Reserved
5	Clock select bit 2 (CSEL2)

CSEL2	CSEL1	CSEL0	CLOCK
0	0	0	25.175 Mhz
0	0	1	28.322 Mhz
0	1	0	65 Mhz
0	1	1	44.9 Mhz
1	0	0	14.161Mhz (derived from 28.322)
1	0	1	18 Mhz (derived from 36 Mhz)
1	1	0	40 Mhz
1	1	1	36 Mhz

4:3	Extended graphics mode selection

Bit 4	Bit 3	Mode Selection
0	0	Non extended graphics modes
0	1	640x480 256 colors, 800x600 256 colors
1	0	1024x768 4 colors
1	1	1024x768 16 colors

2:0	FIFO depth control

8.7.5 Backward Compatibility Register

Table 8-63. Backward Compatibility Register Bit Assignment

Bit	Function
7	Graphics Latch read mode
6	CRT test
5	When this bit and bit 0 are both set to 1, it enables the NMI function
4	It enables 64K address mapping at B0000 when set this bit to 1
3	Page select during Hercules mode **Bit 3** **Page** 0 0 1 1
2:1	Backward Compatibility Mode **Bit 2** **Bit 1** **Mode** 0 0 VGA 0 1 EGA 1 0 CGA 1 1 HERCULES & MDA
0	When both this bit and bit 5 are set to 1, the NMI based I/O trap is enabled for downward compatibility emulation

8.7.6 NMI Data Cache Register

Table 8-64. NMI Data Cache Register Bit Assignment

Bit	Function
7.0	The address of the trapped I/O

8.7.7 DIP Switch Read Register

Table 8-65. DIP Switch Read Register Bit Assignment

Bit	Function
7	JP2 (OFF/ON)
6	JP1 (OFF/ON)
5	DIP Switch 6 (Reserved)
4	DIP Switch 5 (Reserved)
3	DIP Switch 4
2	DIP Switch 3
1	DIP Switch 2
0	DIP Switch 1

.7.8 Segment Register

Table 8-66. Segment Register Bit Assignment

Bit	Function
7	Reserved
6:4	Write segment for CPU memory write
3	Reserved
2:0	Read segment for CPU memory read

.7.9 Configuration Register

Table 8-67. Configuration Register Bit Assignment

Bit	Function
7	HSYNC
6	VSYNC
5:3	CSEL0-2
2	RA14
1	RA13
0	RA12

8.7.10 Bus Control Register

Table 8-68. Bus Control Register Bit Assignme

Bit	Function
7	0=8-bit memory access 1=16-bit memory access
6	0=8-bit I/O access 1=16-bit I/O access
5	0=Enable video BIOS ROM access 1=Disable video BIOS ROM access
4	0=Enable 8-bit video BIOS ROM interface 1=Disable 16-bit video BIOS ROM interface
3:1	Reserved
0	0=Enable access of C6000 to C67FF address 1=Disable access of C6000 to C67FF address

.7.11 OTI Overflow Register

Table 8-69. OTI Overflow Register Bit Assignment

Bit	Function
7	Enable interlaced display
6	Page select for video memory access
5	Page select for CRT display
4	High Order Cursor Location Bit 8
3	High Order Start Address Bit 8
2	Vertical Retrace Start Bit 10
1	Vertical Blank Start Bit 10
0	Vertical Total Bit 10

.7.12 Hsync Divided By 2 Start Register

Table 8-70. Hsync Divided By 2 Start Register Bit Assignment

Bit	Function
7:0	This 7 bit value indicates when the vertical retrace will start in every odd frame during interlaced mode

8.8 Supported Screen Formats

Table 8-71. Standard VGA Modes Supported

MODE	Type	COLxROW	Colors	Pages	Map A
00h	Text	40x25	16	8	B800
01h	Text	40x25	16	8	B800
02h	Text	80x25	16	8	B800
03h	Text	80x25	16	8	B800
00h*	Text	40x25	16	8	B800
01h*	Text	40x25	16	8	B800
02h*	Text	80x25	16	8	B800
03h*	Text	80x25	16	8	B800
00h+	Text	40x25	16	8	B800
01h+	Text	40x25	16	8	B800
02h+	Text	80x25	16	8	B80
03h+	Text	80x25	16	8	B800
07h	Text	80x25	2	8	B000
07h+	Text	80x25	2	8	B000
04h	Graphics	320x200	4	1	B800
05h	Graphics	320x200	4	1	B800
06h	Graphics	640x200	2	1	B800
0Dh	Graphics	320x200	16	8	A00
0Eh	Graphics	640x200	16	4	A00
0Fh	Graphics	640x350	2	2	A000
10h	Graphics	640x350	16	2	A000
11h	Graphics	640x480	2	1	A000
12h	Graphics	640x480	16	1	A000
13h	Graphics	320x200	256	1	A00

NOTES:

1. **Modes marked with * or + are Expanded Character of the original modes.**

2. **Mode 3+(color) or 7+(monochrome) is the default m up.**

Table 8-72. Extended Modes Supported

MODE	Type	COLxROW	Colors	Pages	Map Addr	CharCell
4Fh	Text	132x60	16	2	B800h	8x8
50h	Text	132x25	16	4	B800h	8x14
51h	Text	132x43	16	2	B800h	8x8
52h	Graphics	800x600	16	1	A000h	8x16
53h	Graphics	640x480	256	1	A000h	8x16
54h	Graphics	800x600	256	1	A000h	8x16
55h	Graphics	1024x768	4	1	A000h	8x16
56h	Graphics	1024x768	16	1	A000h	8x16
57h	PORTRAIT	768x1024	4	1	A000h	8x16

Table 8-73. Sync Specifications for Standard VGA Modes

Dot Clk (MHz)	Hsync (KHz)	Vsync (Hz)	Mode
25.172	31.5	60	11, 12
25.172	31.5	70	0, 1, 0*, 1*, 2, 3, 2*, 3*, 4, 5, 6, D, E, F, 10, 13
28.322	31.5	70	0+, 1+, 2+, 3+, 7, 7+

Table 8-74. Sync Specifications for OTI Extended Modes

Dot Clk (MHz)	Hsync (KHz)	Vsync (Hz)	Mode
25.175	31.47	59.94	53
28.322	22.27	59.22	50m, 51m
36.000	35.16	56.16	52, 54
40.000	31.25	59.64	4F
40.000	31.25	69.60	50, 51
44.900	35.52	43.32	55i, 56i
44.900	46.77	43.15	57i
65.000	48.08	59.80	55, 56
65.000	59.74	55.22	57

NOTES: m : multifrequency
i : interlaced

8.9 Signal Definitions

8.9.1 OTI-067 Signal Definitions

Table 8-75. OTI-067 Signal Name

Pin Number	OTI-067 Signal Name
1	-CAS
2	-RAS
3	-WE23
4	MBO
5	MB1
6	MB2
7	MB3
8	GND
9	MB4
10	MB5

Table 8-75. (Cont.) OTI-067 Signal Name

Pin Number	OTI-067 Signal Name
11	MB6
12	MB7
13	MB8
14	VCC
15	MD0
16	MD1
17	MD2
18	MD3
19	MD4
20	MD5
21	GND
22	MD6
23	MD7
24	MD8
25	MD9
26	MD10
27	MD11
28	MD12
29	MD13
30	GND
31	MD14
32	MD15
33	SD15
34	SD14
35	SD13
36	SD12
37	SD11
38	SD10
39	SD9
40	SD8

Table 8-75. (Cont.) OTI-067Signal Name

Pin Number	OTI-067 Signal Name
41	GND
42	LA17
43	LA18
44	LA19
45	LA20
46	LA21
47	LA22
48	LA23
49	-BHEN
50	-1016
51	-M16
52	GND
53	BD0
54	BD1
55	BD2
56	BD3
57	VCC
58	BD4
59	BD5
60	BD6
61	BD7
62	VCC
63	-ROMENL
64	RA12
65	RA13
66	RA14
67	SA0
68	SA1
69	SA2
70	SA3

Table 8-75. (Cont.) OTI-067 Signal Name

Pin Number	OTI-067 Signal Name
71	SA4
72	SA5
73	SA6
74	SA7
75	SA8
76	SA9
77	SA10
78	SA11
79	SA12
80	SA13
81	SA14
82	SA15
83	SA16
84	SA17
85	SA18
86	SA19
87	AEN
88	-RFSH
89	-IOR
90	-IOW
91	GND
92	-MRD
93	-MWR
94	VCC
95	SD0
96	SD1
97	SD2
98	SD3
99	SD4
100	SD5

Table 8-75. (Cont.) OTI-067 Signal Name

Pin Number	OTI-067 Signal Name
101	GND
102	SD6
103	SD7
104	-CINT
105	-NMI
106	RSET
107	RDY
108	-RDSW
109	VSYNC
110	HSYNC
111	PCLK
112	-BLANK
113	-DACR
114	-DACW
115	P7
116	P6
117	GND
118	P5
119	P4
120	P3
121	P2
122	P1
123	P0
124	GND
125	SWSENSE
126	VSETUP
127	ENVGA
128	VCC
129	MCLK
130	VCLK

Table 8-75. (Cont.) OTI-067 Signal Name

Pin Number	OTI-067 Signal Name
131	CSEL2
132	CSEL1
133	CSEL0
134	MA0
135	MA1
136	MA2
137	MA3
138	MA4
139	GND
140	MA5
141	MA6
142	MA7
143	MA8
144	-WE01

8.9.2 OTI-066 Signal Definitions

Table 8-76. OTI-066 Signal Name

Pin Number	OTI-066 Signal Name
1	RED
2	GREEN
3	BLUE
4	IREF
5	P0
6	P1
7	P2
8	P3
9	P4
10	P5
11	P6
12	P7
13	PCLK
14	VSS
15	VCC
16	RS1
17	RS0
18	-WR
19	D7
20	D6
21	D5
22	D4
23	D3
24	D2
25	D1
26	D0
27	-BLANK
28	-RD

8.9.3 OTI-069 Signal Definitions

Table 8-77. OTI-069 signal Name

Pin Number	OTI-069 Signal Name
1	FS3
2	STROBE
3	VDD
4	FREQ1
5	XTAL1
6	XTAL2
7	FREQ0
8	VSS
9	FOUT
10	CPSEL
11	OUT
12	AVDD
13	VCO(IN)
14	OP(OUT)
15	OP(-)
16	OP(+)
17	AVSS
18	FS0
19	FS1
20	FS2

8.10 Signal Description

8.10.1 OTI-067 Signal Description

8.10.1.1 CPU Bus Interface

AEN
ADDRESS ENABLE. This signal is used to qualify the video me
access from CPU. When it is active high, the DMA controller h
the address bus, data bus, and command lines.

-RFSH
REFRESH. This signal is used to qualify the video memory acc
CPU. When it is active low, it indicate a memory refresh cycle.

-IOR
I/O READ. This is an active low I/O read strobe, asserted in 8/
read cycle.

-IOW
I/O WRITE. This is an active low I/O write strobe, asserted in 8
write cycle.

-MRD
MEMORY READ. This is an active low memory read strobe, as
16 bit memory read cycle.

-MWR
MEMORY WRITE. This is an active low memory write strobe, a
16 bit memory write cycle.

REST
RESET. Active high system reset signal. This input signal will
OTI-067 and initialize the configuration register based on the
on CSEL0-2, RA[14:12], HSYNC, and VSYNC pins at power-u

RDY
CUP READY. An open collector active high output to signal p
it is ready for memory access. This signal is used to add wait
bus cycle during video memory access. It is pulled low by OT
after the video memory access request by CPU to allow addit
finish the memory cycle.

-NMI
NON MASKABLE INTERRUPT. An active low open collector signal. This signal is used to activate the interrupt-driven programs.

-CINT
CRT INTERRUPT REQUEST. An interrupt request is generated when vertical retrace occurs if it is enabled by bit 5 in the Vertical Retrace End register. It is an active low open collector output.

-M16
16-BIT MEMORY. It is an active low open collector output signal used to indicate to the system that the present data transfer is a 16-bit memory cycle. It is derived from the decode of LA17 through LA23.

-IO16
16-Bit I/O. It is an active low open collector output signal used to indicate to the system that the present data transfer is a 16-bit I/O cycle. It is derived from an address decode.

-BHEN
BYTE HIGH ENABLE. When the OTI-067 is in 16 bit mode, this active low signal indicates a transfer of data on the high byte of the data bus (SD[15-8]).

SD[15:8]
DATA LINE 15-8. CPU data bus bit 15-8.

SD[7:0]
DATA LINE 7-0. CPU data bus bit 7-0.

SA[19:0]
ADDRESS LINE 19-0. CPU address bus bit 19-0.

LA[23:17]
UNLATCHED ADDRESS LINE 23-17. CPU unlatched bus line 23-17.

8.10.1.2 BIOS ROM Control

-ROMENL
ROM LOW BYTE ENABLE. An active low signal to enable/control the low byte of BIOS data to CPU data bus in 16 bit BIOS mode. In 8 bit BIOS mode, this pin is not used.

RA[14:12]
ROM ADDRESS LINE 14-12. This signal is output to the addı
of BIOS ROM as a final address input.

BD[7:0]
DATA LINE 7-0. Data bit 7-0 of BIOS high byte data in 16 bit
or single byte data in 8 bit BIOS mode. Also, data bit of DAC
dipswitch.

8.10.1.3 Clock Interface

VCLK
VIDEO CLOCK. This is the master input dot clock for VGA cl

MCLK
MEMORY CLOCK. This is a direct input clock used for DRAI
timing.

CSEL0-2
CLOCK SELECT 0-2. Clock select line 0-2.

8.10.1.4 CRT And RAMDAC Interface

HSYNC
HORIZONTAL SYNC. Horizontal synchronization pulse to th
monitor. The polarity of the pulse is determined by bit 6 of th
ous Output Register. (Bit 7 of 3DF index 12.)

VSYNC
VERTICAL SYNC. Vertical synchronization pulse to display
polarity of the pulse is determined by bit 7 of the Miscellane
Register. (Bit 6 of 3DF index 12.)

-BLANK
BLANK. Active low output signal to RAMDAC to blank the p
the display monitor.

P[7:0]
PIXEL DATA. Pixel data bit 7-0, output to external color pale
mapping.

-DACR
RAMDAC READ. An active low I/O read signal generated for reading external color palette registers.

-DACW
RAMDAC WRITE. An active low I/O write signal generated for writing external color palette registers.

PCLK
PIXEL CLOCK. Pixel clock output to DAC to latch the pixel data P7-P0. It is derived from the current dot clock rate of operating mode.

8.10.1.5 Video Memory Interface

MA[8:0]
MEMORY ADDRESS. Memory address line 8-0 for memory maps 0, 1 (bank A).

MB[8:0]
MEMORY ADDRESS. Memory address line 8-0 for memory maps 2, 3 (bank B).

MD[15:0]
MEMORY DATA. Memory data line 15-0. With 2 DRAMS bits 0-3 are for maps 0,1 and bits 4-7 are for maps 2,3. With 4 DRAMS bits 0-3, 8-11 are for maps 0,1 and bits 4-7, 12-15 are for maps 2,3.

-RAS
ROW ADDRESS STROBE. Active low output signal to all video memory maps.

-CAS
COLUMN ADDRESS STROBE. Active low output signal to all video memory maps.

-WE01
WRITE ENABLE. Active low write enable pulse to memory map 0 and 1.

-WE23
WRITE ENABLE. Active low write enable pulse to memory map 2 and 3.

8.10.1.6 Miscellaneous

ENVGA
ENABLE VGA. This active high input signal enables I/O and video memory access. Valid only for motherboard implementations. For adapter card implementations, pull high or low. See section on adapter card/ motherboard configuration.

VSETUP
VGA SETUP. An active low input signal puts VGA in setup mode. During setup mode, only internal port 102 can be accessed. A writing logic 1 to port 102 awaken the OTI-067 after power up. Valid only for motherboard implementations. For adapter card implementations, pull high or low. See section on adapter card/motherboard configuration.

-RDSW
READ DIP SWITCH. An active low read pulse enables to read the DIP switch setting.

SWSENSE
SWITCH SENSE. An input signal used to auto detect the monitor type.

8.10.1.7 Power and Ground

VCC
Power: +5 V

GND
Ground

.10.2 OTI-066 Signal Description

RED, BLUE, GREEN
These are the analog outputs of the 6-bit DACs. The RGB (red, blue, green) voltage will be developed at this output pin with the current flowing from this point into the terminating resistors. Each DAC is composed of 63 current sources. The output of these current sources is summed together based on the 6-bit binary value from the static RAM table.

IREF
The reference current forced out of this pin determines the current sourced by each of the 63 current sources in each of the 6-bit DACs. Each current source produces 1/30 of IREF when activated by the 6-bit digital code.

P0-P7
These are high-speed Pixel Address inputs. The address is latched and masked by the Pixe Register. It is used for addressing the Color Palette RAM and generating the final color value.

PCLK
This is the high-speed Pixed Clock signal. The rising edge samples and latches the Pixed Address and Blanking inputs. It controls progress of these values through the three-stage pipeline of the Color Palette and through the DACs to outputs.

VSS
Power supply ground.

-RD
Active low Read bus control signal. Enables Data I/O lines D0-D7.-RD and -WR should not be active at the same time.

-BLANK
Active low signal forces zero voltage at the DAC outputs. When -BLANK is asserted,the Color Palette can still be updated through D0-D7.

D0-D7
Bi-directional data lines to read or write information for the OTI-066 internal registers. During the write cycle, the rising edge of -WR latches the data into the selected register. The rising edge of -RD determines the

end of the read cycle. When -RD and -WR go high, the Data I/O lines will be in a tri-state mode.

-WR
Active low Write signal controls the timing of the write operations on the microprocessor interface inputs D0-D7. When asserted, the rising edge of -WR will sample and latch data into internal registers. -RD and -WR signals should not be asserted at the same time.

RS0, RS1
Register Select inputs. These two inputs are sampled during the faling edges of the enable signals (-RD or -WR) and select one of the three internal registers.

VCC
Positive power supply pin. It is normally connected to +5V and bypassed with a 10µF tantalum capacitor and a 0.1µF chip capacitor.

8.10.3 OTI-069 Signal Description

FS0
Frequency Selcet input, TTL compatible (LSB)

FS1
Frequency Select input, TTL compatible (LSB)

FS2
Frequency Select input, TTL compatible (LSB)

FS3
Frequency Select input, TTL compatible (MSB)

STROBE
Negative edge clock for select input, TTL compatible

FREQ0
Externally generated frequency input

FREQ1
Externally generated frequency input

FOUT
Clock output, TTL compatible

XTAL1
Crystal interface / External oscillator input

XTAL2
Crystal interface

VDD
5-Volt digital power pin

AVDD
5-Volt analog power pin

VSS
Digital ground

AVSS
Analog ground

CPSEL
Phase comparator polarity select (pull up to VDD if left open)

OUT
Phase comparator output

VCO(IN)
voltage-controlled oscillator input

OP(OUT)
Op-amp output

OP(-)
Op-amp negative input

OP(+)
Op-amp positive input (AVDD referenced, if open)

9

POWER SUPPLY

This chapter describes the specifications of the DECpc 320sxLP/325sxLP power supply. The power supply is a 115 Watt power supply.

9.1 115 Watt Power Supply Output Specifications

Table 9-1 lists the output specifications for the 115 Watt power supply.

Table 9-1. 115 Watt Power Supply Output Specification

PARAMETER		REQUIREMENT			UNITS
		MIN.	TYP.	MAX.	
OUTPUT VOLTAGE	+5V	+4.80	+5.00	+5.25	VOLTS
	+12V	+11.40	+12.00	+12.60	
	-12V	-11.40	-12.00	-12.60	
	-5V	-4.75	-5.00	-5.25	
LOAD RANGE	+5V	1.0	-	12.0	AMPS
	+12V	40m	-	4.2	
	-12V	0	-	0.3	
	-5V	0	-	0.3	
RIPPLE & NOISE	+5V	-	-	50	mV
	+12V	-	-	100	
	-12V	-	-	150	
	-5V	-	-	100	
HOLD-UP TIME		20	-	-	ms

NOTE:

1. Noise Test: Use 20 MHz bandwidth frequency oscilloscc

2. Add 0.1μF/10μF capacitor at output connector terminals Ripple & Noise measurements.

3. +12V output should withstand 5.0A surge current for 15 seconds during this period the +12V regulation toleranc should be +7%,-6%.

A.2 BIOS Services

All calls to the BIOS are made through software interrupts (that is, by means of assembly-language "INT x " instructions). Each I/O device is provided with a software interrupt, that transfers execution to the BIOS service routine. Input parameters to BIOS routines are normally passed in CPU registers. Similarly, output parameters are generally returned from these routines to the caller in CPU registers. To execute a BIOS call, load the registers with input parameter. (When a BIOS service is capable of running more than one function, functions are selected by placing the proper function number in the AH register. Subfunctions are selected via either the AL register or the BL register.) Then issue the interrupt given for the call. For example, the following can be used to read a character from the keyboard:

```
MOV AH,0
INT 16h
```

Upon return, AL contains the ASCII character and AH contains the keyboard scan code.

Note: All registers except those used to return parameters to the caller are saved and restored by the BIOS routines.

Table A-2 is a quick reference list of software interrupts for all device I/O and system status services. Tables A-3 through A-13 briefly define each BIOS service and list each BIOS function and subfunction.

Table A-1. (Cont.) Interrupt Functions and Types

INT	Function	Type	Vector
07h	Math coprocessor not present	Hardware	
08h	Double exception error	Hardware	
08h	System timer (IRQ 0)	Hardware	FFEA5h
09h	Keyboard (IRQ 1)	Hardware	FE987h
09h	Math coprocessor segment overrun	Logical	
0Ah	IRQ 2 cascade from second programmable interrupt controller	Hardware	
0Ah	Invalid task segment state	Logical	
0Bh	Serial communications (COM2)	Hardware (IRQ 3)	
0Bh	Segment not present	Logical	
0Ch	Serial communications (COM1)	Hardware (IRQ 4)	
0Ch	Stack segment overflow	Logical	
0Dh	Parallel printer (LPT2)	Hardware (IRQ 5)	
0Dh	General protection fault	Logical	
0Eh	IRQ 6 diskette	Hardware	FEF57h
0Eh	Page fault (80386 only)	Logical	
0Fh	Parallel printer (LPT1) IRQ7	Hardware	
10h	Video	Software	C17BDh
10h	Numeric coprocessor fault	Logical	
11h	Equipment list	Software	FF84Dh
12h	Memory size	Software	FF841h
13h	Fixed disk/diskette	Software	F7FE5h
14h	Serial communication	Software	FE739h
15h	System services	Software	FF859h
16h	Keyboard	Software	FE82Eh
17h	Parallel printer	Software	FEFD2h
18h	Process boot failure	Software	F79A9h
19h	Bootstrap loader	Software	FE6F2h
1Ah	Time-of-day	Software	FFE6Eh
1Bh	Keyboard break	Software	FFF53h
1Ch	User timer tick	User	FFF53h
1Dh	Video parameter table	BIOS Table	C789Bh

Table A-1. (Cont.) Interrupt Functions and Types

INT	Function	Type	Vector
1Eh	Diskette parameter table	BIOS Table	FEFC7h
1Fh	Video graphics characters	User	C572Ah
20h to 3Fh	Reserved for DOS		
40h	Diskette BIOS revector	Software	FEC59h
41h	Fixed disk parameter table	BIOS Table	004C0h
42h	EGA default video driver	BIOS Table	
43h	Video graphics characters	User	
44h to 45h	Reserved		
46h	Fixed disk parameter table	BIOS Table	FE401h
47h to 49h	Reserved		
4Ah	User alarm	User	
4Bh to 59h	Reserved		
5Ah	Cluster adapter		
5Bh to 5Fh	Reserved		
60h to 66h	Reserved for user program Interrupts	User	
67h	LIM EMS driver		
68h to 6Fh	Reserved		
70h	Real-time clock (IRQ 8)	Hardware	FCCEDh
71h	IRQ 2 redirect (IRQ 9)	Hardware	FD179h
72h	Reserved (IRQ 10)	Hardware	FD182h
73h	Reserved (IRQ11)	Hardware	FD182h
74h	Reserved (IRQ 12)	Hardware	F925Ah
75h	80287 exception (IRQ 13)	Hardware	FD16Ah
76h	Fixed disk (IRQ 14)	Hardware	F7FCBh
77h	Reserved (IRQ 15)		FFF53h
78h to 7Fh	Reserved		
80h to F0h	Reserved for BASIC	BASIC	
F1h to FFh	Reserved for user program interrupts	User	

A.2 BIOS Services

All calls to the BIOS are made through software interrupts (th
means of assembly-language "INT x " instructions). Each I/O
provided with a software interrupt, that transfers execution to
service routine. Input parameters to BIOS routines are norma
CPU registers. Similarly, output parameters are generally ret
these routines to the caller in CPU registers. To execute a BI
the registers with input parameter. (When a BIOS service is c
running more than one function, functions are selected by pl
proper function number in the AH register. Subfunctions are
either the AL register or the BL register.) Then issue the inter
the call. For example, the following can be used to read a ch
the keyboard:

```
MOV AH,0
INT 16h
```

Upon return, AL contains the ASCII character and AH co
keyboard scan code.

**Note: All registers except those used to return parameter
caller are saved and restored by the BIOS routines.**

Table A-2 is a quick reference list of software interrupts for a
and system status services. Tables A-3 through A-13 briefly
BIOS service and list each BIOS function and subfunction.

Table A-2. Software Interrupts

Service	Software Interrupts
Print Screen	05 h
Video Display	10 h
Equipment List	11 h
Memory Size	12 h
Diskette	13 h
Fixed Disk	13 h
Serial Communications	14 h
Multi-Tasking Support	15 h
Joystick	15 h
Microsecond Delay	15 h
Extended Memory	15 h
Virtual Mode	15 h
Mouse	15 h
Keyboard	16 h
Parallel Printer	17 h
Time - of - Day	1A h

Table A-3. Print Screen Service

INT	Parameter	Function
05h	None	Print screen

Table A-4. Video Services

INT	AH	Function
10h	00h	Set video mode
	01h	Set text mode cursor size
	02h	Set cursor position
	03h	Read current cursor position
	04h	Read light pen position
	05h	Select active video page
	06h	Scroll active page up
	07h	Scroll active page down
	08h	Read character/attribute from screen
	09h	Write character/attribute to screen
	0Ah	Write character only to screen
	0Bh	Set color palette
	0Ch	Write pixel
	0Dh	Read pixel
	0Eh	Write teletype to active page
	0Fh	Return video status

Table A-4. (Cont.) Video Services

INT	AH	Function	
10h	10h	Set palette/color registers:	
		Parameter	**Subfunction**
		AL = 00h	Set single palette
		AL = 01h	Set overscan register
		AL = 02h	Set all palette registers and overscan
		AL = 03h	Toggle intensify/blinking bit
		AL = 04h-06h	Reserved
		AL = 07h	Read individual palette register
		AL = 08h	Read overscan register (border color)
		AL = 09h	Read all palette registers and overscan register (border color)
		AL = 10h	Set individual color register
		AL = 11h	Reserved
		AL = 12h	Set block of color registers
		AL = 13h	Select color paging mode (not valid for mode 13h)
		BL = 00h	Select paging mode
		BL = 01h	Select page
		AL = 14h	Reserved
		AL = 15h	Read single DAC color register
		AL = 16h	Reserved
		AL = 17h	Read block of color registers
		AL = 18h-19h	Reserved
		AL = 1Ah	Read color paging status
		AL = 1Bh	Sum color values to gray shades

Table A-4. (Cont.) Video Services

INT	AH	Function	
10h	11h	Load character generator:	
		Parameter	**Subfunction**
		AL = 00h	Load user text mo
		AL = 01h	Load ROM 8x14 te
		AL = 02h	Load ROM 8x8 do mode font
		AL = 03h	Set block specifie only)
		AL = 04h	Load 8x16 ROM te
		AL = 10h	Load user text mo (after mode set)
		AL = 11h	Load ROM 8x14 te (after mode set)
		AL = 12h	Load ROM 8x8 do mode font (after m
		AL = 14h	Load 8x16 ROM te (after mode set)
		AL = 20h	Set user graphics pointer at INT 1Fh
		AL = 21h	Set user graphics at INT 43h
		AL = 22h	Use ROM 8x14 fo graphics
		AL = 23h	Use ROM 8x8 dou for graphics
		AL = 24h	Use ROM 8x16 fo graphics
		AL = 30h	Get font pointer in

Table A-4. (Cont.) Video Services

INT	AH	Function	
10h	12h	Alternate select:	
		Parameter	**Subfunction**
		BL = 10h	Return configuration information
		BL = 20h	Switch to alternate print screen routine
		BL = 30h	Select scan lines for text modes
		BL = 31h	Enable/disable default palette loading during set mode
		BL = 32h	Enable/disable video
		BL = 33h	Enable/disable summing to gray shades
		BL = 34h	Enable/disable cursor scaling
		BL = 35h	Switch display
		BL = 36h	Video screen off/on
	13h	Write string:	
		Parameter	**Subfunction**
		AL = 00h	Cursor not moved
		AL = 01h	Cursor is moved
		AL = 02h	Cursor not moved (text modes only)
		AL = 03h	Cursor is moved (text modes only)

Table A-4. (Cont.) Video Services

INT	AH	Function	
10h	14h-19h	Reserved	
	1Ah	Read/write display combination code:	
		Parameter	**Subfunction**
		AL = 00h	Read display combination code
		AL = 01h	Write display Combination code
	1Bh	Return functionality/state information	
	1Ch	Save/restore video state	
	1Dh-FFh	Reserved	

Table A-5. Equipment List Service

INT	Parameter	Function
11h	None	Read equipment list

Table A-6. Memory Size Service

INT	Parameter	Function
12h	None	Read memory size

Table A-7. Diskette Service

INT	AH	Function
13h	00h	Reset diskette system
	01h	Read diskette status
	02h	Read diskette sectors
	03h	Write diskette sectors
	04h	Verify diskette sectors
	05h	Format diskette track
	06h-07h	Reserved
	08h	Read drive parameters
	03h-14h	Reserved
	15h	Read drive type
	16h	Detect media change
	17h	Set diskette type
	18h	Set media type for format
	19h-FFh	Reserved

Table A-8. Fixed Disk Service

INT	AH	Function
13h	00h	Reset diskette(s) and fixed disk
	01h	Read fixed disk status
	02h	Read sectors
	03h	Write sectors
	04h	Verify sectors
	05h	Format cylinder
	08h	Read drive parameters
	09h	Initialize drive parameters
	0Ah	Read long sectors
	0Bh	Write long sectors
	0Ch	Seek to cylinder
	0Dh	Alternate fixed disk reset
	10h	Test for drive ready
	11h	Recalibrate drive
	14h	Controller internal diagnostic
	15h	Read fixed disk type
	16h-FFh	Reserved

Table A-9. Serial Communication Service

INT	AH	Function
14h	00h	Initialize serial communications
	01h	Send character
	02h	Receive character
	03h	Read serial port status
	04h to FFh	Reserved

Table A-10. System Services

INT	AH	Function
15h	04h to 4Eh	Reserved
	4Fh	Keyboard intercept
	50h to 7Fh	Reserved
	80h	Device open
	81h	Device close
	82h	Program termination
	83h	Set event wait interval
	84h	Joystick support
	85h	System request key
	86h	Wait
	87h	Move block
	88h	Read extended memory size
	89h	Switch processor to protected
	8Ah to 8Fh	Reserved
	90h	Device busy
	91h	Interrupt complete
	97h to BFh	Reserved
	C0h	Return system configuration p

Table A-11. Keyboard Service

INT	AH	Function
16h	00h	Read keyboard input
	01h	Return keyboard status
	02h	Return shift flag status
	03h	Set typematic rate and delay
	05h	Store key data
	06h to 0Fh	Reserved
	10h	Read extended keyboard input
	11h	Return extended keyboard status
	12h	Return extended shift flag status
	13h to FFh	Reserved

Table A-12. Parallel Printer Service

INT	AH	Function
17h	00h	Print character
	01h	Initialize printer
	02h	Read printer status
	03h to FFh	Reserved

Table A-13. Time-of-Day Service

INT	AH	Function
1Ah	00h	Read system timer time counter
	01h	Set system timer time counter
	02h	Read real time clock time
	03h	Set real time clock time
	04h	Read real time clock date
	05h	Set real time clock date
	06h	Set real time clock alarm
	07h	Reset real time clock alarm

APPENDIX B

PRODRIVE LPS 52/15AT HARD DISK DRIVES

The LPS 52/105AT hard disk drive features an embedded AT drive controller and uses AT commands to optimize system performance. Because the drive manages media defects and error recovery internally, these operations are fully transparent to the user. The LPS 52AT hard disk drive provides 52 megabytes of formatted capacity on one disk, with two read/write heads; while the LPS 105AT hard disk drive provides 105 megabytes on two disks, with four read/write heads.

NOTE: As defined by Quantum, a megabyte (MB) is 1,000,000 bytes.

Key features of the LPS 52/105AT hard disk drive include:

- **Formatted storage capacity of 52 or 105 megabytes**
- **Low-profile, 1-inch height**
- **Industry-standard 3 1/2 inch form factor**
- **Data-transfer rate of up to 4.0 megabytes/second, using programmed I/O**
- **Average seek time of 17 milliseconds**
- **Proprietary 64K, look-ahead, programmable DisCache**
- **48-bit, computer-generated, cyclic Error Correcting Code (ECC), with 11-bit burst correction**
- **Automatic retry on read errors**
- **Transparent media-defect mapping**
- **High-performance, in-line defective sector skipping**

- **Reassignment of defective sectors discovered in the field, out reformatting**
- **Patented AIRLOCK automatic shipping lock and dedicated ing zone**
- **1:1 interleave on read/write operations**
- **Ability to daisy-chain two drives on the interface**

B.1 Physical Specifications

Table B-1. Environmental Limits

Attribute	Specifications
Ambient Temperature, Non-operating	-40°F to 140°F (-40°C to 6 42°F/hr (20°C/hr) gradient
Ambient Temperature, Operating	39°F to 122°F (4°C to 50° 23°F/hr (10°C/hr) gradient
Ambient Relative Humidity, Non-operating	5% to 95%, without conde Maximum wet bulb 115°F
Ambient Relative Humidity, Operating	8% to 85%, without conde Maximum wet bulb 70°F
Altitude (relative to sea level), Non-operating	-200 (-60M) to 40,000 ft (
Altitude (relative to sea level), Operating	-200 (-60M) to 10,000 ft (

Table B-2. Mechanical Dimensions

Attribute	Specifications
Height	1.0 in (25.4 mm)
Width	4.0 in (101.6 mm)
Depth	5.75 in (146.2 mm)
Weight	1.05 lb (0.48 kg)

NOTE: All dimensions are exclusive of the faceplate.

Table B-3. Heat Dissipation

Attribute	Specifications
Average Power Consumption (ready, on track idle)	5.5 Watts
Typical Power Consumption (random read/write)	6.5 Watts

NOTE: Quantum defines random read/write as:

40% random seeks
40% read/Write (1 write plus 10 reads)
20% ready (idle)

Table B-4. Vibration and Shock Specifications

Attribute	Specifications	
	Operating	Nonoperating
Vibration:		
5-500 Hz sine wave (peak-to-peak) 1 oct/min sine sweep	1.0G	2.00G
Shock:		
1/2 sine wave of 11 msec duration (10 hits maximum)	6 G (no soft errors) 10G (1 soft error/block)	60 G

NOTE: When packed in its shipping container, the LPS 52/105AT can withstand a drop from 36 inches, onto a concrete surface-on any of its surfaces, six edges, and three corners. The drive can withstand vibration applied to the container of 0.5 G, 5-100 Hz (0-to-peak) and 1.5 G, 100-500 Hz (0-to-peak).

B.2 Performance Specifications

Table B-5. Physical Capacity

Attribute	Specifications	
	LPS 52AT	LPS 105AT
Physical capacity (MB)	52	105
Number of 512-byte sectors	102,171	205,561

NOTE: The LPS 52/105AT receives a low-level format at the factory, which creates the actual tracks and sectors on the drive. Formatting done at the user level, for operation with DOS, UNIX, or other operating systems, will result in less capacity than the physical capacity shown.

Table B-6. Logical Addressing Format

Attribute	Specifications	
	52AT	105AT
Logical Cylinders	751	755
Logical Heads	8	16
Logical Sectors/Track	17	17
Total Number Logical Sectors	102,136	205,360

NOTE: A low-level format is not required.

Table B-7. Data-Transfer Rates

Attribute	Specifications
Buffer to AT Bus	Up to 4 0 MB/sec, using programmed I/O
Disk to Buffer	Up to 1.75 MB/sec in burst

Table B-8. Timing Specifications

DESCRIPTION	NOMINAL CONDITIONS		WORST-CASE CONDITIONS
	TYPICAL	MAXIMUM	
Single-Track Seek (msec)	5	6	6
Average Seek (msec)	17	19	21
Third-Stroke Seek (msec)	18	21	23
Full-Stroke Seek (msec)	33	38	43
Average Rotational Latency (msec)	8.2	8.2	8.2
Sequential Head Switch (msec)	2.0	2.0	2.0
Power-Up Time (sec)	8	10	10

NOTE: **Defined as the time required for the actuator to seek and settle on track, seek time is measured by averaging 1000 seeks of the indicated length. Seek time includes head settling time, but not command overhead or rotational-latency delays.**

Average seek time is the average of 1000 random seeks. When a seek error occurs, recovery for that seek may take up to seven seconds.

Sequential head-switch time is the time required for the head to move from the end of the last sector on a track, to the beginning of the next sequential sector-which is on the next track in the same cylinder. Track skewing determines the sequential head-switch time. See Appendix A.

Power-up time is the time elapsed between the supply voltages reaching operating range and the drive being ready to accept all commands.

An ambient temperature of 25•C, nominal supply voltages, and no applied shock or vibration constitute nominal conditions. Worst-case extremes of temperature and supply voltages constitute worst-case conditions.

Table B-9. Error Rates

Attribute	Specifications
Random Data Errors	1 per 10^{10} bits read (maximum)
Defect Data Errors	1 per 10^{12} bits read (maximum)
Unrecoverable Data Errors	1 per 10^{14} bits read (maximum)
Seek Errors	1 per 10^{6} seeks (maximum)

NOTE: Error rates are defined as:

Data Error: A data error occurs whenever the drive fails to read or write a sector of data correctly. Data error rates are average rates measured over at least 1000 different sectors, under any specified operating conditions, except applied shock or vibration.

Random Error: An error that does not exhibit a repeating error pattern-that is, the error does not occur successively within a specified number of retry reads. The default is eight. Retries terminate once the drive reads the data correctly. The drive does not automatically reallocate the sectors, because the error is probably not due to media defects. See Appendix B for information about defect handing.

Defect Errors: Errors that exhibit a repeating error pattern-that is, the error occurs successively within eight retry reads, before the drive can read the sector successfully. Such errors are likely due to media defects.

Unrecoverable Errors: Errors with a final retry error pattern that is uncorrectable using ECC. The drive terminates retry reads either when a repeating error pattern occurs or after eight unsuccessful retries.

Seek Error: A seek error occurs when the actuator fails to reach or remain on the requested cylinder, or the drive requires the execution of the full recalibration routine to locate the requested cylinder. A full recalibration takes approximately seven seconds.

B.3 Functional Specifications

Table B-10. LPS 52/105AT Functional Specific

Attribute	Specifications	
	LPS 52AT	LP
Nominal Rotational Speed (RPM)	3,662±0.2%	3,6
Maximum Recording Density (bpi)	29,307	29,
Maximum Flux Density (fci)	19,538	19,
Track Density (tpi)	1,330	1,3
Data Tracks	2,438	4,8
Data Sectors/Track		
Zone 0	49	49
Zone 1	42	42
Zone 2	35	35
Data Tracks/Cylinder		
Zone 0	2	4
Zone 1	2	4
Zone 2	2	4
Data Cylinders (total)	1,219	1,2
Zone 0	454	45
Zone 1	382	38
Zone 2	383	38
Spare Sectors/Cylinder	1	1
Read/Write Heads	2	4
Disks 1	2	
Encoding Scheme	RLL 2,7	RL

3.4 Power Requirements

Table B-11. DC Power Requirements

	DC VOLTAGES	
REQUIREMENT	**+12V**	**+5V**
Maximum Tolerance	**±10%**	**±5%**
Current:		
Ready (on track idle)	0.32A	0.32A
Random Read/Write	0.41A	0.31A
Maximum (at power on)	1.0A (±10%)	0.31A
Ripple and Noise (maximum peak-to peak)	100 mV	50 mV

NOTE: random read/write are defined as:

40% random seeks
40% read/write (1 write plus 10 reads)
20% ready (idle)

3.5 Jumper Setting

This section describes hardware options that should be set prior to installation. The configuration of three jumpers controls the drive's mode of operation:

- **DS - Drive Select**
- **SP - Slave Present**
- **DM - Drive Mode**

B.5.1 Drive Select (DS) Jumper

You can daisy-chain two drives on the AT-bus interface. When daisy-chaining two drives, use their Drive Select (DS) jumpers to configure one drive as the Master and the other as the Slave. To configure a drive as the Master (Drive 0), install a jumper at the DS pins. Quantum ships ProDrive 52AT and 105AT hard disk drives from the factory with the DS jumper installed - that is, configured as Drive 0. To configure a drive as the Slave (Drive 1), remove the DS jumper.

NOTE: The order in which drives are connected in a daisy chain has no significance.

B.5.2 Slave Present (SP) Jumper

In combination with the current DS jumper setting, the Slave Present (SP) jumper implements one of two possible configurations:

- **When the drive is configured as a Master-that is, with the DS jumper installed-the SP jumper indicates to the drive that a Slave drive is present. The SP jumper should be installed on the Master drive only if the Slave drive does not use the Drive Active/Slave Present (DASP) signal to indicate its presence.**

- **When the drive is configured as a Slave-that is, without the DS jumper installed-the SP jumper enables the self-seek test. When power is applied to the drive with the self-seek test enabled, the drive executes seeks in butterfly pattern.**

- **During the self-seek test, the LED remains on while the test proceeds without error. If the test encounters a seek error, the test terminates and the LED flashes continuously until the SP jumper is removed.**

B.5.3 Drive Mode (DM) Jumper

When the Drive Mode (DM) jumper is installed, the drive is in the ProDrive 40/80AT compatible mode and can communicate with a ProDrive 40/80AT hard disk drive. In this mode, the drive does not use the PDIAG signal to control Master/Slave communications. The configuration of the DS and SP jumpers determines whether the drive is the Master or the Slave.

APPENDIX C

FLEXIBLE DISK DRIVE (FDD)

DECpc 320sxLP/325sxLP computer supports up to four disk drives. This section describes the SONY 3.5" 2MB Micro Floppy Disk Drive and the TEAC FD-55GFR, 5.25" flexible disk drive which are installed in DECpc 320sxLP/325sxLP.

C-1 SONY 3.5" 2MB Micro Floppy Disk Drive

C-1-1 Configuration

The drive consists of Read/Write heads, a head positioning mechanism,a spindle motor circuit board, a Read/Write interface and logic control circuit board, and a 1" high front panel.

C-1-2 Physical Specifications

Table C-1. Mechanical Dimensions

Attribute	Specifications
Height	25.4 mm (1.0 inch)
Width	101.6 mm (4.0 inches)
Depth	150.0 mm (5.9 inches)
Weight	425 g (0.94 pound)

Table C-2. Environmental Limits

Attribute	Specifications
Operating temperature	5°C to 50°C ambient (40° (no condensation)
Non-Operating temperature	-40°C to 60°C (-40°F to 1 (no condensation)
Operating relative humidity	8% to 80%, with a wet bu 29°C and no condensatio
Non-Operating relative humidity	5% to 95%, with a wet bu 29°C and no condensatio

Table C-3. Vibration and Shock Specifica

Attribute	Specificat Operating	I
Vibration 10Hz to 500 Hz continuous vibration	0.5G max.	2
Shock 1/2 sine wave for 11 msec	5.0G max.	1

Table C-4. Power Consumption

Attribute	Specifications
Stand-by	0.1W max
Operation (Read/Write mode)	1.1W typ.

NOTE: Stand-by is specified under the conditions
1. **The drive is NOT selected.**
2. **The DIRECTION and the HEAD SELECT lines are low. The other lines are false (high).**

Table C-5. Supply Voltage

Voltage	Max. Ripple	Current
+5.0V ± 10%	0.1Vpp	20 mA max. (Standby) 220 mA typ. (Read/Write) 680 mA max. (Motor Starts) 890 mA max. (Step during motor rotation)

C-1-3 Performance Specifications

Table C-6. Recording Capability

Attribute	Specifications	
	2MB mode	1MB mode
Recording Capacity (unformatted, MFM)	2Mbytes/disk 1Mbytes/disk	1Mbytes/surface 0.5Mbytes/surface
Recording density (Side 1, Track 79)	17,434 BPI	8,717 BPI

Table C-7. Data Transfer Rates

Burst transfer rate	500Kbits/sec for MFM (2MB m 250Kbits/sec for MFM (1MB m

Table C-8. Timing Specifications

Description	Timing Specifications
Track to Track slew Rate	3 msec
Head Setting Time	15 msec max.
Average Access Time	94 msec
Motor Start Time	500 msec max.
Rotational Latency	100 msec ave.
Rotation Speed	300 rpm
The continuous speed variation is within ±1.5%	
The instantaneous speed variation is within ±1.5%	

Table C-9. Structure

Attribute	Specifications
Track Density	135 TPI
Number of Cylinders	80
Number of Tracks	160
R/W Heads	2

Table C-10. Reliability

Attribute	Specifications
Mean Time Between Failure (MTBF)	30,000 POH
Mean Time To Repair (MTTR)	30 minutes
Preventive Maintenance (PM)	Not Required
Component life	5 years or 15,000 POH
Error Rate:	
1. Soft Read Error	1 per 10^9 bits read
2. Hard Read Error	1 per 10^{12} bits read
3. Seek Error	1 per 10^6 seeks

C-2 TEAC-55GFR-159 Mini Flexible Disk Drive

C-2-1 General

The FDD is equipped with an input signal for switching high/normal densities. It can read and write the data of 5.25", 96tpi, single/double sided flexible disks, and it can also read the data of conventional 5.25", 48tpi, single/double sided disks.
For the normal density mode, two disk rotational speeds are offered for selection using internal switching strap. One is 300rpm which is currently used in 5.25" FDDs and the other is 360rpm which is the same speed as in high density mode.

C-2-2 Physical Specifications

Table C-11. Mechanical Dimensions

Attribute	Specifications
Height	41.3 mm (1.63 in), Nom.
Width	146 mm (5.75 in), Nom.
Depth	203 mm (7.99 in), Nom.
Weight	1.00 kg (2.20 lbs), Nom.
	1.10 kg (2.43 lbs), Max.

Table C-12. Environmental limits

Attribute	Specifications
Operating Temperature	4°C to 46°C ambient (40°F to 115°F)
Non Operating : Storage Transportation	-22°C to 60°C (-8°F to 140°F) -40°C to 65°C (-40°F to 149°F)
Operating relative humidity	20% to 80% (no condensation) with max. wet bulb temperature of 29°C.
Non-operating Storage	10% to 90 (no condensation) with max. wet bulb temperature of 40°C.
Non-operating Transportation	5% to 95% (no condensation) with max. wet bulb temperature of 45°C.

Table C-13. Vibration and Shock Specifications

AttributeSpecifications	**Operating**	**Transportation**
Vibration:		
less than 55Hz	0.5G max.	
55 - 500Hz	0.25G max.	
less than 100Hz		2G max.
Shock:		
less than 11 msec	5.0G max.	50G max.
Altitude:	less than 5,000m (16,500 feet)	less than 12,000m (40,000 feet)

Table C-14. Power Consumption

Attribute	**Specifications**
Waiting	1.0W typ.
Operating	4.0W typ.

Table C-15. Supply Voltage

Voltage	Max. Ripple	Current	
DC + 12V	200mVpp	operating	220 mA typ. Read/Write
tolerence R/W ± 5% others ± 10%			540 mA max. average 1.0 A max. 400msec, max. at spindle motor start
		waiting	10 mA typ. Spindle motor off 20 mA max. spindle motor off
DC + 5V tolerence ± 5%	100mVpp	operating	280 mA typ. Read/Write 350 mA max. average 430 mA Peak
		waiting	180 mA typ 230 mA max

C-2-3 Performance Specifications

Table C-16. High Density Mode Data Capacity

Recording method		**FM**	**MFM**
Data transfer rate (K bits/sec)		250	500
Tracks/disk		154 (160)	154 (160)
Innermost track bit density (bpi)		4823 (4935)	9646 (9870)
Innermost track flux density (frpi)		9646 (9870)	9646 (9870)
Data capacity			
Unformatted	(Kbytes/track)	5.208	10.416
	(Kbytes/disk)	802.0 (833.3)	1604
Formatted 26 sectors/track	(Kbytes/sector)	0.128	0.256
	(Kbytes/track)	3.328	1604.1 (1666.6)
	(Kbytes/disk)	512.5 (532.5)	1025.0 (1065.0)
Formatted 15 sectors/track	(Kbytes/sector)	0.256	0.512
	(Kbytes/track)	3.840	7.680
	(Kbytes/disk)	591.4 (614.4)	1182.7 (1228.8)
Formatted 8 sectors/track	(Kbytes/sector)	0.512	1.024
	(Kbytes/track)	4.096	8.192
	(Kbytes/disk)	630.8 (655.4)	1261.6 (1310.7)

NOTE: Up to 80 cylinders are available for the FDD. The table in the blackets are for 80 cylinder's operation (160 tracks).

Table C-17. Normal Density Mode Data Capacity

Recording method		FM	MFM
Data transfer rate (Kbits/sec)			
Dual speed (300rpm)		125	250
Single speed (360rpm)		150	300
Tracks/disk		160	160
Innermost track bit density (bpi)		2961	5922
Innermost track flux density (frpi)		5922	5922
Data capacity			
Unformatted	(Kbytes/track)	3.125	6.250
	(Kbytes/disk)	500	1000
Formatted 16 sectors/track	(Kbytes/sector)	0.128	0.256
	(Kbytes/track)	2.048	4.096
	(Kbytes/disk)	327.68	655.36
Formatted 9 sectors/track	(Kbytes/sector)	0.256	0.512
	(Kbytes/track)	2.304	4.608
	(Kbytes/disk)	368.64	737.28

Table C-18. Disk Rotation Mechanism

Attribute	Specifications
Spindle motor	Direct DC brushless motor
spindle motor speed	
Dual speed	360rpm (high density) /300rpm (normal density)
Single speed	360rpm (high and normal densities)
Motor servo method	Frequency servo by AC tachometer and ceramic oscillator
Start Time, 360rpm	less than 500 msec
300rpm	less than 400 msec
Average latency, 360rpm	83.3 msec
300rpm	100 msec
Speed change time (360rpm ⇄ 300rpm)	less than 400msec (only for dual speed mode)

Table C-19. Track Construction

Attribute	specifications
Track Density	96 TPI
Number of Cylinders	
high density mode	77
normal density mode	80
Number of Tracks	
high density mode	154
normal density mode	160
Magnetic head (Read/Write)	2 sets.

Table C-20. Reliability

Attribute	Specifications
Mean Time Between Failure (MTBF)	20,000 POH
Mean Time To Repair (MTTR)	30 minutes
Preventive Maintenance (PM)	Not Required
Component life	5 years
Error Rate:	
1. Soft Read Error	1 per 10^9 bits
2. Hard Read Error	1 per 10^{12} bits
3. Seek Error	1 per 10^6 seeks
Safety standard	Complying with UL

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