
DEC LANcontroller
400

DEC LANcontroller 400 Installation Guide

Order Number: EK-DEMNA-IN-001

The DEC LANcontroller 400 adapter (also known as the DEMNA controller) is an Ethernet/802 controller for systems that have an XMI bus. This guide is intended for use by Digital customer service representatives and self-maintenance customers.

digital equipment corporation
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Preface

Purpose of This Manual

This manual describes how to install the DEC LANcontroller 400 adapter. The DEC LANcontroller 400 provides an interface between an Ethernet/IEEE 802 local area network and a system that has an XMI bus.

This manual also describes the adapter's self-test and gives advice for troubleshooting.

The DEC LANcontroller 400 is also known as the DEMNA controller. Throughout the rest of this manual, the DEC LANcontroller 400 is referred to as the DEMNA.

Intended Audience

This manual is for Digital and customer personnel who install or replace the DEMNA in the field.

Document Structure

This manual has three chapters and nine appendixes, which are described below:

Chapter 1 briefly describes the DEMNA module, its functions, its logic, and what you should have received.

Chapter 2 describes installation of the module.

Chapter 3 describes the DEMNA self-test and how to interpret the results.

Appendix A gives environmental requirements for the DEMNA module.

Appendix B gives register information.

Appendix C describes how to convert an Ethernet address to a DECnet address.

Appendix D describes three customer-modifiable flags in DEMNA EEPROM and indicates how to modify the flag settings.

Appendix E lists the device type codes of all XMI modules available at the printing of this manual.

Appendix F lists some commonly used Ethernet protocol types.

Appendix G lists some commonly used multicast addresses.

Appendix H lists some commonly used 802 SAPs and SNAP SAP protocol IDs.

Appendix I describes how to read the DEMNA Ethernet address.

Associated Documents

Related documentation includes:

- *DEC LANcontroller 400 Console User's Guide*, EK–DEMNA–UG
- *DEC LANcontroller 400 Programmer's Guide*, EK–DEMNA–PG
- *DEC LANcontroller 400 Technical Manual*, EK–DEMNA–TM
- *Ethernet Installation Guide*, EK–ETHER–IN
- *VAX 9000 Family System Maintenance Guide, Vol. 2*, EK–KA902–MG
- *VMS Network Control Program Manual*, AA–LA50A–TE

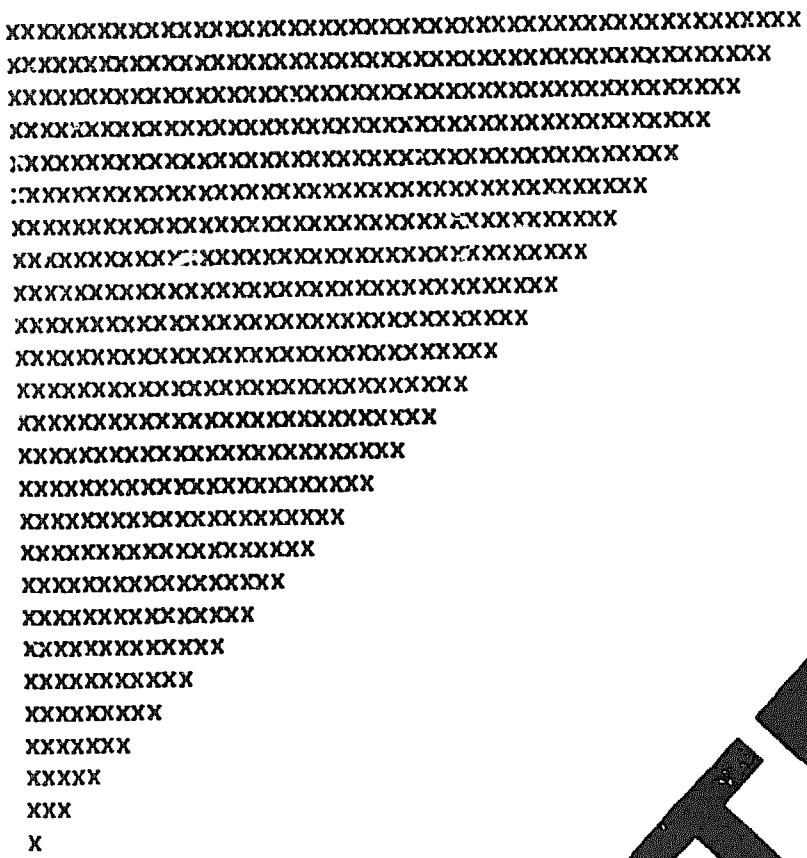
Conventions Used

- All addresses are in hexadecimal (hex). All bit patterns are in binary notation. All other numbers are decimal unless otherwise indicated.
- Ranges are inclusive. For example, the range 0–4 includes the integers 0, 1, 2, 3, 4.
- Bits are enclosed in angle brackets (for example, <12>).
- Bit ranges are indicated by two bits in descending order separated by a colon; for example, <12:1>. Bit ranges are inclusive.
- K = kilo (1024); M = mega (1024**2); G = giga (1024 **3).
- The term "asserted" indicates that a signal line is in the true state. The term "deasserted" indicates that a signal line is in the false state. "Assertion" is the transition from the false to the true state. "Deassertion" is the transition from the true to the false state.

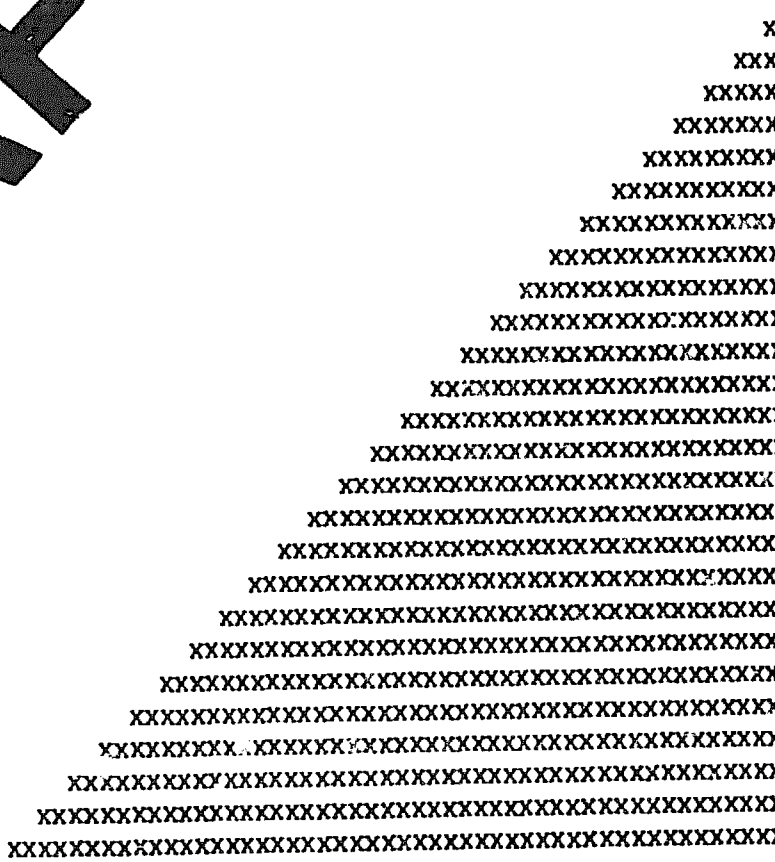
Command Notation

The following command notation is used in this manual:

Convention	Meaning
{ }	Large braces enclose lists from which you must choose one item. For example: { KERNEL / USER }
. . .	Horizontal ellipsis points mean that you can repeat the item preceding the points. For example: */qualifier* . . .
. . .	Horizontal or vertical ellipsis points in an example indicate that not all the information the system would display is shown or that not all the information a user is to supply is shown.
{ }, . . .	Braces followed by a comma and horizontal ellipsis points mean that you can repeat the enclosed items one or more times, separating two or more items with commas.
[ ]	Square brackets enclose items you can omit. For example: [=*option*, . . .]
UPPERCASE characters	Language-specific reserved words and identifiers are printed in uppercase characters. However, you can enter them in uppercase, lowercase, or a combination of uppercase and lowercase characters.
italic lowercase characters	Elements you must replace according to the description in the text are printed in italic lowercase characters. However, you can enter them in lowercase, uppercase, or a combination of lowercase and uppercase characters.



CHAPTER 1



1 DEC LANcontroller 400 Module Overview

The DEC LANcontroller 400 is an intelligent, high-performance I/O controller that enables a host processor on the XMI bus to communicate with other nodes in an Ethernet/802 local area network. The DEC LANcontroller 400 is compatible with the Ethernet and IEEE 802 specifications.[1] Digital's *Systems and Options Catalog* indicates which systems support the DEMNA option.

A single XMI bus can support multiple DEC LANcontroller 400s. An XMI bus can thus connect to multiple Ethernet/802 networks. Each DEC LANcontroller 400 connects to a single network through a standard 15-pin Sub-D connector.

The DEC LANcontroller 400 is also called the DEMNA controller. Throughout the rest of this manual, the DEC LANcontroller 400 is referred to as the DEMNA.

1.1 BASIC FUNCTIONS

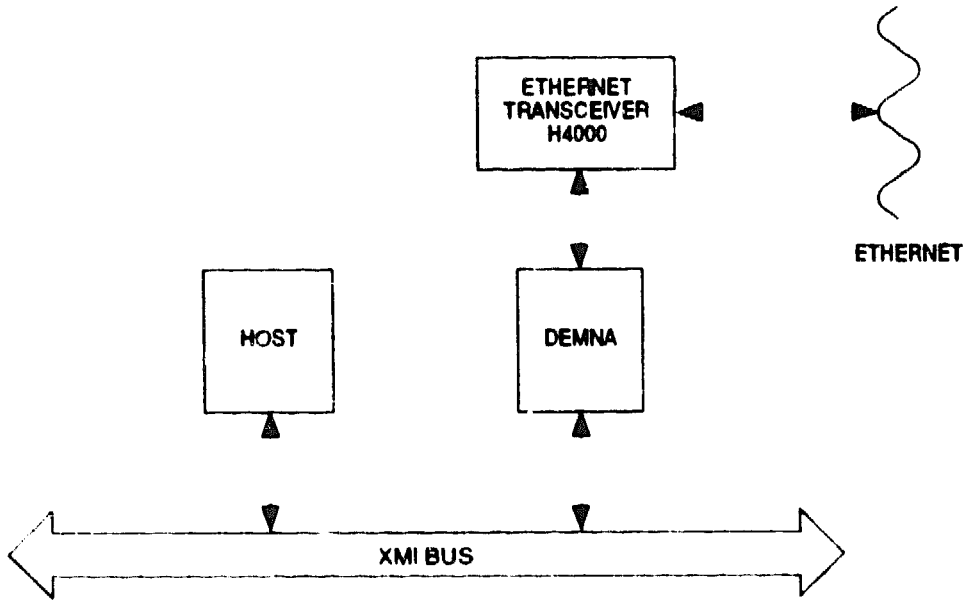
The DEMNA supports one Ethernet/IEEE 802 port, which provides the physical link layer and portions of the data link communication layer of the Ethernet and 802 protocols, as defined by the Ethernet and IEEE 802 specifications.

With its own onboard CVAX processor, the DEMNA can control operations independently of the host processor. The details of Ethernet transactions, including data transfer over the XMI bus, are thus transparent to the host processor (see Figure 1–1).

The onboard firmware is contained in EEPROM, which allows revised firmware to be loaded without hardware modification. The firmware can thus be easily upgraded in the field. In addition, various DEMNA operating parameters can be modified easily in the field.

[1] In this manual, 802 refers specifically to the CSMA/CD local area network defined in the IEEE 802.2 and 802.3 specifications (physical and data link layers).

Figure 1–1 DEMNA Module In an XMI System



The DEMNA firmware includes a console monitor program that allows a user at virtually any terminal on the network to monitor DEMNA operation and network traffic. The console monitor program can be accessed over the network or from a terminal (called the physical console) attached directly to the DEMNA. (See the *DEC LANcontroller 400 Console User's Guide*, *DEC LANcontroller 400 Technical Manual*, or the *DEC LANcontroller 400 Programmer's Guide* for a description of the console monitor program.)

The DEMNA has extensive onboard tests. On power-up or reset, the DEMNA tests itself and makes its status (pass or fail) available through LEDs on the module and through an onboard Power-Up Diagnostic (XPUD) Register. In addition, a customer service engineer may invoke other onboard diagnostics from the system console or the DEMNA physical console to test the DEMNA's logic and functionality more extensively.

The DEMNA may participate in network boot operations. The DEMNA may be specified as the boot device by its host system or be enabled to involuntarily boot its host system on receiving a valid Boot message over

the network. (See the *DEC LANcontroller 400 Technical Manual* for further information.)

1.2 LOGIC OVERVIEW

The DEMNA logic is divided into the following four subsystems, as shown in Figure 1–2:

- Microprocessor subsystem
- Shared memory subsystem
- XMI interface subsystem
- Ethernet interface subsystem

1.2.1 Microprocessor Subsystem

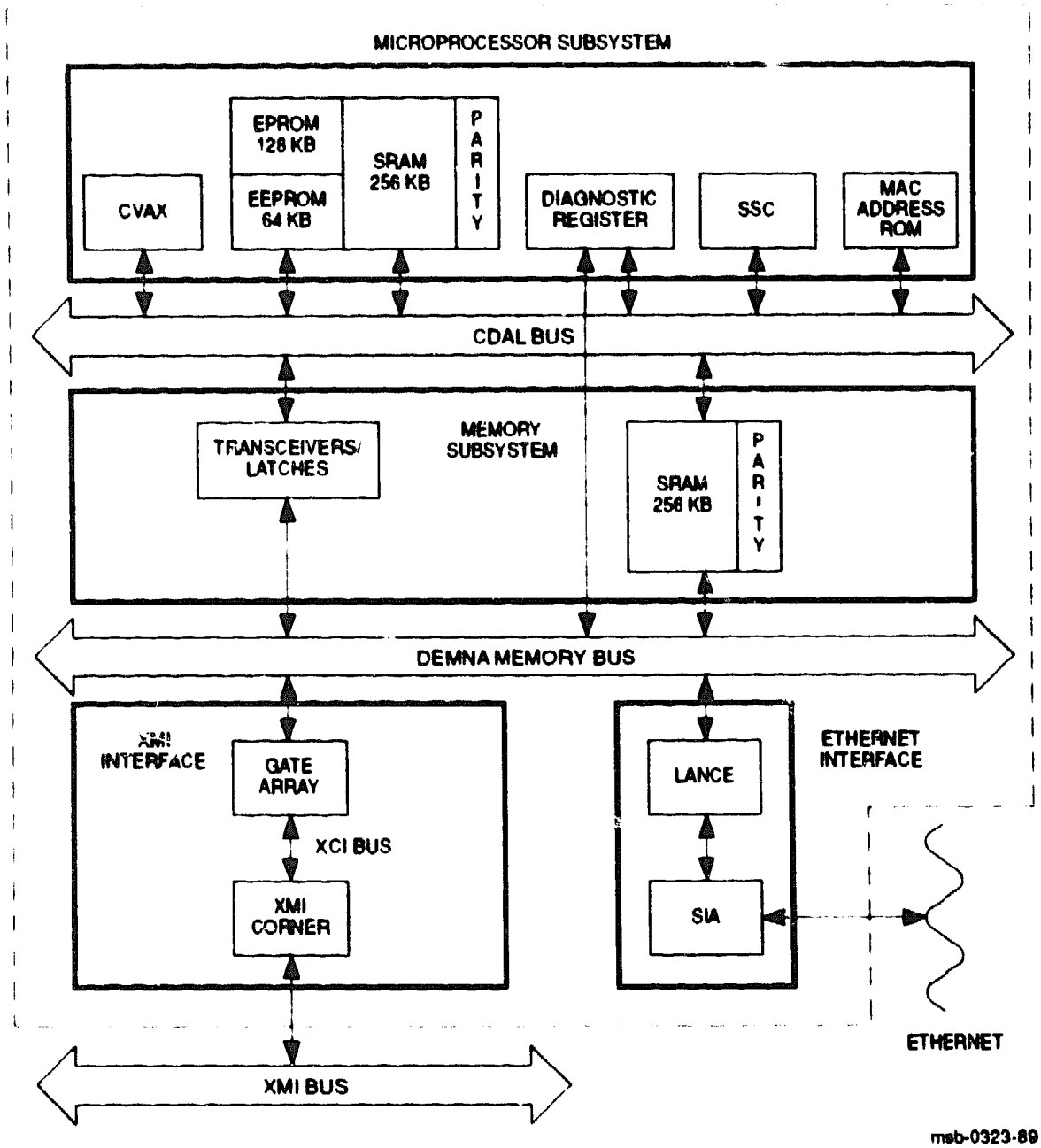
The microprocessor subsystem performs the following major functions:

- Stores and executes the module firmware, including onboard diagnostics and the console monitor program
- Stores and supplies the module's default (MAC) Ethernet address

The microprocessor subsystem contains the following major components:

- CVAX—a 32-bit CMOS processor dedicated to running firmware. The CVAX cannot be used directly by application programs running on the host processor or by a user at the system console.
- System Support Chip (SSC)—This chip provides control logic for the microprocessor subsystem, including timers, address decode logic, internal processor registers, and a UART for connection with the DEMNA physical console.
- EEPROM and CVAX RAM—The EEPROM stores the module's operational firmware, which executes from CVAX RAM (SRAM). The EEPROM also stores history data on DEMNA failures and errors.

Figure 1–2 DEMNA Simplified Block Diagram



- MAC Address (ENET) PROM—This PROM stores the module's default physical (Ethernet) address (DPA),[1] which is also called the Medium Access Control (MAC) address. The PROM also stores a PROM test pattern.
- EPROM—The EPROM stores a working copy of the DEMNA firmware minus the console monitor program. If the DEMNA self-test finds that the EEPROM contents are invalid, the EPROM code is loaded into CVAX RAM so that diagnostics can be executed.
- Diagnostic Register—This register is a control/status register that controls certain low-level diagnostic operations, such as the disabling of CVAX RAM parity.

The CVAX, SSC, CVAX RAM, and Diagnostic Register connect to each other through the CDAL bus, which in turn connects to the DEMNA memory bus through latched transceivers.

1.2.2 Shared Memory Subsystem

The shared memory subsystem performs the following major functions:

- Buffers packets to and from the Ethernet interface
- Buffers transfers to and from the XMI bus
- Stores shared data structures that allow the CVAX and LANCE to communicate

The shared memory subsystem has the following major components:

- 256 Kbytes of parity-protected SRAM—The SRAM buffers Ethernet and XMI transfers and stores data structures shared by the CVAX and LANCE.
- Bus control logic—This logic controls read/write timing and read/write signals.
- DMA logic—This logic controls access to the SRAM.
- DEMNA timeout logic—This logic detects when a DMA grant on the DEMNA memory bus has been outstanding longer than the timeout period.

[1] At the request of applications starting up a protocol such as DECnet, the port driver may assign one or more alternative addresses to the DEMNA. This type of address is called an actual physical address (APA).

The SRAM is on the DEMNA memory bus, which connects to the Ethernet interface, XMI interface, and the CDAL bus. The SRAM can be accessed by the LANCE chip (Ethernet interface), CVAX, or DEMNA gate array (XMI interface). The DMA access priority for these devices is LANCE, CVAX, and gate array.

1.2.3 Ethernet Interface Subsystem

The Ethernet interface provides an interface between the DEMNA's shared memory and the Ethernet wire. The Ethernet interface performs transmits (reads) from the shared memory and receives (writes) to the shared memory.

The Ethernet interface has the following major components:

- Local Area Network Controller for Ethernet (LANCE) chip—The LANCE chip implements the microprocessor interface, performs DMA to and from the DEMNA shared memory, implements the CSMA/CD network access algorithm, does packet handling on transmits and receives, and reports errors.
- Serial Interface Adapter (SIA) chip—The SIA chip performs Manchester encoding for transmits, Manchester decoding for receives, and implements a TTL/differential signal interface between the LANCE (TTL) and the Ethernet wire (differential signals).
- Bus interface logic—This logic generates byte parity on transfers to DEMNA shared memory and checks byte parity on transfers from shared memory.

1.2.4 XMI Interface Subsystem

The XMI interface provides an interface between the DEMNA's shared memory and the XMI bus. The XMI interface performs the following major functions:

- Transfers Ethernet read and write data between DEMNA shared memory and host memory
- Performs control operations for the DEMNA CVAX (high-priority quadword XMI reads and writes to memory and longword XMI I/O reads and writes)
- Implements the DEMNA port registers
- Implements the XMI-required registers

- Implements XMI interrupt logic

The XMI interface has the following major components:

- Gate array—The gate array implements most of the XMI interface logic.
- XMI resistors, clocks, and module-decoupling capacitors.
- XMI timeout logic—This logic detects timeouts for XMI operations.

1.3 PHYSICAL DESCRIPTION

The DEMNA option consists of a single board. The DEMNA has the following two cables:

- An internal Ethernet cable that connects the DEMNA with the transceiver cable and provides power to an H4000 transceiver (Section 2.4). This cable is not part of the DEMNA option but is included in the cabinet kits for the DEMNA.
- An internal cable for the physical console that connects the DEMNA with a terminal cable. This cable has its own cabinet kit.

An external Ethernet cable runs from the bulkhead to an Ethernet transceiver. This cable is not part of the DEMNA option and is not included in the cabinet kits for the DEMNA. The cable must be ordered separately. (See Digital's *Systems and Options Catalog* for more information.)

Table 1–1 lists the items on the DEMNA packing list. These are the items included with the DEBNI option (DEMNA-M).

Table 1–1 Packing List for DEMNA Option

Part Number	Quantity	Description
T2020	1	DEMNA module
EK-DEMNA-IN	1	*DEC LANcontroller 400 Installation Guide*
EK-DEMNA-RN	1	*DEC LANcontroller 400 Release Note*
EK-DEMNA-UG	1	*DEC LANcontroller 400 Console User's Guide*

1.3.1 Cabinet Kits

Table 1–2 lists DEMNA cabinet kits for VAX 6000 and 9000 systems. Cabinet kits must be ordered separately from the DEMNA option. For new systems not included in this table, please see Digital's *Systems and Options Catalog*.

Table 1–2 Cabinet Kits for DEMNA Options

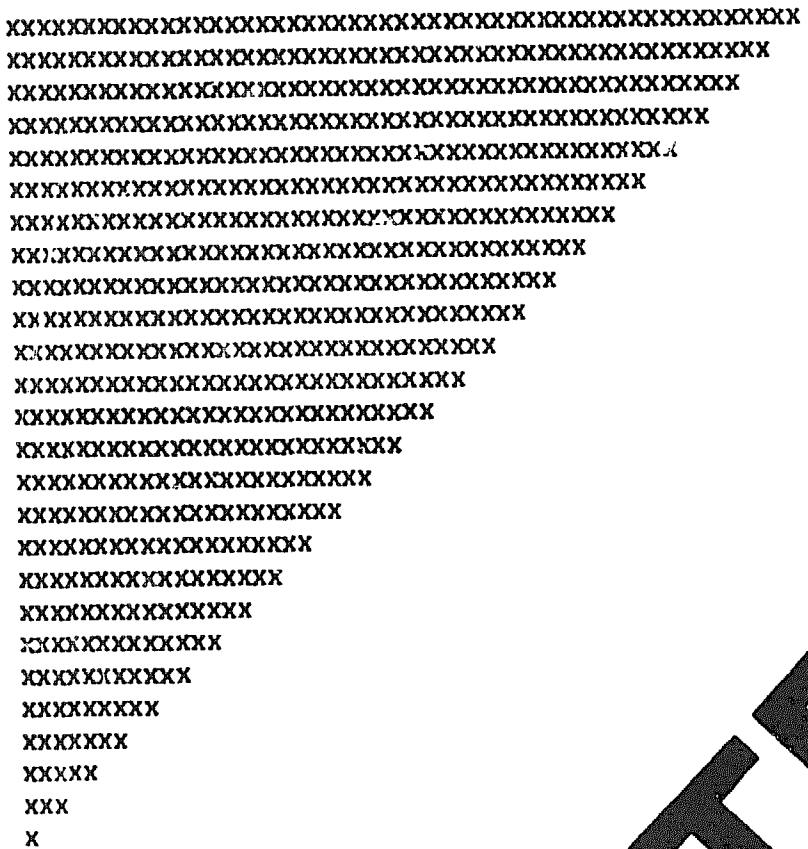
Description	Kit Number	Contents
Internal Cable for Physical Console	CK-DEMNA-AM	I/O connector panel for VAX 6000 cabinets (74-26407-32) I/O connector panel for VAX 9000 cabinets (70-28010-01) Blank panel for I/O connector panel (74-26407-01) Internal cable for physical console (17-02168-01) *DEC LANcontroller 400 Installation Guide* (EK-DEMNA-IN) *DEC LANcontroller 400 Console User's Guide* (EK-DEMNA-UG)
VAX 6000 cabinet kit	CK-DEMNA-KD	Ethernet I/O connector panel (74-26407-41) 8-ft. internal Ethernet cable (17-01496-02) Blank panel (74-26407-01) Ethernet loopback connector (12-22196-02)
VAX 9000 Model 2xx cabinet kit	CK-DEMNA-KE	Ethernet I/O connector panel (70-27894-01) 3-ft. internal Ethernet cable (17-01496-01) Ethernet loopback connector (12-22196-02)
VAX 9000 Model 4xx cabinet kit	CK-DEMNA-KM	Ethernet I/O connector panel (70-27894-01) 8-ft. internal Ethernet cable (17-01496-02) Ethernet loopback connector (12-22196-02)

1.3.2 Status LEDs

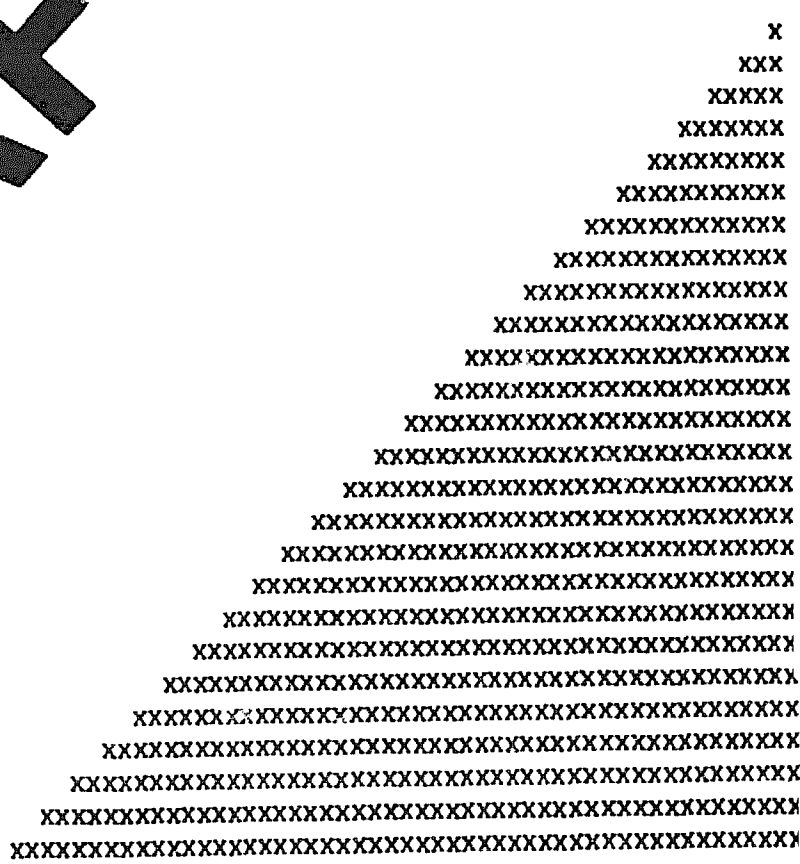
The DEMNA module has two status-indicator lights:

- One DEMNA OK LED (yellow)—the self-test LED required by the XMI bus specification
- One External Loopback LED (green)

Immediately after power-up or reset, both status-indicator lights are off. If all the tests in the self-test pass (except the LANCE external loopback test), the self-test lights the yellow DEMNA OK LED. If the LANCE external loopback test passes (indicating that the DEMNA can transmit and receive a loopback packet over the network), the self-test lights the green External Loopback LED.



CHAPTER 2



2 Installation

This chapter explains how to install the DEMNA option into a system that has an XMI bus. The installation procedure has three major parts:

- Hardware Installation
- Verification of Hardware Installation
- Verification of DEMNA Operation in Network

It is very important to perform all parts of the installation procedure. Do not skip any part of the procedure.

The installation procedure does not describe how to install an Ethernet transceiver. For instructions on installing an Ethernet transceiver, see the installation guide for the host computer system.

WARNINGS

POWER OFF—Shut off system power and disconnect the system power cord before performing any procedure in this chapter.

WEAR ESD WRIST STRAP—You must wear an antistatic wrist strap that is connected to the processor cabinet whenever you work inside the cabinet.

USE CONDUCTIVE CONTAINERS—Whenever you remove a circuit board from an XMI card cage, place it in a conductive container.

2.1 HARDWARE INSTALLATION

When installing a DEMNA in a VAX 6000 system, use the procedure in Section 2.1.1. When installing a DEMNA in a VAX 9000 system, use the procedure in Section 2.1.2.

2.1.1 Hardware Installation in a VAX 6000 System

Up to three DEMNAs can be installed in an XMI card cage in a VAX 6000 system.

The following steps describe how to install the DEMNA hardware in a VAX 6000 system:

1 Power down the host computer system by:

   a. Turning the Power switch to the Off position

   b. Setting the system circuit breaker in the rear to Off

2 Open front door of the cabinet.

3 Put on the ESD wrist strap that is attached to the system chassis. This grounds you and thus prevents you from damaging the electronic components by discharging static electricity.

4 Locate the XMI card cage. Figure 2–1 shows the location of the XMI card cage in a VAX 6000 system.

5 Remove the door on the front of the XMI card cage.

6 Determine the slot into which the DEMNA should be installed. In a VAX 6000 system, the DEMNA can be put into any of the following slots: 1–4, B–E (see Figure 2–2). In general, the DEMNA should be put in the highest-numbered slot available within the ranges specified above. CPUs are usually put in lower-numbered slots.

7 Lift the lever to open the chosen slot.

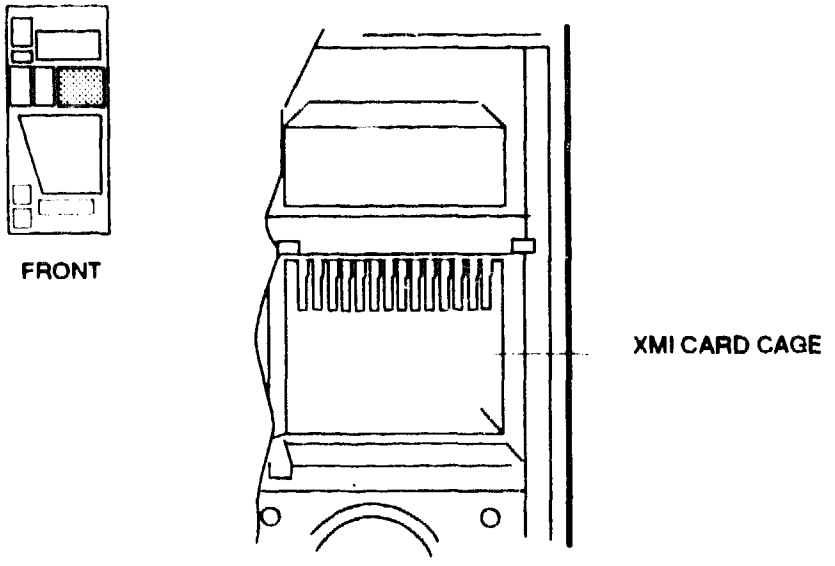
8 Slide the DEMNA module into the slot until it stops: this is a zero-insertion-force card cage.

9 Close the locking lever.

10 Replace the door on the front of the card cage.

11 Install an I/O connector panel (74-26407-41) for an Ethernet connector over one of the bulkhead cutouts. If you are replacing the first Ethernet controller in the system, this is unnecessary.

Figure 2–1 Location of XMI Card Cage in a VAX 6000 System



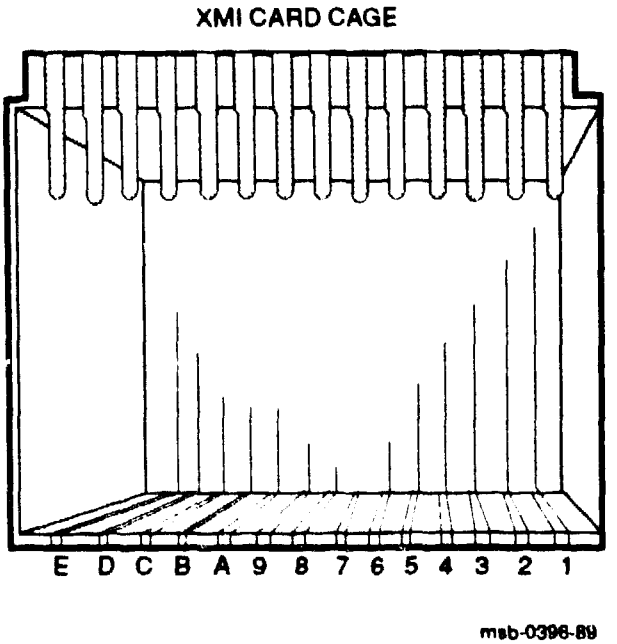
12 Install the internal Ethernet cable as follows:

a. Connect the P1 connector of the internal Ethernet cable to backplane segment E2 for the DEMNA slot (see Figure 2–3). The connector is right-side-up when the key on the connector is on the right. The P1 connector is not uniquely keyed for backplane segment E2. It is thus possible to insert the connector into the wrong backplane segment.

CAUTION

Do not connect the DEMNA to the network until you have verified the DEMNA installation. If the DEMNA cabling is connected to the wrong slot, an arbitrary signal may be output on the transmit line, which might bring down the entire network.

Figure 2–2 XMI Card Cage Slots



b. Attach the P2 connector of the internal Ethernet cable to the I/O connector panel. (If you are replacing the first Ethernet controller in a VAX 6000 system, connect the P2 connector to the system interconnect panel. The P2 connector plugs into the rear of the Ethernet connector on the panel. Figure 2–4 shows the system interconnect panel for a VAX 6000 Model 400 system.)

c. Connect the pigtail connector (P3) from the internal Ethernet cable to a +15V 2-prong connector (J2) from any of the H7214 power supplies. These power supplies are located in the rear of the cabinet.

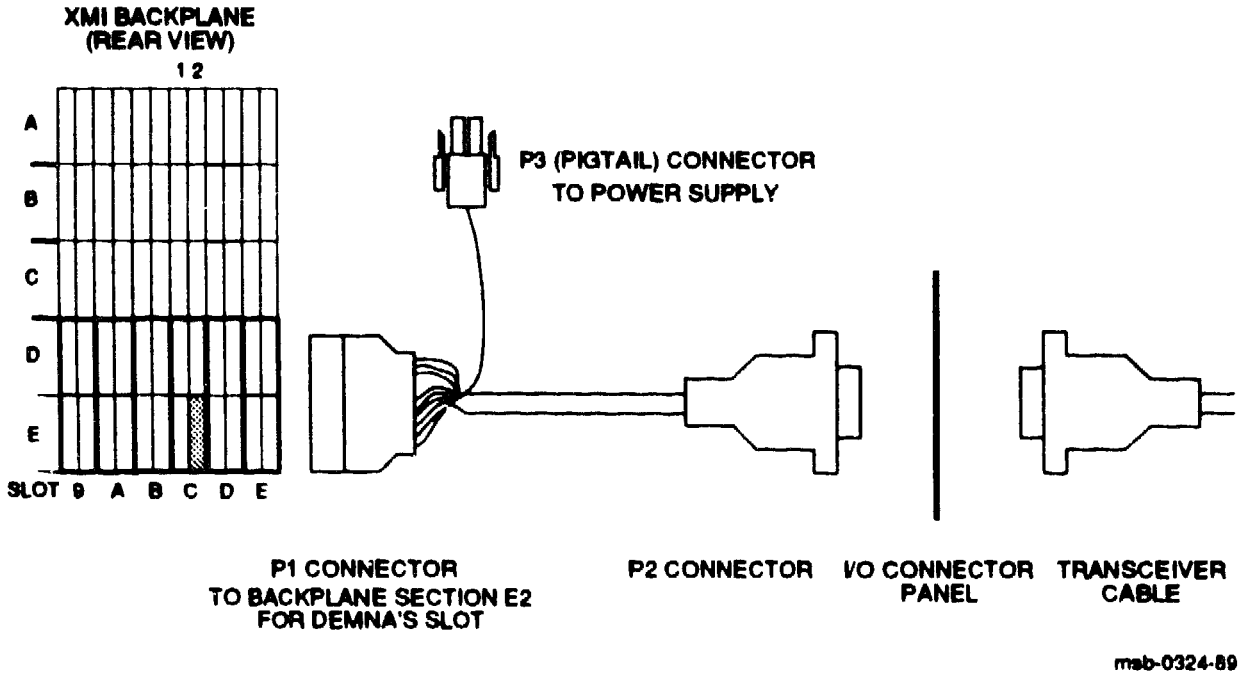
NOTE

All the connectors from the power supply may already be used. In this case, the external transceiver cable must not be connected directly to an H4000 transceiver, a DESTA (a thin-wire box), or a DECOM broadband transceiver—none of which has its own power supply. The transceiver cable may, however, be connected to one of the following devices, each of which has its own

power supply and which, in turn, may be connected to an H4000:

- **A DELNI**
- **A DEMPR (a thin-wire version of the DELNI)**
- **A DEBET (a bridge)**

Figure 2–3 Internal Ethernet Cable Connections



13 If a physical console is going to be used, install the internal cable for the physical console as follows:

a. Install an I/O connector panel (74-26407-32) for the cable over one of the bulkhead cutouts.

b. Connect the P1 connector of the cable to backplane segment D2 for the DEMNA slot (see Figure 2–5). The connector is right-side-up when the key on the connector is on the right. The P1 connector is not uniquely keyed for backplane segment D2. It is thus possible to insert the connector into the wrong backplane segment.

c. Attach the P2 connector of the cable to the I/O connector panel.

Figure 2–4 System Interconnect Panel—VAX 6000 Model 400 System

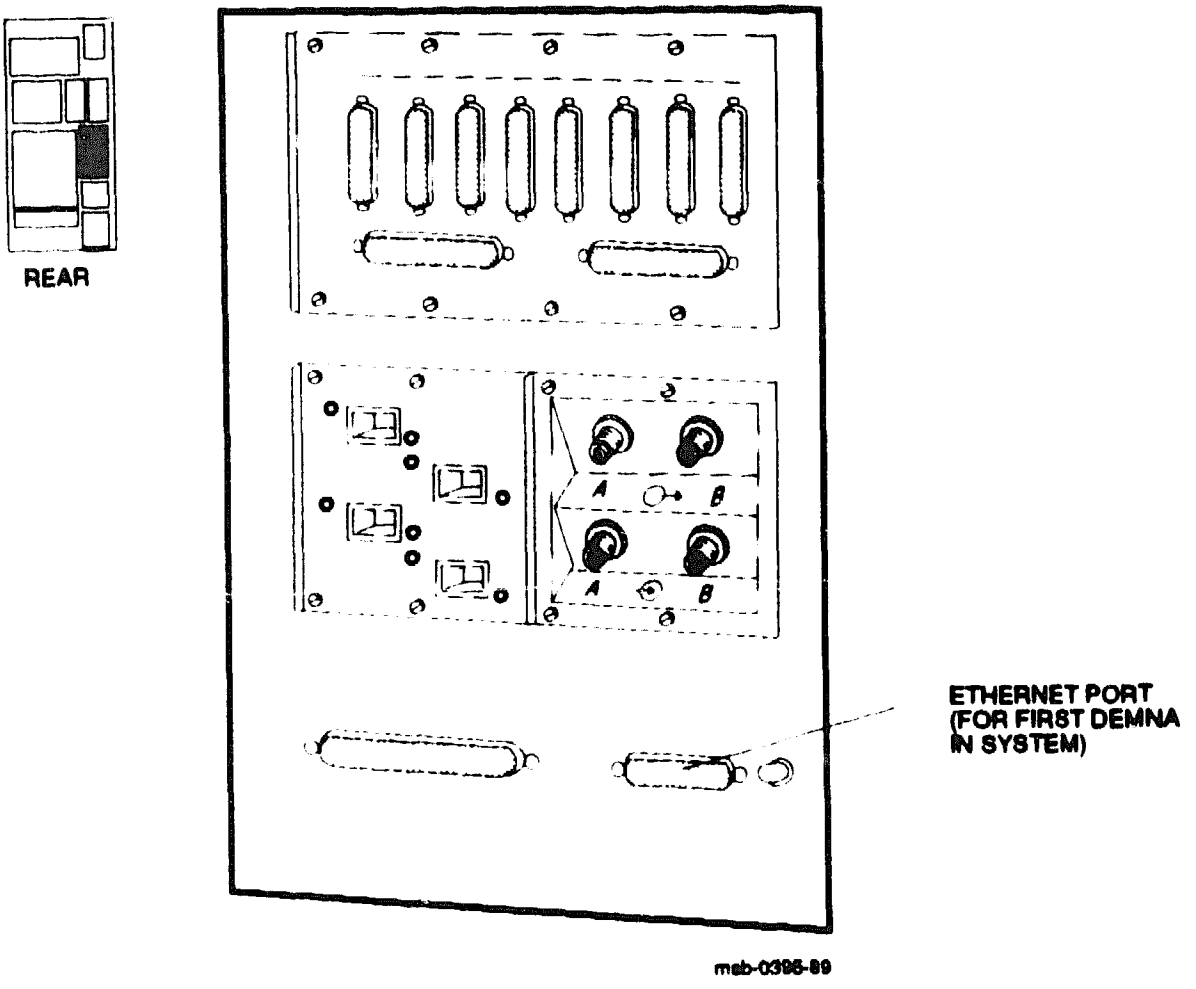
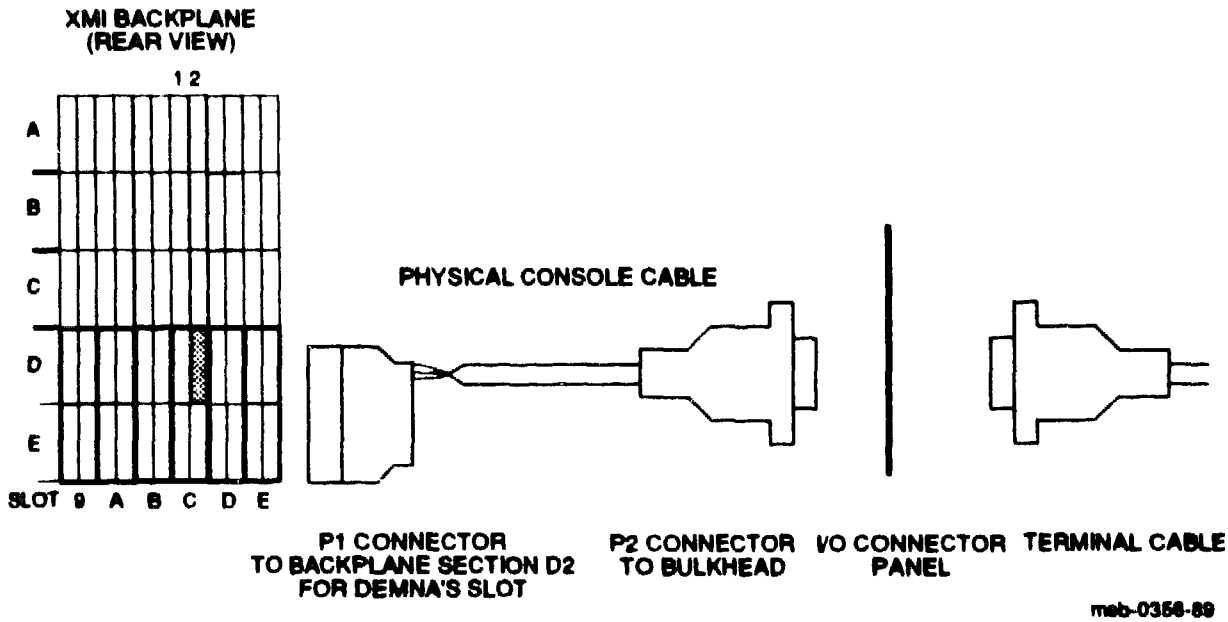


Figure 2–5 Internal Cable for Physical Console



2.1.2 Hardware Installation in a VAX 9000 System

Up to four DEMNAs can be installed per XMI card cage in a VAX 9000 system.

The following steps describe how to install the DEMNA hardware in a VAX 9000 system:

1 Power down the host computer system by:

   a. Turning the Power switch to the Off position

   b. Setting the appropriate system circuit breaker(s) to Off

2 Open front door of the appropriate cabinet.

3 Put on the ESD wrist strap that is attached to the system chassis. This grounds you and thus prevents you from damaging the electronic components by discharging static electricity.

4 Locate the XMI card cage into which the DEMNA is to be installed. Figure 2–6 shows the location of the XMI card cage in a VAX 9000 Model 2xx. Figure 2–7 shows the location of the XMI card cage in a VAX 9000 Model 4xx.

Figure 2–6 Location of XMI Card Cage in a VAX 9000 Model 2xx System

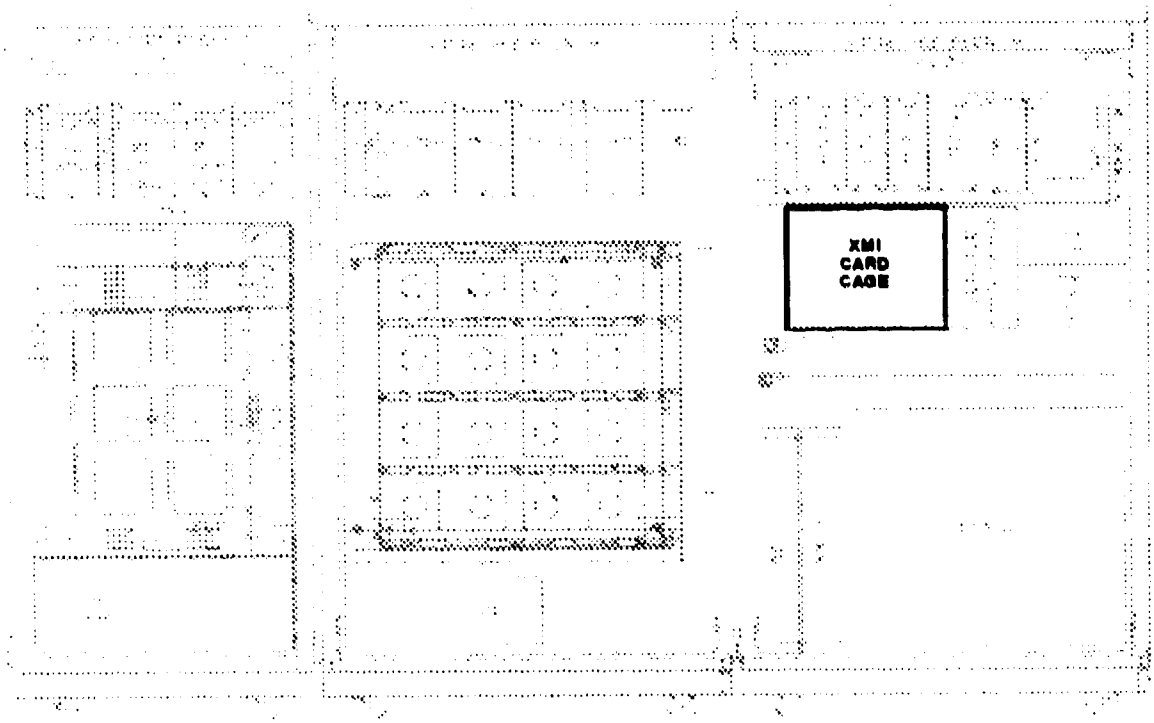
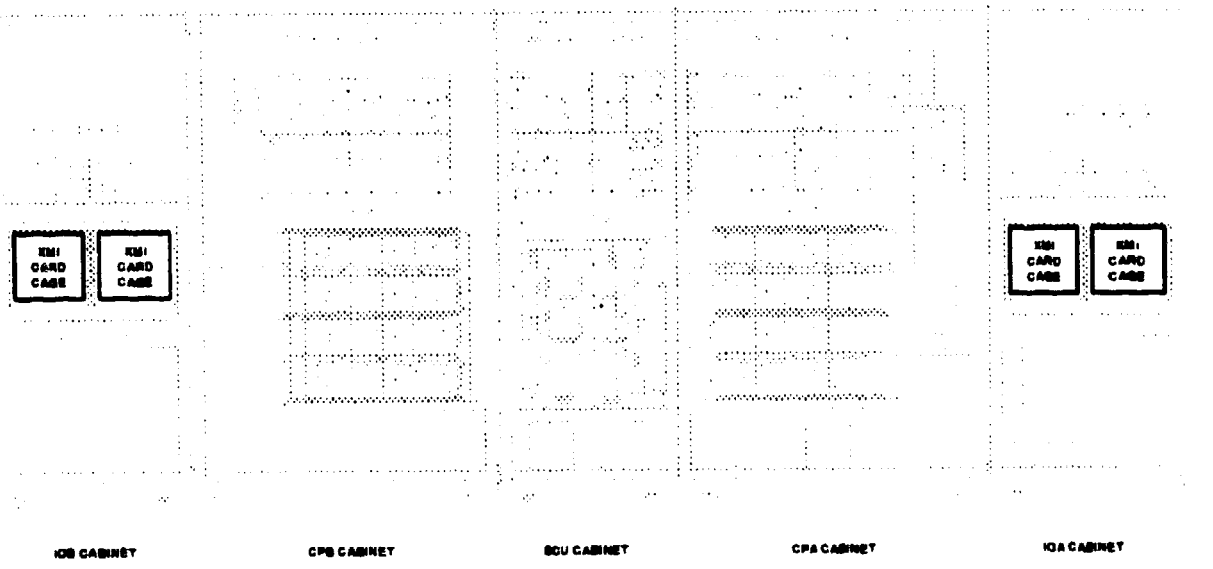


Figure 2–7 Location of XMI Card Cages in a VAX 9000 Model 4xx System



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5 Open the door on the front of the appropriate XMI card cage.

6 Determine the slot into which the DEMNA should be installed (see Figure 2–8). In a VAX 9000 system, the DEMNA can be put into any XMI slot except slot 7 or 8.

7 Lift the lever to open the chosen slot.

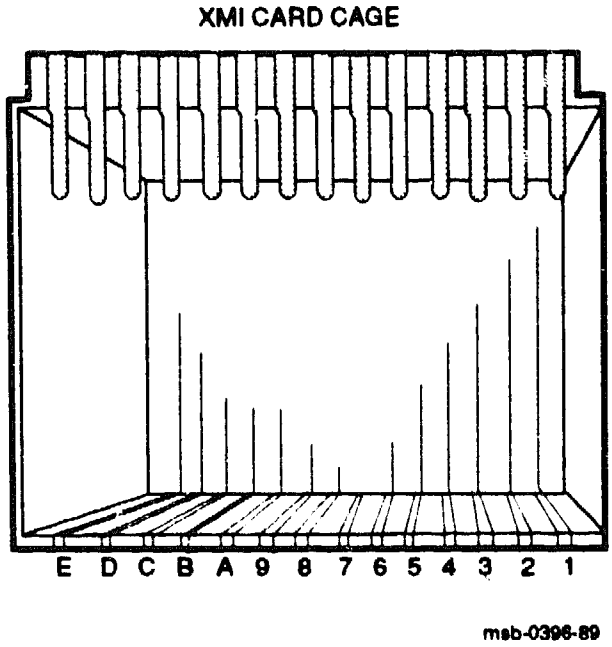
8 Slide the DEMNA module into the slot until it stops: this is a zero-insertion-force card cage.

9 Close the locking lever.

10 Close the door on the front of the XMI card cage.

11 Install an I/O connector panel (70-27894-01) for an Ethernet connector over one of the bulkhead cutouts. (If you are installing the second DEMNA in the cabinet, this is unnecessary, since the I/O connector panel accommodates two DEMNAs.)

Figure 2–8 XMI Card Cage



12 Install the internal Ethernet cable as follows:

a. Connect the P1 connector of the internal Ethernet cable to backplane segment E2 for the DEMNA slot (see Figure 2–9). The connector is right-side-up when the key on the connector is on the right. The P1 connector is not uniquely keyed for backplane segment E2. It is thus possible to insert the connector into the wrong backplane segment.

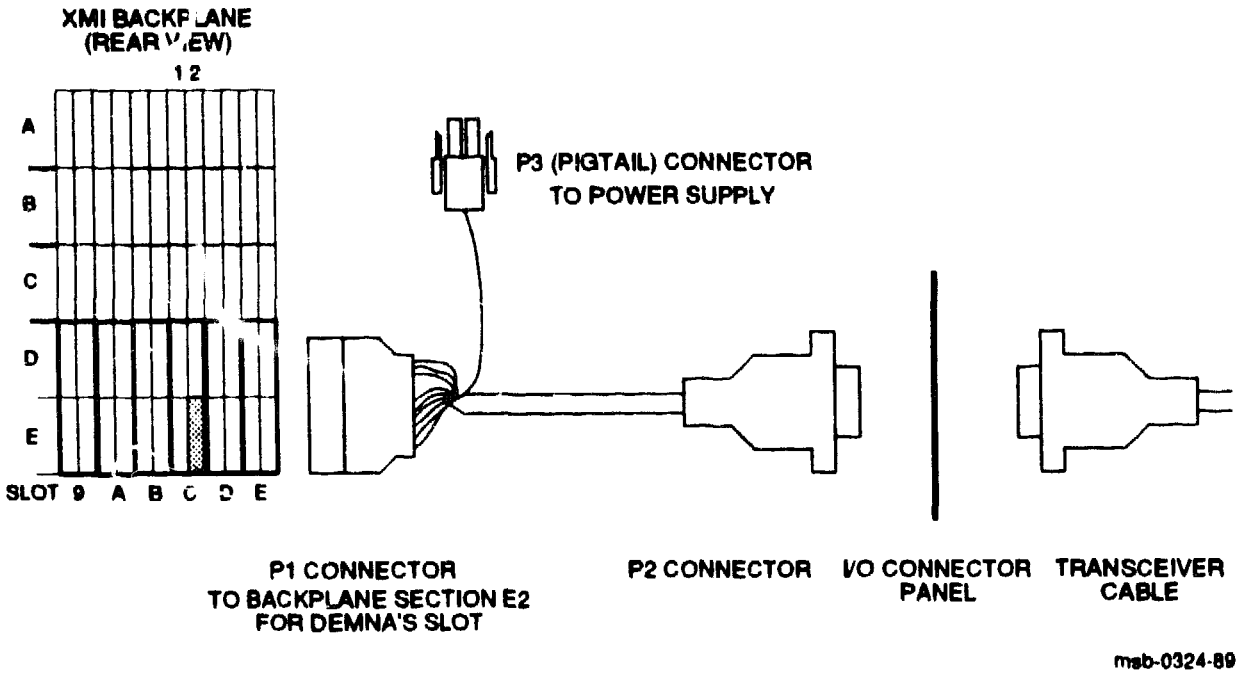
CAUTION

Do not connect the DEMNA to the network until you have verified the DEMNA installation. If the DEMNA cabling is connected to the wrong slot, an arbitrary signal may be output on the transmit line, which might bring down the entire network.

b. If you are installing the second DEMNA in the cabinet, remove the plate over the second cutout of the I/O connector panel.

c. Attach the P2 connector of the internal Ethernet cable to the I/O connector panel.

Figure 2-9 Internal Ethernet Cable Connections

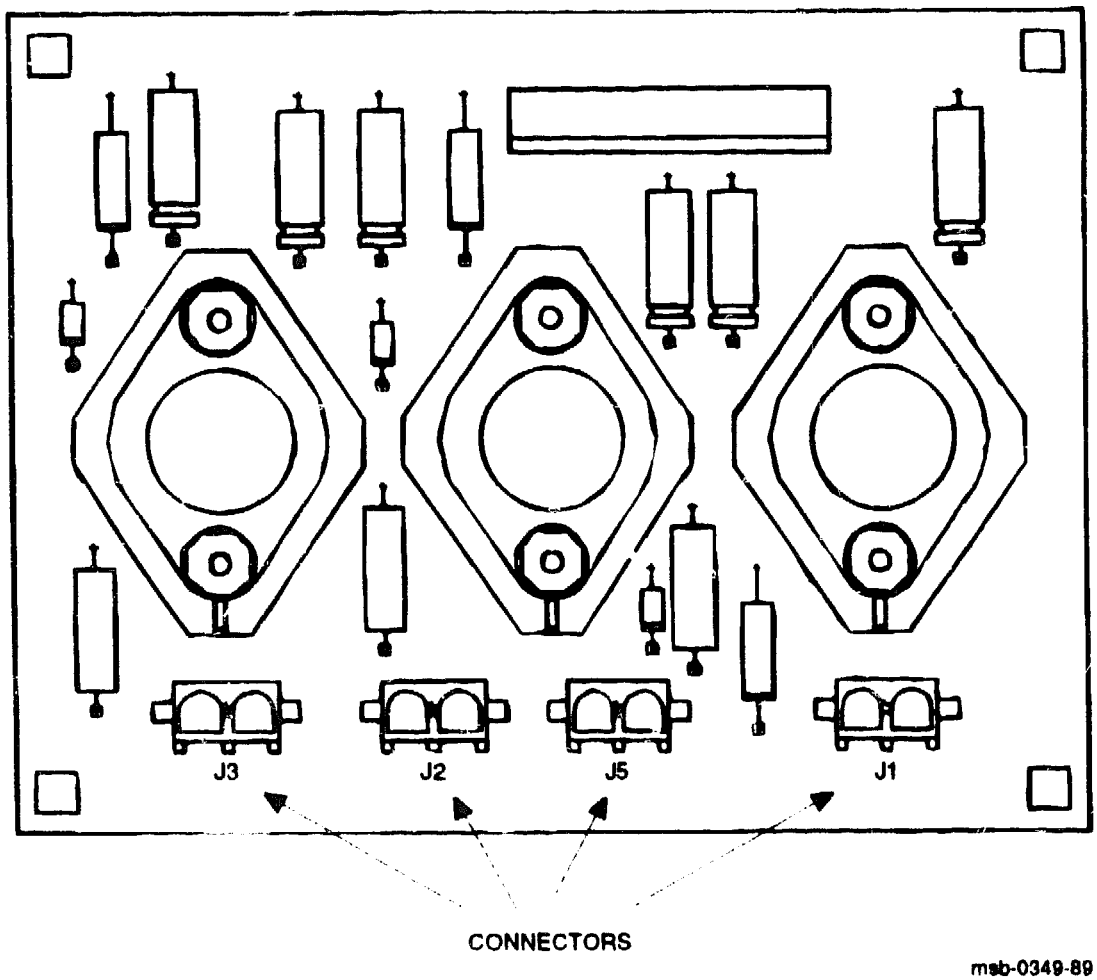


d. Connect the pigtail connector (P3) from the internal Ethernet cable to a +15V 2-prong connector on the power distribution adapter for the XMI card cage (see Figure 2–10). The J2 connector on the power distribution adapter is connected to the main power supply (H7214). The J1, J3, J5 connectors are connected to the auxiliary power supply. Table 2–1 summarizes the power connections for VAX 9000 systems.

Table 2–1 Power Connection for Internal Ethernet Cable—VAX 9000 Systems

System	Maximum Number of DEMNAs Per Card Cage	Power Connection
VAX 9000 Model 2xx	4	Any connector on the power distribution adapter (part no. 54-19045-01) located in the rear of the cabinet on the left-hand rails
VAX 9000 Model 4xx	4	Any connector on the power distribution adapter (part no. 54-19045-01) located in the rear of the cabinet on the right-hand rails

Figure 2–10 Power Distribution Adapter—VAX 9000 Systems



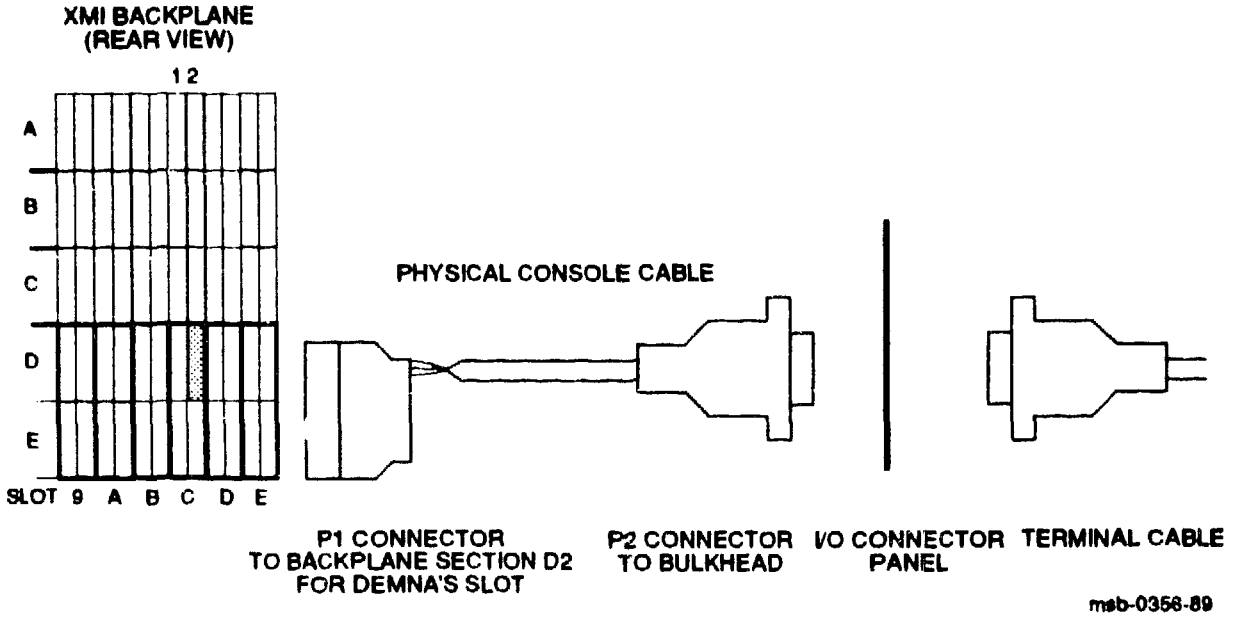
13 If a physical console is going to be used, install the internal cable for the physical console as follows:

a. Install an I/O connector panel (70-28010-01) for the cable over one of the bulkhead cutouts.

b. Connect the P1 connector of the cable to backplane segment D2 for the DEMNA slot (see Figure 2–11). The connector is right-side-up when the key on the connector is on the right. The P1 connector is not uniquely keyed for backplane segment D2. It is thus possible to insert the connector into the wrong backplane segment.

c. Attach the P2 connector of the cable to the I/O connector panel.

Figure 2–11 Internal Cable for Physical Console



2.2 VERIFICATION OF HARDWARE INSTALLATION

CAUTION

It is very important that you verify that the DEMNA is properly installed. If the DEMNA is improperly installed, you may bring down the entire network when you connect the DEMNA to the network.

Follow these steps to verify that the DEMNA is properly installed:

1 Connect the loopback connector (part number 12-22196-02) to the Ethernet connector (P2 connector) of the internal Ethernet cable.

2 Set the appropriate system circuit breaker(s) to On.

3 Turn on the system power. This causes each module in the system to execute its self-test.

4 Verify that the green LED on the loopback connector is lit, indicating that the pigtail (P3) connector of the internal Ethernet cable is properly connected and is supplying +12V for the transceiver. If the LED is not lit, power down the system, make sure that the pigtail connector is connected to the right power connection, and reseat the pigtail connector. Continue with step 2.

5 Verify that the DEMNA passes both self-test (the yellow DEMNA OK LED lights) and the LANCE external loopback test (the green External Loopback LED lights). (See Section 3.2.1 for further information on the DEMNA LEDs.)

6 If the self-test and/or external loopback test fails, check to see that the DEMNA module is properly seated in the card cage and that all three connectors of the internal Ethernet cable are properly installed.

7 If the module continues to fail self-test, swap in a different DEMNA module if one is available. You can also try installing the module in a different slot.

8 If the module still fails self-test, run the DEMNA ROM-based diagnostics (RBDs), which are described in the *DEC LANcontroller 400 Technical Manual*.

2.3 VERIFICATION OF DEMNA OPERATION IN NETWORK

Proper operation of the DEMNA was verified up to the system bulkhead (Ethernet connector) in Section 2.2. Now, follow these steps to verify that the DEMNA can communicate with other network nodes:

1 Connect the external transceiver cable to the P2 (Ethernet) connector of the internal Ethernet cable (available at the system bulkhead) or, for the first Ethernet controller in a VAX 6000 system, to the Ethernet connector on the system interconnect panel.

2 Boot the operating system.

3 Configure the network database and start the network software.

4 If the system is unable to communicate over the network, verify that the network software is installed and configured properly.

5 If the network software is properly installed and configured and the system is still unable to communicate over the network, shut down

the system and check the transceiver and the transceiver cable as follows:

a. Disconnect the external Ethernet transceiver cable (BNE3) at the transceiver end.

b. Install the loopback connector (12-22196-02) on the cable.

c. Run the DEMNA self-test and observe one of the following:

- If the External Loopback LED on the DEMNA module lights, the transceiver is bad. Replace the transceiver, reconnect the cable to the new transceiver, and rerun the self-test to verify proper operation. No further action is required.
- If the External Loopback LED on the DEMNA module does not light, the transceiver cable is bad and/or the P3 power connection for the internal Ethernet cable is not good. First, check the LED on the loopback connector. If the LED did not light, reseat the P3 connector and rerun the self-test. If the LED on the loopback connector is lit, replace the transceiver cable.

2.4 INTERNAL ETHERNET CABLE

The internal Ethernet cable connects to the XMI backplane at the DEMNA slot and provides Ethernet signals and power (if required) to an H4000 transceiver or other network interface device. See Table 1–2 for part numbers.

The cable has three connectors (Figure 2–3): P1, P2, and P3. The P1 connector connects to segment E2 on the XMI backplane opposite the DEMNA slot. The P2 connector is an industry-standard Ethernet connector that connects to an I/O connector panel on the bulkhead or to the rear of the Ethernet connector on the system interconnect panel in a VAX 6000 system. The P3 (pigtail) connector is a +15V direct-current power connection that supplies power to a device (such as an H4000 transceiver, a DESTA thin-wired box, or a DECOM broadband transceiver) that does not have its own power supply. The pigtail connector should be plugged in regardless of the type of transceiver.

Figure 2–12 shows the P1 connector pinouts of the internal Ethernet cable. Table 2–2 describes these pinouts. Figure 2–13 shows the pinouts for the P2 connector of the internal Ethernet cable, and Table 2–3 describes these pinouts.

Figure 2–12 P1 Connector Pinouts of Internal Ethernet Cable

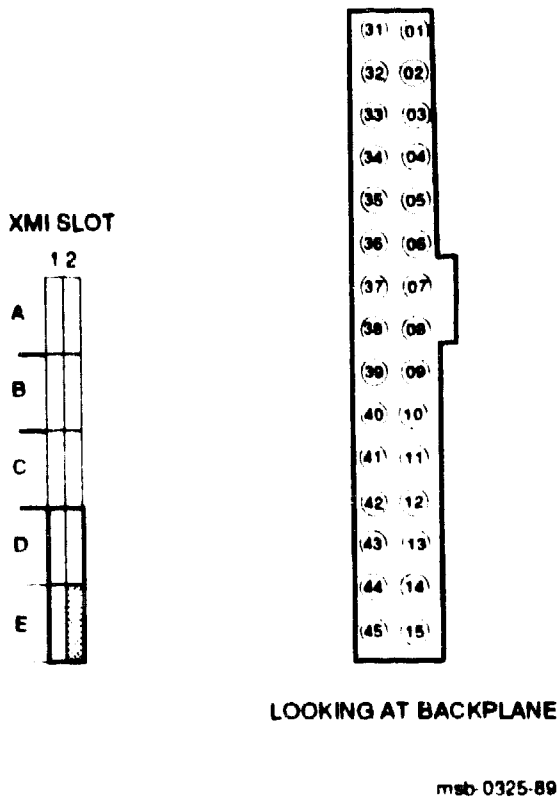


Table 2–2 P1 Connector Pinouts of Internal Ethernet Cable

Pin	Signal	Description
E01–E04	Unconnected	
E05–E09	Logic Ground	
E10	Ethernet Collision L	Differential collision detect signals
E11	Ethernet Collision H	from the Ethernet bus.
E12	Ethernet Receive L	Differential receive signals from the
E13	Ethernet Receive H	Ethernet bus.
E14	Ethernet Transmit L	Differential transmit signals to the
E15	Ethernet Transmit H	Ethernet bus.

Figure 2–13 P2 Connector Pinouts of Internal Ethernet Cable

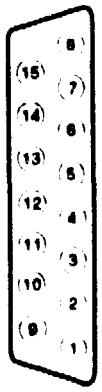


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Table 2–3 P2 Connector Pinouts of Internal Ethernet Cable

Pin	Signal	Description
1	Shield	
2	Collision Presence H	Differential signals that indicate a failure of
9	Collision Presence L	the collision detection logic
3	Transmit H	Differential transmit signals to the Ethernet
10	Transmit L	bus
4	Reserved	
5	Receive H	Differential receive signals from the
12	Receive L	Ethernet bus
6	Power Return	Power return line
7	Reserved	
8	Reserved	
11	Reserved	
13	Power	
14	Reserved	
15	Reserved	

2.5 EXTERNAL TRANSCEIVER CABLE

The external transceiver cable runs from the Ethernet connection provided at the bulkhead or system interconnect panel to an Ethernet transceiver, such as an H4000 baseband transceiver, DECOM broadband transceiver, or DELNI local network interconnect. The cable is ordered as a separate item.

2.6 INTERNAL CABLE FOR PHYSICAL CONSOLE

The internal cable for the physical console connects the XMI backplane at the DEMNA slot to the system bulkhead and provides a connector for a terminal cable. The cable is ordered as a separate item.

The cable has two connectors: P1 and P2 (see Figure 2–5). The P1 connector connects to segment D2 on the XMI backplane opposite the DEMNA slot. The P2 connector is a standard 25-pin Sub-D connector that connects to the bulkhead and is used as a connector for a terminal cable.

Figure 2–14 shows the P1 connector pinouts for the internal cable for the physical console. Table 2–4 describes these pinouts. Figure 2–15 shows the P2 connector pinouts for the internal cable for the physical console. Table 2–5 describes these pinouts.

Figure 2–14 P1 Connector Pinouts of Internal Cable for Physical Console

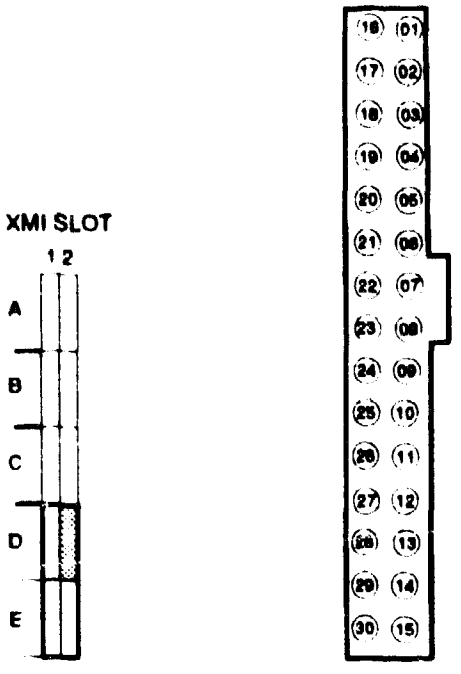

Table 2–4 P1 Connector Pinouts of Internal Cable for Physical Console

Pin	Signal
D01	Transmit
D02	Receive
D03	Logic Ground
D04–D30	Unconnected

Figure 2–15 P2 Connector Pinouts of Internal Cable for Physical Console

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Table 2–5 P2 Connector Pinouts of Internal Cable for Physical Console

Pin	Signal
1	Unconnected
2	Transmit
3	Receive
4-6	Unconnected
7	Logic Ground
8-25	Unconnected

2.7 REMOVAL

To remove a DEMNA module, follow these steps:

1 Power down the host computer system by:

   a. Turning the Power switch to the Off position

   b. Setting the appropriate system circuit breaker(s) to Off

2 Open the appropriate cabinet.

3 Make sure you are wearing an ESD wrist strap that is attached to the system chassis.

4 Open or remove the door on the front (module-insertion side) of the XMI card cage that contains the DEMNA to be removed.

5 Locate the desired card cage slot.

6 Lift the lever to open the slot.

7 Slide the module out of the card cage slot.

8 Put the module into a conductive container.

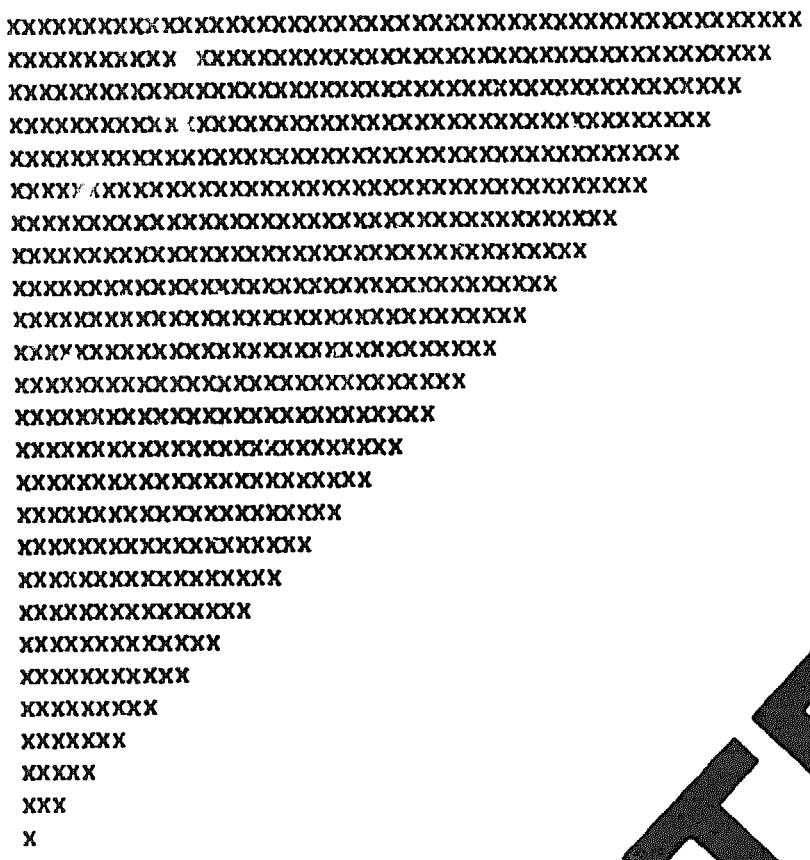
9 Close the locking lever.

10 If another DEMNA will not be installed:

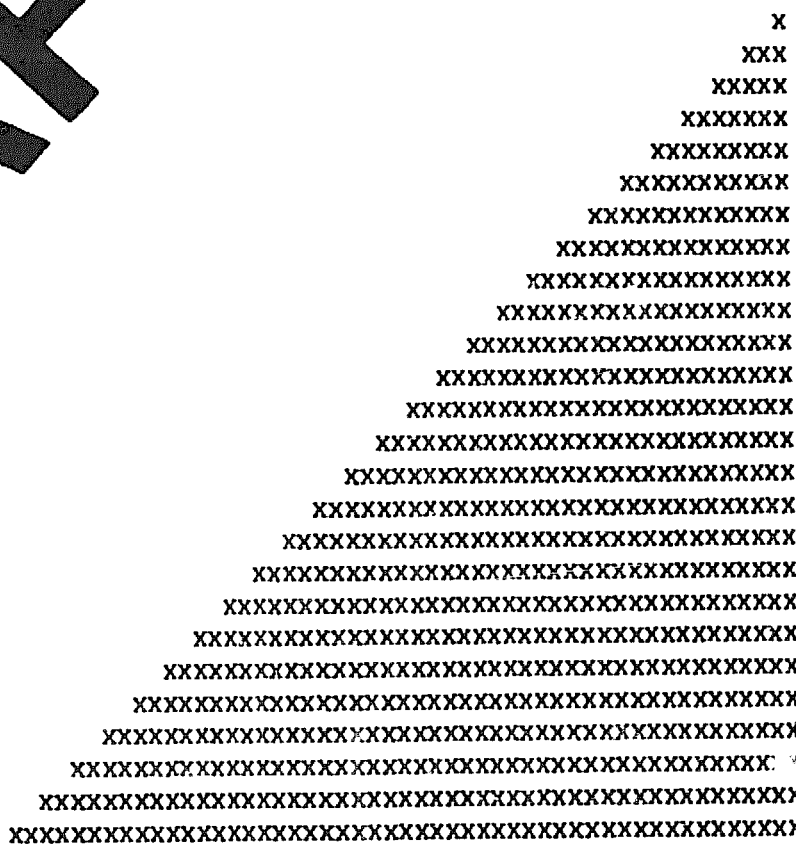
   a. Close or replace the door on the front of the XMI card cage from which the DEMNA was removed.

   b. Remove the cables from the slot that contained the DEMNA.

   c. Close the cabinet.



CHAPTER 3



3 Power-Up Self-Test

The DEMNA power-up self-test consists of ROM-resident diagnostic routines that run automatically on power-up or reset. The power-up self-test verifies that the hardware at the node is operational and that the DEMNA can transmit and receive a loopback packet over the network.

Since the routines are contained in ROM, their execution requires no operating system. The self-test routines are thus stand-alone programs independent of any software environment.

3.1 HOW TO RUN SELF-TEST

There are several ways of running self-test for the DEMNA:

1 On system power-up—When the user powers up the host system, the DEMNA automatically runs power-up self-test. Front panel controls vary among host systems; see the system *Owner's Manual* for the specific system.

2 On XMI system reset—For VAX 6000 systems: When the user presses the reset or restart button on the host system's front panel, the system goes through its reset sequence, which causes each XMI node to run its own self-test. For VAX 9000 systems: The user can issue the following console command to reset a particular XMI card cage:

```
>>>UNJAM /XJA=n
```

where *n* is the unit number of the XJA adapter for the XMI card cage. If the XJA unit number is not supplied, the command resets all XMI card cages in the system.

3 Running self-test as a ROM-based diagnostic (RBD)—A Digital customer service engineer can invoke the self-test as an RBD from the system console of a VAX 6000 or VAX 9000 system or from the DEMNA physical console (a terminal attached directly to the DEMNA). This is the same diagnostic that runs during power-up or reset self-test.

Example 3–1 shows how to use VAX console commands on a VAX 6000 system to run the self-test on a DEMNA located at XMI node 3. For a description of the Z command used in this example, see the system *Owner's Manual*.

Example 3–1 Running Self-Test on a VAX 6000 System

```
>>>Z 3 [RETURN]
?33 Z connection successfully started
T/R [RETURN]
RBD3>ST 0 [RETURN]

;Selftest      3.00
;        P          3      0C03          1
;00000000 00000000 00000000 00000000 00000000 00000000 00000000
RBD3 [CTRL/Z] [CTRL/P]
?31 Z connection terminated by ^P
>>>
```

Example 3–2 shows how to use VAX console commands on a VAX 9000 system to run the self-test on a DEMNA at node E through XJA number 2. For a description of the Z command used in this example, see the system *Owner's Manual*.

Example 3–2 Running Self-Test on a VAX 9000 System

```
>>> Z 2E [RETURN]
[Use ^P to exit Z-mode]
T/R [RETURN]
RBD3>ST 0 [RETURN]

;Selftest      3.00
;        P          3      0C03          1
;00000000 00000000 00000000 00000000 00000000 00000000 00000000
RBD3 [CTRL/Z] [CTRL/P]
xxx Z connection terminated by ^P
>>>
```

If you do not know which XMI node the DEMNA is at, use the SHOW CONFIGURATION command at the system console prompt to locate the DEMNA.

Another way of locating the DEMNA node is to use the EXAMINE command to read the Device (XDEV) Register at each node until you find the DEMNA, which has a device type of 0C03 (hex). A module's XDEV Register is always at the module's base address.

3.2 REPORTING SELF-TEST RESULTS

Test results (pass or fail) are indicated by LEDs on the module and by the DEMNA Power-Up Diagnostic (XPUD) Register.

3.2.1 Self-Test Results in LEDs

There are two status-indicator lights on the module:

- 1 yellow DEMNA OK LED
- 1 green External Loopback LED

The location of the LEDs is shown in Figure 3–1.

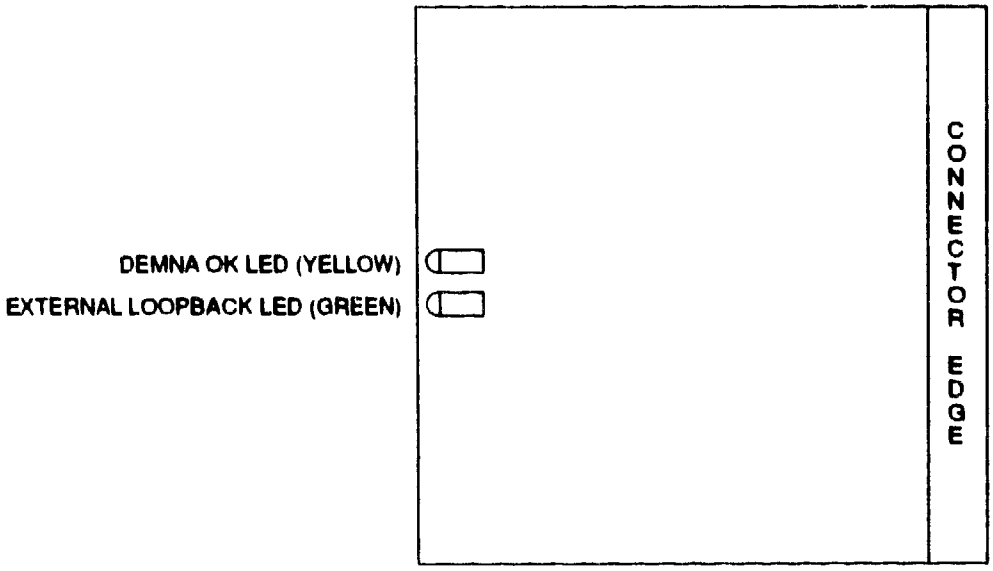
The yellow DEMNA OK LED shows the status of the module after the node self-test. The green External Loopback LED indicates whether the DEMNA passed the LANCE external loopback test, which tests the DEMNA's ability to transmit and receive a loopback packet over the network.

At power-up or reset, both LEDs are off. If the DEMNA passes all the executed tests (excluding the LANCE external loopback test), the self-test lights the yellow DEMNA OK LED; otherwise, this LED remains off. If the LANCE external loopback self-test passes, the self-test lights the green External Loopback LED; otherwise this LED remains off.

3.2.2 Self-Test Results in the Power-Up Diagnostic Register

The Power-Up Diagnostic (XPUD) Register indicates which tests in the self-test diagnostic passed. In addition, the Self-Test Complete (STC) bit indicates whether the self-test has completed execution. See Appendix B for a detailed description of the XPUD Register.

Figure 3–1 LED Locations



3.3 INTERPRETING TEST RESULTS

If the External Loopback LED fails to light, indicating that the LANCE external loopback self-test failed, this does not necessarily indicate that a DEMNA component failed self-test. The problem could be a bad cable, bad Ethernet transceiver connector, improper seating of the transceiver cable, or simply that the DEMNA is disconnected from the transceiver.[1] In any case, such an error condition prevents the DEMNA from transmitting or receiving Ethernet packets.

If the XPUD Register indicates that all of the self-test routines failed, the problem is probably the CVAX, ROM, or bus transceivers.

Self-test could also fail because of a systemwide fault. For example, a faulty power supply or missing XMI bus terminators could be the problem. Make sure that system power is OK and check for other possible systemwide faults.

[1] Note also that the External Loopback LED does not light if another test in the self-test diagnostic fails. When another self-test fails, the external loopback test is not executed.

After a problem discovered by the self-test has been corrected, the DEMNA LED(s) will light only if the self-test is rerun. However, if the self-test is not rerun, the DEMNA will still function properly even though the LED(s) don't light.

3.4 TESTED COMPONENTS

The self-test tests the following components and functions on the DEMNA module:

- CVAX
- EPROM
- EEPROM
- CVAX ROM
- All RAM
- System Support Chip (SSC)
- CVAX Interrupt Request (IRQ) lines
- Gate Array
- LANCE chip

3.5 UNTESTED COMPONENTS AND FUNCTIONS

The following components and functions are not tested:

- A complete CVAX instruction set
- Ethernet interface logic functions:
  - More (multiple retries of packet transmission)
  - One (one retry of a packet transmission)
  - Babble error
  - Time domain reflectometry
  - Late collision
  - Loss of carrier

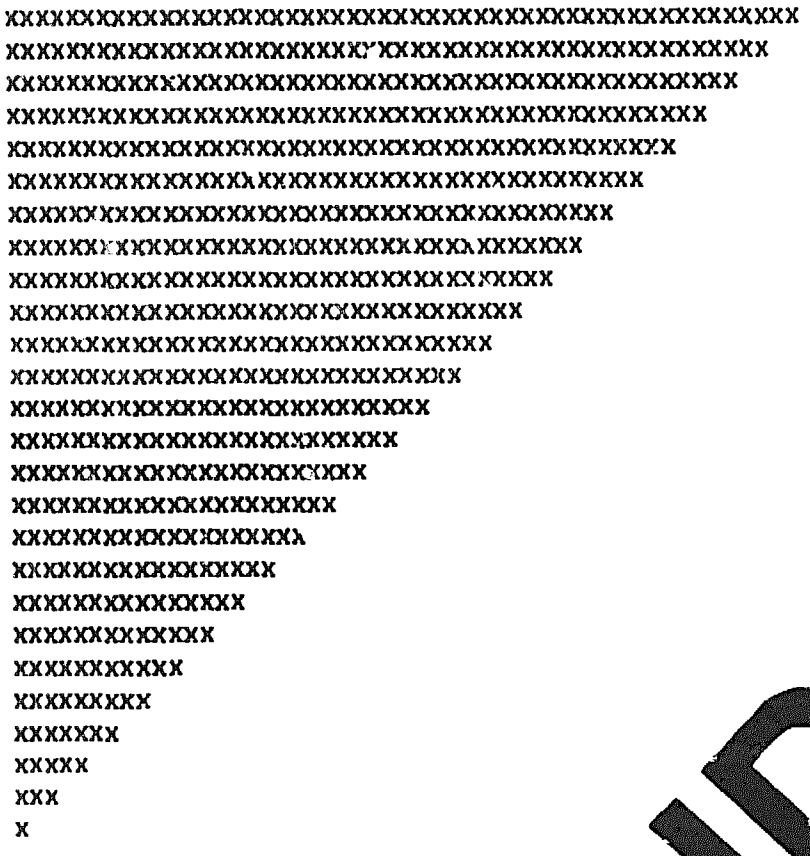
The datamove logic, which is implemented in the gate array, is tested in loopback mode only.


APPENDIX A

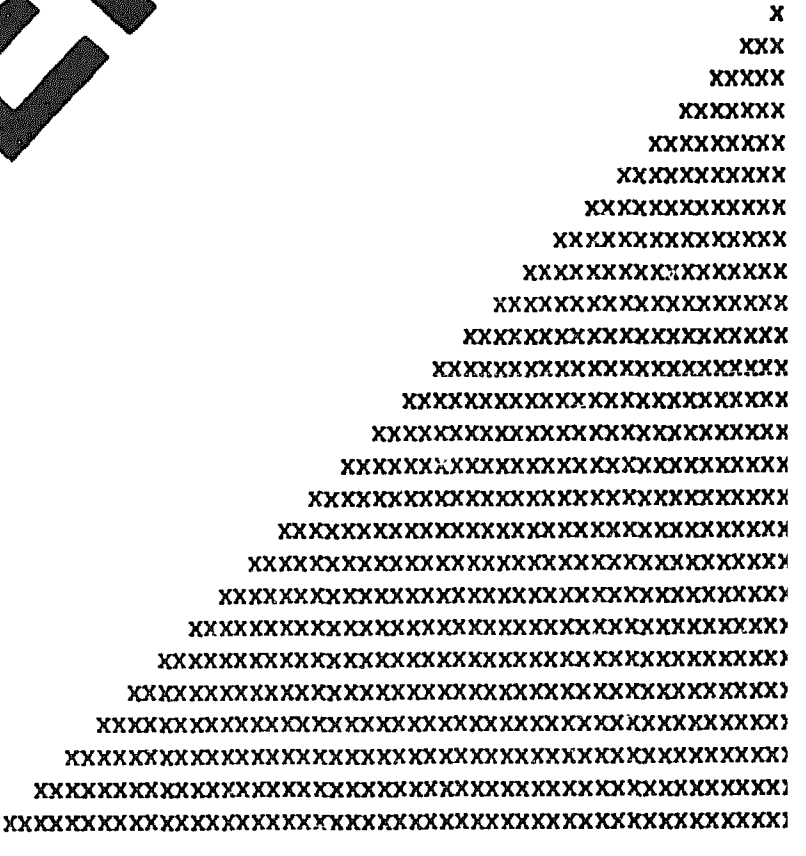
A Environmental Requirements

Operating Environment	
Temperature	5°C to 50°C (41°F to 122°F)
Humidity	10% to 95% with maximum wet bulb of 32°C (89.6°F) and minimum dew point of 2°C (36°F) noncondensing
Altitude	To 2.4 km (8,000 ft)

Storage Environment	
Temperature	-40°C to 66°C (-40°F to 151°F)
Humidity	To 95% noncondensing
Altitude	To 9.1 km (30,000 ft)



APPENDIX B



B Registers

This appendix describes the DEMNA registers that are useful for troubleshooting problems that may occur during installation. Table B–1 summarizes these registers. Table B–2 explains the access types for these registers, as well as the bit types for the registers. Each register is then described in detail.

Table B–1 Registers Useful During Installation—Summary

Name	Mnemonic	XMI Address	Type[1]	Description
Device	XDEV	bb + 0	RO	Indicates the XMI node's device type and device firmware revision level.
Bus Error	XBER	bb + 4	R/W	Records XMI bus errors and loopback errors.
Power-Up Diagnostic	XPUD	bb + 10C	RO	Indicates whether self-test has completed and which tests in the self-test passed.
Failing Address	XFADR	bb + 8	RO	Provide information on failing XMI transactions initiated by the DEMNA.
Failing Address Extension	XFAER	bb + 2C	RO	
Gate Array CSR	GACSR	None	—	Provides status on the gate array. This register is part of the fatal error block and nonfatal error block, which are described in the *DEC LANcontroller 400 Technical Manual.*

[1] With respect to the port driver

Table B–2 Abbreviations for Bit Types

Abbreviation	Definition
0	Initialized to logic level zero
1	Initialized to logic level one
X	Initialized to either logic state
RO	Read only
R/W	Read/write
R/W1C	Read/cleared by writing a 1

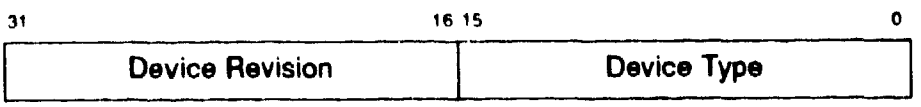
Device Register (XDEV)

The Device Register identifies the DEMNA device type, hardware revision, and EEPROM firmware revision. The device type for the DEMNA is 0C03 (hexadecimal).

The port loads the Device Register on power-up or reset. The port driver reads the Device Register to determine the module device type before attempting to initialize the port.

ADDRESS

Nodespace base address + 0



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BITS<31:16>

Name: Device Revision

Mnemonic: DREV

Type: RO, 0

Indicates the device revision of the DEMNA. The high-order byte of the field is the hardware revision number, which indicates the functional revision of the hardware. This is identical to the hardware functional revision indicated on the module label. The low-order byte of the field is the revision number of the loaded firmware. If the EEPROM firmware is loaded (which is normally the case), the firmware revision field indicates the EEPROM firmware revision. However, if the EPROM firmware is loaded (which occurs if the EEPROM fails selftest), the firmware revision field indicates the EPROM firmware revision.

The hardware revision field is decoded as follows for the first 10 hardware revisions of the DEMNA. Note that letters G and I, as well as their corresponding codes, are skipped.

Code (hex)	Hardware Revision Level
01	A
02	B
03	C
04	D
05	E
06	F
08	H
0A	J
0B	K
0C	L

The firmware revision field is decoded as follows for the first 10 EEPROM firmware revisions for a given hardware revision level.

Code (hex)	EEPROM Firmware Revision Level
01	01
02	02
03	03
04	04
05	05
06	06
07	07
08	08
09	09
0A	10

Note that the firmware revision levels of both the EEPROM and the EPROM are zeroed when the hardware revision level changes.

Device Register (XDEV)

Table B–3 shows how the Device Revisions field is encoded for the first three firmware revisions of hardware revision F and for the first firmware revision of hardware revision H.

Table B–3 Example of Device Revision Field

Hex Value	Hardware Revision	Firmware Revision
0600	F	0
0601	F	1
0602	F	2
0603	F	3
0800	H	0

BITS<15:0>

Name: Device Type

Mnemonic: XDEV

Type: RO, 0

A value of 0C03 (hex) indicates that the adapter is a DEMNA module.

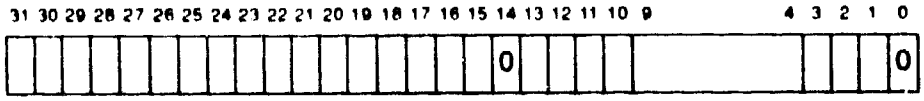
Bus Error Register (XBER)

The Bus Error Register contains error status on a failed XMI transaction. This status includes the failed command, commander ID, and an error bit that indicates the type of error that occurred. This status remains locked until software resets the error bit(s).

Bus Error Register (XBER)

ADDRESS

Nodespace base address + 0000 0004



Enable MORE Protocol
Disable XMI Timeout
Enable Hexword Writes
Failing Commander ID
Self-Test Fail
Extended Test Fail
Node-Specific Error Summary

Commander Errors

Transaction Timeout
Command NO ACK
Read Error Response
Read Sequence Error
No Read Response
Corrected Read Data
Write Data NO ACK

Responder Errors

Read/IDENT Data NO ACK
Write Sequence Error
Parity Error
Inconsistent Parity Error

Miscellaneous

Write Error Interrupt
XMI Fault
Corrected Confirmation
XMI Bad
Node Halt
Node Reset
Error Summary

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Bus Error Register (XBER)

BIT<31>

Name: Error Summary

Mnemonic: ES

Type: RO, 0

ES represents the logical OR of the command error bits and the Self-Test Fail bit in this register. Therefore, ES asserts when any error bit asserts.

BIT<30>

Name: Node Reset

Mnemonic: NRST

Type: R/W, 0

The host writes a one to NRST to cause the DEMNA to execute a complete power-up reset. This sequence is similar to the response caused by a real power-up sequence, which is triggered by the assertion and deassertion of XMI DC LO L. The DEMNA asserts XMI BAD L until the self-test completes successfully. Nodes should not access the DEMNA from the time it is reset until it completes self-test (or the maximum self-test time is exceeded).

While the DEMNA is responding to node reset, it does not access other nodes on the XMI bus. In response to a real power-up sequence (caused by XMI DC LO L), the NRST bit will be cleared. However, when set by the host to cause a node reset, the bit remains set, thus indicating to the DEMNA CVAX that the host issued a node reset. The DEMNA self-test clears this bit once the node reset has completed.

BIT<29>

Name: Node Halt

Mnemonic: NHALT

Type: R/W, 0

The host sets NHALT to force the DEMNA to execute its halt sequence. The halt causes the DEMNA to go into a quiet state and retain as much state information as possible. Firmware execution jumps to the initialization code in EPROM (Boot ROM), shuts down the port, and loops on the NHALT bit. When the host clears NHALT, the DEMNA executes its restart sequence, which is identical to the power-up/reset sequence, except that the DEMNA does not execute its self-test, clear its internal data link or error counters, or clear its fatal and nonfatal error blocks.

BIT<28>

Name: XMI BAD

Mnemonic: XBAD

Type: R0, 1

The DEMNA does not use this bit.

BIT<27>

Name: Corrected Confirmation

Mnemonic: CC

Type: R/W1C, 0

This bit sets when the DEMNA detects a single-bit CNF error. Single-bit CNF errors are automatically corrected by the XCLOCK chip in the XMI Corner.

BIT<26>

Name: XMI FAULT
Mnemonic: XFAULT
Type: RO, 0
The DEMNA does not use this bit.

BIT<25>

Name: Write Error Interrupt
Mnemonic: WEI
Type: RO, 0
The DEMNA does not use this bit.

BIT<24>

Name: Inconsistent Parity Error
Mnemonic: IPE
Type: RO, 0
The DEMNA does not use this bit.

BIT<23>

Name: Parity Error
Mnemonic: PE
Type: R/W1C, 0
When set, indicates that the DEMNA has detected a parity error on an XMI cycle.

Bus Error Register (XBER)

BIT<22>

Name: Write Sequence Error

Mnemonic: WSE

Type: R/W1C, 0

When set, indicates that an XMI node attempting a write to the DEMNA aborted the write transaction due to missing data cycles. Only XMI responder nodes are required to implement this bit. If not implemented, nodes return zero.

BIT<21>

Name: Read/IDENT Data NO ACK

Mnemonic: RIDNAK

Type: R/W1C, 0

When set, indicates that a Read or IDENT data cycle (GRDn) transmitted by the DEMNA has received a NO ACK confirmation.

BIT<20>

Name: Write Data NO ACK

Mnemonic: WDNAK

Type: R/W1C, 0

When set, indicates that a Write data cycle (WDAT) transmitted by the DEMNA has received a NO ACK confirmation.

BIT<19>

Name: Corrected Read Data

Mnemonic: CRD

Type: R/W1C, 0

When set, indicates that the node has received a CRDn read response.

BIT<18>

Name: No Read Response
Mnemonic: NRR
Type: R/W1C, 0
When set, indicates that a transaction initiated by the DEMNA failed due to a read response timeout.

BIT<17>

Name: Read Sequence Error
Mnemonic: RSE
Type: R/W1C, 0
When set, indicates that a transaction initiated by the DEMNA failed due to a read sequence error.

BIT<16>

Name: Read Error Response
Mnemonic: RER
Type: R/W1C, 0
When set, RER indicates that a node has received a Read Error Response.

BIT<15>

Name: Command NO ACK
Mnemonic: CNAK
Type: R/W1C, 0
When set, indicates that a command cycle transmitted by the DEMNA has received a NO ACK confirmation caused either by a reference to a nonexistent memory location or by a command cycle parity error.

BIT<14>

Name: Reserved
Mnemonic: None
Type: RO, 0
Reserved; must be zero.

BIT<13>

Name: Transaction Timeout
Mnemonic: TTO
Type: R/W1C, 0
When set, indicates that a transaction initiated by the DEMNA failed due to a transaction timeout.

BIT<12>

Name: Node-Specific Error Summary
Mnemonic: NSES
Type: RO, 0
When set, NSES indicates that a node-specific error condition has been detected. The DEMNA does not use this bit.

BIT<11>

Name: Extended Test Fail
Mnemonic: ETF
Type: RO, 0
This bit is not used by the DEMNA.

BIT<10>

Name: Self-Test Fail

Mnemonic: STF

Type: R/W1C, 1

When the STF bit is set, indicating that the DEMNA has not passed self-test, the DEMNA hardware asserts XMI BAD L on the XMI bus. When the STF bit is cleared, indicating that the DEMNA has passed self-test, the hardware clears the STF bit, thus causing the DEMNA to deassert XMI BAD L.

BITS<9:4>

Name: Failing Commander ID

Mnemonic: FCID

Type: RO

Bits <9:6> log the commander ID of a failing transaction during a command cycle. The failing commander ID is recorded for command errors detected by XBER bits <20> and <18:13>. Bits <5:4> indicate the type of operation that failed: 00 = a failed peek or interrupt operation; 01 = a failed datamove operation.

BIT<3>

Name: Enable Hexword Write

Mnemonic: EHWW

Type: RO, 0

The DEMNA does not use this bit.

Bus Error Register (XBER)

BIT<2>

Name: Disable XMI Timeout

Mnemonic: DXTO

Type: RW, 0

This bit enables or disables the reporting of all XMI timeouts by a commander. When this bit is set, the node will never encounter a No Read Response (NRR) error or a transaction timeout (TTO) if retries are disabled.

BIT<1>

Name: Enable MORE Protocol

Mnemonic: EMP

Type: RW, 0

When cleared, prevents the gate array from asserting the More signal on the XMI bus. When set, enables the DEMNA gate array to assert the More signal.

BITS<0>

Name: Reserved

Mnemonic: None

Type: RO, 0

Reserved; must be zero.

Power-Up Diagnostic Register (XPUD)

The XPUD Register displays the results of the DEMNA self-test, which runs automatically on power-up or reset. After the self-test finishes, the port driver can read the register and pass the register contents to higher-level software that can determine which DEMNA components passed self-test.

The XPUD Register is treated as follows:

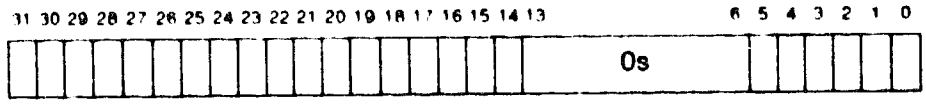
- The DEMNA initializes the XPUD Register to all zeros on power-up or reset.
- When a piece of DEMNA logic passes self-test, its corresponding bit in the XPUD Register sets.
- If a piece of logic fails self-test, the corresponding bit remains cleared.

The XPUD Register of a DEMNA that passes self-test has a value of FFFFC0007 (if there are no error history entries) or FFFFC027 (if there are error history entries).

Power-Up Diagnostic Register (XPUD)

ADDRESS

Nodespace base address + 10C



Firmware Initialized
External Loopback
EEPROM Loaded
EPROM Loaded
Bad Diagnostic Patch Table
EEPROM Error History Exists
XNAGA
Ethernet Subsystem Parity
LANCE
Shared Parity RAM
Shared RAM
XNADAL Timeout Logic
XNADAL Readback
EEPROM
ENET PROM
CVAX
CVAX Parity RAM
CVAX RAM
Console UART Drivers
SSC
Diagnostic Register
CVAX Interrupt Lines
Boot ROM
Self-Test Complete

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Power-Up Diagnostic Register (XPUD)

BIT<31>

Name: Self-Test Complete

Mnemonic: STC

Type: RO to port driver, 0

When set, indicates that the DEMNA self-test has completed and that the contents of the XPUD Register are valid. The register contents are invalid when the bit is cleared.

BIT<30>

Name: Boot ROM

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the contents of the Boot ROM (also called the EPROM) are valid.

BIT<29>

Name: CVAX Interrupt Lines

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the CVAX interrupt lines are not stuck (always asserted) or being driven by onboard logic.

BIT<28>

Name: Diagnostic Register

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that all bits in the Diagnostic Register powered-up to the correct state and can be read and written.

BIT<27>

Name: SSC

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the SSC chip can perform all its functions.

BIT<26>

Name: Console UART Drivers

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the console UART drivers are functioning correctly.

BIT<25>

Name: CVAX RAM

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the CVAX RAM is functioning correctly (that is, passed the CVAX RAM march test).

BIT<24>

Name: CVAX Parity RAM

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the CVAX parity RAM is functioning correctly.

BIT<23>

Name: CVAX
Mnemonic: None
Type: RO to port driver, 0
When set, indicates that the CVAX chip is functioning correctly.

BIT<22>

Name: ENET PROM
Mnemonic: None
Type: RO to port driver, 0
When set, indicates that the contents of the ENET PROM are valid.

BIT<21>

Name: EEPROM
Mnemonic: None
Type: RO to port driver, 0
When set, indicates that the contents of the EEPROM are valid.

BIT<20>

Name: XNADAL Readback
Mnemonic: None
Type: RO to port driver, 0
When set, indicates that the address latches and bus transceivers for the gate array/DEMNA memory bus interface are functioning correctly.

BIT<19>

Name: XNADAL Timeout Logic

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the timeout logic for the gate array/DEMNA memory bus interface is functioning correctly.

BIT<18>

Name: Shared RAM

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the shared RAM is functioning correctly (that is, passed the RAM march test).

BIT<17>

Name: Shared Parity RAM

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the shared parity RAM is functioning correctly.

BIT<16>

Name: LANCE

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the LANCE chip can perform all its functions.

BIT<15>

Name: Ethernet Subsystem Parity

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the parity circuit in the Ethernet subsystem is functioning correctly.

BIT<14>

Name: XNAGA

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the gate array can perform all its functions.

BITS<13:6>

Name: Reserved

Mnemonic: None

Type: RO to port driver, 0

Reserved; must be zeros.

BIT<5>

Name: EEPROM Error History Exists

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the EEPROM error history has one or more entries. When cleared, indicates that there are no entries in the EEPROM error history.

BIT<4>

Name: Bad Diagnostic Patch Table

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the diagnostic patch table in EEPROM is invalid. When cleared, indicates that this table is valid.

BIT<3>

Name: EPROM Loaded

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the contents of the EPROM have been loaded into CVAX RAM. The EPROM contains a subset of the EEPROM code. If the EEPROM fails self-test, the contents of the EPROM are loaded into CVAX RAM. The EPROM code provides enough functionality for the CVAX to run diagnostics, update the EEPROM, and perform transmit and receive operations.

BIT<2>

Name: EEPROM Loaded

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the contents of the EEPROM have been loaded into CVAX RAM. The EEPROM contains the operational firmware for the DEMNA.

BIT<1>

Name: External Loopback

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the DEMNA is connected to a live Ethernet or a loopback connector and that the external loopback test has passed.

BIT<0>

Name: Firmware Initialized

Mnemonic: None

Type: RO to port driver, 0

When set, indicates that the DEMNA firmware is initialized.

Failing Address Register (XFADR)

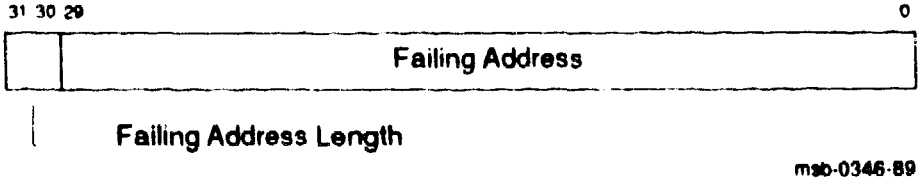
The Failing Address Register logs address and data length information associated with a failing XMI transaction. The register is locked when any of the following bits in the Bus Error Register (XBER) sets (these are commander errors):

- Write Data NO ACK (WDNAK), XBER<20>
- No Read Response (NRR), XBER<18>
- Read Sequence Error (RSE), XBER<17>
- Read Error Response (RER), XBER<16>
- Command NO ACK (CNAK), XBER<15>
- Transaction Timeout (TTO), XBER<13>

The XFADR is unlocked (free to latch new information) when the XBER bits that lock the register are cleared. If none of the above listed errors has occurred, the XFADR contains the address and data length of the last XMI transaction.

ADDRESS

Nodespace base address + 8



BITS<31:30>

Name: Failing Length

Mnemonic: FLN

Type: RO, 0

FLN logs the value of XMI D<31:30> during the command/address cycle of a failed XMI commander transaction. FLN loads on every C/A cycle issued by the DEMNA. It locks only after all retries of the transaction fail, and it unlocks when the error that caused the lock is cleared.

XMI D<31:30>, the Length field, is used to define the number of words in the XMI data transfer. The table below shows the Length field coding. Longword-length transactions are used only in I/O space. Quadword-, octaword-, and hexword-length transactions are used only in memory space. Hexword lengths are used only for Read or Interlock Read transactions.

XMI D<31:30> L Logic Level		
31	30	Size
0	0	Hexword
0	1	Longword
1	0	Quadword
1	1	Octaword

BITS<29:0>

Name: Failing Address

Mnemonic: None

Type: RO, 0

The Failing Address field logs the value of XMI D<29:0> during the command cycle of a failing transaction. Failing Address loads on every C/A cycle issued by the DEMNA. It locks only after all retries of the transaction fail, and it unlocks when the error that caused the lock is cleared.

XMI D<29:0> defines the address of an XMI read or write transaction. If an XMI transaction has a 40-bit address, the XMI D bits decode to the address as follows:

A<39>	XMI D<29>
A<38:29>	XMI D<57:48>
A<28:0>	XMI D<28:0>

The number of significant bits in the address depends on the transaction type and length.

Failing Address Extension Register (XFAER)

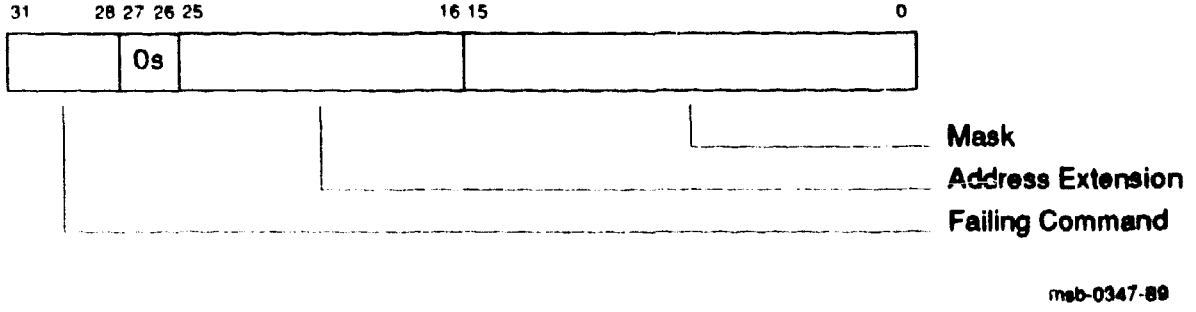
XFAER logs the address extension, command, and mask information associated with a failed XMI commander transaction. The register is locked when any of the following bits in the Bus Error Register (XBER) sets (these are commander errors):

- Write Data NO ACK (WDNAK), XBER<20>
- No Read Response (NRR), XBER<18>
- Read Sequence Error (RSE), XBER<17>
- Read Error Response (RER), XBER<16>
- Command NO ACK (CNAK), XBER<15>
- Transaction Timeout (TTO), XBER<13>

XFAER is unlocked (free to latch new information) when the XBER bits that lock the register are cleared. If none of the above listed errors has occurred, the XFADR contains the command code, address extension, and mask of the last XMI transaction.

ADDRESS

XMI nodespace base address + 2C



BITS<31:28>

Name: Failing Command

Mnemonic: FCMD

Type: RO, 0

FCMD logs XMI D<63:60> during the C/A cycle of a failed XMI commander transaction. FCMD is loaded on every C/A cycle issued by the DEMNA but locks only if the transaction fails and unlocks when the error that caused the lock is cleared.

XMI D<63:60> is the Command field. The Command field specifies the transaction being initiated in the command cycle. The table below shows how the Command field is encoded.

XMI D<63:60> L Logic Level					
63	62	61	60	Command	Mnemonic
0	0	0	0	Reserved	
0	0	0	1	Read	READ
0	0	1	0	Interlock Read	IREAD
0	0	1	1	Reserved	
0	1	0	0	Reserved	
0	1	0	1	Reserved	
0	1	1	0	Unlock Write Mask	UWMASK
0	1	1	1	Write Mask	WMASK
1	0	0	0	Interrupt	INTR
1	0	0	1	Identify	IDENT
1	0	1	0	Reserved	
1	0	1	1	Reserved	
1	1	0	0	Reserved	
1	1	0	1	Reserved	
1	1	1	0	Reserved	
1	1	1	1	Implied Vector Interrupt	IVINTR

Failing Address Extension Register (XFAER)

BITS<27:26>

Name: Reserved

Mnemonic: None

Type: RO, 0

Unused; must be zero.

BITS<25:16>

Name: Failing Address Extension

Mnemonic: None

Type: RO, 0

Failing Address Extension logs XMI D<57:48> during the C/A cycle of a failed XMI commander transaction or bits <38:29> of the address specified in the transaction for DMA reads and writes.

Failing Address Extension is loaded on every C/A cycle issued by the DEMNA but locks only if the transaction fails and unlocks when the error that caused the lock is cleared.

XMI D<57:48> are the extended portion of the XMI address. If an XMI transaction has a 40-bit address, the XMI D bits decode to the address as follows:

A<39>	XMI D<29>
A<38:29>	XMI D<57:48>
A<28:0>	XMI D<28:0>

BITS<15:0>

Name: Failing Mask

Mnemonic: None

Type: RO, 0

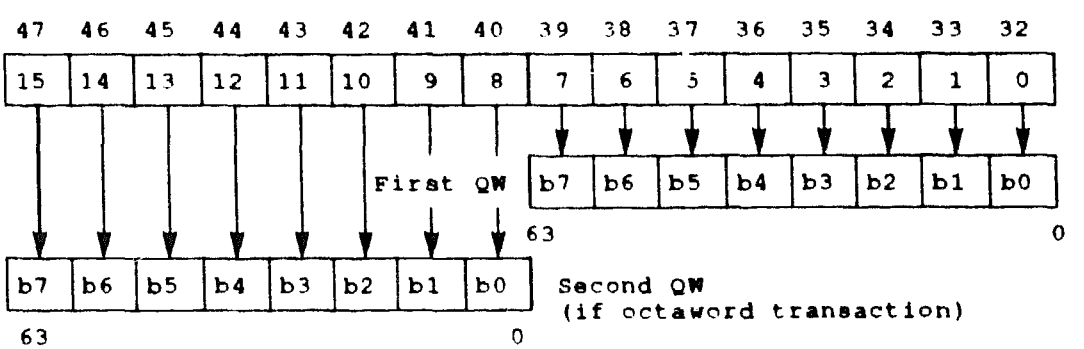
Failing Mask logs XMI D<47:32> during the C/A cycle of a failed XMI commander transaction or the write mask for DMA writes. The field is undefined for other transactions.

Failing Mask is loaded on every C/A cycle issued by the DEMNA but locks only if the transaction fails and unlocks when the error that caused the lock is cleared.

XMI D<47:32> is the Mask field, which supplies byte-level mask information for the XMI Write Mask and Unlock Write Mask transactions. During nonwrite transactions this field is a "don't care," but proper parity is still generated (see Figure B–1).

The maximum length of a write transaction is an octaword, which requires 16 mask bits in the upper longword of the command. The mask bits define which bytes of the following write data cycles are to be written to the specified locations. For longword- and quadword-length writes, the unused mask bits (D<47:36> L and D<47:40> L, respectively) are unspecified and are ignored by responders, other than to check parity.

Figure B–1 Mask Field Bit Assignments



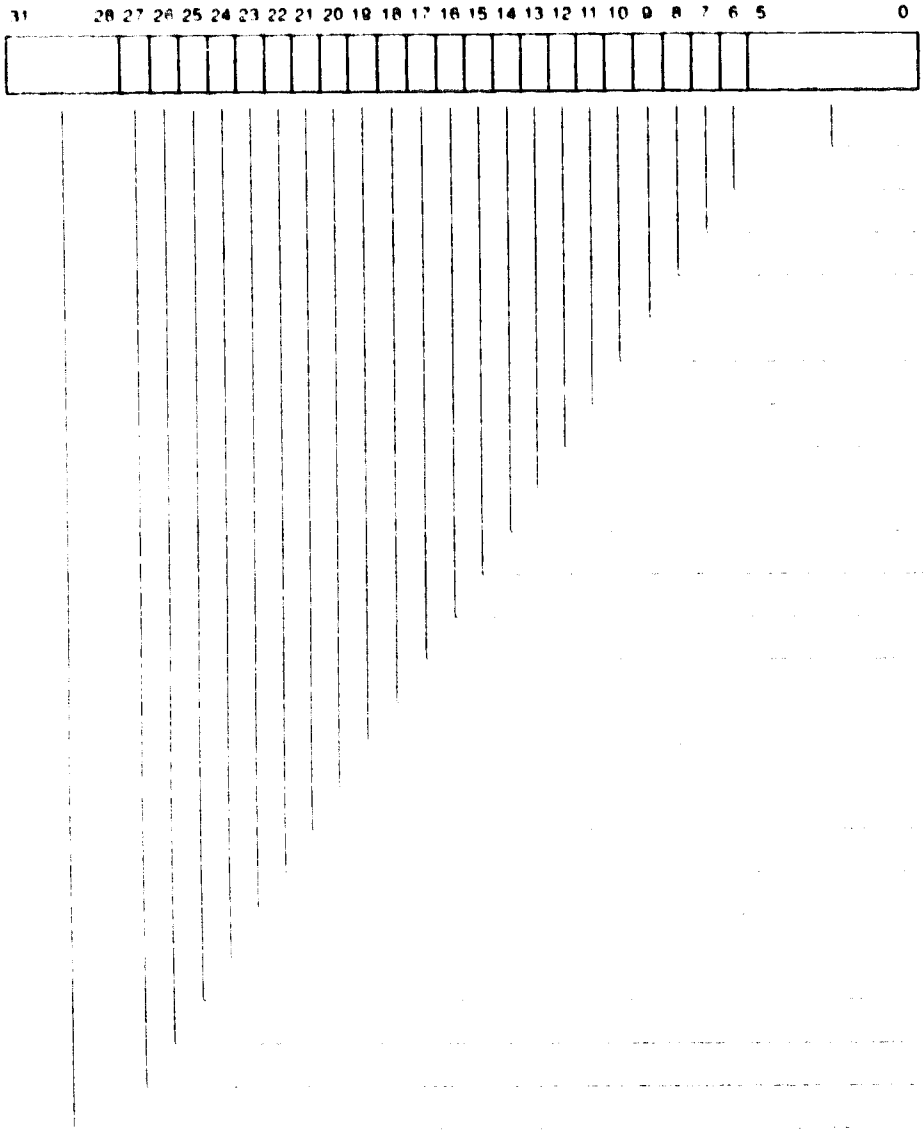
Gate Array Control and Status Register (GACSR)

The Gate Array Control and Status Register is used by the DEMNA operational and diagnostic firmware to initialize the DEMNA gate array, obtain gate array status, and to issue host interrupts. The GACSR is part of the fatal error block and nonfatal error block, which are described in the *DEC LANcontroller 400 Technical Manual*.

Gate Array Control and Status Register (GACSR)

ADDRESS

Not accessible over XMI bus



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BITS<31:28>

Name: Node ID
Mnemonic: None
Type: RO
The physical node ID (XMI Node ID<3:0>) for the DEMNA.

BIT<27>

Name: RLockout
Mnemonic: None
Type: RO
When set, indicates that the XCI Receive Lockout line is asserted. When cleared, indicates that this line is deasserted.

BIT<26>

Name: TLockout
Mnemonic: None
Type: RO
When set, indicates that the XCI Transmit Lockout line is asserted. When cleared, indicates that this line is deasserted.

BIT<25>

Name: Linear Feedback Shift Register Enable
Mnemonic: LFSR ENABLE
Type: RW, 0 after reset, unaffected by INIT
This bit is not implemented by the DEMNA.

BIT<24>

Name: Initialize Gate Array

Mnemonic: INIT

Type: RW, 0 after reset, unaffected by INIT

When set, causes the gate array to clear all its control logic, transfer Ownership bits in the datamove and peek registers back to firmware ownership, and clear most gate array registers (aside from the XMI registers and port registers). This bit thus provides a way of resetting the gate array without losing error information. The gate array clears this bit when initialization is finished.

BIT<23>

Name: Reserved

Mnemonic: None

Type: RW, 0 after reset, unaffected by INIT

Reserved; must be zero.

BIT<22>

Name: Disable Retry on NO ACKs

Mnemonic: DISABLE RETRY

Type: RW, 0 after reset, unaffected by INIT

When set, causes the gate array to indicate an error on the first NO ACK received from the XMI.

BIT<21>

Name: Force Read Sequence Error

Mnemonic: FORCE RSE

Type: RW, 0 after reset, unaffected by INIT

When set, causes GRD1 to be forced onto the XCI function lines when the gate array is a responder and returning read data. This function can be used in Loopback Peek or Datamove Read operations.

BIT<20>

Name: Datamove Loopback Buffer

Mnemonic: DM LOOPBACK BUF

Type: RW, 0 after reset, unaffected by INIT

Used in conjunction with the Loopback Datamove bit in this register. For loopback datamove transmits: When cleared, the DM LOOPBACK BUF bit causes the gate array to use the first or second quadword in the internal memory buffer, depending on the byte offset of the datamove loopback address. When set, this bit causes the gate array to use the third or fourth quadword in the internal memory buffer, depending on the byte offset of the datamove loopback address. For loopback datamove receives: When cleared, the bit causes the gate array to use the first two quadword locations in the internal memory buffer. When set, causes the gate array to use the last two quadword locations in the buffer.

BIT<19>

Name: Loopback Datamove

Mnemonic: LOOPBACK DM

Type: RW, 0 after reset, unaffected by INIT

When set, enables XMI loopback datamove transactions. When cleared, disables such transactions.

BIT<18>

Name: Force Bad XMI Receive Parity

Mnemonic: FPARX

Type: RW, 0 after reset, unaffected by INIT

When set, disables XMI parity checking and forces bad receive parity on XMI P<2>. Since the gate array checks parity on every XMI cycle the Parity Error bit in the Bus Error Register (XBER) should be set one cycle after the FPARX bit is set.

BIT<17>

Name: XPD2 Register Written Mask

Mnemonic: XPD2 REG WRT MSK

Type: R/W1C, 0 after reset, unaffected by INIT

When set, indicates that Port Data Register 2 (XPD2) was written by the host. The firmware writes a one to this bit to clear the bit.

BIT<16>

Name: XPD1 Register Written Mask

Mnemonic: XPD1 REG WRT MSK

Type: R/W1C, 0 after reset, unaffected by INIT

When set, indicates that Port Data Register 1 (XPD1) was written by the host. The firmware writes a one to this bit to clear the bit.

BIT<15>

Name: XPCP Register Written Mask

Mnemonic: XPCP REG WRT MSK

Type: R/W1C, 0 after reset, unaffected by INIT

When set, indicates that the Port Control Poll (XPCP) Register was written by the host. The firmware writes a one to this bit to clear the bit.

BIT<14>

Name: XPCS Register Written Mask

Mnemonic: XPCS REG WRT MSK

Type: R/W1C, 0 after reset, unaffected by INIT

When set, indicates that the Port Control Shutdown (XPCS) Register was written by the host. The firmware writes a one to this bit to clear the bit.

BIT<13>

Name: XPCI Register Written Mask

Mnemonic: XPCI REG WRT MSK

Type: R/W1C, 0 after reset, unaffected by INIT

When set, indicates that the Port Control Initialize (XPCI) Register was written by the host. The firmware writes a one to this bit to clear the bit.

BIT<12>

Name: XPRR Register Written Mask

Mnemonic: XPRR REG WRT MSK

Type: R/W1C, 0 after reset, unaffected by INIT

When set, indicates that the Port Ring Release (XPRR) Register was written by the host. The firmware writes a one to this bit to clear the bit.

BIT<11>

Name: XCOMM Register Written Mask

Mnemonic: XCOMM REG WRT MSK

Type: R/W1C, 0 after reset, unaffected by INIT

When set, indicates that the XMI Communications (XCOMM) Register was written by the host. The firmware writes a one to this bit to clear the bit.

BIT<10>

Name: XMI Interrupt Active

Mnemonic: INTR ACTIVE

Type: R0, 0 after reset and INIT

When set, indicates that the gate array has received an ACK for an interrupt that it sent to the host. The gate array clears this bit on receiving an IDENT.

BIT<9>

Name: Interrupt Host

Mnemonic: INTR

Type: R/W, 0 after reset and INIT

After setting up the appropriate interrupt information in the gate array, the firmware writes a one to this bit to initiate a host interrupt. The gate array clears the bit when interrupt processing is finished. The firmware can clear this bit only by resetting the gate array.

BIT<8>

Name: Abort Host Interrupt

Mnemonic: INTAB

Type: R0, 0 after reset and INIT

The firmware writes a one to this bit to abort a host interrupt in progress. The gate array clears the bit after the interrupt is successfully aborted. The gate array will not issue another host interrupt until the abort is completed. The firmware can clear this bit only by resetting the gate array.

BIT<7>

Name: Interrupt Error

Mnemonic: INTR ERROR

Type: R/W1C, 0 after reset, unaffected by INIT

When set, indicates that a host interrupt issued by the gate array experienced an error. The following errors can cause this bit to set: a transaction timeout, an IDENT coming back at the wrong IPL, an IDENT response that was NO ACKed, and an INTERRUPT command that was NO ACKed on the XMI bus. The firmware writes a one to this bit to clear the bit.

BIT<6>

Name: Gate Array Busy

Mnemonic: BUSY

Type: R0, 0 after reset, unaffected by INIT

When set, indicates that the gate array is busy processing a datamove operation or peek operation. This bit is an OR of all the Ownership bits in the datamove and peek registers.

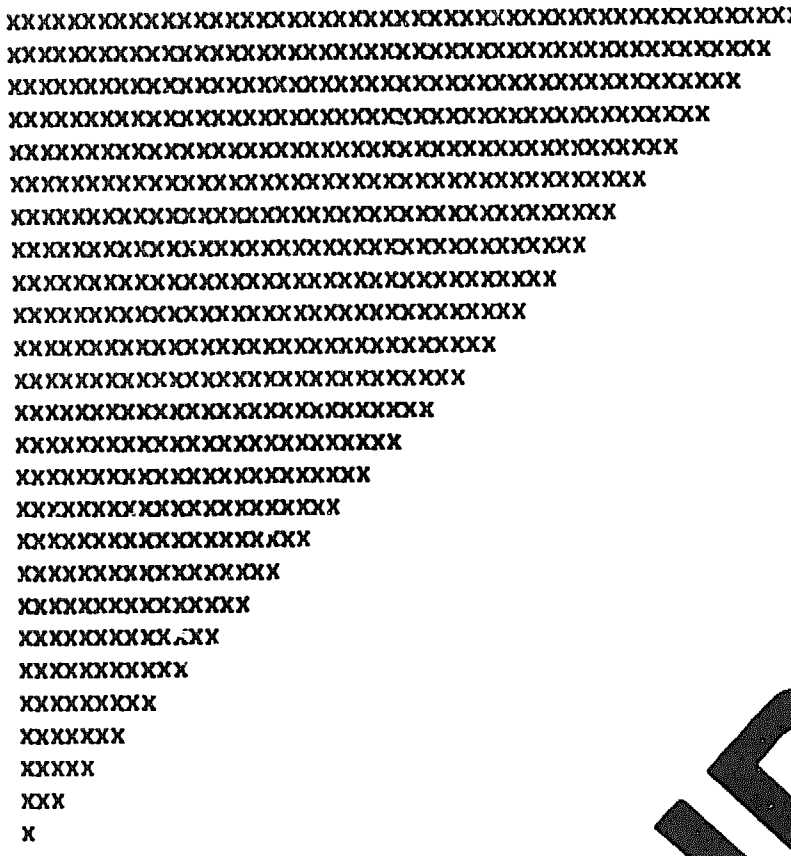
BITS<5:0>

Name: XMI Command ID

Mnemonic: XMI CMD ID

Type: R0

The last XMI command ID that was on the XMI bus.



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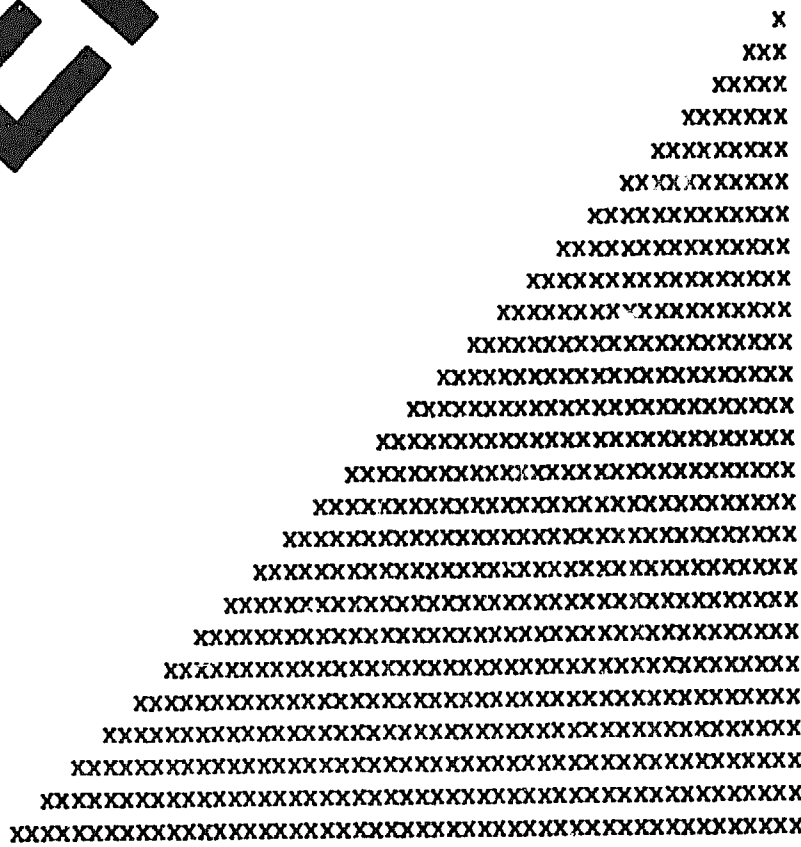


C How to Convert an Ethernet Address to a DECnet Address

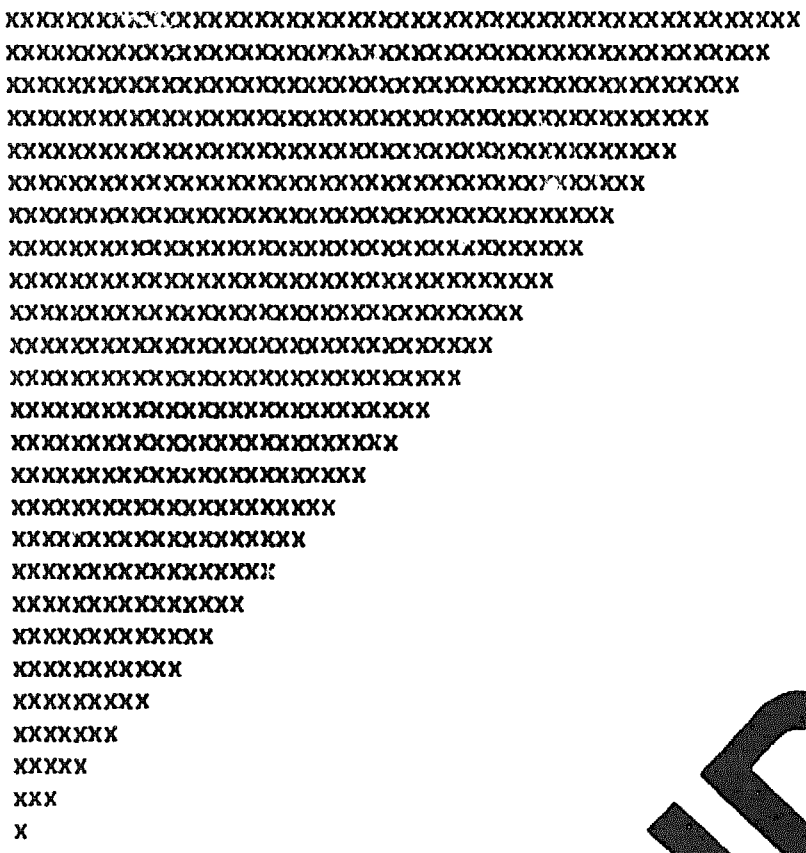
An Ethernet address is converted to a DECnet address as follows:

1. Take the two low-order bytes of the Ethernet address and swap them so that the low-order byte precedes the next-to-low-order byte.
2. Convert the hex value of the two bytes into a decimal number.
3. Divide the decimal number by 1024.
4. The quotient is the DECnet area number.
5. The remainder is the DECnet node number.

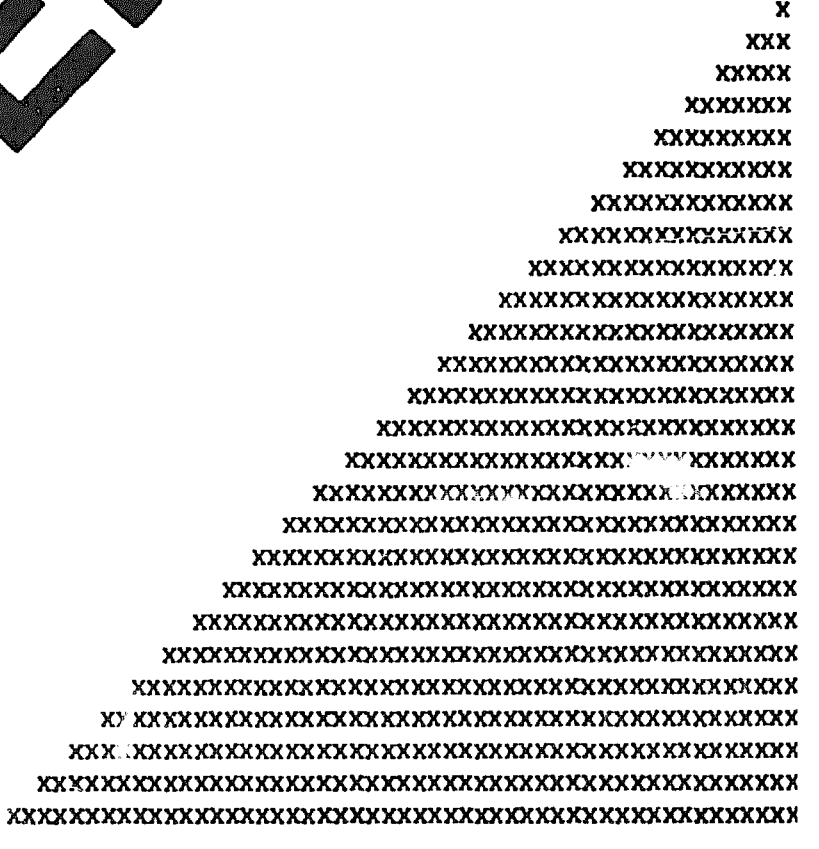
For example, the Ethernet address AA-00-04-00-00-26 is converted to a DECnet address as follows:

1. Swap the two low-order bytes of the address to get the hex value 2600.
2. Convert 2600 (hex) to the decimal number 9728.
3. Divide 9728 by 1024 to get a quotient of 9 and a remainder of 512.
4. The DECnet area number is 9.
5. The DECnet node number is 512.

The Ethernet address AA-00-04-00-00-26 converts to DECnet address 9.512, which references DECnet node 512 in DECnet area 9.



APPENDIX D



D How to Modify Flags in EEPROM

This appendix describes how to modify three flags in the DEMNA EEPROM. Two of these flags affect the operation of the console monitor program. Table D–1 describes the flags.

NOTE

The DEMNA EEPROM contains additional flags and parameters not described in this appendix. See the *DEC LANcontroller 400 Technical Manual* for a description of these flags and parameters.

Table D–1 EEPROM Flags

Name	Description
Enable Remote Boot	When set to Yes, enables the DEMNA to participate in remote booting over the network. When set to No, disables this function. See the *DEC LANcontroller 400 Technical Manual* for further information.
Enable Remote DEMNA Console	When set to Yes, enables the DEMNA console monitor program to be accessed from a remote network node. When set to No, denies access to the console monitor program from a remote node.
Enable Promiscuous Mode	When set to Yes, the DEMNA operates by default in promiscuous mode. When set to No, the DEMNA does not operate in promiscuous mode by default. (An application can override a flag setting of No by starting up a promiscuous user.) In promiscuous mode, the DEMNA receives all packets on the network, regardless of a packet's destination. The DEMNA console monitor program uses this information to determine characteristics of the network traffic. If no users defined to the DEMNA are enabled for promiscuous mode, the DEMNA discards the packets not addressed to a DEMNA user. Otherwise, the DEMNA delivers all received packets to each DEMNA user for whom promiscuous mode is enabled. (See the *DEC LANcontroller 400 Technical Manual* for further information on DEMNA operation in promiscuous mode.)

The setting of the flags in EEPROM can be modified by running the EEPROM Update Utility (EVGDB), which is a software diagnostic. Table D–2 specifies the distribution media for EVGDB for VAX 6000 and VAX 9000 systems.

Table D–2 Distribution Media for EVGDB

System	Tape Name	Tape Part Number
VAX 6000 Model 2xx	VAX 6200 Console Tape	AQ-FJ77B-ME
VAX 6000 Model 3xx	VAX 6300 Console Tape	AQ-FK60A-ME
VAX 6000 Model 4xx	VAX 6400 Console Tape	AQ-FK87A-ME
VAX 9000	VAX9000 CNSL + UCODE Tape	AQ-PAKJA-ME

EVGDB can be run under the VAX Diagnostic Supervisor (VAX/DS) or under the VAX/VMS operating system. Step 1 of the following procedure indicates how to run EVGDB under VAX/DS. Step 2 indicates how to run EVGDB under the VAX/VMS operating system.

Use the following procedure to modify the flags in EEPROM:

1 To run EVGDB under VAX/DS, do the following:

   a. Invoke the console prompt by typing CTRL/P on the system console.

   b. Boot the VAX Diagnostic Supervisor (VAX/DS) with the console BOOT command. See the system *Owner's Manual* for a description of this command. The following is the BOOT command used on a VAX 6000 system:

```
>>>BOOT/XMI:n/BI:x /R5:10 CSA1 RETURN
```

   where:

   n is the XMI node number of the DWMBA (XMI-to-VAXBI adapter)

   x is the VAXBI node number of the controller for the boot device

   The following is the BOOT command used on a VAX 9000 system:

```
>>>B VDS RETURN
```

See the *VAX 9000 Family System Maintenance Guide, Vol. 2* for further information on booting VAX/DS on a VAX 9000 system.

c. To run EVGDB under the VAX/VMS operating system, do the following:

   a. Log into the field service account, or, at the system prompt, enter the following command:

      ```
      $SET DEFAULT SYS$MAINTENANCE
      ```

   b. Run the VAX Diagnostic Supervisor (VAX/DS) with the following command:

      ```
      $RUN filename
      ```

      where *filename* is the executable VAX/DS file as follows:

VAX System	VAX/DS File
6000 Model 2xx/3xx	ELSAA
6000 Model 4xx	ERSAA
9000	EWSAA

d. The VAX/DS header is displayed. The following VAX/DS header is displayed on a VAX 6000 Model 2xx/3xx system:

```
                VAX DIAGNOSTIC SOFTWARE
                     PROPERTY OF
              DIGITAL EQUIPMENT CORPORATION

            ***CONFIDENTIAL AND PROPRIETARY***

Use Authorized Only Pursuant to a Valid Right-to-Use License
Copyright, Digital Equipment Corporation,  1989.  All Rights Reserved.

DIAGNOSTIC SUPERVISOR.  ZZ-ELSAA-11.7-870   1-JAN-1989 00:00:28
```

e. On a VAX 6000 system, enter the following commands at the VAX/DS prompt (DS>):

```
DS>LOAD EVGDB
DS>ATTACH DEMNA HUB EXm0 n [RETURN]
DS>SELECT ALL [RETURN]
DS>STAP    CTION=PARAM [RETURN]
```

where:

m is the unit number of the DEMNA. The DEMNA with the lowest XMI node number is unit A, the DEMNA with the second lowest XMI node number is unit B, and so on.

n is the XMI node number of the DEMNA

f. On a VAX 9000 system, enter the following commands at the VAX/DS> prompt:

```
DS>LOAD EVGDB
DS>ATTACH XJA HUB XJAx x [RETURN]
DS>ATTACH DEMNA XJAx0 EXm0 n [RETURN]
DS>SELECT ALL [RETURN]
DS>START/SECTION=PARAM [RETURN]
```

where:

m is the unit number of the DEMNA. The DEMNA with the lowest XMI node number is unit A, the DEMNA with the second lowest XMI node number is unit B, and so on.

n is the XMI node ID of the DEMNA

x is the XJA unit number (0–3)

g. When run in standalone mode, EVGDB runs the DEMNA self-test to verify the module operation. If self-test fails, EVGDB prints an error message and continues.

```
   Program  EVGDB - DEMNA EEPROM Update Utility, revision 1.1, 6 tests,
   at 15-06-50-29
Testing   EXA0

Initiating DEMNA self-test, wait 10 seconds...
```

h. EVGDB asks you to verify that the appropriate key switch on the front panel is set to the Update position.

```
Please insure that Front Panel Switch is in Update position.
Ready [(Yes), No]
```

If the key switch is set to Update, answer Yes. If the key switch is not set to Update, set it to Update before answering Yes.

NOTE

On VAX 9000 systems, the Service Processor Access switch on the operator control panel must be set

to LOCAL/SPU or REMOTE/SPU. Then issue the following command to enable EEPROM updating:

```
SET XMI_UPDATE/XMI:n ON
```

where *n* is the XMI card cage number (0-3)

i. EVGDB then asks whether you want to clear the EEPROM error log

```
Do you wish to clear the EEPROM error log?  [(No), Yes]
```

Normally, you should not clear the EEPROM error log.

j. EVGDB displays the firmware revision number and date, the module serial number, and the default settings of the parameter flags in EEPROM.

```
Reading parameters from EEPROM...

EEPROM firmware rev:      0601 04-APR-1990

DEMNA Serial Number:      *SG909T1488*

Enable Remote Boot?              (Default =  No)  N
Enable Remote DEMNA console?     (Default = Yes)  Y
Enable Promiscuous Mode?         (Default = Yes)  Y
```

k. EVGDB asks whether you want to modify any of the flag settings.

```
Do you wish to modify any of these parameters?  [(No), Yes]
```

l. If you answer No, the program prints the following message and then exits to the VAX/DS prompt (DS>):

```
No parameter changes made.
.. End of run, 0 errors detected, pass count is 1,
   time is  2-NOV-1989 11:14:58.77
DS>
```

If you answer Yes, EVGDB prompts you for the desired setting for each of the three flags:

```
Enable Remote Boot?              (Default =  No)     [(No), Yes]
Enable Remote DEMNA console?     (Default = Yes)     [(Yes), No]
Enable Promiscuous Mode?         (Default = Yes)     [(Yes), No]
```

Set the flags according to the customer's requirements.

m. The program asks twice whether you really want to modify the flag settings as you have indicated.

```
OK to modify EEPROM parameters?  [(No), Yes] Y

Are you sure?  [(No), Yes]
```

If you want to modify the parameters, answer Yes to both prompts.

n. EVGDB writes the modified flag settings to EEPROM and exits to the VAX/DS prompt (DS>):

```
Writing new parameters to EEPROM...
.. End of run, 0 errors detected, pass count is 1,
   time is  2-NOV-1989 11:14:17.08
DS>
```

o. Exit VAX/VDS.

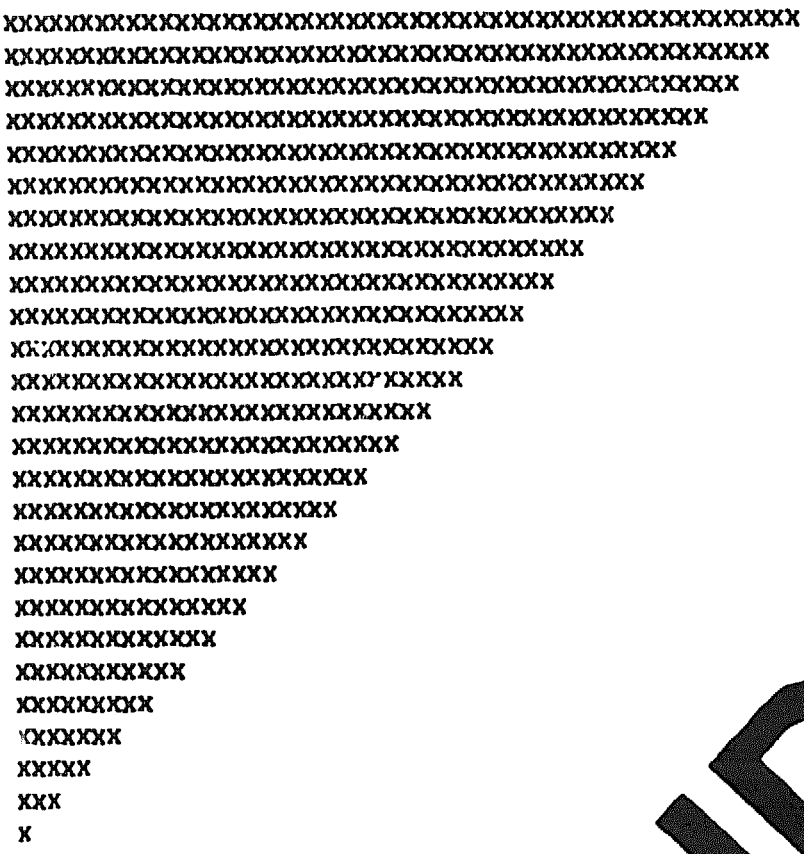
```
DS>EXIT [RETURN]
```

p. If you are on a VAX 6000 system, set the key switch to its former position (Halt or Auto Start). If you are on a VAX 9000 system, issue the following system console command to disable EEPROM updating:

```
SET XMI_UPDATE/XMI:n OFF
```

where *n* is the XMI card cage number (0-3)

and then set the Service Processor Access switch to the appropriate position.



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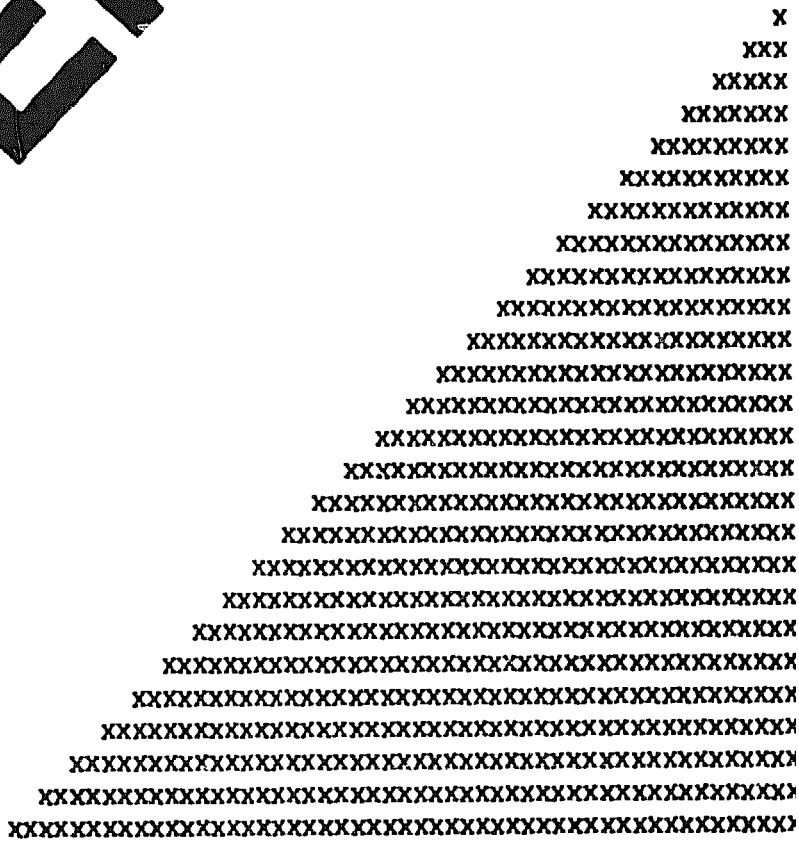
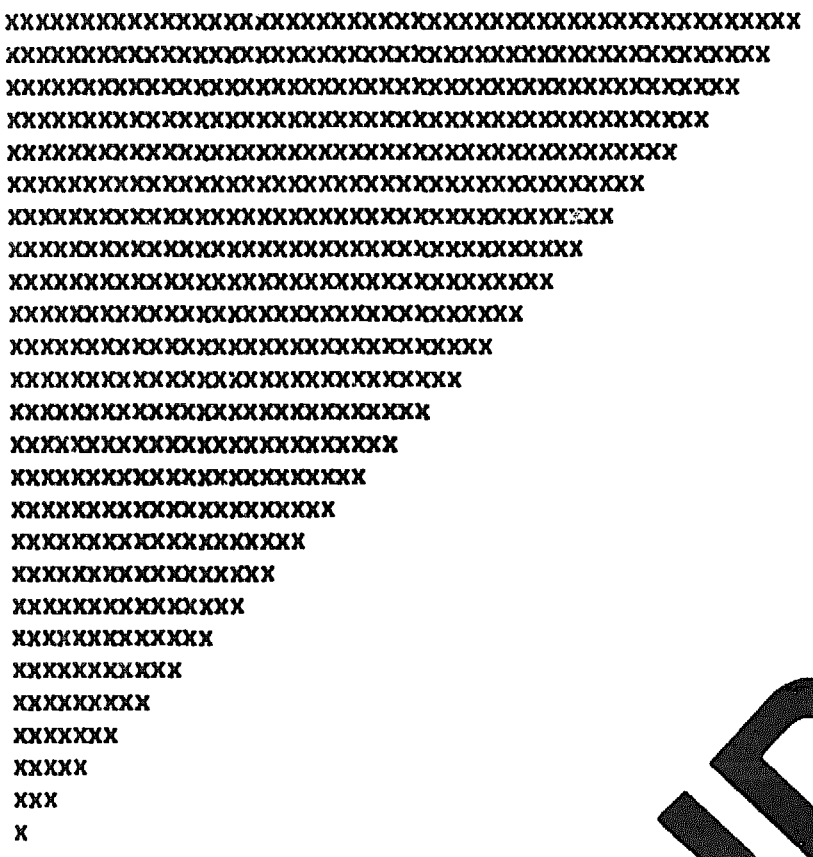


E Device Type Codes for XMI Modules

Table E–1 lists the device type codes for XMI modules available at the printing of this manual.

Table E–1 Device Type Codes for XMI Modules

Code	Device	Function
0C03	DEMNA	Ethernet/802 controller
0C05	CIXCD	CI Interface adapter
0C22	KDM70	Disk and tape controller
1001	XJA	XMI-to-SCU adapter
2001	DWMBA/A	XMI-to-VAXBI adapter (unmapped)
2002	DWMBB/A	+3.3V XMI-to-VAXBI adapter (mapped)
4001	MS62A	Memory module
8001	KA62A	VAX 6000 Model 200 CPU
8001	KA62B	VAX 6000 Model 300 CPU
8081	KN58A/A	DECsystem 5800 CPU
8082	KA64A	VAX 6000 Model 400 CPU



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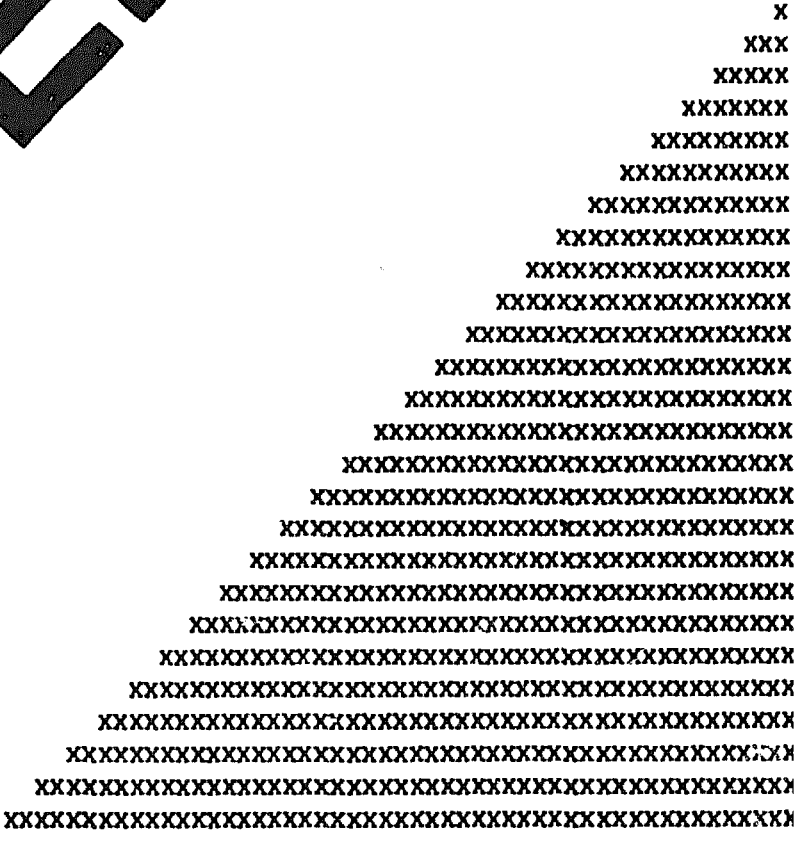


F Ethernet Protocol Types

Table F–1 lists the only cross-company (universally administered) Ethernet protocol type. Table F–2 lists the Ethernet protocol types assigned by Digital.

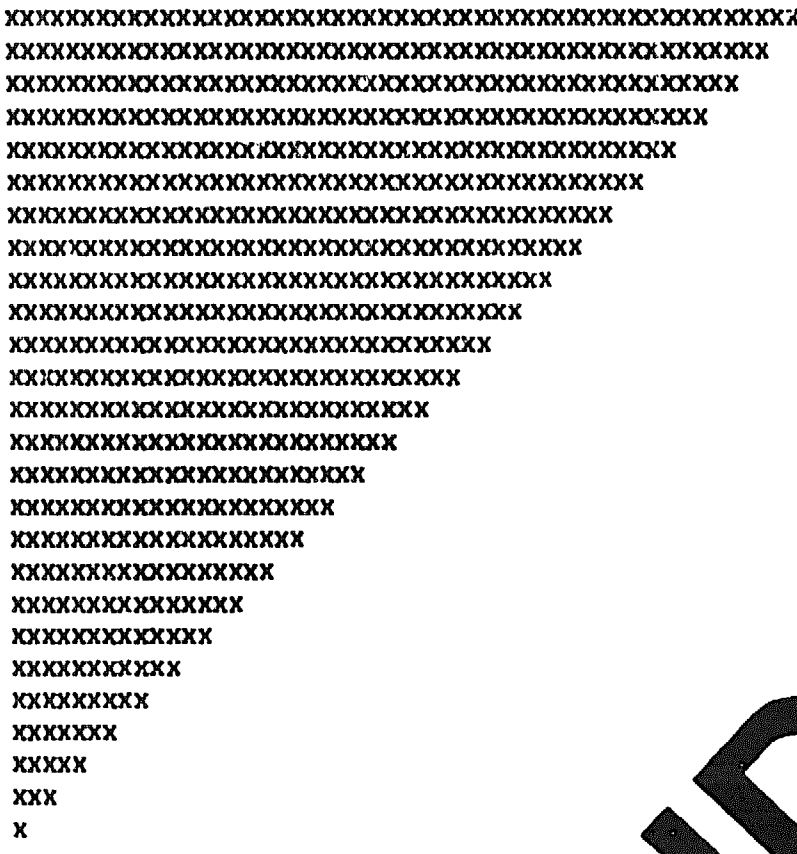
Table F–1 Cross-Company Ethernet Protocol Type

Protocol Type	Description
90-00	Ethernet loopback

Table F–2 Digital's Ethernet Protocol Types

Protocol Type	Description
60-01	DNA Dump/Load (MOP)
60-02	DNA Remote Console (MOP)
60-03	DNA Routing
60-04	Local Area Transport (LAT)
60-05	Diagnostics
60-06	Customer use
60-07	System Communication Architecture (SCA)
30-38	Bridge
80-3B	VAXELN
80-3C	DNA Naming Service
80-3D	CSMA/CD Encryption
80-3F	LAN Traffic Monitor
80-40	NetBios emulator (PCSG)
80-42	Reserved

The protocol types 00-00 through 05-DC are reserved so that 802.3 format frames can be distinguished from Ethernet format frames. Use of these protocol types in Ethernet format frames is incompatible with correct operation of the CSMA/CD Data Link.



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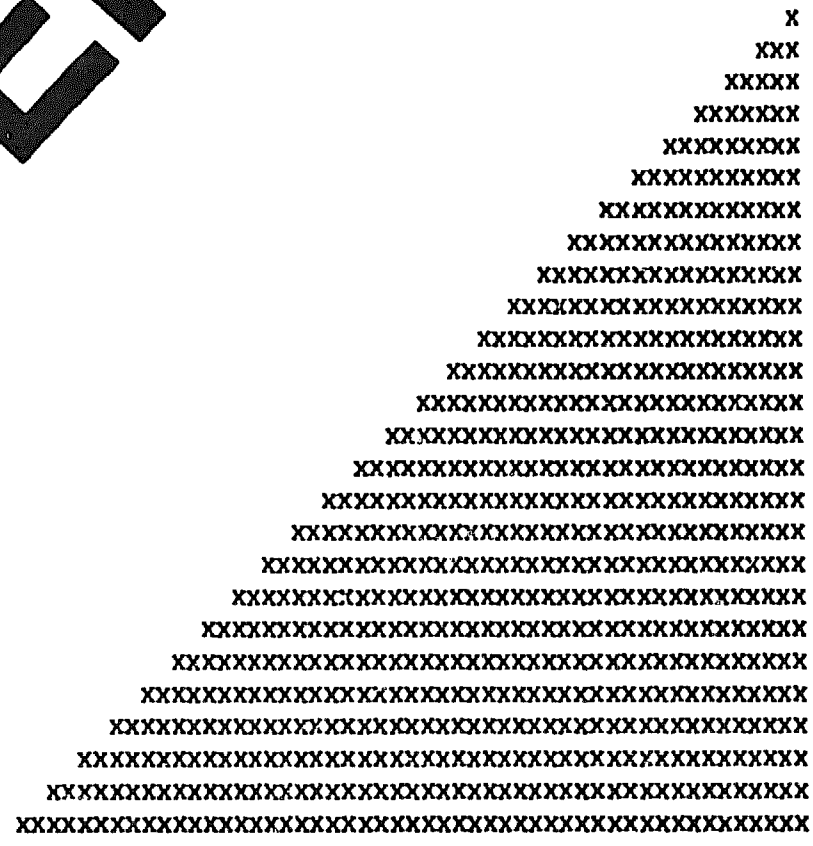


G Ethernet Addresses

Table G–1 lists the cross-company (universally administered) Ethernet multicast addresses. Table G–2 lists the Ethernet multicast addresses assigned by Digital. Table G–3 lists the Ethernet physical addresses assigned to Digital prototypes, parts, or units. Table G–4 lists the address blocks assigned to other organizations but used in Digital products.

Table G–1 Cross-Company Multicast Addresses

Multicast Address	Description
01-80-C2-00-00-00	IEEE 802.1d Bridge group address
01-80-C2-00-00-0X	IEEE 802.1d Reserved (always filtered by bridges)
01-80-C2-00-00-10	IEEE 802.1d All LANs Bridge Management group address
01-80-C2-00-00-11	IEEE 802.1e Load Server group address
01-80-C2-00-00-12	IEEE 802.1e Loadable Device group address
09-00-2B-00-00-04	ISO 9542 End System Hello
09-00-2B-00-00-05	ISO 9542 Intermediate System Hello
CF-00-00-00-00-00	Loopback Assistance
FF-FF-FF-FF-FF-FF	Broadcast

Table G–2 Digital's Multicast Addresses

Multicast Address	Description
AA-00-00-01-00-00	DNA Dump/Load Assistance (MOP)
AA-00-00-02-00-00	DNA Remote Console (MOP)
AB-00-00-03-00-00	DNA Level 1 Routing Layer routers
AB-00-00-04-00-00	DNA Routing Layer end nodes
AB-00-04-00-XX-XX	Customer use
AB-00-04-01-XX-XX	System Communication Architecture (SCA)
09-00-2B-00-00-02	VAXELN

Table G–2 (Cont.) Digital's Multicast Addresses

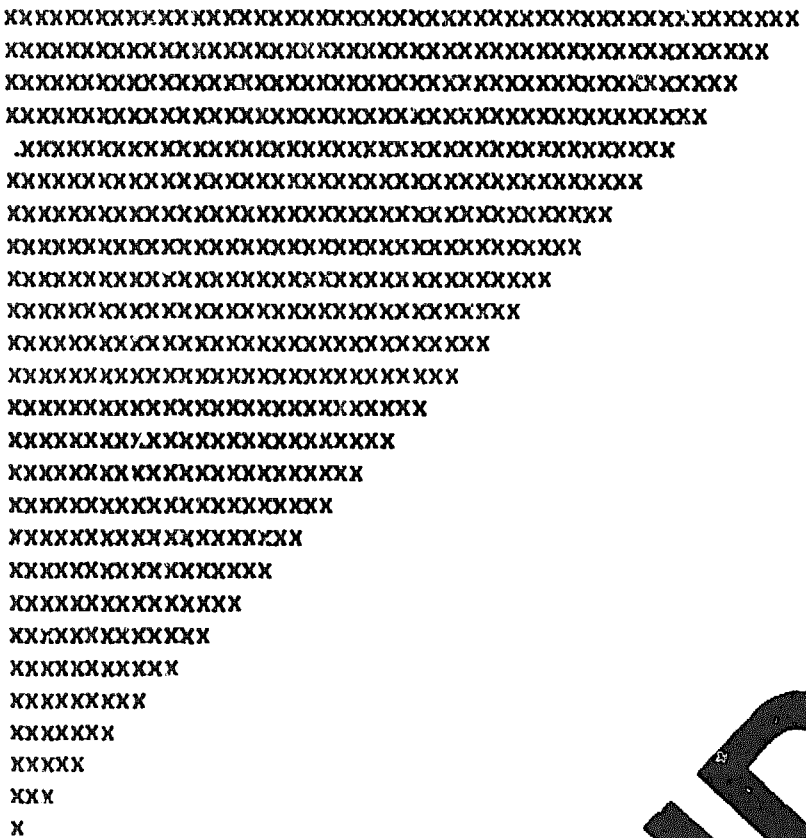
Multicast Address	Description
09-00-2B-00-00-03	LAN Traffic Monitor
09-00-2B-00-00-06	CSMA/CD Encryption
09-00-2B-00-00-07	NetBios Emulator (PCSG)
09-00-2B-00-00-0F	Local Area Transport (LAT)
09-00-2B-01-00-00	All bridges
09-00-2B-01-00-01	All local bridges
09-00-2B-02-00-00	DNA Level 2 Routing Layer routers
09-00-2B-02-01-00	DNA Naming Service Advertisement
09-00-2B-02-01-01	DNA Naming Service Solicitation

Table G–3 Digital's Physical Addresses

Physical Address	Description
AA-00-04-00-XX-XX	DECnet Phase IV station addresses
AA-00-03-00-XX-XX	UNA prototype
AA-00-03-01-XX-XX	DEUNA products
AA-00-03-02-XX-XX	Miscellaneous assignments
AA-00-03-02-00-00	H4000-TA Ethernet Transceiver Tester
AA-00-03-03-XX-XX	NI20 products
08-00-2B-0X-XX-XX	PROM 23-365A1-00
08-00-2B-1X-XX-XX	PROM 23-365A1-00
08-00-2B-22-00-00	Bridge management

Table G–4 Other Physical Addresses

Physical Address	Description
00-00-69-02-XX-XX	DTQNA, Concord Communications Inc.



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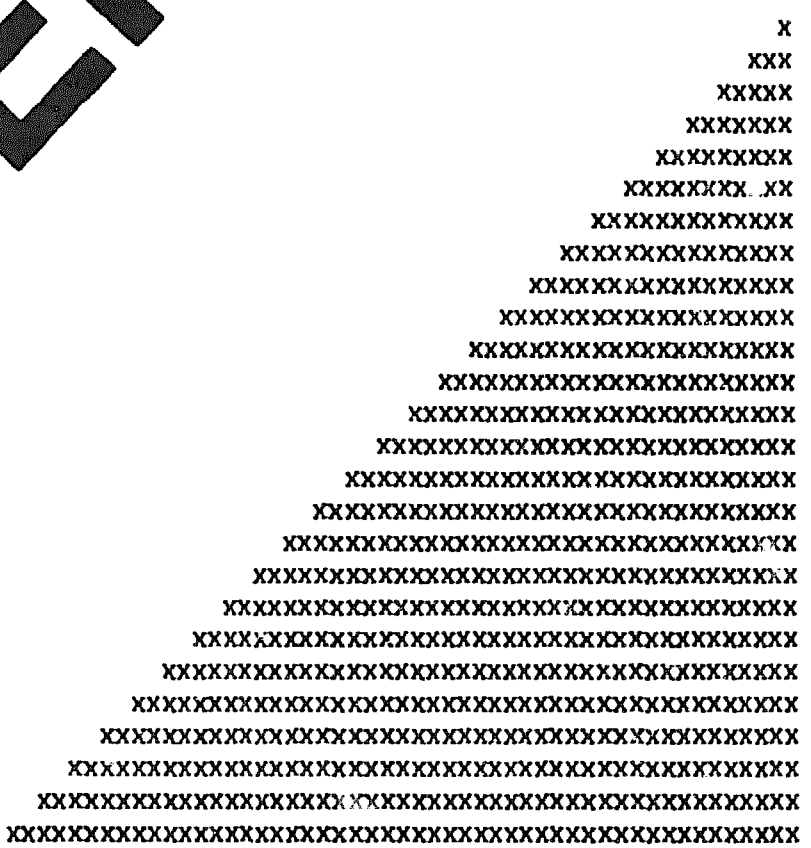

H SAP Assignments and SNAP Protocol ID Assignments

Table H–1 lists the cross-company (universally administered) SAP assignments. No SAPs are assigned by Digital. Table H–2 lists the SNAP protocol IDs (PIDs) assigned by Digital. There are no cross-company (universally administered) SNAP PIDs.

Table H–1 Cross-Company SAP Assignments

SAP	Description
03	LLC sublayer management function group SAP (IEEE 802.1b)
FF	Global DSAP
00	Null SAP
02	LLC sublayer management function individual SAP (IEEE 802.1b)
06	ARPAnet IP
0E	PROWAY (IEC 955) network management and initialization
42	IEEE 802.1d (ISO 10038) transparent bridge protocol
4E	EIA RS-511 Manufacturing Message Service
7E	ISO 8208 (X.25 over IEEE 802.2 type 2 LLC)
8E	PROWAY (IEC 955) active station list maintenance
AA	SNAP SAP
FE	ISO Network Layer entity

Table H–2 Digital's SNAP Protocol IDs

Protocol ID	Description
08-00-2B-60-01	DNA Dump/Load (MOP)
08-00-2B-60-02	DNA Remote Console (MOP)
08-00-2B-60-03	DNA Routing
08-00-2B-60-04	Local Area Transport (LAT)

Table H–2 (Cont.) Digital's SNAP Protocol IDs

Protocol ID	Description
08-00-2B-60-05	Diagnostics
08-00-2B-60-06	Customer use
08-00-2B-60-07	System Communication Architecture (SCA)
08-00-2B-80-3B	VAXELN
08-00-2B-80-3C	DNA Naming Service
08-00-2B-80-3D	CSMA/CD Encryption
08-00-2B-80-3F	LAN Traffic Monitor
08-00-2B-80-40	NetBios emulator (PCSG)
08-00-2B-90-00	MOP LAN Loopback protocol


APPENDIX I

I How to Read the DEMNA Ethernet Address

The DEMNA's default Ethernet address, which is also called the default physical address (DPA), is stored in the DEMNA MAC address (ENET) PROM. The DEMNA uses the DPA as its Ethernet address unless the operating system assigns it a DECnet address.

I.1 Systems with DECnet

If DECnet is running on your system, invoke the Network Control Program (NCP) and use the following commands to display the DEMNA's DPA:

```
$ MC NCP [RETURN]
NCP>TELL node SHOW KNOWN LINE CHARACTERISTICS
```

where *node* is the name of the Ethernet node at which the DEMNA resides

The line characteristics of the selected node are displayed in a format similar to the following

```
Known Line Volatile Characteristics as of 26-APR-1989 16:06:41

Line = MNA-0

Receive buffers          = 6
Controller               = normal
Protocol                 = Ethernet
Service timer            = 4000
Hardware address         = 08-00-2B-09-CD-F3
Device buffer size       = 1498
```

The hardware address is the DEMNA's DPA.

I.2 From the Console Monitor Program

When using the DEMNA console monitor program, you can read the DEMNA DPA from the DEMNA ENET PROM as follows:

1 Examine address 20007000 to read the first four bytes of the DPA.

2 Examine address 20007004 to read the last two bytes of the DPA.

Example I–1 illustrates this procedure.

Example I–1 Examining the DEMNA DPA from the DEMNA Console Monitor Program

```
>>>E 20007000                    ! Read first four bytes of DPA from
                                 ! ENET PROM.
     20007000/ 092B0008
>>>E 20007004                    ! Read last two bytes of DPA from
                                 ! ENET PROM.
     20004004  0000F3CD
```

The above Ethernet address bytes are transmitted in the following order (left-to-right) over the network: 08-00-2B-09-CD-F3.

I.3 VAX 6000 System

If you are on a VAX 6000 system, use the SHOW ETHERNET console command to display the DEMNA DPA as follows:

```
>>>SHOW ETHERNET
XMI:3 08-00-2B-09-CD-F3
```

The command displays the XMI node number of the DEMNA and the DEMNA DPA.

If the SHOW ETHERNET command cannot find the DEMNA, you can read the DEMNA DPA by depositing and examining the DEMNA's XMI Communications (XCOMM) Register as indicated below:

```
>>> D XCOMM_address FFFFFFFF
>>> E XCOMM_address
>>> D XCOMM_address FFFFFFFE
>>> E XCOMM_address
```

where *XCOMM_address* is the address of the DEMNA's XCOMM Register. The XCOMM Register is at address BB + 10, where address (BB) is the base address of the DEMNA nodespace computed (in hex) as follows:

21800000 + (80000 * XMI_ID)

where XMI_ID is the DEMNA's XMI node ID

Example I–2 shows how to examine the DPA of a DEMNA at XMI node 3. The XDEV Register is examined first to confirm that the module being examined is a DEMNA (device type = 0C03).

Example I–2 Examining the DEMNA DPA on a VAX 6000

```
>>>E 21980000                    ! Examine XDEV Register
   P 21980000    06010C03

>>>D 21980010    FFFFFFFF        ! Deposit FFFFFFFF into XCOMM Register
>>>E 21980010                    ! Examine XCOMM Register to obtain
                                 ! first four bytes of DPA
   P 21980010    092B0008

>>>D 21980010    FFFFFFFE        ! Deposit FFFFFFFE into XCOMM Register
>>>E 21980010                    ! Examine XCOMM Register to obtain
                                 ! last two bytes of DPA
   P 21980010    0000F3CD
```

The above Ethernet address bytes are transmitted in the following order (left-to-right) over the network: 08-00-2B-09-CD-F3.

I.4 VAX 9000 System

If you are on a VAX 9000 system, you can read the DEMNA DPA by depositing and examining the XCOMM Register as described in Section I.3. The XCOMM Register is at address BB + 10, where address (BB) is the base address of the DEMNA nodespace computed (in hex) as follows:

20000000 + (XJA_ID * 800000) + (XMI_ID * 8000)

where:

XJA_ID is the XJA unit number

XMI_ID is the DEMNA's XMI node number

Example I–3 shows how to examine the DPA of a DEMNA at XMI node 4 through XJA number 2. The XDEV Register is examined first to confirm that the module being examined is a DEMNA (device type = 0C03).

Example I–3 Examining the DEMNA DPA on a VAX 9000

```
>>>E 21020000                    ! Examine XDEV Register

   P 21020000    06010C03

>>>D 21020010    FFFFFFFF        ! Deposit FFFFFFFF into XCOMM Register
>>>E 21020010                    ! Examine XCOMM Register to obtain
                                 ! first four bytes of DPA
   P 21020010    092B0008
>>>D 21020010    FFFFFFFF        ! Deposit FFFFFFFE into XCOMM Register
>>>E 21020010                    ! Examine XCOMM Register to obtain
                                 ! last two bytes of DPA
   P 21020010    0000F3CD
```

The above Ethernet address bytes are transmitted in the following order (left-to-right) over the network: 08-00-2B-09-CD-F3.


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