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# VAX 11/750 INFORMATION

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</table>
1 - GENERAL INFORMATION
SUMMARY OF SPECIFICATIONS

CPU

TYPE: KA750 (VAX 11/750)
CPU CYCLE TIME: 320ns
INTERNAL DATA PATHS: 32-bit
INSTRUCTION BUFFER: 8-byte
TRANSLATION BUFFER: 512 entries
TRANSLATION BUFFER TYPICAL HIT RATIO: 98-99%
PERFORMANCE FACTOR: 0.6
CONTROL STORE: 6KW ROM Standard, 1KW RAM OPTION or, 6KW ROM and 1KW RAM Standard (W=80 bits)

CACHE MEMORY

TYPE: DIRECT MAPPING
SIZE: 4KB
TYPICAL CYCLE TIME: 320ns
TYPICAL HIT RATIO: 90%

MAIN MEMORY

PHYSICAL ADDRESS SIZE: 24-bits (16MB)
MAXIMUM PHYSICAL MEMORY EXPANSION: 8MB
PARITY: 7-bit ECC
CYCLE TIME:
READ - 800ns
WRITE - 640ns

POWER REQUIREMENTS

MAINS SUPPLY: SINGLE PHASE 240V AC
MAXIMUM POWER CONSUMPTION: 1700 watts
PHYSICAL ADDRESS SPACE

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
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<tbody>
<tr>
<td>FFFFFF</td>
<td>UNIBUS 0 MEMORY SPACE 128KB</td>
</tr>
<tr>
<td>FC0000</td>
<td>UNIBUS 1 MEMORY SPACE 128KB</td>
</tr>
<tr>
<td>FBFFFF</td>
<td>UNIBUS 1 MAP REGISTERS</td>
</tr>
<tr>
<td>F28000</td>
<td>UNIBUS 0 DATA PATH CONTROL &amp; STATUS</td>
</tr>
<tr>
<td>F20000-C</td>
<td>UNIBUS 0 MAP REGISTERS</td>
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<td>F30000-C</td>
<td>UNIBUS 0 DATA PATH CONTROL &amp; STATUS</td>
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<tr>
<td>F2C800</td>
<td>MASSBUS ADAPTOR 2 MAP REGISTERS</td>
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<td>F2C400</td>
<td>MASSBUS ADAPTOR 2 EXT. REGISTERS</td>
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<tr>
<td>F2C000</td>
<td>MASSBUS ADAPTOR 2 INT. REGISTERS</td>
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<td>&quot;BOOTSTRAP ROM C&quot;</td>
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<td>F20004</td>
<td>MEMORY CONTROL/STATUS REG. 1</td>
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<td>F20000</td>
<td>MEMORY CONTROL/STATUS REG. 0</td>
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<tr>
<td>F10000</td>
<td>&quot;10 KB USER CONTROL STORE&quot;</td>
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<tr>
<td>F00000</td>
<td>&quot;---I/O SPACE&quot;</td>
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7FFFFF 8 MB
700000  7 MB
6FFFFF  6 MB
600000  5 MB
5FFFFF  4 MB
500000  3 MB
4FFFFF  2 MB
400000  1 MB
3FFFFF  1 MB
300000  0 MB
2FFFFF
200000
1FFFFF
100000
0FFFFF
000000

MAXIMUM FULLY POPULATED ARRAYS

1 ARRAY BOARD
# INTERNAL PROCESSOR REGISTERS

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<th>IPR No.</th>
<th>Mnemonic</th>
<th>RW*</th>
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<tbody>
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<td>00</td>
<td>KSP</td>
<td>RW</td>
<td>Kernel Stack Pointer</td>
</tr>
<tr>
<td>01</td>
<td>ESP</td>
<td>RW</td>
<td>Executive Stack Pointer</td>
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<td>SSP</td>
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<td>Supervisor Stack Pointer</td>
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<td>USP</td>
<td>RW</td>
<td>User Stack Pointer</td>
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<td></td>
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<tr>
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<td>P0BR</td>
<td>RW</td>
<td>P0 Base Register</td>
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<tr>
<td>09</td>
<td>P0LR</td>
<td>RW</td>
<td>P0 Length Register</td>
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<td>RW</td>
<td>Pl Base Register</td>
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<tr>
<td>0B</td>
<td>PlLR</td>
<td>RW</td>
<td>Pl Length Register</td>
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<td>SLR</td>
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<td>AST Level Register</td>
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<td>RW</td>
<td>Software Interrupt Summary Register.</td>
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<td>CMIERR</td>
<td>RO</td>
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<td>ICCS</td>
<td>RW</td>
<td>Interval Clock Control/Status</td>
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<tr>
<td>19</td>
<td>NICR</td>
<td>WO</td>
<td>Next Interval Count Register</td>
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<td>ICR</td>
<td>RO</td>
<td>Interval Count Register</td>
</tr>
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<td>TODR</td>
<td>RW</td>
<td>Time of Day Register</td>
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<tr>
<td>1C</td>
<td>CSRS</td>
<td>RW</td>
<td>Console Storage Receiver Status</td>
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<tr>
<td>1D</td>
<td>CSRD</td>
<td>RO</td>
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<td>CSTS</td>
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<td>RW</td>
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<td>CADR</td>
<td>RW</td>
<td>Cache Disable Register</td>
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<td>MCESR</td>
<td>RW</td>
<td>Machine Check Error Summary Register.</td>
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<td>Accelerator Control/Status Register.</td>
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</tr>
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<td>37</td>
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<td>WO</td>
<td>Initialize Unibus</td>
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<td>MME</td>
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<td>Memory Management Enable</td>
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<td>TIBIA</td>
<td>WO</td>
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<td>TBIS</td>
<td>WO</td>
<td>Translation Buffer Invalidate Single.</td>
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<td>TB Data</td>
<td>RW</td>
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<td>3C</td>
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<td></td>
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<tr>
<td>3D</td>
<td>PMR</td>
<td>RW</td>
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<td>SID</td>
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<tr>
<td>3F</td>
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</table>

*RO means read-only; WO means write-only. RW means both read and write.
INTERNAL PROCESSOR REGISTERS, BIT DEFINITIONS

The following diagrams illustrate the format of the 8750 specific internal processor registers.

**IPR 17 CMI ERROR REGISTER**

<table>
<thead>
<tr>
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<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
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<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

0=CMI
ENABLED
1=CMI
DISABLED

READ=1,
MODIFY=0

VIRTUAL=0,
PHYSICAL=1

CPU MODE, (__________
K,E,S,U. (__________

READ LOCK TIMEOUT

TB G1 TAG ERROR

TB G0 TAG ERROR

TB G1 DATA ERROR

TB G0 DATA ERROR

TB HIT

MEMORY ERROR

READ DATA SUBSTITUTE

LOST ERROR

CORRECTED READ DATA
Console Storage Receiver Status

31 8 7 6 5 0
IPR 1C CSRS

Console Storage Receiver Data

31 7 6 5 4 3 2 1 0
IPR 1D CSRD

RECEIVE FROM TU58

Console Storage Transmit Status

31 8 7 6 5 0
IPR 1E CSTS

Console Storage Transmit Data

31 7 6 5 4 3 2 1 0
IPR 1F CSTD

TRANSMIT FROM TU58

Console Receive Control/Status

31 0 8 0 7 0 6 0 5 0 0
IPR 20 RXCS

DONE
Console Receive Data Buffer

31  08 07  00

IPR 21 RXDB

0  BYTE 0

READ ONLY

Console Transmit Control/Status

31  08 07 06 05  00

IPR 22 TXCS

0  IE  0

READY

ENABLE
INTERRUPTS
&
EXCEPTIONS
= 1

Console Transmit Buffer

31  08 07  00

IPR 23 TXDB

0  BYTE 0

WRITE ONLY

Translation Buffer Group Disable Register

31

IPR 24 TBGDR

0

0 = RANDOM REPLACEMENT
1 = FORCE REPLACEMENT

0 = REPLACE GROUP 0
1 = REPLACE GROUP 1

FORCE MISS GROUP 1
FORCE MISS GROUP 0

This IPR is read/write to all bits
Cache Disable Register

31  0

IPR 25 CADR

DISABLE CACHE

This IPR is read/write

Machine Check Error Summary Register

This IPR is read/write to all bits. Writing a 1 to bit 3 clears the bus error register. Writing a 1 to bit 2 clears the TB Group Parity Register.

31  3 2 1 0

IPR 26 MCESR

BUS ERROR, REFER TO BUS ERROR REG.

TB PARITY ERROR

UNALIGNED UNIBUS REFERENCE

XB FETCH = 1, OPERAND FETCH = 0

Cache Error Register

31  3 2 1 0

IPR 27

CACHE TAG PARITY ERROR

CACHE DATA PARITY ERROR

LOST ERROR

CACHE HIT

This IPR is read/write
Reset Initialize Unibus

IPR 37 IO

ISSUE UNIBUS INIT

System Identification (Read Only)

IPR 3E SID

<table>
<thead>
<tr>
<th>SYSTEM TYPE</th>
<th>MICROCODE REVISION LEVEL</th>
<th>HARDWARE REVISION LEVEL</th>
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<tbody>
<tr>
<td>00</td>
<td>UNDEFINED</td>
<td>FROM MICRO</td>
</tr>
<tr>
<td>01</td>
<td>8780</td>
<td>FROM WORD</td>
</tr>
<tr>
<td>02</td>
<td>8750</td>
<td>FROM LITERAL</td>
</tr>
<tr>
<td>03</td>
<td>8730</td>
<td>FROM FIELD</td>
</tr>
</tbody>
</table>

Reserved Operand Fault if Write
MEMORY REGISTERS

CSRO Bit Allocations

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>24</th>
<th>23</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>PAGE ADDRESS OF ERROR</td>
<td>0</td>
<td>ERROR SYNDROME</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- CRD ERROR LOG REQUEST (1 BIT ERROR)
- RDS HIGH ERROR RATE
- RDS ERROR LOG REQUEST (MORE THAN 1 BIT ERROR)

CSRL Bit Allocations

<table>
<thead>
<tr>
<th>31</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>PAGE MODE ADDRESS</td>
<td>0</td>
<td>CHECK SYNDROME</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- DISABLE ERROR CORRECTION
- DIAGNOSTIC CHECK MODE (FOR VERIFY SYNDROME BITS FUNCTION)
- PAGE MODE
- ENABLE REPORTING CORRECTED ERRORS ENABLE CRD INTERRUPT

Control/Status Register 2 (RO)

<table>
<thead>
<tr>
<th>31</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>UNDEFINED</td>
<td>STARTING ADDRESS</td>
<td>MEMORY PRESENT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- 0 INDICATES 16K RAMS USED IN MEMORY ARRAY

- BACKPLANE JUMPER SELECTABLE

- BITS <15:0> INDICATE MEMORY PRESENT IN 128KB INCREMENTS (2 BITS PER MODULE)

- INIT - COLD/WARM RESTART FLAG
  - 1 ON POWER UP OR BATTERY DEAD
  - 0 AFTER FIRST 4 BYTE WRITE
UET REGISTERS

FFFF464 UET Control Register

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

- ISSUE UNIBUS INIT (WRITE 1 TO CLEAR UET CR<11:5>)
- SELECT BUS REQUEST LEVEL (WRITE 1 TO CAUSE UET TO REQUEST UNIBUS VIA BR/BG)
- 1 = PARITY ERROR (PB) RECEIVED ON UNIBUS
- 1 = TIME OUT WHEN UET WAS MASTER
- WRITE 1 TO FORCE PB LINE ON UNIBUS
- HIGHEST ORDER ADDRESS BITS <17:16> FOR UET NPR CYCLES

UNIBUS TRANSFER SELECT
00 DATI
01 DATIP
10 DATO
11 DATOB

INITIATE BUS REQUEST (NPR) FOR D.M.A.

FFFF460 UET Bus Address Register (BAR)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
FFF462 UET Data Register (DR)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

FFF466 PROM Register (RO)

15

08 07

F F

F F
PROCESSOR STATUS LONGWORD

31 30 27 26 25 24 23 22 20 16 15 8 7 6 5 4 3 2 1 0

Bits | Description
--- | ---
0-C | Bit 0 is the carry condition code.
1-V | Bit 1 is the overflow condition code.
2-Z | Bit 2 is the zero condition code.
3-N | Bit 3 is the negative condition code.
4-T | Bit 4 is the Trace enable.
5-IV | Bit 5 is the Integer Overflow trap enable.
6-FU | Bit 6 is the Floating Underflow trap enable.
7-DV | Bit 7 is the Decimal Overflow trap enable.
15:8-MBZ | These eight bits are reserved and Must Be Zero.
20:16-IPL | Bits 10 through 16 make up the Interrupt Priority Level or IPL field.
21-MBZ | Bit 21 is reserved and Must Be Zero.
23:22-PREVMOD | Bits 22 and 23 are the Previous Mode Field.
25:24-CURMOD | Bits 24 and 25 are the Current Mode Field.
26-IS | Bit 26 is the Interrupt Stack active bit.
27-FPD | Bit 27 is the First Part Done Bit.
29:28-MBZ | These two bits are reserved and Must Be Zero.
30-TP | Bit 30 is the Trace Pending Bit.
31-CM | Bit 31 is the Compatibility Mode Bit.

Note: There are other trap conditions which are always enabled - division by zero and floating overflow.
GENERAL PURPOSE REGISTERS

The VAX architecture defines 16, 32-bit General Purpose Registers shown below.

- GPR 0
- GPR 1
- GPR 2
- GPR 3
- GPR 4
- GPR 5
- GPR 6
- GPR 7
- GPR 8
- GPR 9
- GPR A
- GPR B

- GPR C - AP (ARGUMENT POINTER)
- GPR D - FP (FRAME POINTER)
- GPR E - SP (STACK POINTER)
- GPR F - PC (PROGRAM COUNTER)
11/750 INTERRUPT PRIORITY LEVELS

<table>
<thead>
<tr>
<th>IPL</th>
<th>CONDITION</th>
<th>VECTOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1F</td>
<td>MACHINE CHECK - CS PARITY</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>- TB PARITY</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- BAD IRD</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- MEMORY ERROR</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- CACHE PARITY</td>
<td></td>
</tr>
<tr>
<td></td>
<td>KERNEL STACK NOT VALID</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>INTERRUPT STACK NOT VALID</td>
<td></td>
</tr>
<tr>
<td>1E</td>
<td>POWER FAIL</td>
<td>C</td>
</tr>
<tr>
<td>1D</td>
<td>WRITE BUS ERROR</td>
<td>60</td>
</tr>
<tr>
<td>1C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1A</td>
<td>CORRECTED READ DATA</td>
<td>54</td>
</tr>
<tr>
<td>19</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>INTERVAL TIMER</td>
<td>CO</td>
</tr>
<tr>
<td>17</td>
<td>TU58 RECEIVE</td>
<td>F0</td>
</tr>
<tr>
<td></td>
<td>TU58 TRANSMIT</td>
<td>F4</td>
</tr>
<tr>
<td></td>
<td>UNIBUS BR7</td>
<td>200 + VEC</td>
</tr>
<tr>
<td>16</td>
<td>CONSOLE RECEIVE</td>
<td>F8</td>
</tr>
<tr>
<td></td>
<td>CONSOLE TRANSMIT</td>
<td>FC</td>
</tr>
<tr>
<td></td>
<td>UNIBUS BR6</td>
<td>200 + VEC</td>
</tr>
<tr>
<td>15</td>
<td>MBA0</td>
<td>150</td>
</tr>
<tr>
<td></td>
<td>MBA1</td>
<td>154</td>
</tr>
<tr>
<td></td>
<td>MBA2</td>
<td>158</td>
</tr>
<tr>
<td></td>
<td>UNIBUS BR5</td>
<td>200 + VEC</td>
</tr>
<tr>
<td>14</td>
<td>UNIBUS BR4</td>
<td>200 + VEC</td>
</tr>
<tr>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td></td>
<td>BC</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SOFTWARE INTERRUPTS

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NORMAL PROCESS PRIORITY -
OPERATOR CONTROL PANEL

INDICATORS (meaning when on)
- POWER: DC Power OK
- RUN: VAX CPU is Running
- ERROR: Control Store Parity Error (Lit Brightly)

KEYSWITCH
- OFF: DC Power Off
- SECURE: DC Power On, Console I/O Mode Disabled
- LOCAL: DC Power On, Console I/O Mode and Program I/O mode enabled.

POWER-ON ACTION SWITCH
- BOOT: Will boot device selected by the boot device switch on power-up or if RESET switch activated.
- RESTART: On power-up or RESET will attempt to RESTART VMS, if fails will reboot VMS.
- HALT: CPU will halt in console I/O mode after power-up or RESET.
- RESTART: On power-up or RESET will attempt to restart VMS, if fails will HALT.

BOOT DEVICE SWITCH
- A - D: Will select one of four possible boot proms.

RESET
- (PUSHBUTTON) Initiates a power-up/down sequence to reset the CPU.
PROCESSOR MODULES

L0002 DATA PATHS MODULE - DPM

Arithmetic Logic
Rotator Logic
Scratch Pad Register and Control
Main Microsequencer Logic

L0003 MEMORY INTERCONNECT MODULE - MIC

Address Logic
Translation Buffer
Cache Memory
Data Routing and Alignment

L0004 UNIBUS INTERFACE MODULE - UBI

Console TUE Interface
Console Terminal Interface
Interrupt Handling
CMI/UNIBUS Interface
T.O.Y. Clock
Power-up/down Sequencing

L0005 CPU CONTROL STORE MODULE - CCS

6KW PROM Control Store
CPU Clock Source Oscillators
Space for Systime PCS Update

L0008 PATCHABLE CONTROL STORE MODULE - PCS

6KW PROM Control Store
1KW RAM Control Store
CPU Clock Source Oscillators
PROCESSOR MODULES

L0011  COMET MEMORY CONTROLLER 256KB ARRAYS - CMC

Memory Controller for:

SYSTIME 256KB Arrays
M8728 256KB Arrays

L0011 (modified) - CMC 1MB ARRAYS

Memory Controller for:

Systime MK1 1MB Arrays
Systime MK2 1MB Arrays
NS753 Arrays

L0016  MEMORY CONTROLLER 256KB/1MB ARRAYS

Memory Controller for:

Systime 256KB Arrays
Systime MK1 1MB Arrays
Systime MK2 1MB Arrays
NS753 1MB Arrays
M8750 1MB Arrays
M8728 256KB Arrays

M9313  UNIBUS EXERCISER AND TERMINATOR - UET
TU58 CARTRIDGE

TU58 Drive Unit

TU58 Tape Cartridge

Drive Roller  Swing-out Headgate
Write Protect Tab

Tape  Elastomer Belt

SUPPLY HUB  TAKE UP HUB
TU58 Controller

- J4: Drive 1 (Option)
- J3: Drive 0
- J2: Signal
- Diagnostic LED
- J1: Power
- Normal Link Position
MACHINE CHECKS

A Machine Check is an exception that is reported when the CPU or external device detects a serious error. Examples of 8750 machine checks are:

a) Control store parity error
b) Bad instruction register decode address
c) Double bit memory error.
d) Bus error
e) Cache parity error
f) Translation buffer parity error.

A machine check occurring while VMS is running may cause a FATAL BUGCHECK, which shuts the system down in an orderly fashion. The console terminal will print information about the bugcheck, including a reason for the bugcheck.

If the reason is a machine check, the STACK contents part of the console print out can be decoded. The first entry on the stack must be 28 to be able to decode the correct information.

A machine check that does not cause a FATAL error will be logged in the error log.

The diagram over the page describes the information as it appears on the stack in the event of a fatal bugcheck.
MACHINE CHECK STACK LOGOUT

<table>
<thead>
<tr>
<th>STACK (SP)</th>
<th>LENGTH PARAMETER</th>
<th>MUST BE 28</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>Summary Parameter</td>
<td>1 = CS Parity Error</td>
</tr>
<tr>
<td>(SP)+4</td>
<td></td>
<td>2 = Memory, Bus, Cache, TB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6,7 = Bad or no IRD ROM Address</td>
</tr>
<tr>
<td>(SP)+8</td>
<td>Virtual Address</td>
<td>PC at time of error</td>
</tr>
<tr>
<td>(SP)+C</td>
<td>PC</td>
<td>PC at time of error</td>
</tr>
<tr>
<td>(SP)+10</td>
<td>MDR</td>
<td>Memory Data Register</td>
</tr>
<tr>
<td>(SP)+14</td>
<td>Mode (Part of IPR 17)</td>
<td>0=modify</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1=read</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1=physical</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2=kernel</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3=exec</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0=virtual</td>
</tr>
<tr>
<td>(SP)+18</td>
<td>Read Lock Timeout</td>
<td>1 = Read Locked Timeout</td>
</tr>
<tr>
<td></td>
<td>or Write Vector Occurred</td>
<td>0</td>
</tr>
<tr>
<td>(SP)+1C</td>
<td>Translation Buffer Error (IPR 24)</td>
<td>GROUP 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GROUP 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GROUP 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GROUP 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TAG</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PARITY ERROR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DATA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PARITY ERROR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LOST ERROR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CACHE HIT</td>
</tr>
<tr>
<td>(SP)+20</td>
<td>Cache Register (IPR 27)</td>
<td>TAG</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PARITY ERROR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DATA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PARITY ERROR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LOST ERROR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CACHE HIT</td>
</tr>
<tr>
<td>(SP)+24</td>
<td>Bus Error Register (Part of IPR 17)</td>
<td>MEMORY</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ERROR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UNCORRECTABLE (DOUBLE) (BIT) ERROR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LOST ERROR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CORRECTABLE (SINGLE) (BIT) ERROR</td>
</tr>
<tr>
<td>(SP)+28</td>
<td>Machine Check Error Summary (IPR 26)</td>
<td>BUS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ERROR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(SEE BUS ERROR REG.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TRANSLATION BUFFER PARITY ERROR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LAST READ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = OPERAND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = XB</td>
</tr>
<tr>
<td>(SP)+2C</td>
<td>PC at Start of Instruction</td>
<td>0</td>
</tr>
<tr>
<td>(SP)+30</td>
<td>Start of Instruction</td>
<td>1</td>
</tr>
</tbody>
</table>

1-23
PERIPHERAL OPTIONS

The 8750 may utilise any of the following controllers and peripherals.

Terminal Controllers

SZ11 or DZ11 8 Line Terminal Multiplexor
CS11/U2 DH11/DM11 Emulator
CS11/F1 DMP32 Emulator
CS21 DMP32 Emulator

Magtape Controllers

SE LABS TU10 Emulator
8800
TC12 TS11 Emulator
TC13 TS11 Emulator
DU132 TS11 Emulator

Disk Controllers

SC21/V1 RH11 Emulator (Unibus)
SC31/BX RH11 Emulator (Unibus)
SI9400 RH11 Emulator (Unibus)
SC750 RH750 Massbus Emulator

Other

DMC11 High Speed Interprocessor Link
DMR11 High Speed Interprocessor Link
LP11 Parallel Printer Interface
SYSTEM REVISION LEVELS

The current hardware revision level is:

REV: 7

The module revisions are:

L0003 - REV J
L0004 - REV M
PCS - L0008
      - MODIFIED L0005

To perform a check on the hardware revision level:

Examine the system ID register:

>>> E/I 3E <cr>
>>> I 000003E 02005EXX

XX = Hardware Revision Level

NOTE This is only true for systems using the SID switch module
2 - HARDWARE LOCATION
EXTERNAL COVER REMOVAL

Access to the CPU and Unibus modules and backplanes is through the front and rear doors of the CPU cabinet. The doors are opened by releasing the keylock on both the front and rear door.

There is a metal cover over the module and the backplane access, both are removed in the same way, unscrewing the four retaining screws and lifting the covers off. Take care not to drop any screws. For this reason it is best done with the power switched OFF.
MAJOR ASSEMBLIES

DEC CAB

TU58 CONTROLLER

S.I.9400 DISK CONTROLLER

Power Supplies at Rear

SYSTIME CAB

TU58 CONTROLLER AT THIS SIDE

TU58 DRIVE

Power Supply Tray at Rear
<table>
<thead>
<tr>
<th>Processor Backplane 1</th>
<th>BACKPLANE SLOT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Processor</td>
</tr>
<tr>
<td>1</td>
<td>UNIBUS</td>
</tr>
<tr>
<td></td>
<td>QUAD SPC</td>
</tr>
<tr>
<td>2</td>
<td>HEX SPC</td>
</tr>
<tr>
<td>3</td>
<td>HEX SPC</td>
</tr>
<tr>
<td>4</td>
<td>HEX SPC</td>
</tr>
<tr>
<td>5</td>
<td>HEX SPC</td>
</tr>
<tr>
<td>6</td>
<td>HEX SPC</td>
</tr>
<tr>
<td>7</td>
<td>HEX SPC</td>
</tr>
<tr>
<td>8</td>
<td>HEX SPC</td>
</tr>
<tr>
<td>9</td>
<td>HEX SPC</td>
</tr>
<tr>
<td></td>
<td>M9313</td>
</tr>
<tr>
<td></td>
<td>QUAD SPC</td>
</tr>
</tbody>
</table>

### Module Location

<table>
<thead>
<tr>
<th>Processor</th>
<th>Backplane 1</th>
<th>BACKPLANE SLOT</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>L0001 FPA</td>
<td></td>
<td>Floating Point Accelerator Option</td>
</tr>
<tr>
<td>3</td>
<td>L0002 DPM</td>
<td></td>
<td>Remote Diagnostic Module Option</td>
</tr>
<tr>
<td>4</td>
<td>L0003 MIC</td>
<td></td>
<td>Option (One L0010 may be placed in slot 7, 8 or 9).</td>
</tr>
<tr>
<td>5</td>
<td>L0004 UBI</td>
<td></td>
<td>Option Memory Controller and Boot ROM's</td>
</tr>
<tr>
<td>6</td>
<td>L0005/L0008 CCS</td>
<td></td>
<td>The memory slots 12 to 18 are for additional memory arrays</td>
</tr>
<tr>
<td>7</td>
<td>L0006 RDM</td>
<td></td>
<td>Bus Jumper/Reserved</td>
</tr>
<tr>
<td>8</td>
<td>SC750</td>
<td></td>
<td>Bus Jumper/Any Quad SPC</td>
</tr>
<tr>
<td>9</td>
<td>SC750</td>
<td></td>
<td>Any Hex SPC (SZ11 etc)</td>
</tr>
<tr>
<td>10</td>
<td>L0011/L0016 CMC</td>
<td></td>
<td>As for slot 3</td>
</tr>
<tr>
<td>11</td>
<td>MEMORY 1MB</td>
<td></td>
<td>As for slot 3</td>
</tr>
<tr>
<td>12</td>
<td>MEMORY</td>
<td></td>
<td>As for slot 3</td>
</tr>
<tr>
<td>13</td>
<td>MEMORY</td>
<td></td>
<td>As for slot 3</td>
</tr>
<tr>
<td>14</td>
<td>MEMORY</td>
<td></td>
<td>As for slot 3</td>
</tr>
<tr>
<td>15</td>
<td>MEMORY</td>
<td></td>
<td>As for slot 3</td>
</tr>
<tr>
<td>16</td>
<td>MEMORY</td>
<td></td>
<td>As for slot 3</td>
</tr>
<tr>
<td>17</td>
<td>MEMORY</td>
<td></td>
<td>As for slot 3</td>
</tr>
<tr>
<td>18</td>
<td>MEMORY</td>
<td></td>
<td>Terminator/Any Quad SPC</td>
</tr>
</tbody>
</table>
LO011 BOOTSTRAP ROM LOCATIONS

RED LED

GREEN LED

D C B A
1MB SYSTIME MEMORY AND ERROR-LOGGING

The V.M.S. error-log decodes the array of Systime 1Mb arrays wrongly giving very large numbers for the array number.

The correct array number can be identified using CSR0 bits as follows as given by the error-log printout.

BIT 18
BIT 19 used to select ROMS 0-3

BIT 20
BIT 21
BIT 22 used to select ARRAYS 0-7
11/750 OPTIONS

L0001 FLOATING POINT ACCELERATOR - FPA
This is installed in slot 1 of the CPU Backplane.

L0006 DIAGNOSTIC MODULE - RDM
This is installed in slot 6 of the CPU Backplane. It is for engineering use only and is not normally installed in the field.

L0010 SECOND UNIBUS INTERFACE - SUB
This is installed in slot 7, 8 or 9 depending on what other options are also using these slots.

WCS WRITEABLE CONTROL STORE
This option is not normally used and it depends on the module type of CCS being used.

MEMORY BATTERY BACK-UP

H7112 For systems using DEC PSU's only.

SYSTIME For systems with Farnell PSU's.
3 - SWITCH AND LINK SETTINGS
SYSTIME 256KB MEMORY ARRAY LINKS

The SYSTIME 6700 memory board blank PCB can be filled with either 16K memory chips (256KB board) or 64K memory chips (1MB board). In each case the link settings on the board are different.

The 256KB board is normally used with a standard L0011 memory controller although it will work on the L0016. In both cases the links on the board are as follows:

256KB Array on the Standard L0011:

Links IN:

1, 2, 4, 6, 7, 9, 10, 12, 13, 14, 16, 18, 20, 22, 23, 25, 26, 28, 29.

Links OUT:

3, 5, 8, 11, 15, 17, 19, 21, 24, 27.
MK1 MEMORY ARRAY LINKS

This is the Systime 1MB version of the 6700 memory array. It may be used with the modified L0011 or the L0016 memory controller. Using the following link settings a single link (WL), has to be modified depending on the controller.

<table>
<thead>
<tr>
<th>LINK</th>
<th>Modified L0011</th>
<th>L0016</th>
</tr>
</thead>
<tbody>
<tr>
<td>WL</td>
<td>IN</td>
<td>OUT</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>LINK</th>
<th>Modified L0011 or L0016</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>IN</td>
</tr>
<tr>
<td>3</td>
<td>IN*</td>
</tr>
<tr>
<td>4</td>
<td>OUT</td>
</tr>
<tr>
<td>5</td>
<td>IN</td>
</tr>
<tr>
<td>6</td>
<td>OUT</td>
</tr>
<tr>
<td>7</td>
<td>IN</td>
</tr>
<tr>
<td>8</td>
<td>IN</td>
</tr>
<tr>
<td>9</td>
<td>OUT</td>
</tr>
<tr>
<td>10</td>
<td>OUT</td>
</tr>
<tr>
<td>11</td>
<td>IN</td>
</tr>
<tr>
<td>12</td>
<td>OUT</td>
</tr>
<tr>
<td>13</td>
<td>IN</td>
</tr>
<tr>
<td>14</td>
<td>IN</td>
</tr>
<tr>
<td>15</td>
<td>IN</td>
</tr>
</tbody>
</table>

* No battery back-up.
See page 2.B-1 for using battery back-up.
M8750 MEMORY ARRAY LINKS

Shaded links should be fitted when installed on L0011

a) Using the M8750 array on the modified L0011 is not recommended, as the L0011 will require further modification.

b) The links that should be IN when using the M8750 array on the L0016 are:

w2, 3, 4, 6, 8, 10, 12, 13, 15, 16, 18, 19, 20, 22, 25.
NS753 MEMORY ARRAY LINKS

NORMAL LINK SETTINGS

W3 - OUT
W4 - OUT
W7 - OUT
W8 - IN
W9 - IN
W10 - OUT (IN WITH MODIFIED L0011)*
W11 - OUT
W12 - OUT
W13 - OUT

* To use the NS753 on the modified L0011 requires an ECO to be fitted to the L0011 module. This is detailed on page 2.B-2.
SYSTIME MK2, MEMORY ARRAY LINKS

NORMAL LINK SETTINGS

LK3 - IN FOR MODIFIED L0011
     - OUT FOR L0016

LK7 - OUT FOR MEMORY BATTERY BACK-UP

LK1 (Normally both IN)
SID REGISTER SWITCH

For example, to set the SID switch pack for a hardware revision level of 70 (HEX) is as follows:

SYS ID <7> <6> <5> <4> <3> <2> <1> <0>
SWITCH ON OFF OFF OFF OFF ON ON ON ON

NOTE

Use the System ID Register bit positions etched on the board to set the switches. Ignore the numbers stamped on the switch pack.

Install the Backplane Connector Housing in slot 4 so that the blind holes at each end of the connector cover SLOT 4 pins B17 and B18 on the top, and SLOT 4 pins B59 and B60 on the bottom.
4 - SET-UP PROCEDURES
SET-UP PROCEDURES

Note

There are no adjustments on any of the CPU modules. The power supplies are adjustable on systems using the Farnell PSU's. This is detailed on page 2.5-5.
5 - POWER SUPPLY
DEC PSU COMPONENTS

875 SINGLE PHASE POWER CONTROLLER

H7104C  +2.5v 85A POWER SUPPLY
+12v Plug-in Regulator 10a  H7102
+ and - 5v Plug-in Regulator  H7106
2.5v Control Board

H7104D  +5V 135A POWER SUPPLY
+ and - 15V Plug-in Regulator  H7105
H7104 Bias Control Card

NOTE:
The plug-in regulators are dedicated to each power supply.
## DEC PSU FAULT ISOLATION GUIDE

<table>
<thead>
<tr>
<th>CONTROL PANEL</th>
<th>POWER CONTROLLER</th>
<th>POSSIBLE FAULT AREA(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Five Position Keyswitch</td>
<td>Power</td>
<td>Circuit Breaker</td>
</tr>
<tr>
<td>CPU State/Power</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>ON</td>
<td>OFF</td>
</tr>
</tbody>
</table>

+ Set at any position other than off.
X Don’t care condition
++ REM = Remote position
FARNELL PSU

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Qty</th>
<th>Pt. No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>G15-45 (+15,-15)</td>
<td>2</td>
<td>0510590</td>
</tr>
<tr>
<td>G6-1P</td>
<td>1</td>
<td>0510592</td>
</tr>
<tr>
<td>G12-20</td>
<td>1</td>
<td>0510951</td>
</tr>
<tr>
<td>GS-120(ALCO,+5)</td>
<td>1</td>
<td>0510589</td>
</tr>
<tr>
<td>GS-120(Modified to +2.5)</td>
<td>1</td>
<td>0510588</td>
</tr>
<tr>
<td>D.C. Monitor PCB</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Full P.S.U. Kit</td>
<td></td>
<td>0100376</td>
</tr>
</tbody>
</table>

POWER SUPPLY TRAY

![Diagram of power supply tray]

NOTE: The 2.5V supply is a modified 5V supply.
FARNELL PSU ADJUSTMENTS

DC Low boards as supplied by Farnell should already be set up for our requirements. If this is not true then the adjustments can be made as follows:

1. All supply voltages must be set as accurately as possible +2.5V, +5V, -5V, +15V and +12V. The Farnell 'DC Low' boards are set to detect voltage variations of 5% i.e. if +5V drops to 4.75V then DCLO is asserted on the Unibus.

2. Once the voltages are set up correctly (all PSU's are adjustable) the board should work. If ACLO or DCLO do not work correctly (i.e. either signal is a logic '0' - causing the CPU to halt), then there are one or two things to look at.

A brief explanation of the operation of these boards follows:
'DC Low' board 2 (Farnell board with two IC's on it) monitors -5V, -15V, +15V and +12V on pins 1, 2, 3 and 4 respectively. If these voltage rails are correct then pin 7 should be a logic high. This logic high is passed to 'DC Low' board 1. If this signal is not high then either the voltage levels at the board are incorrect, or the threshold level on the board needs altering. This is achieved by moving the potentiometer on the board. Turn this pot. Until pin 7 goes 'high' - if it does not then the board is duff.

'DC Low' board 1 monitors the +5V and +2.5V. Assuming these are correct (and the DC OK signal from board 2 pin 7 is high), then pin 7 on this board should be high. Again if this signal is not high then either the DC voltage levels are incorrect or the potentiometer needs adjusting.

Before rejecting the unit it is advisable to adjust this pot. Until pin 7 goes high. Once this signal is high the ACLO/DCLO sequence is generated from the mother board.

Monitoring the pins in connector P1 will determine whether these signals are generated correctly.

NB: ACLO and DCLO are open collector outputs so they must be connected to the CPU in order to work correctly.

Lastly if the ACLO signal is high yet the DCLO signal is low then there exists an error on the mother board. A recent ECO was issued to cure this problem, and this should be checked. A 560pF capacitor should be soldered between pin 11 and 12 on E2.

If these adjustments still fail then request replacement.
AC/DC LOW BOARD

VIEW A

VIEW B

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>FROM</th>
<th>TO</th>
<th>COLOUR</th>
</tr>
</thead>
<tbody>
<tr>
<td>ITEM 1</td>
<td>GND</td>
<td>GND [PAD]</td>
<td>DC1 6</td>
</tr>
<tr>
<td>ITEM 2</td>
<td>GND</td>
<td>DC1 6</td>
<td>DC2 6</td>
</tr>
<tr>
<td>ITEM 3</td>
<td>GND</td>
<td>DC2 6</td>
<td>P1 9</td>
</tr>
<tr>
<td>ITEM 4</td>
<td>DC LOW</td>
<td>DC1 7</td>
<td>DC LOW [PAD]</td>
</tr>
<tr>
<td>ITEM 5</td>
<td>DC LOW</td>
<td>DC LOW [PAD]</td>
<td>P1 3</td>
</tr>
<tr>
<td>ITEM 6</td>
<td>5v</td>
<td>P1 3</td>
<td>DC1 5</td>
</tr>
<tr>
<td>ITEM 7</td>
<td>5v</td>
<td>DC1 5</td>
<td>DC2 5</td>
</tr>
<tr>
<td>ITEM 8</td>
<td>5v</td>
<td>DC2 5</td>
<td>5v [PAD]</td>
</tr>
<tr>
<td>ITEM 9</td>
<td></td>
<td>DC1 4</td>
<td>DC2 7</td>
</tr>
<tr>
<td>ITEM 10</td>
<td>2.5v MONITOR</td>
<td>DC1-3</td>
<td>P1 5</td>
</tr>
<tr>
<td>ITEM 11</td>
<td>AC LOW</td>
<td>AC LOW [PAD]</td>
<td>P1 6</td>
</tr>
<tr>
<td>ITEM 12</td>
<td>+12v MONITOR</td>
<td>DC2 4</td>
<td>P1 11</td>
</tr>
<tr>
<td>ITEM 13</td>
<td>+5v MONITOR</td>
<td>DC2 3</td>
<td>P1 2</td>
</tr>
<tr>
<td>ITEM 14</td>
<td>+5v MONITOR</td>
<td>DC2 2</td>
<td>P1 13</td>
</tr>
<tr>
<td>ITEM 15</td>
<td>+5v MONITOR</td>
<td>DC2 1</td>
<td>P1 14</td>
</tr>
</tbody>
</table>
8750 BATTERY BACK-UP UNIT

MAINS OK-LED
BATTERY IN-LED
BATTERY ON-SWITCH
FUSE

DC CONNECTOR

MAINS PLUG

PSU ADJUSTMENT COVER
6 - POWER-UP ACTIONS AND RESPONSE
POWER-UP ACTIONS

The CPU will automatically enter the console I/O mode from power-up without the use of the console storage device.

The front panel switches are tested on power-up and will normally be set to boot VMS which again does not require the console storage device.

To override the switches place the power-up action switch into the halt position before powering on the CPU. The console will respond as shown on page 2.6-2, and await further commands.
TYPICAL RESPONSE

NORMAL POWER-UP

00000000 16

This is with Power-up Action Switch at HALT position.
7 - CONSOLE COMMANDS
COMMAND SUMMARY

^P  Enter Console I/O Mode

^U  Ignore current line

H  HALT, reset console defaults

E[/qualifier][address]  EXAMINE

D[/qualifier][address][data]  DEPOSIT

I  INITIALISE CPU and Unibus.

T  TEST the CPU by running Microverify.

S[address]  START Program (at address if specified).

C  CONTINUE program at address in PC.

B  BOOT (see page 2.8-1)

N  NEXT, executes one instruction

EXAMINE AND DEPOSIT QUALIFIERS

Data Type
/B  Byte
/W  Word
/L  Longword

Address Type
/G  GPR 0 to F
/I  IPR
/P  Physical Memory
/V  Virtual Memory

SYMBOLIC ADDRESSES

P  Processor Status Longword
*  Last Address
+  Next Address
CONSOLE HALT ERROR CODES

Example

00010003 06

>>>  

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>Execute TEST console</td>
</tr>
<tr>
<td>02</td>
<td>CTRL/P halt or single macro instruction mode</td>
</tr>
<tr>
<td>04</td>
<td>Interrupt stack not valid</td>
</tr>
<tr>
<td>05</td>
<td>Double bus error halt</td>
</tr>
<tr>
<td>06</td>
<td>Halt instruction executed</td>
</tr>
<tr>
<td>07</td>
<td>Vector bits&lt;1:0&gt;=3, halt at vector</td>
</tr>
<tr>
<td>08</td>
<td>Vector bits&lt;1:0&gt;=2, WCS disabled or not present</td>
</tr>
<tr>
<td>0A</td>
<td>Change mode instruction executed on interrupt stack</td>
</tr>
<tr>
<td>0B</td>
<td>Change mode instruction executed and vector&lt;1:0&gt;not=0</td>
</tr>
<tr>
<td>11</td>
<td>Power up and can't find RPB, action switch at RESTART/HALT</td>
</tr>
<tr>
<td>12</td>
<td>Power up and warm start flag false, action switch at RESTART/HALT position</td>
</tr>
<tr>
<td>13</td>
<td>Power up and can't find good 64K of memory</td>
</tr>
<tr>
<td>14</td>
<td>Power up and booting, but bad or no Boot ROM</td>
</tr>
<tr>
<td>15</td>
<td>Power up and cold start flag set during boot subroutine</td>
</tr>
<tr>
<td>16</td>
<td>Power up halt, with action switch at HALT position</td>
</tr>
<tr>
<td>FF</td>
<td>Microverify test failure</td>
</tr>
</tbody>
</table>
CONSOLE COMMAND ERROR CODES

Example

?11

>>>  

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>Deposit or Examine of memory failed. (This could mean one of the following has occurred: access violation; translation not valid; bus error; TB parity error; control store parity error.)</td>
</tr>
<tr>
<td>11</td>
<td>Illegal access of an IPR</td>
</tr>
<tr>
<td>30</td>
<td>APT loading checksum error</td>
</tr>
<tr>
<td>33</td>
<td>Attempt to boot from unknown device type (DM, DL, DT, DR)</td>
</tr>
<tr>
<td>34</td>
<td>Boot device controller not A, B, C, or D.</td>
</tr>
</tbody>
</table>
BOOT58 COMMANDS

BOOT [<DEVSPEC>]

Boot from the device specified. If no device is specified, boot from the default boot device. This command cannot be used within an indirect command file.

DEPOSIT/<QUALIFIER> <LOCATION> <VALUE>

Deposit <VALUE> at the location specified by <LOCATION>. The <LOCATION> is interpreted according to <QUALIFIER>.

EXAMINE/<QUALIFIER> <LOCATION>

Display the contents of <LOCATION>, where <LOCATION> is interpreted according to <QUALIFIER>.

HELP

Print this text at the console. This command cannot be used within an indirect command file.

LOAD <FILESPEC>[/START:<VALUE>]

Load a file from the boot device into memory starting at the address specified <VALUE>. If no starting location is specified, load the file beginning at the first free location in memory.

START <VALUE>

Initialise CPU and Jump to <VALUE>.

@ <FILESPEC>

Execute command procedure from tape.

NOTE

You can abbreviate all BOOT58 commands to the first character
BOOT58 Command Parameters

<location>  <value>!<register>
<value>    <number>!<shorthand>
<number>   Any nonnegative hexadecimal number
<register> 0..F! PSL
<shorthand> Any one of the following:
              * = use last <location> specified
              + = use (last<location>)+1
              - = use (last<location>)-1
              0 = use contents of (last<location>)
<qualifier> Any one of the following:
              P = physical memory address
              G = general register
              I = internal processor register
              W = word, 16 bits
              L = longword, 32 bits
<devspec>   A device spec of the form: DDCU, where
              DD = generic device type (e.g. DB)
              C = controller designator (A ! B)
              U = unit number (0..9)
<filespec>  A legal RT-11 filename of the form: name.typ
              where:
              name = any alphanumeric string of not
                     more than 6 characters.
              typ = any alphanumeric string of not
                    more than 3 characters. A null
                    typ is acceptable.
8 - BOOTSTRAP
BOOTSTRAP PROCEDURES

USING OPERATOR CONTROL PANEL SWITCHES

a) Select the device to boot using the BOOT DEVICE switch. The positions correspond to the following devices:
   
   A = TU58
   B = System Disk
   C = Spare
   D = Spare

b) Place the power on action switch in the BOOT position.

c) Ready the disk drive to be booted.

d) Power the system on, or if already on press the RESET button.

USING CONSOLE COMMANDS

a) Place the power on action switch in the HALT position.

b) Power on, or press the RESET switch, if the system is not in the console I/O mode. In console I/O mode the console prints >>>.

c) Enter the BOOT command as shown below:

   B<cr>       This boots the device selected by the BOOT DEVICE SWITCH.

   or:

   B_[dev]<cr> This boots the device whose code is specified.

The boot device codes are as follows:

   DDA0 = TU58
   S1An = Disks on SI 9400 Controller
   UMA0 = Disks on Emulex SC21/31 Controller
   DBAn = Disks on Emulex SC750 Controller

   n = Logical unit number of the drive.
CONVERSATIONAL BOOT

B/l_{dev}<cr>

or:

B/l<cr> (using the boot device switch)

DIAGNOSTIC BOOT

To boot diagnostic supervisor from a VMS disk:

B/10 {dev}<cr>

BOOTSTRAP ROMS

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>PART NO</th>
<th>ASCII CODE</th>
<th>DEVICE CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TU58</td>
<td>905A9</td>
<td>44 44</td>
<td>DD</td>
</tr>
<tr>
<td>DISKS ON</td>
<td>287B</td>
<td>4D 55</td>
<td>UM</td>
</tr>
<tr>
<td>SC21/31</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DISKS ON</td>
<td>8919B</td>
<td>49 53</td>
<td>SI</td>
</tr>
<tr>
<td>UNIBUS S.I. 9400</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DISKS ON</td>
<td>497B</td>
<td>42 44</td>
<td>DB</td>
</tr>
<tr>
<td>SC750</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
BOOTSTRAP EXAMPLE

%%
00000000 16
>>>B DBA0
%%

VAX/VMS Version V4.1 26-APR-1985 16:21

%OPCOM 6-MAR-1985 11:58:05.44, Logfile initialised by operator OPA0:
Logfile is SYS$MANAGER:OPERATOR.LOG

%PURGE-I-NOPILPURG, no files purged for SYS$SYSROOT:([SYSERR]*.*):

Login Quotas - Interactive Limit = 64, current interactive value = 0

SYSTEM Job terminated at 6-MAY-1985 11:59:09.23
9 - DIAGNOSTIC TESTING
MICROVERIFY

Microverify is a microcode based set of test routines which execute a basic sanity check on the DPM and MIC modules of the '750.

The routine uses a "%" character to indicate start of run and end of successful run.

If the microverify sequence fails, an error indication is provided, by printing a character indicating the failing test group. The value printed for the PC indicates the failing test within the identified group.

The example below shows the console response on a Microverify failure.

%F
00000062 FF.

This indicates a microverify failure on the "MTEMP EXPLICIT ADDRESS TEST".

The test is indicated by printed PC+2.

Microverify is invoked on:

Power up, prior to boot sequence execution and by a specific console I/O command.
### MICROVERIFY CODES

<table>
<thead>
<tr>
<th>Code</th>
<th>PC+2</th>
<th>Test Name/Error Message</th>
</tr>
</thead>
<tbody>
<tr>
<td>'g'</td>
<td>000</td>
<td>BAD BIT IN DREG OR SUPPORT</td>
</tr>
<tr>
<td></td>
<td>001</td>
<td>BAD BIT IN RBUS OR WBUS</td>
</tr>
<tr>
<td>'C'</td>
<td>031</td>
<td>BAD BIT IN QREG</td>
</tr>
<tr>
<td></td>
<td>033</td>
<td>BAD BIT IN MBUS</td>
</tr>
<tr>
<td>'E'</td>
<td>051</td>
<td>ERROR CLEARING RTEMP</td>
</tr>
<tr>
<td></td>
<td>052</td>
<td>ERROR FILLING RTEMP WITH ONES</td>
</tr>
<tr>
<td></td>
<td>054</td>
<td>ERROR CLEARING GPR</td>
</tr>
<tr>
<td></td>
<td>057</td>
<td>ERROR FILLING GPR WITH ONES</td>
</tr>
<tr>
<td></td>
<td>058</td>
<td>ERROR CLEARING IPR</td>
</tr>
<tr>
<td></td>
<td>05B</td>
<td>ERROR FILLING IPR WITH ONES</td>
</tr>
<tr>
<td></td>
<td>05D</td>
<td>ERROR CLEARING MTEMP</td>
</tr>
<tr>
<td></td>
<td>05E</td>
<td>ERROR FILLING MTEMP WITH ONES</td>
</tr>
<tr>
<td>'F'</td>
<td>061</td>
<td>MTEMP EXPLICIT ADDRESS TEST</td>
</tr>
<tr>
<td></td>
<td>062</td>
<td>ERROR ADDRESSING MTEMPO</td>
</tr>
<tr>
<td></td>
<td>064</td>
<td>ERROR ADDRESSING MTEMP1</td>
</tr>
<tr>
<td></td>
<td>067</td>
<td>ERROR ADDRESSING MTEMP4</td>
</tr>
<tr>
<td></td>
<td>068</td>
<td>ERROR ADDRESSING MTEMP8</td>
</tr>
<tr>
<td>'I'</td>
<td>091</td>
<td>RTEMP EXPLICIT ADDRESS TEST</td>
</tr>
<tr>
<td></td>
<td>092</td>
<td>ERROR ADDRESSING RTEMP0</td>
</tr>
<tr>
<td></td>
<td>094</td>
<td>ERROR ADDRESSING RTEMP1</td>
</tr>
<tr>
<td></td>
<td>097</td>
<td>ERROR ADDRESSING RTEMP4</td>
</tr>
<tr>
<td></td>
<td>098</td>
<td>ERROR ADDRESSING RTEMP8</td>
</tr>
<tr>
<td>'J'</td>
<td>0A1</td>
<td>IPR EXPLICIT ADDRESS TEST</td>
</tr>
<tr>
<td></td>
<td>0A2</td>
<td>ERROR ADDRESSING IPR0</td>
</tr>
<tr>
<td></td>
<td>0A4</td>
<td>ERROR ADDRESSING IPR1</td>
</tr>
<tr>
<td></td>
<td>0A7</td>
<td>ERROR ADDRESSING IPR2</td>
</tr>
<tr>
<td></td>
<td>0A8</td>
<td>ERROR ADDRESSING IPR8</td>
</tr>
<tr>
<td>'L'</td>
<td>0C1</td>
<td>GPR EXPLICIT ADDRESS TEST</td>
</tr>
<tr>
<td></td>
<td>0C2</td>
<td>ERROR ADDRESSING R0</td>
</tr>
<tr>
<td></td>
<td>0C4</td>
<td>ERROR ADDRESSING R2</td>
</tr>
<tr>
<td></td>
<td>0C7</td>
<td>ERROR ADDRESSING R4</td>
</tr>
<tr>
<td></td>
<td>0C8</td>
<td>ERROR ADDRESSING R8</td>
</tr>
<tr>
<td></td>
<td>0CE</td>
<td>ERROR ADDRESSING DUAL PORT</td>
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</table>
### MICROVERIFY CODES (Cont)

<table>
<thead>
<tr>
<th>Code</th>
<th>PC+2</th>
<th>Test Name/Error Message</th>
</tr>
</thead>
<tbody>
<tr>
<td>'O'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0F1</td>
<td></td>
<td>ERROR IN XB&lt;31:0&gt;</td>
</tr>
<tr>
<td>0F2</td>
<td></td>
<td>ERROR IN XB&lt;63:32&gt;</td>
</tr>
<tr>
<td>0F4</td>
<td></td>
<td>ERROR IN IR</td>
</tr>
<tr>
<td>0F7</td>
<td></td>
<td>ERROR IN OSR</td>
</tr>
<tr>
<td>'Q'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>111</td>
<td></td>
<td>SOURCE XB PC INCREMENT TEST</td>
</tr>
<tr>
<td>112</td>
<td></td>
<td>ERROR SOURCING ONE BYTE FROM XB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>XB OR INCREMENTING PC BY 1</td>
</tr>
<tr>
<td>114</td>
<td></td>
<td>ERROR SOURCING AN UNALIGNED</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LONGWORD OR INC PC BY 2</td>
</tr>
<tr>
<td>117</td>
<td></td>
<td>ERROR INCREMENTING PC BY 4</td>
</tr>
<tr>
<td>'R'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>121</td>
<td></td>
<td>ERROR READING DSIZE ROM OPERAND 1</td>
</tr>
<tr>
<td>122</td>
<td></td>
<td>ERROR LOADING/READING RNUM</td>
</tr>
<tr>
<td>124</td>
<td></td>
<td>ERROR READING SIZE ROM OPERAND 2</td>
</tr>
<tr>
<td>127</td>
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<td>ERROR LOADING/READING RNUM</td>
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<tr>
<td>128</td>
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<td>ERROR READING DSIZE ROM OPERAND 3</td>
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<tr>
<td>12B</td>
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<td>ERROR LOADING/READING RNUM</td>
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<td>12D</td>
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<td>ERROR READING DSIZE ROM OPERAND 4</td>
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<tr>
<td>12E</td>
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<td>ERROR LOADING/READING RNUM</td>
</tr>
<tr>
<td>'T'</td>
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<td></td>
</tr>
<tr>
<td>141</td>
<td></td>
<td>ERROR READING DSIZE ROM OPERAND 5</td>
</tr>
<tr>
<td>142</td>
<td></td>
<td>ERROR LOADING/READING RNUM</td>
</tr>
<tr>
<td>144</td>
<td></td>
<td>ERROR READING DSIZE ROM OPERAND 6</td>
</tr>
<tr>
<td>'X'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>181</td>
<td></td>
<td>CACHE PARITY ERROR TEST</td>
</tr>
<tr>
<td>182</td>
<td></td>
<td>FAILED TO GET CACHE PARITY ERROR</td>
</tr>
<tr>
<td>184</td>
<td></td>
<td>BAD MACHINE CHECK ERROR SUMMARY REGISTER</td>
</tr>
<tr>
<td>']'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1B1</td>
<td></td>
<td>TB PARITY ERROR TEST</td>
</tr>
<tr>
<td>1B2</td>
<td></td>
<td>FAILED TO GET GROUP 0 TB PARITY ERROR</td>
</tr>
<tr>
<td>1B4</td>
<td></td>
<td>BAD TB GROUP PARITY ERROR REGISTER</td>
</tr>
<tr>
<td>1B7</td>
<td></td>
<td>BAD MACHINE CHECK ERROR SUMMARY REGISTER</td>
</tr>
<tr>
<td>1B8</td>
<td></td>
<td>FAILED TO GET GROUP 1 TB PARITY ERROR</td>
</tr>
<tr>
<td>1BB</td>
<td></td>
<td>BAD MACHINE CHECK ERROR SUMMARY REGISTER</td>
</tr>
<tr>
<td>']'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1D1</td>
<td></td>
<td>CONTROL STORE PARITY ERROR TEST</td>
</tr>
<tr>
<td>1D2</td>
<td></td>
<td>FAILED TO GET CONTROL STORE PARITY ERROR</td>
</tr>
<tr>
<td>1E1</td>
<td></td>
<td>ERROR IN CONTROL STORE PARITY ERROR</td>
</tr>
<tr>
<td>1E2</td>
<td></td>
<td>CACHE TEST</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ERROR FILLING CACHE WITH ONES LOCATION</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NOT INITIALLY = 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ERROR FILLING CACHE WITH ONES</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UNABLE TO WRITE ONES</td>
</tr>
</tbody>
</table>
MACRODIAGNOSTIC COMMAND SUMMARY

SET LOAD

This establishes the device from which diagnostics are to be loaded.

SET LOAD CSA0:

This will change the default load device from disk to TU58 on the 8750.

SHOW LOAD

This command displays the current load device and directory from which diagnostics will be loaded using the LOAD command.

LOAD

This command loads programmes from the current load device into memory.

For example: LOAD EVTAA<cr>.

ATTACH

This makes known to diagnostic supervisor the devices that are to be currently tested.

For example: DS>ATT DW750 CMI DWO.

SELECT

After specifying the testable hardware, the ones to be tested at the present time must be selected eg:

    DS> ATT TS04 DWO MSAO
    DS> ATT RM05 RHO DRAO
    DS> SELECT DRAO (alternatively SELECT ALL)

DESELECT

Used to make all or some devices unavailable to testing.
START

Used after LOAD command to initiate program; other options are:

DS>START/SECTION:

DS>START/SECTION: XXXX/TEST:6:12 (starts program execution in section XXXX of the diagnostic and performs tests 6 to 12 within that section)

DS>START/TEST:10 (start program execution at test 10 and continues to end of tests)

DS>START/TEST:5/SUBTEST:6 (starts execution at test 5 and runs subtests 1, 2, 3, 4, 5, 6.)

DS>START/PASS:0 (execute program indefinitely)

RUN

Loads and starts the program.

SET DEFAULT

Sets data length or radix(byte/word/longword, hex/decimal).

SET FLAGS/CLEAR FLAGS

Certain programs use flags to control program flow, error logging etc. The help section of the diagnostics usually list the flags that can be set. Certain flags are always available as follows:

IE1 Inhibit error messages at level 1 (inhibits all error messages except those forced by program)

IE2 Inhibit error messages at level 2 (prints header only)

IE3 Inhibit error messages at level 3 (header and basic information only printed)

IES Inhibit summary report.

QUICK Quick verify test (depends on program)

TRACE Reports execution of each test.
OPER Indicates that operator is present, if not set the supervisor ensures that program is completed without intervention.

PROMPT Display long dialogue, shows limits and faults etc.

ALL Set all flags in this list.

SET/CLEAR event flags (depends on program running but controls program flow).

SUMMARY

Invokes the program's summary report code section which prints statistical reports.

ABORT

Passes control to the clean up code, then returns control to DS> which then enters a wait state. The operator may then enter any command except CONTINUE.

SHOW EVENT FLAGS

Shows event flags currently set.

    DS>SHOW EVENT FLAGS
    EVENT FLAGS SET: 15, 9, 1
LOADING DIANOSTIC SUPERVISOR

STAND ALONE FROM TU58 CARTRIDGES

a) Power-on the system with the power-on action in the HALT position.

b) Insert the TU58 containing ECSAA.EXE, (refer to following lists to locate the correct cartridge).

c) Type:

   B DDA0

   This will load and run diagnostic supervisor, which takes approximately 3 minutes.

STAND ALONE FROM VMS DISK

Currently this only works on SC750 Disks.

a) Ready VMS Disk for use, write protect drive as an extra precaution.

b) Type:

   B/10 DBA\text{n} \quad (n \text{ is the unit number})

UNDER VMS

a) Bring up VMS as normal.

b) Log into the Field Service account, type:

   \text{FIELD SERVICE}

   Type:

   \text{RUN ECSAA}
DIAGNOSTIC DISTRIBUTION

There are currently two revisions of diagnostic cartridge distributions for the 8750 system, revision A and revision B. Revision B was introduced in January 1984.

REVISION A CARTRIDGES

TU58 5  - CACHE, TB, MEMORY
ECKAL  - CACHE/TB DIAGNOSTIC
ECKAM  - MEMORY DIAGNOSTIC
ECKAX  - SPECIFIC CPU CLUSTER EXERCISER
TU58 6  - RH750, DW750
ECSAA  - DIAGNOSTIC SUPERVISOR
ECCAA  - RH750 DIAGNOSTIC(DEC ONLY)
ECCBA  - DW750 DIAGNOSTIC
EVDA  - SZ-11 8-LINE DIAGNOSTIC
TU58 7  - VAX 11 INSTRUCTION EXERCISER
EVKAB  - ARCHITECTURAL INSTRUCTION
EVKAC  - FLOATING POINT INSTRUCTION
EVKAD  - COMPATIBILITY MODE
EVKAE  - PRIVILEGED ARCHITECTURE INSTRUCTION
TU58 9  - CR/DISK USER MODE
EVAAA  - LINE PRINTER DIAGNOSTIC
EVABA  - CARD READER DIAGNOSTIC
EVRAA  - DISK AND TU58 RELIABILITY DIAGNOSTIC
EVRA  - VAX DISK FORMATTER
EVTAA  - LOCAL TERMINAL DIAGNOSTIC
EVTBA  - MULTI-TERMINAL DIAGNOSTIC

REVISION B CARTRIDGES

8750 TAPE 1

ECSAA.EXE  - DIAGNOSTIC SUPERVISOR
EVSAH.HLP  - HELP FILE FOR ABOVE

8750 TAPE 2

ECKIM.EXE  - MEMORY DIAGNOSTIC FOR 1MB SYSTEMS
ECKAL.EXE  - TRANSLATION BUFFER/CACHE TEST
ECKAM.EXE  - MEMORY DIAGNOSTIC FOR 1/4MB SYSTEMS
ECKAX.EXE  - CLUSTER EXERCISER
8750 TAPE 3

EVDBA.EXE - DMC11 DIAGNOSTIC REPAIR LEVEL
EVDBB.EXE - DMC11 EXERCISER DIAGNOSTIC
EVDMA.EXE - DMR11 DIAGNOSTIC REPAIR LEVEL
EVDXA.EXE - DMR11 COMM.MICRO CPU REPAIR LEVEL
EVKAA.EXE - HARDCORE INSTRUCTION EXERCISER

8750 TAPE 4

EVKAB.EXE - ARCHITECTURAL INSTRUCTION TEST
EVKAC.EXE - FLOATING POINT INSTRUCTION TEST
EVKAD.EXE - COMPATABILITY MODE TESTS
EVKAE.EXE - PRIVILEGED ARCHITECTURE INSTRUCTIONS

8750 TAPE 5

ECCBA.EXE - UNIBUS ADAPTER DIAGNOSTIC
ESTAAA.EXE - LOCAL TERMINAL DIAGNOSTIC
EVAAAX.EXE - LINE PRINTER DIAGNOSTIC
EVDAAX.EXE - DZ11 ASYNCHRONOUS MUX TESTS
EVMAAX.EXE - TB16/TU77/TS11 DIAGNOSTICS
EVQT5.EXE - OFFLINE DRIVE FOR TS11
EVTTAA.EXE - TU10 COMPATABLE TESTS(D/DATA, S/E LABS)

8750 TAPE 6 (EMULEX REV H DIAGNOSTICS)

ECS11.730
ECS11.750
ECS11.780
ECS21.730
ECS21.750
ECS21.780
ECS21.790
ECS21.750
ECS21.780
ECS21.780
ECS21.EXE - ATTACH COMMAND FILES
ECS21.780
ESC21.730
ESC21.750
ESC21.780
ESC21.780
ECS11.EXE - CS11 CONTROLLER DIAGNOSTIC
ESC21.EXE - SC21 CONTROLLER DIAGNOSTIC
ETC11.EXE - TC11 CONTROLLER DIAGNOSTIC
EDSKF.EXE - DISK FORMATTER DIAGNOSTIC
EDSRK.EXE - DISK RELIABILITY DIAGNOSTIC
EVQRF.EXE - OFFLINE RP DRIVER
EVQRR.EXE - OFFLINE RM DRIVER
EVQM.EXE - OFFLINE SC21/SC31 DRIVER
ECS11.HLP
ESC21.HLP - HELP FILES FOR EMULEX DIAGNOSTICS
ETC11.HLP

8750 TAPE 7 (EMULEX REV K DRIVERS)

UM-BOOTFILES

DRIVER PATCHES
DRIVERS FOR THE EMULEX DEVICES
EXAMPLES OF ATTACH STRINGS

The following is an example of the more common attach strings used on the 11/750.

DS> ATT KA750 CMI KA0 NO NO YES 0 0
DS> ATT DW750 CMI DW0
DS> ATT LP11 DW0 LP0 777514 200 5
DS> ATT DZ11 DW0 TTA 760100 300 5 EIA
DS> ATT TS11 DW0 MSA0 772520 224 5
DS> ATT TS04 DW0 MSA0 772520 224 5
DS> SEL ALL
DS> SET TRACE

EMULEX SC750:

DS> LOAD <program>
DS> ATT RH750 CMI RH0 5
DS> ATT RM RH0 DRA0
DS> ATT RM RH0 DRA1
DS>

EMULEX SC21 or SC31

See page 2.9-22

S.I. 9400 WITH UNIBUS INTERFACE

(This can only be tested under VMS)

See page 2.9-19.
MACRODIAGNOSTIC PROGRAMS

This is a list of the more common diagnostics used on the 11/750 system:

<table>
<thead>
<tr>
<th>DIAGNOSTIC</th>
<th>STAND ALONE ONLY</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECSAA</td>
<td>-</td>
<td>DIAGNOSTIC SUPERVISOR</td>
</tr>
<tr>
<td>EVKAA</td>
<td>YES</td>
<td>HARDCORE INSTRUCTION</td>
</tr>
<tr>
<td>ECKAL</td>
<td>YES</td>
<td>CACHE/TB DIAGNOSTIC</td>
</tr>
<tr>
<td>EVKAB</td>
<td>NO</td>
<td>ARCHITECTURAL INSTRUCTION</td>
</tr>
<tr>
<td>EVKAC</td>
<td>NO</td>
<td>FLOATING POINT INSTRUCTION</td>
</tr>
<tr>
<td>EVKAD</td>
<td>NO</td>
<td>COMPATABILITY MODE INSTRUCTION</td>
</tr>
<tr>
<td>EVKAEC</td>
<td>YES</td>
<td>PRIVILEGED ARCHITECTURE INSTRUCTION</td>
</tr>
<tr>
<td>ECKAX</td>
<td>YES</td>
<td>SPECIFIC CPU CLUSTER EXERCISER</td>
</tr>
<tr>
<td>ECKAM</td>
<td>YES</td>
<td>MEMORY (256KB ARRAY)</td>
</tr>
<tr>
<td>ECKLM</td>
<td>YES</td>
<td>MEMORY(1MB ARRAY)</td>
</tr>
<tr>
<td>ECCBA</td>
<td>YES</td>
<td>UNIBUS ADAPTER DW750</td>
</tr>
<tr>
<td>EVDAA</td>
<td>YES</td>
<td>D211-8 LINE ASYNC MUX TEST</td>
</tr>
<tr>
<td>EVA3A</td>
<td>VMS ONLY</td>
<td>LINE PRINTER DIAGNOSTICS</td>
</tr>
<tr>
<td>ESTAA</td>
<td>VMS ONLY</td>
<td>LOCAL TERMINAL DIAGNOSTIC</td>
</tr>
<tr>
<td>EVTAA</td>
<td>NO</td>
<td>MAGTAPE RELIABILITY DIAGNOSTIC</td>
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<tr>
<td>EVMAA</td>
<td>NO</td>
<td>TS11 RELIABILITY DIAGNOSTIC</td>
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<td>EVTBA</td>
<td>VMS ONLY</td>
<td>MULTITERMINAL DIAGNOSTIC</td>
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<tr>
<td>EVRAC</td>
<td>NO</td>
<td>DEC RM DISK FORMATTER</td>
</tr>
<tr>
<td>EVRDB</td>
<td>YES</td>
<td>DEC RM DISK EXERCISER</td>
</tr>
<tr>
<td>EVRAA</td>
<td>NO</td>
<td>DEC RM DISK RELIABILITY</td>
</tr>
<tr>
<td>ESC21</td>
<td>YES</td>
<td>EMULEX SC21/SC31 CONTROLLER DIAGNOSTIC</td>
</tr>
<tr>
<td>EDSK5</td>
<td>NO</td>
<td>EMULEX DISK FORMATTER PROGRAM</td>
</tr>
<tr>
<td>EDSKR</td>
<td>NO</td>
<td>EMULEX DISK RELIABILITY PROGRAM</td>
</tr>
<tr>
<td>SIRAC</td>
<td>VMS ONLY</td>
<td>S.I. DISK FORMATTER</td>
</tr>
<tr>
<td>SIRAA</td>
<td>VMS ONLY</td>
<td>S.I. DISK RELIABILITY</td>
</tr>
</tbody>
</table>
EVKAA, ECKAL

>>>B DDAO

%%
EVKAA V7.2 Hardcore Instruction Test
Hit any key to continue
EVKAA DONE!
EVKAA DONE!
EVKAA DONE!
EVKAA DONE!
EVKAA DONE!
V7.2 Pass  1 (x)
V7.2 Pass 10 (x)
V7.2 Pass 32 (x)
V7.2 Pass 38 (x)
V7.2 Pass 64 (x)
00004574  02
>>>B DDAO

%%
End of Pass ECKAL V3.2
End of Pass ECKAL-V3.2
End of Pass ECKAL-V3.2
End of Pass ECKAL-V3.2
End of Pass ECKAL-V3.2
0000461C 02
>>>
ECCBA

DS> ATT DW750 CMI DWO
DS> SEL DWO
DS> SET TRACE
DS> R ECCBA

.. Program: ECCBA-REV. 1.3 VAX 11/750 (UBI), DW750 Diagnostic, Rev 1.3, 32 tests, at 00:01:09.92.

Testing: _DWO

Test 1: Control and Status Register Test
Test 2: Map Data Bus Test
Test 3: Map Chip Select Test
Test 4: Map Address Bus Test
Test 5: Map Entry Test
Test 6: CPU Read/Write Test
Test 7: CMI to Unibus Addressing Test
Test 8: Unibus to CMI Addressing Test
Test 9: Data Path Select Test
Test 10: Direct Data Path DATI Test
Test 11: Direct Data Path DATIP/DATO Test
Test 12: Direct Data Path DATOB Test
Test 13: Buffered Address Register Test
Test 14: Buffered Data Path DATI Test
Test 15: Buffered Data Path DATIP Test
Test 16: Buffered Data Path DATO Test
Test 17: Buffered Data Path DATOB Test
Test 18: Buffered Data Path Autopurse Test
Test 19: Byte Offset DATI Test
Test 20: Byte Offset DATIP/DATO Test
Test 21: Byte Offset DDP DATO Test
Test 22: Byte Offset BDP DATO Test
Test 23: Byte Offset DDP DATOB Test
Test 24: Byte Offset BDP DATOB Test
Test 25: Map Entry Functional Test
Test 26: CSR Status Bit Test
Test 27: UET CSR1 Interrupt Test
Test 28: UET CSR2 Interrupt Test [aborted]
Test 29: UET CSR1/CSR2 ACLOW Test [aborted]
Test 30: Map Invalid Test
Test 31: UET PB Bit Test
Test 32: UBE Block Transfer Test
NO UBES SELECTED, SKIPPING TEST

.. End of run. 0 errors detected. Past count: 1.

Time: 1-JAN-1981 00:01
EVKAB

DIAGNOSTIC SUPERVISOR. ZZ-ECSAA-6.5-22B 1-JAN-1981 00:00:00
DS> ATT KA750 CMI KAO N N Y 0 1 - FPA installed
DS> ATT DW750 CMI DW0
DS> SEL ALL
DS> SET TRACE
DS> R EVKAB

.. Program: VAX Basic Instructions Exerciser, ZZ-EVKAB, Rev 2.6, 10 tests, at 00:00:26.55.

Testing: KAO:

Accelerator type 1 is disabled.
Test 1: Integer Arithmetic and Local Instructions
Test 2: Variable Length Bit Field Instructions
Test 3: Basic Branch Instructions
Test 4: Single Bit Field Control Instructions
Test 5: Integer Arithmetic Control Instructions
Test 6: INDEX Instruction
Test 7: Queue Instructions
Test 8: Character String Instructions
Test 9: Decimal String Instructions
Test 10: Edit Instruction

Accelerator type 1 is enabled.
Test 1: Integer Arithmetic and Logical Instructions
Test 2: Variable Length Bit Field Instructions
Test 3: Basic Branch Instructions
Test 4: Single Bit Field Control Instructions
Test 5: Integer Arithmetic Control Instructions
Test 6: INDEX Instruction
Test 7: Queue Instructions
Test 8: Character String Instructions
Test 9: Decimal String Instructions
Test 10: Edit Instruction

End of run. 0 errors detected. Pass count: 1.
Time: 1-JAN-1981 00:01

NOTE Revision 3 of this diagnostic has changed the print out.
EVKAC, EVKAD AND EVKAE

DS> R EVKAC

.. Program: VAX Floating Point Instructions Exerciser, ZZ-EVKAC, Rev 4.1, 4 tests, at 00:01:15.26.

Testing: _KA0

Test 1: Single Precision Floating Point Instructions
Test 2: Double Precision Floating Point Instructions
Test 3: Extended Range Double Precision Floating Point Instructions
Test 4: Extended Range Quadruple Precision Floating Point Instructions

.. End of run. 0 errors detected. Pass Count: 1.
Time: 1-JAN-1981 00:01

(Revision 5 has changed).

DS> R EVKAD

.. Program: VAX Compatibility Mode Instructions Exerciser, EVKAD, Rev 1.2, 4 tests, at 00:01:21.03.

Testing: _KA0

Test 1: Compatibility Mode ENTRY and EXIT Test
Test 2: Compatibility Mode SINGLE OPERAND Instructions
Test 3: Compatibility Mode DOUBLE OPERAND Instructions
Test 4: Compatibility Mode PROGRAM CONTROL Instructions

.. End of run. 0 errors detected. Pass Count: 1.
Time: 1-JAN-1981 00:01

DS> R EVKAE

.. Program: VAX Privileged Architecture Exerciser, EVKAE, Rev 2, 11 tests, at 00:00:22.73.

Testing: _KA0

Test 1: Interrupt Test
Test 2: Exception Test
Test 3: REI Instruction Test
Test 4: Change Mode Instructions Test
Test 5: Processor Register Instructions
Test 6: Interval Timer
Test 7: MEMORY MANAGEMENT
Test 8: KERNEL STACK NOT VALID
Test 9: CHMx TO WRITE PROTECTED STACKS
Test 10: PROBE Instruction Test
Test 11: Process Context Switching

.. End of run. 0 errors detected. Pass Count: 1.
Time: 1-JAN-1981 00:01

DS>
ECKAX

DS> ATT KA750 CMI KA0 NO NO YES 0 0
DS> SEL KA0
DS> SET TRACE
DS> RUN ECKAX

. . Program:  VAX 11,750 Specific CPU Cluster Exerciser -
    ZZ-ECKAX-3.3, Rev 5.1. 14 tests, at 00:00:36.19.

Testing:  _KA0

Test 1:  Reserved Processor Registers
Test 6:  WCS Memory test
Exiting WCS test, WCS last address = 0

Test 7:  WCS Execution Test
Exiting WCS test, WCS last address = 0

Test 8:  Machine Check Exceptions and Interrupts
Exiting WCS parity subtest, WCS last address = 0

Test 9:  TU58 EXERCISER
Test 10:  TU58 EXERCISER READ/WRITE
The TU58 tape cartridge is not recognised as a scratch tape,
do you wish to overwrite the tape? [(No), Yes] NO

TEST 11:  TU58 EXERCISER (WITH MRSP)
TEST 12:  TU58 EXERCISER READ/WRITE (WITH MRSP)

The TU58 tape cartridge is not recognised as a scratch tape,
do you wish to overwrite the tape? [(No), Yes] NO

TEST 13:  PCS Memory Test
TEST 14:  PCS Execution Test

   Time: 1-JAN-1984 00:01
DS> RUN ECKLM

.. Program: ECKAM - Rev. 2.3 MS750 Diagnostic, Revision 2.16, 12 tests at 00:26:57.33.

Test 1: Memory Map Verification Test
Memory Map Valid: 00000003(X) for: L0011 Controller
Slot[0] is a 1024KB array
Slot[1] is empty
Slot[2] is empty
Slot[3] is empty
Slot[4] is empty
Slot[5] is empty
Slot[6] is empty
Slot[7] is empty
Test 2: Data Bus Test
Test 3: Row Select Bus Test
Test 4: Address Bus Test
Test 5: ECC Logic Test
Test 6: CSRO Test
Test 7: Bootstrap ROM Test
ROM NUMBER: A Device Type: SI
ROM NUMBER: B Device Type: DD
ROM NUMBER: C Device Type: DB
Test 8: CPU Lost Error Test
Test 9: CPU XB Error Bit Test
Test 10: Moving Inversions Test [aborted]
Array [0] Single Bit Errors:
  Row 1 - 0
  Row 2 - 0
  Row 3 - 0
Test 12: Memory Quick Verify Test
Number of correctable errors = 1

<table>
<thead>
<tr>
<th>Address (Page)</th>
<th>Bit Number/Syndrome</th>
</tr>
</thead>
<tbody>
<tr>
<td>00024600(x)</td>
<td>15(D) (Data Bit)</td>
</tr>
</tbody>
</table>
Welcome to VAX/VMS version V3.0

$R ECSAA

DIAGNOSTIC SUPERVISOR. ZZ-ECSAA- 6.10-323 22-NOV-1983
09:33:28

.DS>SET EV FL 1,10,11,12
DS>R EVKAM

-- Program: VAX Memory user mode test, ZZ-EVKAM,
  Revision 1.1, 2 tests, at 09:33:46.70

*************************************************************************
WARNING*************************************************************************
This diagnostic disables cache - system performance will be affected
*************************************************************************
WARNING*************************************************************************

This system is a VAX-11/750

Slot 0 contains a 1024 Kbyte module
Slot 1 contains a 1024 Kbyte module
Slot 2 contains a 1024 Kbyte module
Slot 3 contains a 1024 Kbyte module
Slot 4 contains a 1024 Kbyte module
Slot 5 contains a 1024 Kbyte module
Slot 6 contains a 1024 Kbyte module
No memory present in slot 7
Total memory found -> -> -> 7168 Kbytes.
Beginning address is on the 0 Kbyte boundary.
Memory read test begun at 09:34:10.95
Testing controller number: 0
  1024 Kbytes tested at 09:34:21.34
  2048 Kbytes tested at 09:34:30.69
  3072 Kbytes tested at 09:34:40.03
  4096 Kbytes tested at 09:34:49.36
  5120 Kbytes tested at 09:34:58.70
  6144 Kbytes tested at 09:35:08.04
  7168 Kbytes tested at 09:35:17.38

Memory read test done at 09:35:18.83
Memory error summary as of 09:35:20.28
Controller number 0

<table>
<thead>
<tr>
<th>Array</th>
<th>Correctable Errors</th>
<th>Uncorrectable Errors</th>
<th>Unknown Errors</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>1</td>
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</tr>
<tr>
<td>2</td>
<td>0</td>
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<td>3</td>
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<td>0</td>
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<td>5</td>
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<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

-- End of run. 0 errors detected. Pass Count is 1,
Time is 22-NOV-1983 09:35:40.59
S.I. DISK DIAGNOSTICS

Two of the 8780 S.I. Disk Subsystem Diagnostics may be run on the 8750. They are:

SIRAA - Disk Reliability Diagnostic
SIRAC - Disk Formatter Diagnostic

They have to be run under VMS to utilise the S.I. driver.

SIRAA must be run first in all cases to correct a problem with the drive type, (as seen by the diagnostic). SIRAA will report an illegal drive type error, but allows the program to continue.

After 'yes' has been entered to the question:

Do you wish to override the protection check?

SIRAA may be terminated and SIRAC can be run without error, (SIRAA requires a formatted disk pack).

If SIRAC is run first it will always fail.

Examples of SIRAA and SIRAC on the 8750 are included here.

The drive to be tested must be attached as shown below. The attach string given will only work on revision 6.5 or less of the diagnostic supervisor:

DS> ATT DW750 CMI DWO
DS> ATT RM03 DWO SIAL
DS> SEL ALL
SIRAA DISK RELIABILITY

Username:  FIELD
Password:  Welcome to VAX/VMS Version V2.3
$ R ECSAA
DS>
DS> ATT DW750 CMI DWO
DS> ATT RM03 DWO SIAL
DS> SEL SIAL
DS> SET TR
DS>
DS> RUN SIRAA
.. Program: RELIABILITY TESTS SYSTIME L.S.S. ** EVRAA **
   rev 9.0. 6 tests, Testing: _SIAL

****** RELIABILITY TESTS SYSTIME L.S.S. ** EVRAA ** - 9.0 ******
PASS 0 INITIALIZATION SECTION ERROR 1 19-MAY-1982 18:29:28.05
SYSTEM FATAL WHILE TESTING SIAL: ILLEGAL DRIVE TYPE

Function INITIAT^O
Do you wish to override the protection check? [(NO), YES] YES
Test 1: qualification test
   _SIAL QA begun at 19-may-1982 18:29:40.93
   _SIAL QA complete at 19-MAY-1982 18:30:49.20
Test 2: Seek tests timing
   seek tests on _SIAL started at 19-MAY-1982 18:30:51.62
Seek Cylinder Range    Average Seek Time
   (in milliseconds)
   1       1.180
   2       1.190
   4       1.170
   8       1.190
  16       1.190
  32       1.170
  64       2.0
 128      1.170
 256      1.190
 822      1.160
   Seek tests on _SIAL complete at 19-MAY-1982 18:31:15.61
Test 4: multidrive functional tests
   multi drive tests initiated at 19-MAY-1982 18:31:18.74
Error summary for _SIAL at 19-MAY-1982 18:30:04.91

TOTAL XFERS    READ XFERS    WRITE XFERS    WRITECHECKS
  (BYTES)    (BYTES)    (BYTES)    (BYTES)
  67110412   22368648   22373116   22368648

TOTAL ERRORS   READ ERRORS   WRITE ERRORS   WRITECHECK ERRORS
               0              0              0

   Time: 19-MAY-1982 18:38:17.08
DS>
SIRAC DISK FORMATTER

DS>
DS> RUN SIRAC/SE:PACKINIT
.. Program: SIRAC FORMAT SYSTIME LSS, rev 4.0, 8 tests, at 18:40:14.07.
Testing: _SIA1

Disk Type = RM03, Drive Serial Number = 8D2l(D) for Physical Device _SIA1, Pack Structure = FOREIGN, Pack Label = Pack is not Labelled 'SCRATCH' do you wish to continue? [(NO), YES] YES
Test 1: Initialize manufacture bad sector file

************ WARNING ************
BAD SECTOR FILE WILL BE REFORMATTED

DO YOU WISH TO CONTINUE? [(NO), YES] YES

For physical device _SIA1
Enter pack serial number [(1), 1-2147483647(D)] 123456
Test 2: Display manufacture bad sector file

CONTENTS OF BAD SECTOR FILE
PACK SERIAL NUMBER = 123456(D) FOR DEVICE _SIA1
NO BAD SECTORS IN FILE
Test 3: Format pack
Format started at 18:40:43.80 for device _SIA1
Format completed at 18:43:48.09 for device _SIA1
Test 4: Surface verification
Verify started at 18:43:50.80 for device _SIA1
BAD SECTOR FILE UPDATED BY 0(D) ENTRIES
Verify completed at 18:50:46.65 for device _SIA1
FOR PHYSICAL DEVICE _SIA1 DISK TYPE = RM03
PACK WAS LABELLED
PACK SERIAL NUMBER = 123456(D)
NUMBER OF BAD SECTORS ADDED TO BAD SECTOR FILE = 0(D)
.. End of run. 0 Errors Detected. Pass Count: 1.


DS>
DS>
DS>
ESC21 - SC21/SC31 DISK CONTROLLER DIAGNOSTIC

DIAGNOSTIC SUPERVISOR. ZZ-ECSAA-6.6-185 1-JAN-1982 00:00:00
DS> LOAD ESC21
DS>
DS> ATT DW750 CMI DW0
DS>
DS> ATT SC21 DW0 UMA 776700
DS>
DS> SEL ALL
DS>
DS> SET TRACE
DS>
DS> ST/SECT:ALL

.. Program: Emulex SC21/SC31 Disk Controller Diagnostic, at 00:40:38.02. Revision 1.6, 21 tests
Testing: UMA
Enter drive number to test [(0), 0-7(d)] 0

Test 1: Address all registers
Test 2: CSL register (all 1 & 0)
Test 3: Function bits (moving 1 & 0)
Test 4: WC register (all 1 & 0)
Test 5: WC register (moving 1 & 0)
Test 6: BA register (all 1 & 0)
Test 7: BA register (moving 1 & 0)
Test 8: MRL bits can be set & cleared
Test 9: DC register (all 1 & 0)
Test 10: DC register (moving 1 & 0)
Test 11: DA register (all 1 & 0)
Test 12: DA register (moving 1 & 0)
Test 13: Invalid commands give error
Test 15: SC bit set causes interrupt
Test 16: IE & RDY set cause interrupt
Test 17: Check that pack ack sets VV
Test 18: Test IVC bit
Test 19: Increment bus address register
Test 20: Test BAI bit
Test 21: Get controller configuration

Emulex SC21/SC31 Disk Controller CSR [176700]
Vector [254] is configured as an [RM02]
Port number [08]
Firmware rev [05]
Switches [000] octal
Maximum cylinder address = 823.
Maximum track address = 5.
Maximum sector address = 32.

.. End of run, 0 errors detected, pass count is 1, time is 1-JAN-1982 00:40:57.87

DS>
DS>
EDSKF - EMULEX DISK FORMATTER DIAGNOSTIC (for SC21 or SC31)

DS> LOAD EDSKF
DS>
DS> ATT DW750 CMI DW0
DS> ATT SC21 DW0 UMA0 776700 254 }

For SC750 attach string
see page 2.9-10
DS>
DS> SEL ALL*
DS>
DS> ST/SECT:FORVER

.. Program: Emulex Disk Formatter, revision 2.0, 7 tests, at
00:04:25.03
Testing: _UMA0

UNIT: UMA0
DRIVE SERIAL NUMBER: 88
DRIVE TYPE: RM02 (823 CYLINDERS, 5 TRACKS, 32 SECTORS)
FILE STRUCTURE: FOREIGN
VOLUME LABEL: UNREADABLE
BAD AND/OR SKIP SECTOR FILE UNREADABLE
INIT UMA0 IS NOT A SCRATCH VOLUME;
DO YOU WISH TO CONTINUE? [(NO), Y] Y
DO YOU WISH TO INITIALIZE THE BAD (AND SKIP) SECTOR FILE(S)?
[(NO), YES] Y
FOR UNIT UMA0, ENTER VOLUME SERIAL NUMBER [(U),
1-2147483647(D)] 1234
Test 6: Unit UMA0 Format started at 00:11:12.68
UNIT UMA0 format completed at 00:18:01.12
UNIT UMA0 verify started at 00:18:01.26
UNIT UMA0 verify completed at 00:16:11.56
UNIT: UMA0
No OF ADDITIONAL BAD SECTORS: 14
BAD SECTOR FILE CONTENTS:

<table>
<thead>
<tr>
<th>LOGICAL BLOCK</th>
<th>CYL</th>
<th>TRACK</th>
<th>SECTOR</th>
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</thead>
<tbody>
<tr>
<td>1831</td>
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<tr>
<td>127490</td>
<td>796</td>
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<td>2</td>
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</table>

.. End of run, 0 Errors Detected, Pass Count is 1, time is
1-JAN-1982 00:26:18.41

DS>
* If Stand-Alone and ESC21 was run prior to EDSKF,
Deselect UMA.
EDSKR - EMULEX DISK RELIABILITY DIAGNOSTIC (for SC21 or SC31) *

STAND ALONE

DS> LOAD EDSKR
DS> ATT DW750 CMI DW0
DS> ATT SC21 DW0 UMA 776700 254 5
DS> SEL UMA
DS> START

.. Program: Emulex VAX Disk and TU58 Reliability Test Program, Revision 1.1, 4 tests, at 00:53:41.75.
Testing: _UMA0_UMA
 _UMA, an RM02, with volume label 'SCRATCH', has been added to test queue.
Test 1: Qualification
 _UMA0 Qualification started at 1-JAN-1982 00:53:43.10
 _UMA0 Qualification completed at 1-JAN-1982 00:55:11.79
 _UMA Qualification started at 1-JAN-1982 00:55:11.06
 _UMA Qualification completed at 1-JAN-1982 00:56:40.35
Test 2: Timing
Seek tests on _UMA0 started at 1-JAN-1982 00:56:40.44
Seek Cylinder Range Average Seek Time
            (in milliseconds)
  1          4.150
  2          5.80
  4          7.60
  8          8.150
 16         10.150
 32         14.10
 64         19.30
 128        24.80
 256        32.60
 822        54.60
Seek tests on _UMA completed at 1-JAN-1982 00:58:14.02
.. End of run, 0 errors detected, pass count is 1, time is 1-JAN-1982 00:58:14.10
DS>
DS>
* For SC750 attach string
   see page 2.9-10
DEC DIAGNOSTIC DISTRIBUTION

TU58 11 - VAX 11/750

TU58 7 - VAX Hardcore Instr

<table>
<thead>
<tr>
<th>EXE</th>
<th>HLP</th>
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<tbody>
<tr>
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</table>

TU58 8 - VAX 11 Instr.

<table>
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<tbody>
<tr>
<td>EVKAB</td>
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<td>EVKAC</td>
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TU58 9 - CR/Disk User Mode

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<tr>
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### TU58 20 - VAX SYS EXR/BUS INIT

<table>
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<td>EVQDL</td>
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### TU58 33 - VAX Bus Diagnostics

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### TU58 43 - VAX Bus Test Diag.

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### TU58 51 - VAX Autosizer Diag.

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</table>
APPENDIX A - PRODUCT BULLETINS
11/750 MK1 1MB MEMORY ARRAY

SYSTEM: 8750 with MK1 1MB memory arrays

PROBLEM: MK1 1MB Memory Array will not work with battery backup.

SOLUTION: Remove Link 3. Add Link from BD1 to handle side of Link 3. Connects +5VB to all memory chips.

Link 3 is now:

IN = No battery backup.
OUT = Battery backup installed.
NS753 1MB MEMORY WITH MODIFIED L0011 CONTROLLER

SYSTEM: Systime 8750 with modified L0011

PROBLEM: When installing the NS753 1MB National Semiconductor memory array on the modified L0011 memory controller, there are two modifications which need to be fitted to the modified L0011 and one link to be added to the memory array.

SOLUTION: Install link W10 on the National Semiconductor memory array.

Modifications to the L0011 (see below)

Cut pins: E110 pin 10
          E 94 pin 3

Connect: E111 pin 8 to E110 pin 10*
         E111 pin 1 to E 94 pin 3*

* Note these connections are to the leg of I.C.
T.O.Y. CLOCK PROBLEMS

SYSTEM: Systime 8750 with Farnell power supplies

PROBLEM: There is a high occurrence of T.O.Y. clock failures in the field where the system prompts for the time and date each time the system comes up, rather than using the contents of the T.O.D. register.

The following is a list of "known cures" at the present time.

a) Replace E50 on the L0004 module, from CD40114 to 74C89N.

b) Check presence of wire from PIN A00440 on backplane to connector J5 pin 1, this supplies power from battery to the T.O.Y. circuit on the L0004 board.

c) Failure of first batch of AC/DC low boards - due to glitches on the DC-Low signal, this was cured by extensive mods to the boards. A new revision board is now available.

d) The SYSGEN parameter "SETTIME" must be OFF(0) in order to use the contents of the T.O.D. register rather than having to enter date and time from the console when the system is booted.

e) There is a high failure rate of T.O.Y. batteries, normally one cell going short-circuit, causing the output voltage on load to drop to approximately 4V.
The DW750 will fit in slots 7, 8 or 9 of the processor backplane. Remove the 4 bus grant jumpers in connector A of the backplane on the slot chosen. If installed with other MBA's, for example SC750's, then the CMI arbitration level for the existing devices must be dropped by 1. Refer to the Controllers and Interfaces handbook for switch settings.

If the backplane is a Systime manufactured type (Part No 030-0465) and is revision C or earlier then it is necessary to add the following wires:

- From Slot 4 B89 to Slot 7 C48
- From Slot 7 C48 to Slot 8 C48
- From Slot 8 C48 to Slot 9 C48

The DEC backplane does not require these additions. Attach the three pin guides for the 3 x 40 way cables carrying the Unibus signals. These push over the backplane pins and the correct positions are:

- Cable A from J1 on the M9012 board to pins B53-B92
- Cable B from J2 on the M9012 board to pins C3-C42
- Cable C from J3 on the M9012 board to pins C53-C92

Install the M9012 in slot 1 or 9 AB of the 9 slot backplane and fit a standard M9302 terminator to the end of the bus. A special terminator is not required because the UET test registers are contained on the L0010 module.

Boot Diagnostic Supervisor and attach the DW750:

```
DS> ATT DW750 CMI DW1
```

Run ESCBA, version 1.3 or higher, version 1.2 will fail test 29 (AC LOW TEST).
AC/DCLO INITIALISE PROBLEMS

SYSTEM: Systime 8750 with Farnell power supplies.

PROBLEM: When the 8750 is powered up, AC D. I/O signals remain asserted and the 8750 fails to initialise. This is because the signal DCLO, originating on the mother board remains asserted. The 8750, sensing this, refuses to negate ACLO. The DCLO D-type in position E2, doesn’t clock due to the inadequate delay between pre-set going high and the clock input going to the DCLO D-type.

SOLUTION: On side 1, solder a 1000pf capacitor between E2 pin 11 and E2 pin 7. Bend the capacitor over the body of E2.

PARTS

AFFECTED: Add a 1000pf capacitor part no 0410021.
SYSTEM:  8750 with Systime MK1 Memory

PROBLEM:  When adding MK2 1MB memory modules to the 8750 with MK1 1MB memory boards already installed, due to the link configuration on the new board it may be necessary to alter the links on the existing boards.

If after installing the new memory VMS will not boot, reporting "unexpected exception" before halting, the links on the existing arrays should be checked and installed according to the following tables.

This problem can occur on both the modified L0011 and L0016 memory controllers.

SOLUTION:  The links on the MK1 Memory boards should be as follows:

<table>
<thead>
<tr>
<th>L0016</th>
<th>Modified L0011</th>
</tr>
</thead>
<tbody>
<tr>
<td>LK 15 IN</td>
<td>LK 15 IN</td>
</tr>
<tr>
<td>LK 16 OUT</td>
<td>LK 16 OUT</td>
</tr>
<tr>
<td>LK 17 IN</td>
<td>LK 17 IN</td>
</tr>
<tr>
<td>LK 18 OUT</td>
<td>LK 18 OUT</td>
</tr>
<tr>
<td>LK 19 IN</td>
<td>LK 19 IN</td>
</tr>
<tr>
<td>LK 20 OUT</td>
<td>LK 20 OUT</td>
</tr>
<tr>
<td>LK 21 IN</td>
<td>LK 21 IN</td>
</tr>
<tr>
<td>LK 22 OUT</td>
<td>LK 22 OUT</td>
</tr>
<tr>
<td>LK 1 OUT</td>
<td>LK 1 IN</td>
</tr>
</tbody>
</table>