CS01/H2

(DH11/DM11 COMPATIBLE)

COMMUNICATIONS MULTIPLEXER

TECHNICAL MANUAL

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1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the CS01/H2 communications multiplexer. In addition, this manual provides diagnostics and application information.

1.2 OVERVIEW

1.2.1 General Description

The CS01/H2 Communications Multiplexer connects up to 64 asynchronous serial communications lines with individually programmable parameters to the LSI-11 computers manufactured by Digital Equipment Corporation.

The CS01/H2 emulates 1, 2, 3 or 4 DEC DH11 Asynchronous 16-Line Multiplexers and their associated DM11 Modem Control units. The subsytem consists of a CC01/H controller board and 1 to 4 CP11 Distribution Panels each containing one or two CA11 line adapter boards. The CC01 is a single quad-size board which plugs directly into the LSI-11. The line adapter boards contain the line connection and the line circuitry which interface the serial communication line with the parallel data cable to the communications controller.

The CS01/H2 includes the functions of the DM11 Modem Control unit as part of its emulation. As such the CS01/H2 serves as an interface between the modem and the processor. The modem control signals are available as a standard feature with the RS-232-C line adaptor (CA11/H); however, the current loop line adaptor (CA11/C) does not support modem control.

1.3 FEATURES

1.3.1 Microprocessor Design

The CS01/H2 design incorporates an 8-bit high performance bi-polar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to perform an emulation of the equivelant DEC controller. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up and line-loop test.

1.3.2 Packaging

The CC01/H controller is constructed on a single quad-size PC board which plugs directly into the LSI-11 chassis. A single 34-quad flat cable daisy-chains to a maximum of four CP11 distribution panels which contain the line adapter circuitry. The CA11 line adapter boards are plugable modules in eight line groups.

1.3.3 Configuration Flexibility

Each communications controller emulates up to four 16 line DH11s and four DM11s for a maximum of 64 lines. Various types of line adapters may be mixed in eight line groups.

1.3.4 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, the on-board memory, and the individual line adapters. Although this test does not completely test all circuitry, successful execution indicates a very high probability that the controller and the line adapters are operational. If the controller fails the self-test, it leaves the fault LED ON and the controller cannot be addressed from the CPU.

The power-up self-test also does a loop test on each of the line adapter UART circuits. In addition it is possible to perform either an internal or external loop-back test on groups of eight circuits while the CS01/H2 is on-line.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Diagnostics

The CS01/H2 executes the following standard DEC DH11 and DM11 diagnostics (*16 lines only; patch required, see Appendix D):

ZDHK	DH11 Modem Control Multiplexer Diagnostic*
ZDHM	DH11 Comprehensive Diagnostic
ZDHN	DH11 Data Reliability Test

1.4.2 Operating Systems

The CS01/H2 communications multiplexer is compatible with all DEC LSI-11 operating systems that support DH11s without modification.

Table 1-1
CS01/H2 Subsystem Specifications

Characteristic	Specification
CC01/H CONTROLLER	
Design	High-speed bipolar microprocessor implementation of all CS01 functional operations.
Function	Provides complete functional emulation of four DH11 multiplexers and DM11 modem controls.
Software Compatibility	Diagnostics: ZJ179 (DH11) and ZJ118 (DM11) kits Operating Systems: RSX11M, RSX11M+, RSTS/E
No. of Distribution Panels	1 to 4
No. of Lines	8 to 64
Throughput	50,000 characters per second total
Distribution Panel Interface	Eight-bit bidirectional data bus with necessary addressing and control in a single 34-conductor flat cable.
Receive Silo	64-character FIFO for each functional 16-channel DH11; Interrupt programmable for any FIFO full level.
Expanded Receive Silo	Optional 128-character FIFO for each functional 16-channel DH11.
CPU Interface	Standard Q-Bus interface. One bus load for both DH11 and DM11.
DMA Address Range	0 - 2097K words
DMA Transfer	16-bit word with parity check

Table 1-1 (Cont.)
CS01/H2 Subsystem Specifications

Device Address	Selectable with switches and PROM's to cover all DEC-defined DH11 assignments.
Vector Address	Switch selectable for DM11 and DH11
Priority Level	BR5
Indicator	Controller self-test fault
Option Switches	DIP switches for selection of controller options.
Packaging	Single quad-size two layer printed circuit board
Power	5v +/- 5%, 4 amps.
CP11 DISTRIBUTION PANEL	
Configuration	Seven inch high panel for two 8-channel line adapters, including power supply and cable interface.
Dimensions	7" high x 19" wide x 7" deep
Weight	16 lbs.
Power	Self-contained supply, 50-60 Hz. 115/230 vac, 35 watts
CA11/H LINE ADAPTER	
Configuration	Two-sided PCB measuring 6-1/2" x 8" which plugs into CP11 Distribution Panel.
Interface	RS-232-C, with DM11-compatible modem control
Connectors	Standard EIA RS-232-C, 25-pin male connector.

Table 1-1 (Cont.)
CS01/H2 Subsystem Specifications

Indicators	Fault LED per line.
Transmission Modes	Half-duplex, full-duplex, echo-plex
Line Formats	Character lengths: 5-8 bits Stop bits: 1, 1-1/2, 2 Parity: odd, even, none
Data Rates	50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200 baud and ext. 1X clock
Distortion	Transmitter: less than 2% intersymbol Receiver: up to 43% intersymbol distortion and speed variation
Modem Control Signals	To: RTS, DTR, Secondary Tx From: CTS, CD, RI (or DSR), Secondary Rx
CA11/C LINE ADAPTER	
Configuration	Same as CA11/H.
Interface	20 mA current loop.
Connections	Four screw posts
Transmission Modes	Half-dulpex, full-duplex, echo-plex
Line Formats	Same as CP11/A.
Data Rates	Same as CP11/A.
Distortion	Same as CP11/A.

BLANK

2.1 ORGANIZATION

The CS01/H2 communications multiplexer consists of two units: the CC01/H Communications Controller and one to four CP11 Distribution Panels which are connected to the controller by a single 34-conductor flat cable.

2.1.1 Controller

A block diagram showing the major functional elements of the CC01 controller is shown in Figure 2-1. The controller is organized around an 8-bit high-speed bipolar microprocessor which performs all controller functions. The ALU and register file portion of the microprocessor are implemented with two 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with 12 2K X 4 PROM's.

A 4K x 8 high-speed RAM holds device registers, silo buffer and working storage for the microprocessor. The RAM is both a source and destination to the internal data bus and is addressed directly and indirectly by the microprocessor.

The Q-Bus interface consists of 42 bidirectional and two unidirectional signal lines. The Q-Bus interface is used for programmed I/O, CPU interrupts, and data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all DMA operations and transfers data between the Q-Bus data lines and each line buffer.

The line adapter boards with their UART circuits are interfaced to the controller by a 34-conductor cable. This cable contains an 8-bit bidirectional data path, seven address signals and control signals. The Output Data Register holds data going to the line adapters. The Line Address Register holds the address of the line and the distribution panel.

2.1.2 Distribution Panel

Each distribution panel contains one or two eight-line CA11 Line Adapters and an intergal power supply. Two types of line adaptors are available. The CA11/H provides a RS-232-C interface with modem control. The CA11/C has a 20 mA current loop interface and does not support modem control. The line adapters provide the data and modem interface circuitry plus the UARTs circuits which provide the serial to parallel and parallel to serial conversions normally found in these type devices. The UART also contain the baud rate generator for each line. Data control and status transfers between the line adapters and communication controller are on a parallel byte basis.

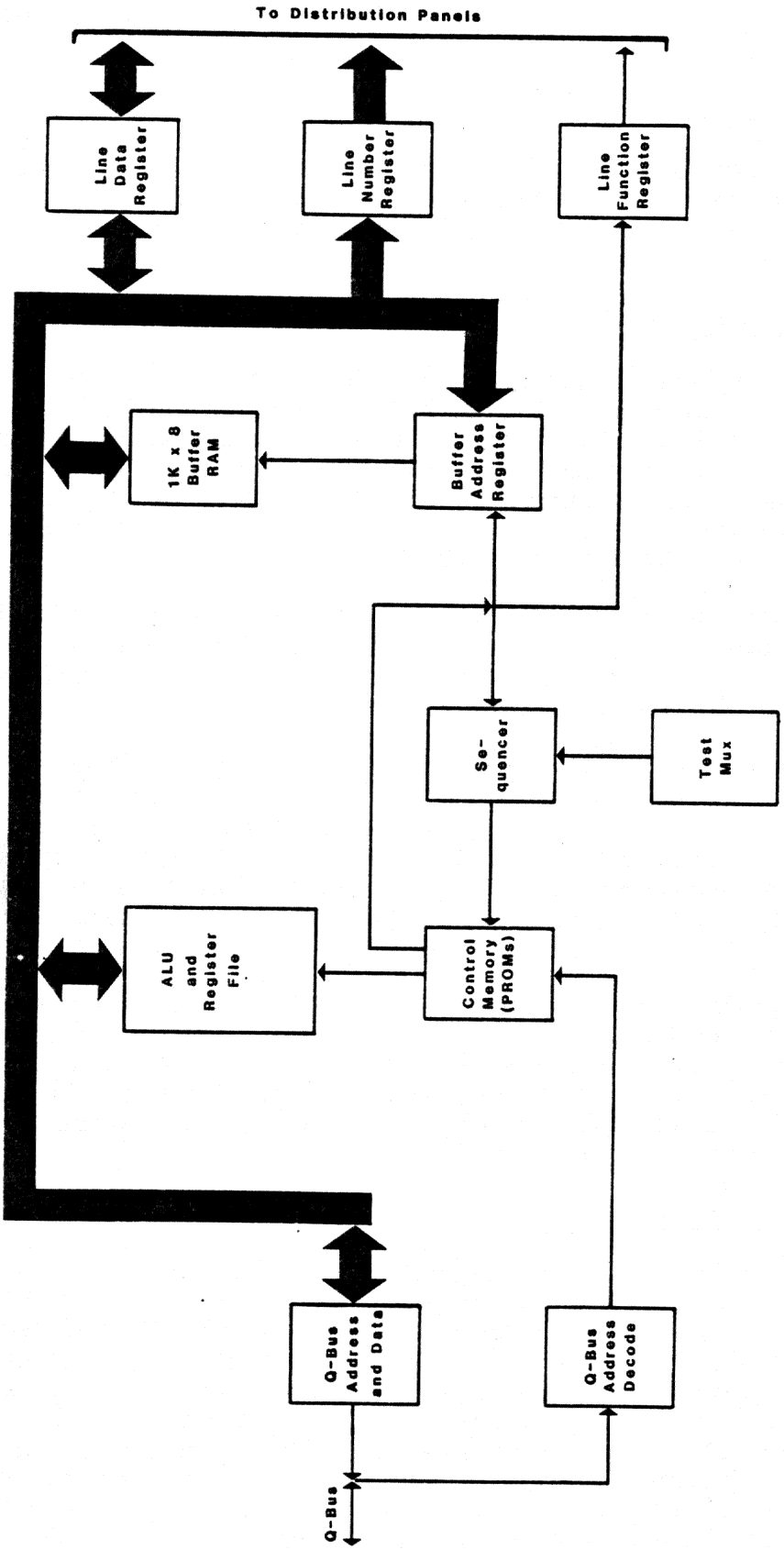


Figure 2-1 CSO1 Block Diagram

2.2 PHYSICAL DESCRIPTION

2.2.1 Controller

The CC01 controller board is designated Part Number CU0110401. The board is shown in Figure 2-2. The board dimensions correspond to the DEC quad-size board. The board is two-sided.

2.2.1.1 Connectors

The distribution panels interface to the controller by means of the 34 pin connector J1 located in the upper right hand corner of the board. Connectors J2 and J3 are used for connecting special test equipment for factory test and repair operations and are not intended for use in normal controller operations.

A quad-sized PCBA, the board interfaces to connector rows A, B, C and D. The 18 pins of each connector row are designated A through V - excluding the letters G, I, O, and Q - from right to left; the top side pins are designated "1" and the bottom side pins are designated "2".

2.2.1.2 Indicators

There are two LED indicators on the located on the top of the CC01 PCBA. LED1 is a fault indicator which will remain ON after powering-up the controller if a fault is detected during the self-test. LED2 is a DMA activity indiactor that flashes during NPR activity.

2.2.1.3 Switches

There are three DIP switches on the board. In addition there is a eight pole switch (SW1) located along the top edge of the board. The switches in these packs are used to select the controller Q-Bus and vector addresses, the number of emulations to be performed and other user selectable options.

2.2.1.4 PROM's

The 12 firmware PROM's are located along the top edge of the board. The PROM locations are designated 0 through 11. The number written on top of the PROM IC is the Emulex part number which identifies the unique pattern of the PROM. These numbers are in the same numerical order as that of the PROM numbers.

The controller makes use of two special PROM's to perform Q-Bus address decoding.

2.2.1.5 RAM Buffer

The two 2168 RAM ICs located on the PCBA are used for configurations of up to 64 lines.

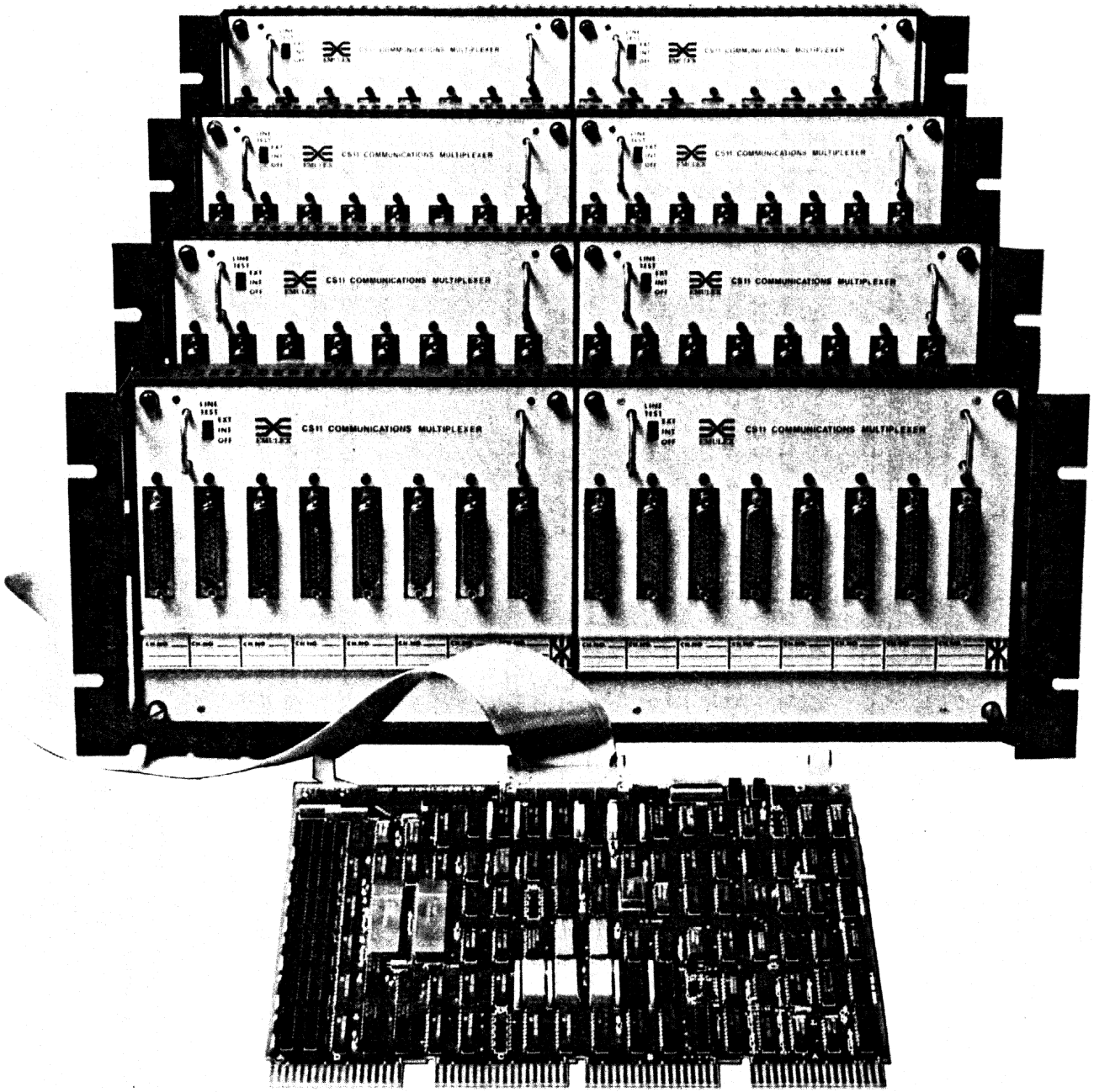


Figure 2-2 CC01 Controller Board and Distribution Panel

2.2.2 Distribution Panel

The distribution panels consist of a mechanical assembly, a power supply, an interface board, and one or two line adapter boards with their cover plates. The distribution panel is shown in Figure 2-2.

2.2.2.1 Line Adapter Boards

Both the CA11/H and CA11/C line adapter boards measure 6-1/2" x 8" and connect to the Interface Board, located in the back of the panel, through a set of 38 AMP MOD 1 pins. The CA11/H board contains eight 25-pin male connectors for interfacing to RS-232-C terminals, modems, or like devices. The CA11/C also provides eight lines, but it uses a four-screw terminal strip for interface to 20 mA current loop devices. Both contain UART and level conversion circuitry for each line.

Each line has a small LED indicator mounted directly above the connector which is used to indicate that the internal self-test of the controller has detected a fault for that line adapter. A three position slide switch in the upper left hand corner of the line adapter board is used to enable an internal, external wrap-around or terminal echo test for the eight line group.

2.2.2.2 Interface Board

The interface board interfaces the daisy-chain cable and the power supply to the two line adapter boards. It is mounted by a set of screws to the Distribution Panel. Each of the line adapter boards plugs into the AMP pins connected to the interface board and inturn is fastened to the panel by four screws. Two daisy-chain cable connectors protrude through the back of the panel so that the cable may be continued or terminated if the panel is the last one on the cable. The power supply cable plugs into a connector on the back of the interface board which also protrudes through the panel.

2.3 INTERFACES

2.3.1 Q-Bus

The LSI-11 Bus consists of 42 bidirectional and 2 unidirectional signal lines. These form the lines along which the processor, memory and I/O devices communicate with each other.

Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The lines are divided as follows:

1. Twenty-two data/address lines - <BDAL21:BDAL00>

2. Six data transfer control lines - BBS7, BDIN, BDOUT, BRPLY, BSYNC, BWTBT

Table 2-1
Q-Bus Connections

	A		B	
	1	2	1	2
A	BIRQ5	+5V	BDCOK	+5V
B	BIRQ6		BPOK	
C	BDAL16	GND	BDAL18	GND
D	BDAL17		BDAL19	
E		BDOUT	BDAL20	BDAL02
F		BRPLY	BDAL21	BDAL03
H		BDIN		BDAL04
J	GND	BSYNC	GND	BDAL05
K		BWTBT		BDAL06
L		BIRQ4		BDAL07
M	GND	BIAKI	GND	BDAL08
N	BDMR	BIAKO	BSACK	BDAL09
P	BHALT	BBS7	BIRQ7	BDAL10
R	BREF	BDMGI	BEVNT	BDAL11
S		BDMGO		BDAL12
T	GND	BINIT	GND	BDAL13
U		BDAL00		BDAL14
V		BDAL01		BDAL15

3. Three direct memory access control lines - BDMG, BDMR, BSACK

4. Six interrupt control lines - BEVNT, BIAK, BIRQ4, BIRQ5, BIRQ6, BIRQ7

5. Five system control lines - BDCOK, BHALT, BINIT, BPOK, BREF.

The MS four data/address lines (BDAL <21:18>) are used only for addressing and do not carry data. BDAL <17:16> reflect the parity status of the 16-bit data word during the data transfer portion of the bus cycle.

2.3.1.1 Q-Bus Starting Addresses

The Q-Bus starting address for the first DH11 and DM11 is selected by SW1. The available addresses are listed in Table 2-2, below. Instructions for setting SW1 are given in paragraph 4.3.2.

Table 2-2
DH11 and DM11 Q-Bus Starting Addresses

DH11	DM11
17760020	17770500
17760040	17770510
17760060	17770520
17760100	17770530
17760120	17770540
17760140	17770550
17760160	17770560
17760200	17770570
17760220	17770600
17760240	17770610
17760260	17770620
17760300	17770630

2.3.1.2 Interrupt Vector Addresses

The DM11 and DH11 interrupt vector addresses are progammed by SW2. Data for setting these switches is given in Table 4-3 and Table 4-4.

2.3.1.3 BR (Interrupt) Priority Level

Both the DH11 and the DM11 interrupt the CPU on BR5.

2.3.1.4 DCOK and INIT Signals

The DCOK and INIT signals both perform a controller clear. The self-test is performed only when DC power is initially applied.

2.3.1.5 DMA Transfers

The controller performs word DMA transfer read operations, so as to halve Q-Bus loading. The controller checks for memory parity errors (if the system has a memory parity controller) which is posted as a NXM error when a parity error is detected.

2.3.2 CAll/H Line Adapter

The CAll/H Line Adapter has eight channel interfaces. Interface pinning assignments are the same as the DEC DHll with DMll modem control. As such, the pinning assignments are those specified for Bell 202C Data Sets (modems). Electrical signal levels are per EIA RS-232-C specifications. The receiver circuits are implemented with 1489 devices; the transmitter circuits are implemented with 1488 devices. Stock Emulex interface pinning assignments are defined in Table 2-3.

Table 2-3
CAll/H Interface Connector

Pin #		Function
Pin 1	-	Chassis Ground
Pin 2	-	Transmit Data
Pin 3	-	Receive Data
Pin 4	-	Request To Send
Pin 5	-	Clear To Send
Pin 7	-	Logic Ground
Pin 8	-	Carrier Detector
Pin 11	-	Secondary Transmit Data
Pin 12	-	Secondary Receive Data
Pin 18	-	Make Busy
Pin 20	-	Data Terminal Ready
Pin 22	-	Ring Indicator

2.3.2.1 CAll/H Line Adapter Options

The CAll/A interface can be reconfigured to allow use of a number of other modems. The following is a list of the modem options and their pinning assignments. The changes are effected using wire wrap jumpers. Instructions for implementing the options are in the chapter on installation, paragraph 4.5.1. Note that the additional modems may not be supported by DEC software and that custom drivers may have to be written for their implementation.

Option	Pinning Assignments
Standard RS-232-C	Secondary Receive, Pin 16. Secondary Transmit, Pin 14.
103 E,G,H,J Modems	Make Busy, Pin 25 = Ready to Send, Pin 4.
212 A Modem	Make Busy, Pin 18 = Ready to Send, Pin 4.
811 B	Receive Signal Element Timing, Pin 17 = Secondary Receive, Pin 12.
DSR for Ring	Data Set Ready, Pin 6 = Ring, Pin 22.

2.3.3 CA11/C Line Adapter

The CA11/C Line Adapter provides a 20 mA current loop interface for each of its eight lines. Modem control is not supported. Both the transmit and receive circuits are optically coupled. This provides common noise rejection that is much greater than RS-232C and 20 ma interfaces that are not optically coupled. LEDs above each channel's interface connector are used to indicate faulty channels.

2.3.3.1 CA11/C Line Adapter Options

There are several options that can be selected using jumpers on the CA11/C. The CA11/C comes from the factory configured with active transmitters and receivers. The transmitters and receivers can be independently reconfigured for passive operation if required. The CA11/C also comes configured from the factory with an open circuit voltage of 12VDC. A Long Line (L.L.) option with an open circuit voltage of 24VDC can be selected if longer line lengths and/or increased imunity to noise are required. To further increase noise rejection, additional filtering may be strapped to the receiver loop. Implementation of these options is described in the Installation Section, paragraph 4.5.2.

2.4 FUNCTIONAL DESCRIPTION

2.4.1 Receiver Operation

2.4.1.1 UART

Reception on each line is by means of universal asynchronous receiver/transmitters (UARTs). These MOS/LSI devices perform all the function of double buffered asynchronous character assembly. The receiver section of the UART samples the line at 16 times the bit rate of the signals to be received on the line. Upon detection of a mark to space transition, the UART counts eight clock pulses and checks the state of the line again. This sampling occurs in the center of the normal start bit. If the sample is a mark, the receiver return to its idling state, ready to detect another mark to space transition. If the sample is a space, the receiver enters

the data entry condition and samples the state of the line at subsequent sample points spaced at multiples of 16 clocks from the center of the start bit. The number of samples taken is determined by the character length information and parity enable programmed in the Line Parameter Register. If parity checking is enabled for the line, the receiver computes the parity of the character received and compares it with the parity sense specified for the reception on the line. If the parity does not check, the parity error bit is set.

The character length, parity, and number of stop bits that are used by the UART to perform the above operations are stored in each UART from information received from the Line Parameter Register for the associated UART.

2.4.1.2 Receiver Scanner

The receiver section of the UARTs' are serviced by a receiver scanner which polls the UARTs for a line which has assembled a received character. The received character and its associated status bits are transferred to the silo, if it is not full. The receiver scanner has priority over the transmitter scanner since the transmitting output is by means of DMA and can be deferred if necessary during conditions of peak activity. In this manner, characters will not be lost or overrun conditions generated because of the operation of the controller itself.

2.4.1.3 Silo Operation

The silo for each DH11 is contained in the RAM memory. A 16-bit wide by 64 word (optional 128 word) deep first-in-first-out (FIFO) storage is maintained by the controller's microprogram. In effect, a 16-bit word entered at the top of the silo is automatically shifted down to the lowest location that does not already contain an entry. The bottom of the silo is the received character register.

There are two registers associated with the silo. The received character register is a read-once register that is the bottom location of the silo. Reading it extracts the character, and its associated status, from the silo and causes all other entries to shift down one word position.

The other register is the Silo Status Register. The high byte of this register is read-only and contains the status of the number of words which fill the silo. The low byte is read-write and contains the number of characters which must be loaded into the silo before a received interrupt request will be generated.

2.4.1.4 Half-Duplex Operation

When the line is programmed for half-duplex operation, the receiver is enabled at all times except when the BAR bit for the line is set indicating that transmission is underway. The receiver is blinded

from receiving the characters being transmitted, since the transmitting is done on the same circuit as the receiving. No transmit characters are sent to the silo. The line may not be in auto-echo mode when operating half-duplex, since transmitting and receiving can not be done at the same time.

2.4.1.5 Received Character Distortion

Received characters may contain up to 43.75 percent distortion on any bit due the sampling rate employed in the UART. However, the overall bit rate must be accurate. Specifically, errors in bit rate are cumulative such that when the receiver samples the first stop bit to see if it is a mark, the error accumulated by that time must not exceed 43.75 percent of the bit time. The accumulated error (called "gross start-stop distortion") is calculated as clock error times number of bits plus one, plus the bias distortion of the final character. Assuming the reception of eight data bits, or seven data bits plus parity, 4.8 percent speed distortion would be permissible. Speed distortion (clock error and bit rate error) of any amount causes severe problems to an echo situation. If a terminal sends at a slightly fast rate and the controller sends the exact same characters back to the terminal at the correct rate, the silo will eventually fill with unechoed characters.

2.4.2 Transmitter Operation

2.4.2.1 UART

Transmission on each line is also performed by UARTs. These MOS/LSI devices perform all the necessary functions for double buffered asynchronous character transmission. The transmitter section of the UART holds the serial output at a marking state when idle. When a character has been loaded into the transmitter holding buffer, the UART will generate a start bit within 1/16 of the bit time. The start space is followed by five, six, seven, or eight data bits and the parity bit if parity is selected. Control of the UART is performed by the Line Parameter Register. Data bits are presented to the line least significant bit first.

The minimal number of stop bits depends upon the setting in the Line Parameter Register. If transmission is in five-bit code, either one or one and half stop bits is transmitted.

If the transmitter's holding register has been loaded while a character is being transmitted, the second character will have its start bit transmitted immediately at the end of the preceding character's stop bits.

2.4.2.2 DMA Transmission

Unlike the receiver operation where the controller transfers received characters from the UART to the silo for programmed input by the CLU, the CS01/H2 performs automatic direct memory access (DMA) of characters to be transmitted. Data is accessed a word at

a time from the LSI-11 memory except for odd bytes at the beginning or end of the buffer. The low-order byte is transferred to the UART's transmitter holding buffer and the high-order byte is held in the controllers memory. The DMA accessing is controlled by the 16-bit Byte Count Register (BCR) and the 22-bit Current Address Register (CAR). The CAR is incremented by two for every word accessed from memory. The BCR is incremented by one for each byte transferred to the UART's transmitter holding buffer. The transmitting operation for a line is active only as long as the bit corresponding to the line is set in the Buffer Active Register (BAR). This bit is set under programmed control to initiate the transmitting of a buffer and is reset after the last character of the buffer has been shifted from the UART.

2.4.2.3 Auto-Echo Operation

There are provisions for the controller to echo (transmit) received characters without software intervention. This feature is enabled for each line by setting the AEE (bit 15) in the Line Parameter Register.

The auto-echo is performed by the receiver scanner. When the receiver scanner finds a received character for a line on which the auto-echo is enabled and which does not have a framing error or overrun error, it transfers the character to the transmitter holding register for the line as well as to the silo. If the transmitter holding register is not empty at the time the received character is found, the character remains in the receiver holding register until the next time the receiver scanner finds the character.

It is not advisable to simultaneously transmit messages on a line and auto-echo characters received on that line. The auto-echo feature of the controller will interlock these functions to some degree, but if more than two characters are received on a line while the scanner is waiting for the transmitter holding buffer to become available, data overrun occurs and characters are lost. Auto-echo and software driven transmission should not be attempted on the same line simultaneously if input from the line is expected.

2.4.3 Modem Control

The line interface board provides level conversion for all modem control lines. The output control functions are: Terminal Ready, Request To Send, and Secondary Transmit. The received control functions are: Clear To Send, Carrier, Secondary Receive and Ring.

The controller has a modem control scanner which scans the four modem control inputs line-by-line. When a transition is detected, the scanner is stopped with appropriate status displayed in the control status register (CSR), and an interrupt is generated. The scanner can be programmed to "free run" or can be sequentially stepped through line-by-line. The scanner may be cleared under program control to reset the scanner, its enable, and all memory associated with the transition detectors.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Initialize

The Q-Bus INIT signal clears the silo, UARTs and all registers except the Current Address and Byte Count Registers. All scanners are forced to line zero and all memory associated with transition detectors is cleared.

MC (SCR bit 11) performs an initialization of the DH11 portion of the controller. CS (CSR bit 11) provides a clear of the scanner and transition detector logic of the DM11 portion of the controller.

2.5.2 22-Bit Memory Addressing

Twenty-two bit addressing capability is available as an option for the CS01. The Emulex part number for the option kit is CS0113001. The kit consists of a single AMD2908 IC which is placed in socket U101 on the CC01 PCBA.

Twenty-two bit memory addressing is enabled by closing SW1-8. Bits <13:10> in the Line Status Register (LSR) then serve as address bits <21:18>. Address extension bits 17 and 16 can be read as bits 09:08 of the LSR when 22-bit addressing is enabled. However, they can only be modified by writing the SCR (bits 05 and 04, respectively).

A 22-bit address is specified by first loading the MS four bits of the address into the LSR, bits A17:A16 and the line number into the SCR, and the LS 16 bits into the CAR. When CAR is loaded, the bits combine to form the 22-bit buffer address for the line specified.

WARNING

> Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing a CS01 with the extended addressing option in such a system will damage the option IC. Before installing the option confirm that there is neither positive or negative potential between lines BC1, BD1, BE1, BF1 and logic ground. A CS01 without the addressing option will not be damaged if power is present on those lines.

2.5.3 Interrupts

The following kinds of interrupts are generated by the controller:

Receiver Interrupt (SCR bit 07) - This interrupt, when enabled by RIE (SCR bit 06), occurs whenever the number of entries in

the silo exceeds the silo alarm level that the program has stored in low-byte of the Silo Status Register.

Storage Overflow Interrupt (SCR bit 14) - This interrupt, when enabled by SIE (SCR bit 12), occurs when the receiver scanner wants to put a character into the silo which is already full with 64 entries. Should this situation occur, it does not necessarily mean that data has been lost since the character which was to have been moved to the silo is still in the UART's receiver holding register.

Transmitter Interrupt (SCR bit 15) - This interrupt, if enabled by TIE (SCR bit 13), occurs whenever a line has finished the transmission of a complete string of characters. Specifically, it occurs when the corresponding BAR bit is reset when the last character has left the shift register of the UART.

Non-Existent Memory Interrupt (SCR bit 10) - This interrupt, when enabled by TIE (SCR bit 13), occurs whenever the controller detects no response from the addressed memory or a parity error is detected in the word which is accessed.

Modem Transition Interrupt (CSR bit 07) - This interrupt, if enabled by IE (CSR bit 06), occurs whenever the modem control scanner detects a transition on a modem control input which is enabled.

3.1 DH11 REGISTERS

There are 53 registers for each DH11 emulation. Three of these registers (LPR, CAR and BCR) are replicated for each of the 16 lines. Selection of a particular three-register set is made by the line number in SCR.

3.1.1 System Control Register (SCR) 17760xx0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TI	SI	TIE	SIE	MC	NXM	MM	CNI	RI	RIE	A17	A16	Line No.			

Read/write, byte addressable.

Transmitter Interrupt (TI) - Bit 15

This bit is a read-write bit which is set whenever the controller increments the byte count to zero, indicating the loading of the last character of a buffer into a UART transmitter holding register. This bit, when set, causes an interrupt to be generated if TIE (bit 13) is set.

Storage Interrupt (SI) - Bit 14

This read-only bit is set whenever the receiver scanner has found a receiver holding register with a character in it and desires to store that character in the silo, but cannot because of lack of space. When set, this bit causes an interrupt to be generated if SIE (bit 12) is set.

Transmitter Interrupt Enable (TIE) - Bit 13

This read/write bit, when set, allows the setting of TI or NXM (bits 15 or 10) to generate a transmitter or non-existant memory interrupt request.

Storage Interrupt Enable (SIE) - Bit 12

This read/write bit, when set, allows the setting of SI (bit 14) to generate an interrupt request.

Master Clear (MC) - Bit 11

This read/write bit, when set, generates an initialize within the controller, clearing the silo, the UARTs and the registers. The exact bits cleared are discussed in Initialize, paragraph 2.5.1.

Non-Existent Memory (NXM) - Bit 10

This read-only bit is set when the controller is bus master during NPR transfer and does not receive a SSYN from the memory within 10 usec. Also set if a parity error is detected during the memory read operation.

Maintenance Mode (MM) - Bit 09

This read/write bit, when set, places the controller in the maintenance mode. When in maintenance mode, it is possible to write bits 07, 10 and 14, which are normally read-only. Also, the transmitted data signal is internally looped to the received data input. All line parameters must be set before setting the maintenance mode bit.

Clear Non-Existent Memory Interrupt (CNI) - Bit 08

This read/write bit, when set, clears the non-existant memory interrupt (bit 10) and clears itself.

Receiver Interrupt (RI) - Bit 07

This read-only bit, when set, indicates that the number of characters stored in silo exceeds the "alarm level" specified by the low byte of the Silo Status Register. Setting of this bit will generate an interrupt request if RIE (bit 06) is also set.

Receiver Interrupt Enable (RIE) - Bit 06

This read/write bit, when set, allows the setting of RI (bit 07) to generate an interrupt request.

Extended Address Bits 17:16 (A17:A16) - Bits <05:04>

These read/write bits are bus address bits A17 and A16 for the line specified in bits <03:00>. The contents of these bits are copied into the 22-bit CAR for the line when the low-order 16 bit are loaded in the CAR.

Line Number - Bits <03:00>

Each of the 16 lines served by the controller has its own storage for line parameter information, current address, and byte count. These storage locations are loaded by the program via the Line Parameter Register, Current Address Register, and Byte Count Register, but the hardware must first be told which line is to have its line parameters, current address or byte count changed. This routing is accomplished by setting the Line Selection bits to the binary address of the desired line. Thse bits are read/write.

3.1.2 Received Character Register (RCR) base address + 2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VDP	DO	FE	PE	Line No.				Received Character							

Read only, byte addressable.

This read-once register is the bottom of the 64 word silo. Valid silo data is displayed if bit 15 is set. When this register is read the bottom word of the silo is removed, the Silo Fill Level in SSR is decremented by one and SI is reset.

Valid Data Present (VDP) - Bit 15

The bit indicates that the data present in bits <14:00> of this register are valid. It permits a character handling program to take characters from the silo until it is empty. This is done by reading this register and checking bit 15 until a word is obtained for which bit 15 is a zero.

Data Overrun (DO) - Bit 14

This bit is set when the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding register or because the silo is full.

Framing Error (FE) - Bit 13

This bit is set if the receiver samples a line for the first stop bit, and finds the line in a spacing condition (logical 0). This condition usually indicates the reception of a Break.

Parity Error (PE) - Bit 12

This bit is set if the parity of the received character does not agree with that designated for the line.

Line Number - Bits <11:08>

These bits indicate the line number on which the received character was received. Bit 08 is the least significant bit.

Received Character - Bits <07:00>

These bits contain the received character, right justified. The least significant bit is bit 00.

3.1.3 Line Parameter Register (LPR) base address + 4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
AEE	HD	Tx Speed				Rx Speed				OP	PE	0	TSB	Char. Length	

Read/write, byte addressable.

The LPR for all lines is cleared by Initialize and Master Clear.

Auto-Echo Enable (AEE) - Bit 15

When this bit is set, characters received on this line will be echoed by the controller.

Half-Duplex (HD) - Bit 14

If this bit is set, this line will operate in half-duplex mode. If reset, this line will operate in full-duplex mode. In half-duplex operation the receiver is blinded during transmission of a character.

Transmitter Speed - Bits <13:10>

The state of these bits determines the operating speed for this line's transmitter. See Table 3-1.

Table 3-1
Tx and Rx Speed

Transmitter / Receiver	Bits 13 / 9	12 / 8	11 / 7	10 / 6	Rate
	0	0	0	0	Disable
	0	0	0	1	50 Baud
	0	0	1	0	75 Baud
	0	0	1	1	110 Baud
	0	1	0	0	134.5 Baud
	0	1	0	1	150 Baud
	0	1	1	0	200 Baud
	0	1	1	1	300 Baud
	1	0	0	0	600 Baud
	1	0	0	1	1200 Baud
	1	0	1	0	1800 Baud
	1	0	1	1	2400 Baud
	1	1	0	0	4800 Baud
	1	1	0	1	9600 Baud
	1	1	1	0	19200 Baud
	1	1	1	1	1x External Rec Clock

Receiver Speed - Bits <09:06>

The state of these bits determines the operating speed for this line's receiver. See Table 3-1. If the receiver speed is different from the transmitter speed, the receive speed is programmed in the split-speed baud rate generator and the UART receiver clock is connected to the generator.

Odd Parity (OP) - Bit 05

If this bit and PE (bit 04) are set, characters of odd parity will be generated on this line and incoming characters will be expected to have odd parity. If this bit is not set, but bit 04 is set, characters of even parity will be generated on this line and incoming characters will be expected to have even parity. If bit 04 is not set, the setting of this bit is immaterial.

Parity Enabled (PE) - Bit 04

If this bit is set, characters transmitted on this line will have an appropriate parity bit affixed, and characters received on this line will have their parity checked.

Two Stop Bits (TSB) - Bit 02

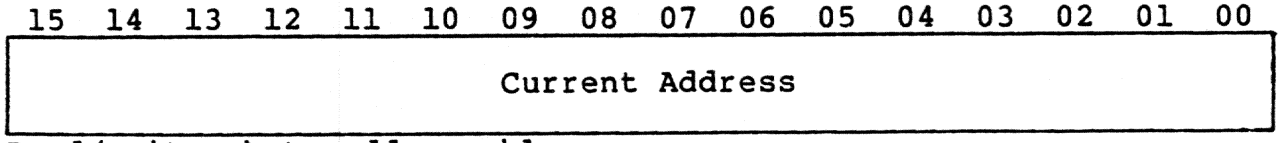
This bit, when set, conditions a line transmitting with six-, seven-, or eight-bit code to transmit characters having two stop marks. If the line is transmitting five-bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop marks. If this bit is not asserted, one stop mark is sent.

Character Length - Bits <01:00>

These bits should be set as shown to receive and transmit characters of the length (excluding parity bit) shown:

Bit 01	Bit 00	Char. Length
0	0	5 bit
0	1	6 bit
1	0	7 bit
1	1	8 bit

3.1.4 Current Address Register (CAR) base address + 6



Read/write, byte addressable.

Current Address (CAR) - Bits <15:00>

This register contains the 22-bit buffer address used by the controller for DMA transfers. There is a buffer address for each line. When read or written, this register relects the LS 16 bits of the buffer address for the line specified by the SCR. This register must be loaded only after the LSR has been loaded with the MS four bits of the address (<A21:A18>) and after SCR has been loaded the desired line number and address bits <A17:A16>. When this register is loaded, address bits <15:00> of this register, bits <A17:A16> from the SCR and bits <A21:A18> from the LSR are transferred into the 22-bit CAR for the line. This register is not cleared by Initialize or Master Clear.

3.1.5 Byte Count Register (BCR) base address + 10

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Two's Complement of Number of Bytes															

Read/write, byte addressable.

Byte Count (BCR) - Bits <15:00>

This register is loaded with the two's complement of the number of bytes to be transferred.

In the same fashion as the Line Parameter and Current Address registers, this register must not be loaded or read with out first selecting the line number in SCR. This register is not cleared by Initialize or Master Clear.

3.1.6 Buffer Active Register (BAR) base address + 12

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Transmit Enable Bits															

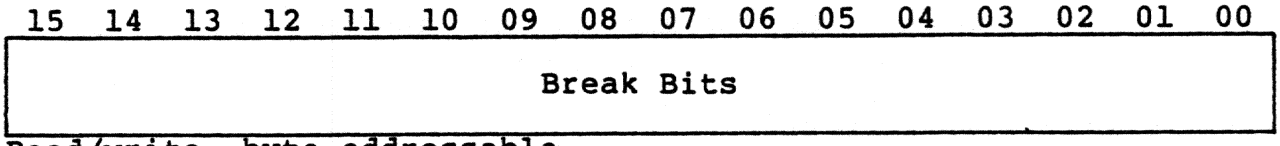
Read/write, byte addressable.

Transmit Enable Bits - Bits <15:00>

This register contains one bit for each line. The bits are set individually using BIS instructions. Setting a bit initiates transmission on the associated line. The bit is cleared by the controller when the last character to be transmitted on that line is loaded in the transmitter holing buffer of the UART. It should be noted that while the clearing of a BAR bit does indicate that a new message may be sent, it does not indicate that the last characters from the preceding message have been completely sent. Specifically, two more characters are sent after the BAR bit

clears. These are the last two characters of the message; one of them is starting when the BAR is cleared, and one is the final character loaded into the holding register at time the BAR is cleared. This effect is a normal consequence of double-buffered transmission and is mentioned here for the benefit of programmers who want to write programs that control such modem leads as Request To Send. Cleared by Initialize and Master Clear.

3.1.7 Break Control Register (BCR) base address + 14

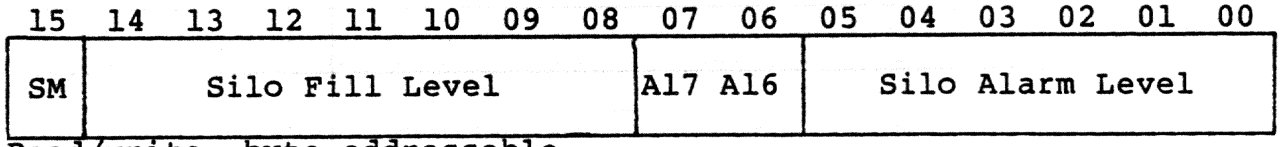


Read/write, byte addressable

Break Control - <15:00>

This register contains one bit for each line. Setting a bit in this register immediately generates a break condition on the line corresponding to that bit number; clearing the bit terminates the break condition. The break condition may be timed by sending characters during the break interval, since these characters never actually reach the line. Cleared by Initialize and Master Clear.

3.1.8 Silo Status Register (SSR) base address + 16



Read/write, byte addressable.

This register is cleared, except for bits 07 and 06, by Initialize and Master Clear.

Silo Maintenance (SM) - Bit 15

Each time this read/write bit is set, a fixed binary pattern (125252_8) is sent to the silo for checking during maintenance. Clearing and setting loads another copy of the pattern.

Silo Fill Level - Bits <13:08>

These read-only bits are an up-down counter that indicates the actual number of characters in the silo. The standard silo will hold 64 charaters. When the silo is full (assuming a Silo Alarm Level of zero and A17:A16 set to zero), the register will contain 040000 when read. If the silo was empty, the register would contain 000000.

When the Expanded Silo option is enabled, the silo can hold 256 characters. The entire upper byte (bits <15:08>) is used to indicate the number of characters in the silo. When the silo is full, however, the register overflows and the upper byte will contain all zeros. The overflow is indicated by the SI bit of the SCR (bit 14). There is no Silo Maintenance function.

Extended Memory Adresss (A17, A16) - Bits <07:06>

These bits are read-only and contain the A17 and A16 bits of the current address for the line which is selected in the SCR.

Silo Alarm Level - Bits <05:00>

The program writes a number between 0 and 63 into this location corresponding to the desired silo alarm level. When the number of characters stored in the silo exceeds that number, the RI (bit 07 in SCR) is set and and interrupt request is generated if enabled by RIE (SCR bit 06).

3.2 DM11 (MODEM CONTROL) REGISTERS

The controller has two registers associated with the modem control for a 16 line group.

3.2.1 Control and Status Register (CSR) 17770xx0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RF	CF	CTS	SRF	CS	CM	MM	STP	DONE	IE	SE	BUSY	Line No.			

Read/write, byte addressable.

This register contains modem control transition information found by the scanner. It also contains maintenance controls.

Ring Flag (RF) - Bit 15

When DONE is set, this flag indicates that a Ring OFF to ON transition has been detected on the line specified by bits <03:00>. This bit is read-only and is cleared by Initialize and Clear Scan.

Carrier Flag (CF) - Bit 14

When DONE is set, this flag indicates that a Carrier transition has been detected on the line specified by bits <03:00>. This bit is read-only and is cleared by Initialize and Clear Scan.

Clear To Send (CTS) - Bit 13

When DONE is set, this flag indicates that a Clear To Send transition has been detected on the line specified by bits <03:00>. This bit is read-only and is cleared by Initialize and Clear Scan.

Secondary Receive Flag (SRF) - Bit 12

When DONE is set, this flag indicates that a Secondary Receive transition has been detected on the line specified by bits <03:00>. This bit is read-only and is cleared by Initialize and Clear Scan.

Clear Scanner (CS) - Bit 11

This write only bit, when set, clears all logic associated with the modem control scanner including the stored values of the Carrier, Clear-To-Send, Ring and Secondary Receive for all 16 lines. This function is especially useful if the programmer requires knowledge of the ON states of Carrier, Clear To Send, Ring and Secondary Receive. When the scanner is enabled (or a step is performed) following a Clear Scanner, an interrupt will occur for all ON states as they will appear as OFF-to-ON transitions. The Clear Scanner function is not completed until BUSY is reset by the controller.

Clear Multiplexer (CM) - Bit 10

This write only bit, when set, clears the Request To Send, Terminal Ready, Secondary Transmit, and Line Enable flip flops for all lines when a one-bit is written into this bit position.

Maintenance Mode (MM) - Bit 09

The scanner inputs (Ring, Clear To Send, Carrier, and Secondary Receive) are set to one. This bit is read/write and is cleared by Initialize and Clear Scanner.

Step (STP) - Bit 08

This write-only bit causes the scanner to increment the Line Number and test that line for interrupt causing transitions. Step may be used in place of Scanner Enable but care should be exercised that the scan rate is great enough (milliseconds) such that double carrier transitions will be detected. DONE does not inhibit the step function. This function is not completed until BUSY is reset by the controller.

Done (DONE) - Bit 07

The DONE flag is set to indicate that the scanner has detected a transition requiring an interrupt to the program. An interrupt will occur if Interrupt Enable is set. When DONE is set, it inhibits the scanner from advancing and makes available:

(a) the Line Number that caused the interrupt
(b) the status of the flags (4 bits)
(c) modem status (8 bits)

The scanner will be released again when DONE is reset. This bit is read/write and is cleared by Initialize and Clear Scanner.

Interrupt Enable (IE) - Bit 06

When set, interrupts may be generated. This read/write bit is cleared by Initialize and Clear Scanner.

Scanner Enable (SE) - Bit 05

When set, the scanner is allowed to "free run", testing all lines sequentially if the DONE is cleared. BUSY will be set as long as the scanner is enabled. This bit is read/write and is cleared by Initialize and Clear Scanner.

Busy (BUSY) - Bit 04

This read-only bit is set when scanner is cycling. It is reset after clearing or stopping the scanner, or after a step function is completed.

Line Number - Bits <03:00>

These bits are the binary address of the modem scanner's position. These bits are read/write and are cleared by Initialize and Clear Scanner.

3.2.2 Line Status Register (LSR) base address + 2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	A21	A20	A19	A18	A17	A16	RNG	CAR	CTS	SR	ST	RTS	DTR	LE

Read/write, byte addressable.

The LSR is replicated for all 16 lines. The LSR being addressed is determined by the line number in the CSR.

Extended Address Bits 21:18 (A21:A18) - Bits <13:10>

When the 22-bit addressing option is enabled (SW1-8 ON), bits <13:10> are used to specify the MS four bits of the 22-bit buffer address in CAR for the line specified by SCR. When read, these bits indicate the status of (A21:A18> in the CAR for the line specified by SCR.

Extended Address Bits 17:16 (A17:A16) - Bits <09:08>

When the 22-bit addressing option is enabled (SW1-8 ON), bits <09:08> reflect the status of A17 and A16 of the buffer address for the line specified by SCR when this register is read. A17 and A16 cannot be written using this register; they may only be written at bits <05:04> of SCR.

Ring (RNG) - Bit 07

This read-only bit is the status of the modem Ring (or Data Set Ready) lead.

Carrier (CAR) - Bit 06

This read-only bit is the status of the modem Carrier Detect lead.

Clear To Send (CTS) - Bit 05

This read-only bit is the status of the modem Clear To Send lead.

Secondary Receive (SR) - Bit 04

This read-only bit is the status of the modem Secondary Receive lead.

Secondary Transmit (ST) - Bit 03

When set, presents a MARK to the modem's Secondary Transmit lead. This bit is read/write and is cleared by Initialize and Clear Multiplexer.

Request To Send (RTS) - Bit 02

This bit is used to condition the modem to transmit if all other conditions are met. This bit is read/write and is cleared by Initialize and Clear Multiplexer.

Data Terminal Ready (DTR) - Bit 01

This bit, when set, presents an ON to the modem's Data Terminal Ready to switch the data communications equipment to the communication channel. This bit is read/write and is cleared by Initialize and Clear Multiplexer.

Line Enable (LE) - Bit 00

This bit enables the input of the Ring, Carrier, Clear To Send and Secondary Receive to be sampled by the program and to be tested for transitions. This bit is read/write and is cleared by Initialize and Clear Multiplexer.

BLANK

This section describes the step-by-step procedure for the installation of the CS01/H2 communication controller in a Q-Bus environment. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the CS01, is covered in paragraph 4.1).

Emulex recommends that Section 4 be read in its entirety before installation is begun.

1. Inspect the CS01.
2. Prepare the CPU.
3. Configure the CC01 controller.
4. Configure the CP11 distribution panel.
5. Configure the CA11 line adapters.
6. Install the distribution panels with the line adaptors.
7. Install the CC01 controller.
8. Cable the subsystem.
9. Test the subystem.

4.1 INSPECTION

Before unpacking the CS01, examine the packaging for any signs of damage. Notify the carrier if any damage is noted.

Make a visual inspection of the CC01 controller board and CP11 distribution panel after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROM's should be examined carefully to insure that they are firmly and completely seated in their sockets.

Be sure that you have received all the components that you ordered.

4.2 PREPARE THE CPU

Power down the system and switch OFF the main AC breakers. If the CPU is mounted in a rack, slide the CPU out to gain access to the card cage. Remove the rear cabinet door to expose the RETMA rails. If the LSI is a stand-alone model, remove the cover.

4.3 CONTROLLER BOARD SETUP

Reference Figure 4-1 for the location of all controller PCBA switches referred to in the paragraphs below.

4.3.1 Number of DH11 Emulations

The number of DH11 emulations is selected by SW1 in accordance with Table 4-1. Each 16 line CP11 distribution panel (even if only eight lines are installed) represents one DH11; consequently, the number of emulations equals the number of panels.

Table 4-1
Number of DH11 Emualtions

No. Panels	SW1-3	SW1-2
1	O	O
2	O	C
3	C	O
4	C	C

4.3.2 Q-Bus Starting Address

The DH11 and DM11 Q-Bus addresses are set in accordance with Table 4-2. The DH11 uses the floating address space that begins at 17760010 and it is located after any DJ11s. Each CS01/H2 requires a set of eight word addresses starting with an address which is a multiple of 20_8. All CS01s should have consecutive addresses. Each DJ11 in the system, plus one for the gap to indicate there are no more, requires a starting address which is a multiple of 10_8 starting at 17760010. Therefore, the first CS01/H2 will have a starting address of 17760020 if there are no DJ11s, and a starting address of 17760040 if there are one or two DJ11s.

If more than one DH11 is being emulated, select an initial starting address with enough starting addresses above it for each emulation. The starting addresses will be contiguous. That is, if three CP11 distribution panels are installed (three DH11 emulations, essentially) and the starting address selected is 17760060, then the CC01 controller will also respond to accesses in the address ranges starting at 17760100 and 17760120. The second and third starting addresses represent the second and third DH11 devices that are being emulated.

The starting address for the DM11 is selected by the same switches that select the DH11 address (see Table 4-2). There is a DM11 for each DH11. The DM11 addresses are a multiple of 10_8.

Table 4-2
Q-Bus Starting Address Selection

Address		SW1-	SW4-				
DH11	DM11	4	5	4	3	2	1
17760020	17770500	C	C	O	O	O	O
17760040	17770510	C	C	O	O	O	C
17760060	17770520	C	C	O	O	C	O
17760100	17770530	C	C	O	O	C	C
17760120	17770540	C	C	O	C	O	O
17760140	17770550	C	C	O	C	O	C
17760160	17770560	C	C	O	C	C	O
17760200	17770570	C	C	O	C	C	C
17760220	17770600	C	C	C	O	O	O
17760240	17770610	C	C	C	O	O	C
17760260	17770620	C	C	C	O	C	O
17760300	17770630	C	C	C	O	C	C

Table 4-3
DH11 Vector Address Selection

	SW2-						SW2-				
Addr	5	4	3	2	1	Addr	5	4	3	2	1
300	0	0	0	0	0	500	C	0	0	0	0
310	0	0	0	0	C	510	C	0	0	0	C
320	0	0	0	C	0	520	C	0	0	C	0
330	0	0	0	C	C	530	C	0	0	C	C
340	0	0	C	0	0	540	C	0	C	0	0
350	0	0	C	0	C	550	C	0	C	0	C
360	0	0	C	C	0	560	C	0	C	C	0
370	0	0	C	C	C	570	C	0	C	C	C
400	0	C	0	0	0	600	C	C	0	0	0
410	0	C	0	0	C	610	C	C	0	0	C
420	0	C	0	C	0	620	C	C	0	C	0
430	0	C	0	C	C	630	C	C	0	C	C
440	0	C	C	0	0	640	C	C	C	0	0
450	0	C	C	0	C	650	C	C	C	0	C
460	0	C	C	C	0	660	C	C	C	C	0
470	0	C	C	C	C	670	C	C	C	C	C

Table 4-4
DM11 Vector Address Selection

	SW3-							SW3-					
Addr	6	5	4	3	2	1	Addr	6	5	4	3	2	1
300	0	0	0	0	0	0	500	C	0	0	0	0	0
304	0	0	0	0	0	C	504	C	O	O	O	O	C
310	0	0	0	0	C	0	510	C	O	O	O	C	O
314	0	0	0	0	C	C	514	C	0	0	0	C	C
320	0	0	0	C	0	0	520	C	0	0	C	0	0
324	0	0	0	C	0	C	524	C	0	0	C	O	C
330	0	0	0	C	C	0	530	C	0	0	C	C	0
334	0	0	0	C	C	C	534	C	0	0	C	C	C
340	0	0	C	0	0	0	540	C	0	C	0	0	0
344	0	0	C	0	0	C	544	C	0	C	0	0	C
350	0	0	C	0	C	0	550	C	0	C	0	C	0
354	0	0	C	0	C	C	554	C	0	C	0	C	C
360	0	0	C	C	0	0	560	C	0	C	C	0	0
364	0	0	C	C	0	C	564	C	0	C	C	0	C
370	0	0	C	C	C	0	570	C	0	C	C	C	0
374	0	0	C	C	C	C	574	C	0	C	C	C	C
400	0	C	0	0	0	0	600	C	C	0	0	0	0
404	0	C	0	0	0	C	604	C	C	0	0	0	C
410	0	C	0	0	C	0	610	C	C	0	0	C	0
414	0	C	0	0	C	C	614	C	C	0	0	C	C
420	0	C	0	C	0	0	620	C	C	0	C	0	0
424	0	C	0	C	0	C	624	C	C	0	C	0	C
430	0	C	0	C	C	0	630	C	C	0	C	C	0
434	0	C	0	C	C	C	634	C	C	0	C	C	C
440	0	C	C	0	0	0	640	C	C	C	0	0	0
444	0	C	C	0	0	C	644	C	C	C	0	0	C
450	0	C	C	0	C	0	650	C	C	C	0	C	0
454	0	C	C	0	C	C	654	C	C	C	0	C	C
460	0	C	C	C	0	0	660	C	C	C	C	0	0
464	0	C	C	C	0	C	664	C	C	C	C	0	C
470	0	C	C	C	C	0	670	C	C	C	C	C	0
474	0	C	C	C	C	C	674	C	C	C	C	C	C

4.3.3 Interrupt Vector Address

4.3.3.1 DH11 Vector

The DH11 interrupt vector address is set by the switches in SW2 in accordance with Table 4-3. Each DH11 requires two interrupt vectors. The receiver vector is XX0; the transmitter vector is XX4. The DH11 falls in behind the DC11, KL11, DP11, DN11, DM11, DR11, PA611, DX11, DL11 and DJ11. Remember to count the vectors of the associated DM11s and any other DM11s or DH11s with lower Q-Bus addresses.

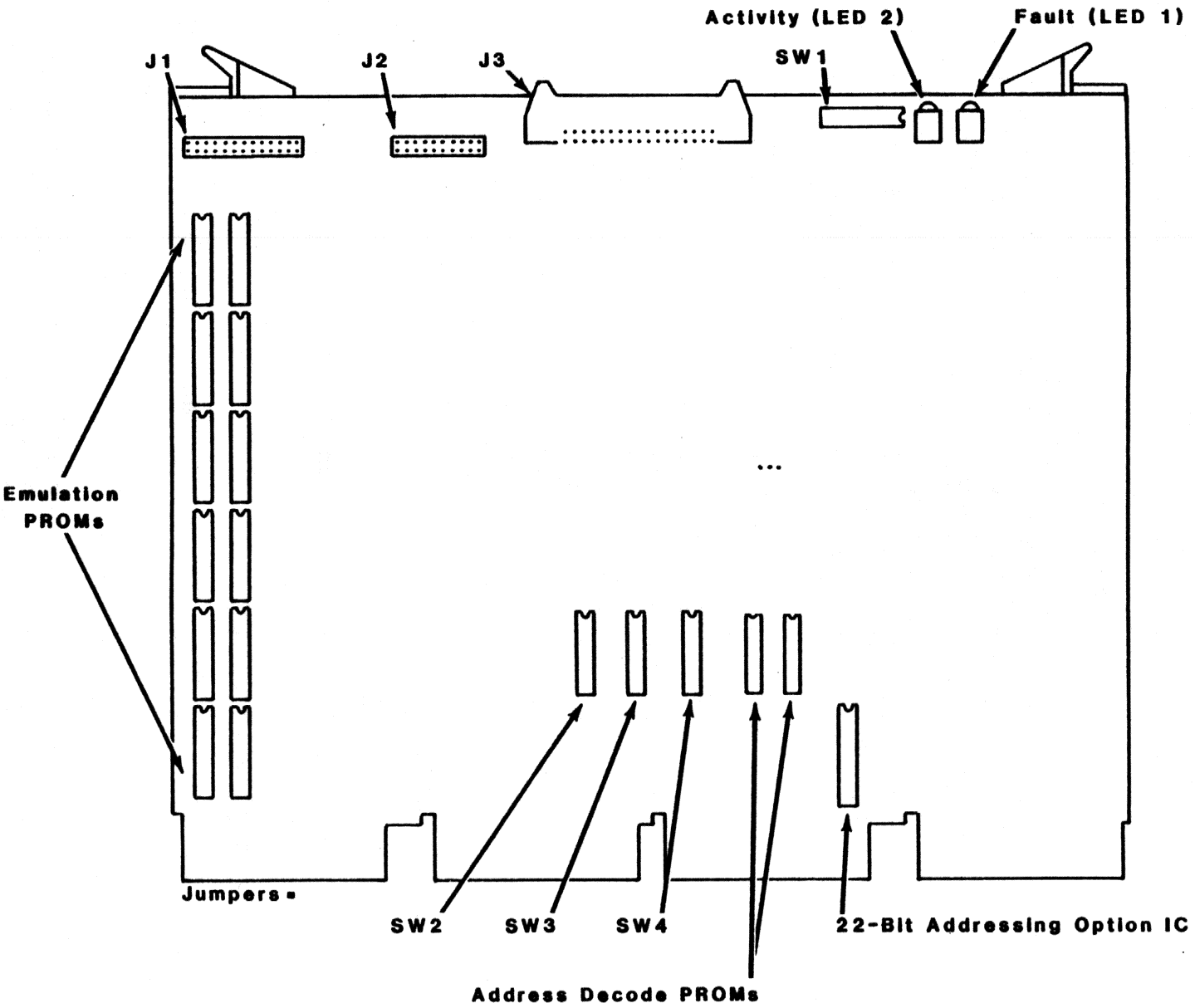


Figure 4-1 CC01 PCBA

4.3.3.2 DM11 Vector

The DM11 interrupt vector address is set by the switches in SW3 in accordance with Table 4-4. Each DM11 requires one interrupt vector. The vector addresses are assigned starting at 300. The DM11 falls in behind the DC11, KL11, DP11 and DN11. Remember to count other DM11s on the bus which have lower Q-Bus addresses.

4.3.3.3 Interleaving DH11 and DM11 Vector Addresses

In order to interleave the DH11 and DM11 interrupt vector address option switch SW1-5 must be closed. When enabling this option, it is important to set the addresses so that they do not overlap. This can be accomplished by setting the first DH11 vector 10_8 higher than the first DM11 vector. Thus, if the first DM11 vector is set at 300, the first DH11 vector must be set at 310, and the second DH11 vector will occupy 314. The next open address is 320, so the DM11 vector will be assigned to that and so on. The chart below provides a sampling of typical interleaved interrupt vector assignments.

DM11	DH11
300	310
	314
320	330
	334
340	350
	354
360	370
	374

4.3.4 Option Selection

4.3.4.1 Option Switches

Reference Appendix A for the selection of options not discussed in the paragraphs below.

4.3.4.2 Extended Silo Option

Setting option switch SW2-7 ON will enable the Extended Silo Option.

4.3.4.3 22-Bit Memory Addressing

Twenty-two bit addressing capability is available as an option for the CS01. The Emulex part number for the option kit is CS0113001. The kit consists of a single AMD2908 IC which is placed in socket U101 on the CS01 PCBA. See paragraph 2.5.2 for programming instructions.

WARNING

Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing a CS01 with the extended addressing option in such a system will damage the option IC. Before installing the option confirm that there is neither positive or negative potential between lines BC1, BD1, BE1, BF1 and logic ground. A CS01 without the addressing option will not be damaged if power is present on those lines.

4.4 CP11 DISTRIBUTION PANEL CONFIGURATION

4.4.1 Panel Numbering

There is no address selection to be done on the CP11 Distribution Panel. Each panel takes on a number corresponding to its position on the daisy-chain cable. The number of CP11 panels is selected by switches SW1-2 and SW1-3 on the CC01 controller PCBA. See Table 4-1 for switch setting information. The switches on the CP11 are not used and should be ignored.

4.4.2 International Power Supply Conversion Instructions

The power supply accompanying your order is wired for 115 v AC. To convert the power supply to 220 v proceed as follows;

1) Make sure the power supply is not plugged in.

2) Replace the existing 1A slow/blow fuse with the enclosed 1/2A slow/blow fuse. The fuse plug is on the left hand side when viewed from the front.

3) Move the slide switch to the 230 v position. The switch is next to the fuse holder.

4) Remove the existing AC plug and replace it with the type desired for your application. The wire coloring code is: green--safety ground; white--neutral; black--AC power.

4.5 LINE ADAPTOR CONFIGURATION

The CA11/H (RS-232-C) has several user selectable options that are effected using a switch and several wirewrap jumpers. The switch is used to select the compatiblity mode of the entire unit (see 4.5.1.1). All of the other available options can be selected for each channel individually by rearranging the jumpers. See Figure 4-2 for the locations of the switches and jumpers on the CA11/H.

The CA11/C (20 mA current loop) Line Adaptor Panels has several user selectable options. All of the options are selected for each

channel individually by rearranging the jumpers. See Figure 4-3 for the locations of the switch and jumpers on the CA11/C.

The following procedure is a general one to be used when reconfiguring either type adaptor. Refer to the appropriate paragraph (below) for specific jumper connections when you reach step 7. When configuring the adaptors for initial installation, only steps 2 through 11 will apply as the distribution panel will not yet have been installed.

1) Unplug the 34-wire ribbon cable from the CP11 Distribution Panel.

2) Turn off the AC power to the Distribution Panel by unplugging the AC line cord.

3) Unscrew the knurled screw at each corner of the adaptor. They need not be completely removed.

4) Grasp the handles in the upper left and right hand corners of the adapter and pull the adapter from the AMP MOD 1 pins on the Distribution Panel.

5) Remove the four screws that hold the two panel handles in place and remove the handles.

6) Unscrew the four counterset screws that hold the face plate on the adaptor PCBA and remove the face plate.

7) Make the wire wrap changes as required.

8) Replace the face plate on the adapter PCBA.

9) Replace the two panel handles.

10) Fit the adapter panel to the AMP pins and press the panel home.

11) Tighten the four knurled screws.

12) Plug in the Distribution Panel's AC line cord.

13) Plug in the 34-wire cable.

14) All of the Adapter Panel LEDs will be lit. Move the LINE TEST slide switch from the OFF to the INT position and back again. This will cause the controller to test each channel. All of the LEDs should go out.

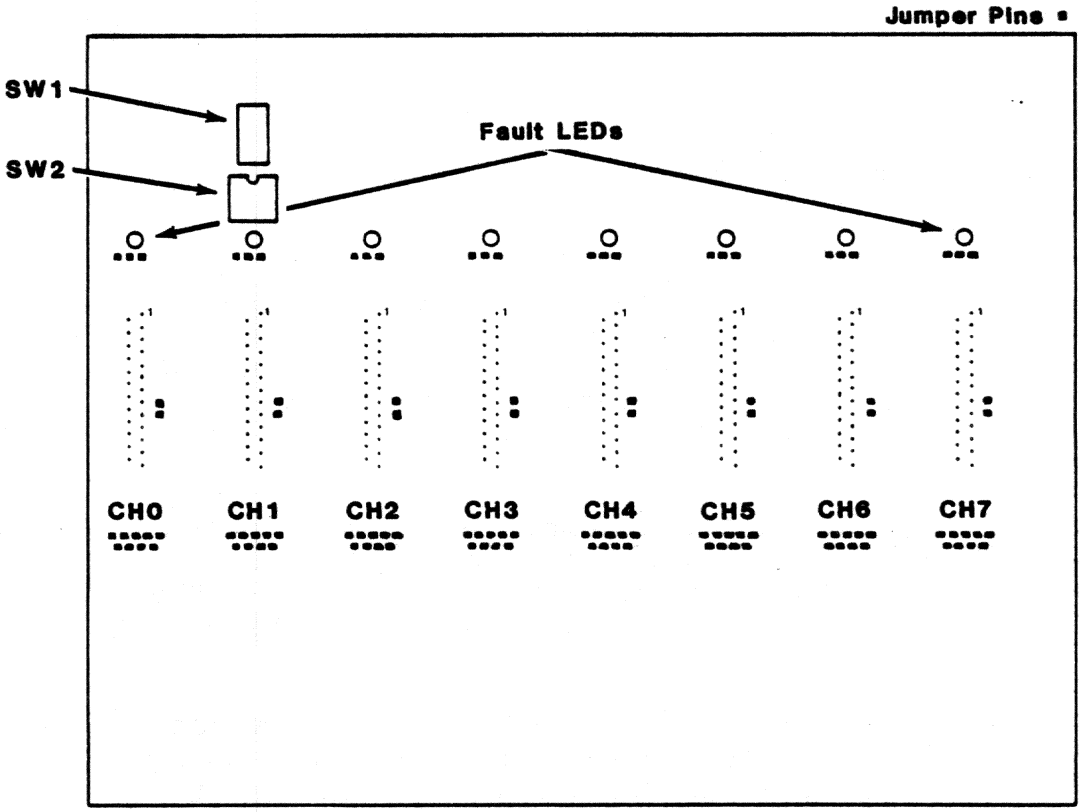


Figure 4-2 CA11/H Line Adapters

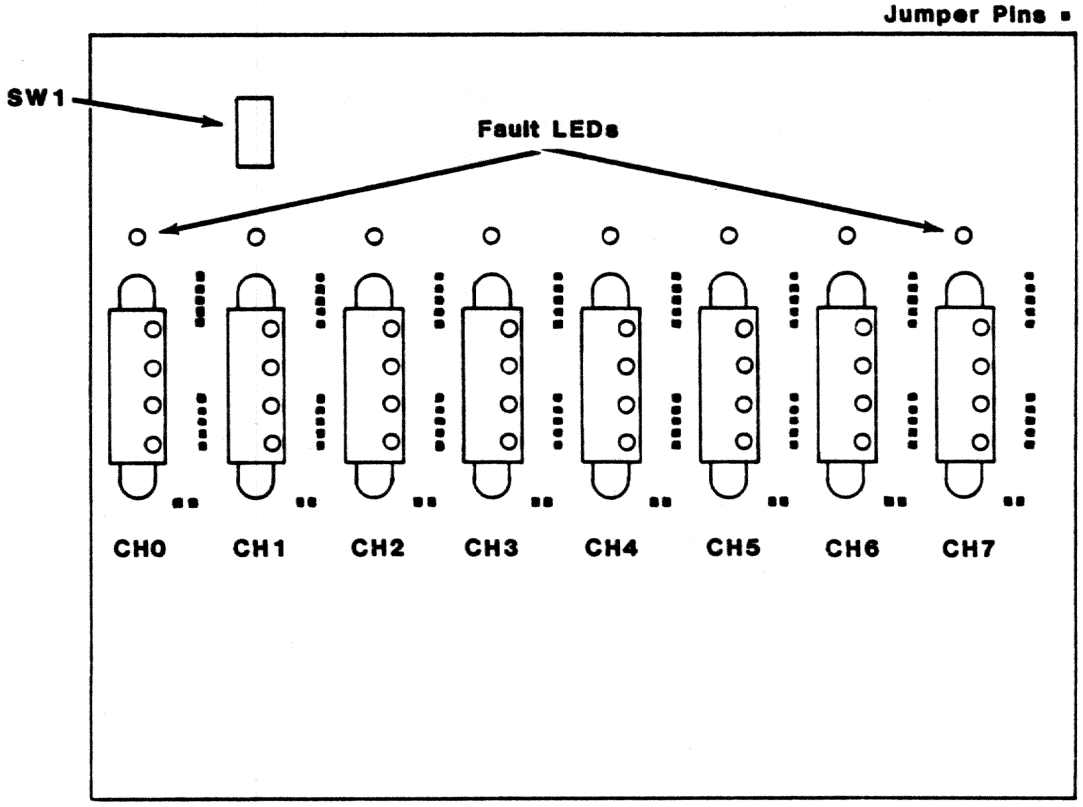


Figure 4-3 CA11/C Line Adapters

4.5.1 CAll/H Option Selection

4.5.1.1 Flow Control Option

If desired, the CAll/H may be configured to use Clear to Send (CTS pin 5) and Carrier Detect (CD pin 8) for flow control as required by some peripheral devices. This is done by opening SW2-2. SW2 is the piano type switch mounted under the face plate on the left edge of the CAll PCBA. If necessary, use a screwdriver to set SW2-2 to the up (open) position.

When in this mode, the UART's transmitter is controlled by the CTS line. When CTS is active (high) the transmitter is enabled. When it is inactive (low) the transmitter is disabled. (The UART will finish transmitting any character it had started before CTS became inactive.)

When this option is enabled, the UARTs receiver is controlled by Carrier Detect (CD). Therefore, if the peripheral can be expected to transmit anything back to the CAll, CD will have to be biased active (high) in order to enable the receiver. Generally, one of the signals generated by the peripheral such as Data Set Ready (DSR pin 6) or Data Terminal Ready (DTR pin 20) is always active and can be connected to CD to accomplish this. Also, some devices have +v on pin 9 of the interface. In all cases, the bias should be in the range +15 to +3 v DC with respect to pin 7 (signal gound).

NOTE: SW2-2 selects the flow control option for all eight lines on the adaptor panel. Consequently, if flow control is required on only one port (for a printer, for example), the rest of the lines must have both CTS and CD biased high in order to function.

4.5.1.2 Pinning Assignment Options

The CAll/H is shipped from the factory with the following jumper connections:

Connection	Function
A to B	Connects RING (pin 22) to DSR input on UART.
Y to X	Connects baud rate generator to external clock input on UART.
R to P	Connects RTS output on UART to pin 4.
S to T	Connects Sec TX output to pin 11.

To effect one of the following options, reconfigure the wirewrap jumpers as indicated for that option. Each channel is reconfigured separately.

1) RS-232 Secondary Receive and Secondary Transmit (pins 16 and 14, respectively) rather than Bell 202C pinning assignments: Remove S - T; Jumper S - J; Jumper U - G on back of board (cut etch H - G if necessary to isolate pin 12).

2) Substitute Data Set Ready for Ring: Remove B - A; Jumper C - A.

3) For 103 E,G,H,J modems, connect Busy (pin 25) with RTS (pin 4): Jumper R - L.

4) For 212 A modems, connect Make Busy (pin 18) with RTS (pin 4): Jumper R - N.

5) Connect 811B Received Signal Element Timing, pin 17, to Secondary Receive: Jumper F - G and cut etch E - D on back of board.

4.5.2 CAll/C Option Selection

The standard jumper connections are:

Connection	Function
A-B, C-D	Active transmitter, active receiver, 12 vDC

To effect one of the following options, reconfigure the wirewrap jumpers as indicated for that option. Each channel is reconfigured separately.

1) Long Line (L.L.) transmit option (active, 24 vDC): Remove C - D; Jumper D - E.

2) Long Line (L.L.) receive option (active, 24 vDC): Remove H - J; Jumper J - K.

3) Passive transmit option (passive operation reverses indicated terminal polarity): Remove A - B, C - D (or D - E); Jumper A - D.

4) Passive receive option (passive operation reverses indicated terminal polarity): Remove F - G, H - J (or J - K); Jumper F - J.

5) Install Receive Filter: Jumper L - M.

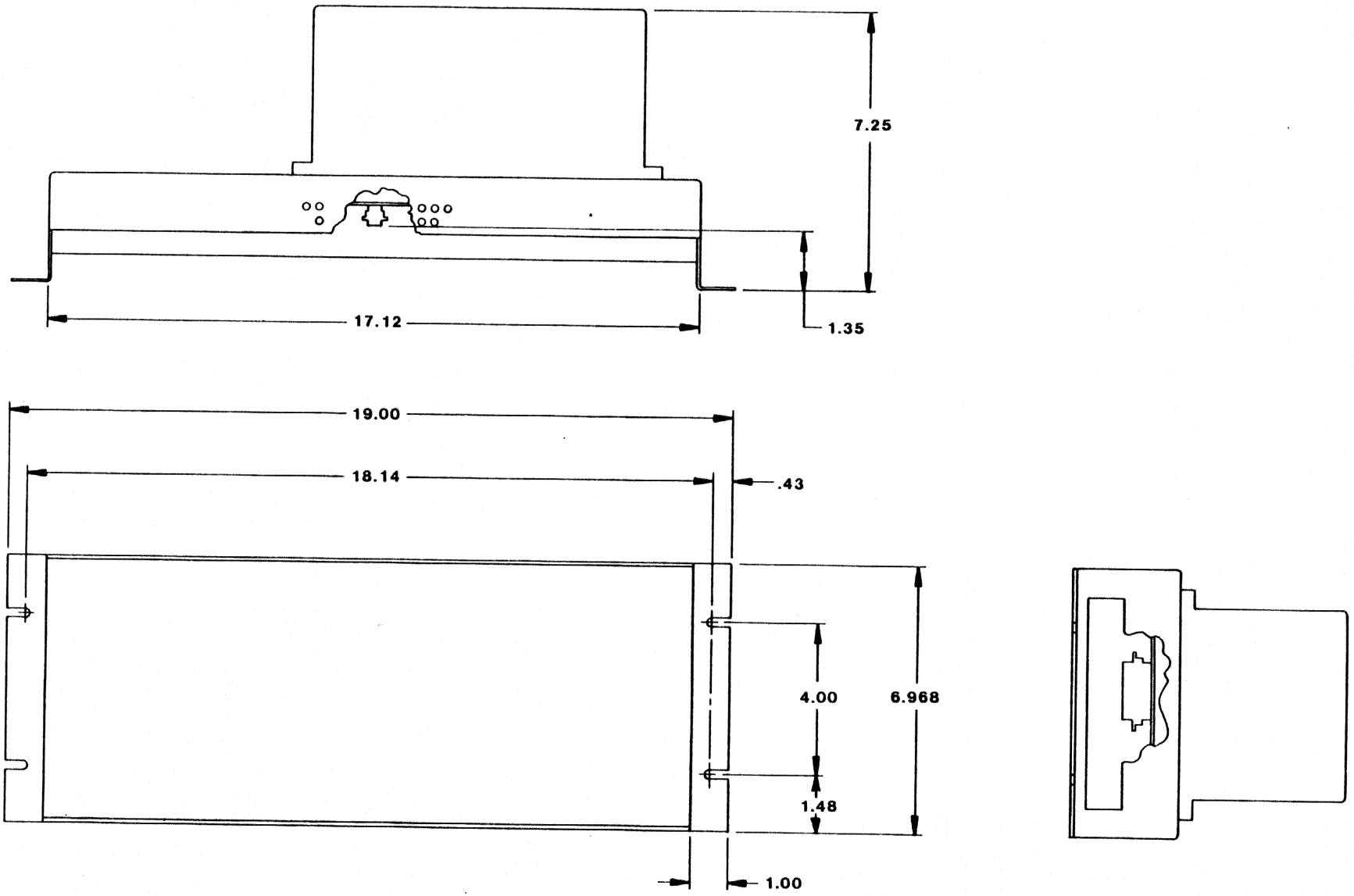


Figure 4-4 Distribution Panel Physical Dimensions

4.6 CP11 DISTRIBUTION PANEL INSTALLATION

The distribution panels can be installed with the line adapters in place. See Figure 4-4 for panel dimensions pertinent to mounting.

The distribution panels are usually mounted to the RETMA rails of a rack or cabinet. The panel is recessed so that the connectors and their cables do not get in the way of the door or side panel of the cabinet.

NOTE: If a panel is not to be mounted in the cabinet with the controller, then the panel case must be connected to the CPU cabinet by a ground strap.

4.7 CC01 CONTROLLER INSTALLATION

4.7.1 Slot Selection

The controller board may be placed in any slot in the LSI-11. The controller should be placed fairly close to the CPU so as to give it higher interrupt priority than other devices even though it does not need a high NPR priority. In all cases, Emulex disk controllers should be after the CC01 since they have a large amount of buffering.

4.7.2 Controller Mounting

The controller board should be plugged into the Q-Bus backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the board with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly in the throat of the connector before attempting to seat the board by means of the extractor handles.

4.8 CABLING

4.8.1 Controller to Distribution Panel

A 34-conductor flat cable daisy-chains between the CC01 controller and the distribution panels. The cable plugs into J1 on the controller with pin 1 on the top (front) of the board. The pin 1 of the cable connector has a notch on the body to identify it. Also, the pin 1 edge of the cable has a black stripe.

The cable from the controller plugs into the top connector (J1) on the back of the distribution panel. If only one panel is to be used with the controller, the terminator plug is inserted into the bottom connector (J2). If more than one panel is to be used, a cable is plugged into J2 and connected to J1 of the next panel. The terminator card must be plugged into J2 of the last panel.

The panels are assigned addresses based on their order on the cable. The first panel will be the DH11 with the lowest Q-Bus address, the next panel will have the next higher Q-Bus address, etc.

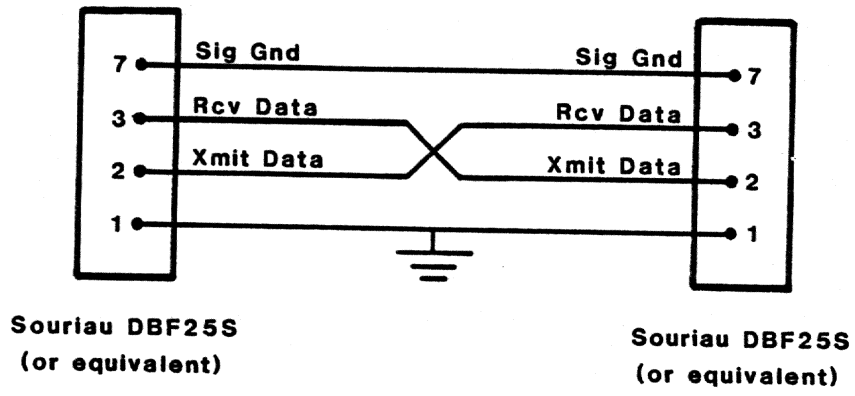


Figure 4-5 Terminal Cable Schematic

4.8.2 CA11/H Line Adaptor to External Device

The CS01 communications multiplexer is used to provide communications between the host CPU and up to 64 external devices through individual ports. The external devices can be of various sorts, but they can be roughly grouped into two classes: local (no modem control signals required) and remote (modem control signals required).

4.8.2.1 Cable Types

Devices that are in the local class (terminals, printers) can be connected to a port using a simple four wire-cable called a terminal cable. A schematic of the standard DEC cable for local devices is shown in Figure 4-5.

Devices that are in the remote class (modems, other computers) require cables that can carry the modem control signals. Figure 4-6 is a schematic of a modem cable.

The CS01 hardware is unable to make the distinction between local and remote devices. The host operating system is told whether to use the remote or local mode for each line. If this is impractical because modems are constantly being moved from one line to another, then the remote mode is often specified for all of the communications ports. In such cases, the four-wire cable described for local devices will not work because the software will generate

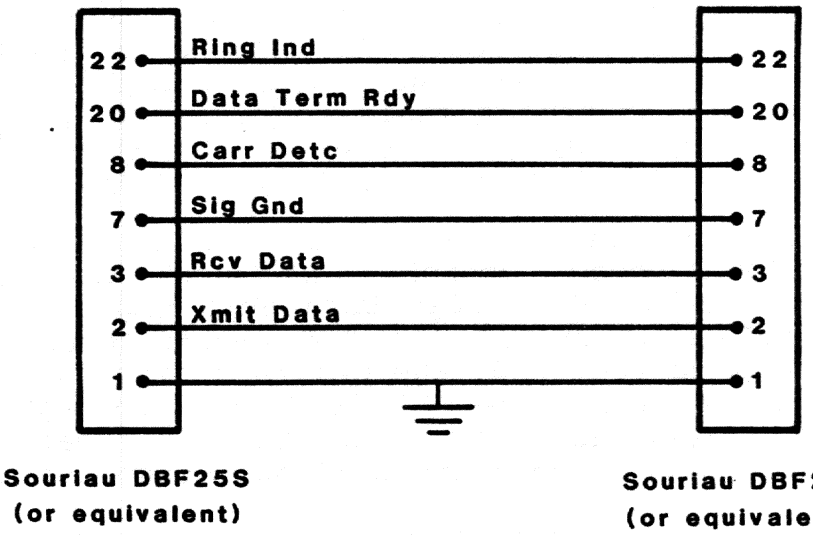


Figure 4-6 Modem Cable Schematic

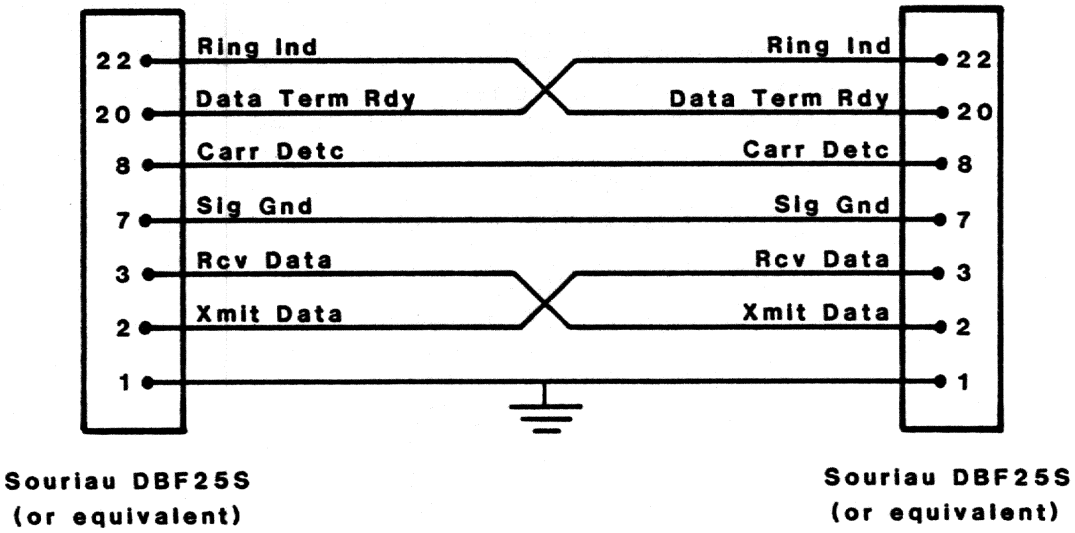


Figure 4-7 Null-Modem Cable Schematic

modem control signals and expect to receive the correct responses in return. Thus, devices that would normally be in the local class are connected to their ports using null-modem cables. These cables interconnect the modem control signals to give the software the illusion that it is talking to a modem. The standard DEC null-modem cable is shown schematically in Figure 4-7.

The standard CA11/H interface pinning assignments are the same as DEC's DH11 with DM11 modem control. As such, the pinning assignments are those for Bell 202C Data Sets (modems). The CS01/H2 may be used as delivered with DEC equipment and software. If a different modem is required, the CA11/H's pinning assignments may be changed as needed. See CA11/H Option Configuration, paragraph 4.5.1, for instructions. Note, however, that DEC software drivers may not support the optional modem configurations.

If any alternate pinning assignments described in paragraph 4.5.1 are used, the cables described above may not work.

4.8.2.2 Cable Lengths

The EIA RS-232-C interface standard to which the CS01 conforms guaranties error free transmission over cables of no longer than fifty feet. EMULEX DOES NOT WARRENTY OPERATION OVER CABLE LENGTHS GREATER THAN 50 FEET IN ANY CIRCUMSTANCES. However, satisfactory performance over cables of several thousand feet in length can be obtained depending on the speed of data transmission required and the environment in which the cable is placed. Emulex offers the following table as a guide for the pratical application of the CS01.

NOTE: The ground potential difference between the CS01 and terminal must not exceed 2 v. This requirement will generally limit operation without modems to within a single building served by one AC power service. In other cases, or in noisy electrical environments, 20 mA operation should be considered.

Table 4-5
RS-232-C Cable Lengths

Baud	Shielded[1] (in feet)	Unshielded[2] (in feet)
110	5000	3000
300	5000	3000
1200	3000	3000
2400	1000	500
4800	1000	250
9600	250	250

[1] Cable is two, 22 AWG twisted pairs shielded in Belden 8777 (three pair). Shields tied to ground.
[2] Cable is 22 AWG 4-conductor (quad) inside station wire.

4.8.3 CAll/C Line Adaptor to External Device

The CAll/C provides 20 mA current loop interface for use with older teletype-style equipment or in environments with a great deal of electrical noise.

4.8.3.1 Cable Type

The CAll/C comes configured with active transmitters and receivers. As such, each device with which the CAll/C interfaces must have a passive transmitter and receiver. Determine whether or not individual devices have active or passive interfaces by consulting the manual for that device. If a device has an active transmitter and/or receiver, the CAll/C may be reconfigured for passive operation as described in paragraph 4.5.2.

NOTE: When passive operation is selected for a CAll/C channel, THE TERMINAL POLARITY IS REVERSED from that which is printed on the CAll/C's face.

When connecting a device to an adaptor channel, these rules must be followed. Remember, if a channel receiver and/or transmitter has been reconfigured for passive operation, the polarity of the terminals will be reversed.

1) The T+ terminal of the CAll/C is connected to the R+ terminal of the slave device.

2) The T- terminal of the CAll/C is connected to the R- terminal of the slave device.

3) The R+ terminal of the CAll/C is connected to the T+ terminal of the slave device.

4) The R- terminal of the CAll/C is connected to the T- terminal of the slave device.

4.8.3.2 Cable Length

No definitive 20 mA current loop specification exists. The length of cable that may be used is a function of electrical noise, loop resistance, cable type and speed of operation. The following table is given as a practical guide to the cable lengths that can be used with the CAll/C adaptor panel; however, there is no guarantee of error free operation under all circumstances.

Table 4-6
20 mA Current Loop Cable Lengths

Baud	Shielded[1] (in feet)	Unshielded[2] (in feet)
9600	500	1000
4800	1000	1800
2400	2000	3000
1200	4000	5000

[1] Belden 8777, 22 AWG, shielded, twisted pairs (sheild floating).
[2] 22 AWG, 4 conductor inside station wire.

4.9 VERIFICATION

4.9.1 Self-Test

When power is applied to the CPU, the controller will automatically execute a built-in self-test. The test is not executed with every bus INIT but only on powering-up. If the self-test has been executed successfully, the Fault LED on the top edge of the board will be off. If the LED is ON, the controller did not pass its self-test and the controller cannot be addressed from the CPU.

In addition to the controller self-tests executed when powering-up, the electronics associated with each line on the distribution panel and each line adaptor are tested. If any failures occur, the LED above the faulty line or lines will remain ON. LED1 on the CC01 will also be ON in the event of a line failure. If the overide switch (SW1-6) is OFF and a fault is detected with one of the lines, the controller will hang. If the override switch is ON, the Fault light above the bad channel will still come ON, but the controller will not hang. In this mode LED1 will not come ON.

NOTE: If any distribution panel has only one line adaptor (eight lines), then the controller will detect a line adaptor fault. If such a configuration is used, the override switch must be on to prevent the controller from hanging.

The override switch has nothing to do with the controller's own self-test. That is, if the controller detects a fault in itself, it will hang regardless of the override switch's position.

4.9.2 Register Examination

After powering-up the CPU and noting that the FAULT indicator is not ON, a quick check should be made to insure that the controller registers can be read from the computer console. This can be done by depositing 177777 in location SCR + 10 (BCR) and then examining the location for 177777.

4.9.3 Line Adaptor Wrap-Around Test

The CC01 controller is capable of running both internal and external wrap-around tests for each channel that is connected to it. For both the CA11/H and the CA11/C Line Adaptors, the internal wrap-around tests are performed during the controller power-up self-test. If desired, both the internal and external wrap around tests may be initiated on a adaptor-by-adaptor basis by the slide switch located on each adaptor panel. The internal test should be run during verification. The external test need only be run if a fault is suspected. The following paragraphs describe the test procedure for both Line Adaptors.

4.9.3.1 CA11/H Tests

1) Internal Wrap-Around Test: The internal wrap-around test is run by simply placing the slide switch in the INT position for each adaptor panel that is to be tested. The controller will then select a loop-back data path, transmit a character, and then read the receive buffer to verify that the data has been received correctly. If an error is detected, the LED above the faulty channel will be illuminated. The controller will do this continuously, one character at a time. If the error is intermittent, the LED will flicker on and off. If a hard error occurs, the LED will remain illuminated after the slide switch is returned to the OFF position.

   This test may be run without affecting the operation of any other adaptor. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

2) External Wrap-Around Test: The line receivers and drivers are not tested by the internal loopback test. If such a fault is suspected, the external wrap-around test will detect it.

   There are two kinds of external tests, both executed with the slide switch in the EXT position. When the microcode detects the presence of a wrap-around connector, it will run the second of the two tests on that particular line.

   The first test causes the line adaptor to echo characters received from a terminal at 9600 baud back to that terminal. A fault within the terminal, the connecting cable or the Line Adaptor will cause the character to be echoed incorrectly or not at all.

   Once the identity of the faulty line has been determined, the second external test can be executed to further isolate the fault. Unplug the line from the adaptor panel that is to be tested. The controller will then transmit a character out each line driver, and it will expect to see a character

looped back through the respective line receiver. Because no loop back path has been provided, the fault LED will be illuminated. Plug the H315 wrap-around connector (see 4.9.6) that is provided with the CS01 into the channel. While the connector is in place, the LED above that channel should go out. If it does not, there is a problem with that channel.

If one of the channels has failed the external test yet passes the internal test, then the problem is either the line driver or receiver for that channel. This test may be run without affecting the operation of any other adaptor. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

4.9.3.2 CAll/C Tests

1) Internal Wrap-Around Test: The internal wrap-around test is run by simply placing the slide switch in the INT position for each panel that is to be tested. The controller will then select a loop-back data path, transmit a character, and then read the receive buffer to verify that the data has been received correctly. If an error is detected, the LED above the faulty channel will be illuminated. The controller will do this continuously, one character at a time. If the error is intermittent, the LED will flicker on and off. If a hard error occurs, the LED will remain illuminated after the slide switch is returned to the OFF position.

This test may be run without affecting the operation of any other adaptor panel. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

2) External Wrap-Around Test: The line receivers and drivers are not tested by the internal loopback test. If such a fault is suspected, the external wrap-around test will detect it.

There are two kinds of external tests, both executed with the slide switch in the EXT position. When the microcode detects the presence of a loop-back data path, it will run the second of the two tests on that particular line.

The first test causes the line adaptor to echo characters received from a terminal at 9600 baud back to that terminal. A fault within the terminal, the connecting cable or the Line Adaptor will cause the character to be echoed incorrectly or not at all.

The second test uses a loop-back data path from the transmit to the receive terminals of a given channel to test that

channels line drivers and receivers. However, to perform the test, either the line driver or receiver must be configured for passive operation while the other is configured for active operation. Reconfiguring a driver or receiver is somewhat involved. Consequently, it is recommended that the character echo test be performed a second time on a channel that is suspected of being faulty using a different terminal and line. If the channel still fails the character echo test with the new terminal and line, then the problem is probably in the Line Adaptor. If performance of the loop-back test is convenient, the procedure is outlined below.

Before running the external test, either the receiver or transmitter for each channel to be tested must be in the passive configuration. Follow the procedure in paragraph 4.5.2 to reconfigure one of the drivers. Also, the receiver filter must not be connected for external loop back testing.

After either the transmitters or receivers have been reconfigured for passive operation, the transmit and receive line for each channel must be connected together. Regardless of which half of the channel is active or passive, connect the two outermost terminals one another and the two innermost terminals to one another. Do this for each channel to be tested. Place the slide switch in the EXT position. The controller will then continually transmit characters out the line drivers, and it will expect to see the characters looped back through the line receivers. All of the LEDs should remain unlit. If one does not, there is a problem with that channel.

After the test has been completed, return the channels to their original configurations. Place the slide switch in the INT position to reset the LEDs. If one of the channels has failed the external test yet passes the internal test, then the problem is either the line driver or receiver for that channel.

This test may be run without affecting the operation of any other adaptor. That is, the system need not be taken down to run this test. If a fault is detected, the controller will not hang.

4.9.4 Mini-Test

If diagnostics are not available or it is decided not to run them, it is possible to prove out the NPR function which is not checked by the self-test, by running the following simple procedure from the CPU console:

1) Deposit 000400 into memory location 0; deposit 000377 into location 2.

2) Deposit 004000 into SCR location to clear controller.

3) Deposit 001000 into SCR location to set Maintenance Mode to achieve wrap-around. Could use different line number here.

4) Deposit 033503 into SCR + 4 location (LPR).

5) Deposit 000000 into SCR + 6 location (CAR).

6) Deposit 177775 into SCR + 10 location (BCR).

7) Deposit 000001 into SCR + 12 location (BAR) to enable line 0 transmitter.

8) Examine location SCR + 2 (RCR) four times and check the following:

   100000 100001 100377 000377

9) Examine SCR and the following seven locations and check for the following:

   101000 000377 033503 000003 000000 000000 000000 000000

The above procedure performs a transmission of three characters in wrap-around mode on line 0. Another line could be used. The silo is read out by examining RCR to see that the characters were transmitted and received properly.

4.9.5 Diagnostics

The ZDHM diagnostic should be run to insure that the controller and all the lines are operational. This program is a very comprehensive diagnostic and includes most of the functions of the other diagnostics. Instructions for running this program can be found in Appendix B. Patches for running this program with the Expanded Silo option can be found in Appendix C.

4.9.6 Test Connector

The diagnostics and the online "Line Test" activated by the Line Adapter Board slide switch require an H315 type wrap-around connector. One connector is supplied with each panel and a full set of 16 can be ordered from Emulex. The standard DEC H315 must have a jumper added from pin 4 to pin 6 if Data Set Ready is being used rather than Ring. The H315 connector has the following connections:

2 - 3	Tx Data - Rx Data
11 - 12	Sec. Tx Data - Sec. Rx Data
20 - 5 - 8	DTR - CTS - Carrier
4 - 22 - 6	RTS - Ring - DSR

Appendix A

CONTROLLER OPTION SWITCHES

A.1 CC01 CONTROLLER PCBA

TABLE A-1
DISTRIBUTION PANEL

Option Sw	Open	Closed	Function
SW1-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW1-2			Number of CP11 Panels[2]
SW1-3			Number of CP11 Panels[2]
SW1-4			DH11/DM11 Starting Address[4]
SW1-5	Disable	Enable	Interleave DH and DM vector locations
SW1-6	Halt	Override	Override power-up line test failures (if this switch is open, the controller will hang with the FAULT LED ON if any line fails)[3]
SW1-7	Disable	Enable	Force two Stop Bits on all lines
SW1-8	18 BIT	22 BIT	ADDRESSING MODE

[1]
[2]All unused switches MUST BE OFF.
[3]See Table 4-1.
[4]See paragraph 4.9.1.
[4]See Table 4-2.

TABLE A-2
INTERRUPT VECTOR SELECTION

Switch	Open	Closed	Function
SW2-1			DH11 Vector Address[2]
SW2-2			DH11 Vector Address[2]
SW2-3			DH11 Vector Address[2]
SW2-4			DH11 Vector Address[2]
SW2-5			DH11 Vector Address[2]
SW2-6	2K	1K	PROM Address Range[3]
SW2-7	Disable	Enable	Expanded Silo
SW2-8			Not used[1]

[1]
[2]All unused switches MUST BE OFF.
[3]See Table 4-3 for settings.
[3]Must be open (OFF).

TABLE A-3
DISTRIBUTION PANELS

Switch	Open	Closed	Function
SW3-1			DM11 Vector Addresses[2]
SW3-2			DM11 Vector Addresses[2]
SW3-3			DM11 Vector Addresses[2]
SW3-4			DM11 Vector Addresses[2]
SW3-5			DM11 Vector Addresses[2]
SW3-6			DM11 Vector Addresses[2]
SW3-7			Not used[1]
SW3-8			Not used[1]

[1]All unused switches MUST BE OFF.
[2]See Table 4-4 for settings.

TABLE A-4
CONTROLLER STARTING ADDRESS

Switches	Open	Closed	Function
SW4-1			DH11/DM11 Starting Address[2]
SW4-2			DH11/DM11 Starting Address[2]
SW4-3			DH11/DM11 Starting Address[2]
SW4-4			DH11/DM11 Starting Address[2]
SW4-5			DH11/DM11 Starting Address[2]
SW4-6			Not used[1]
SW4-7			Not used[1]
SW4-8			Not used[1]

[1]All unused switches MUST BE OFF.
[2]See Table 4-2 for settings.

A.2 CA11/H LINE ADAPTER

TABLE A-5
LINE TEST SWITCH

Switches	Open	Closed	Function
SW1			Online Self-Test[2]

[2]See paragraph 4.9.3

TABLE A-6
OPTION SWITCHES

Switches	Open	Closed	Function
SW2-1			Not used[1]
SW2-2	Enabled	Disabled	CTS/CD Flow Control
SW2-3			Not used[1]
SW2-4			Not used[1]

[1] All unused switches MUST BE OFF.

BLANK

Appendix B

ZDHM DIAGNOSTIC

B.1 GENERAL DESCRIPTION

ZDHM is a comprehensive diagnostic test program designed to aid in the acceptance testing, installation checkout, and corrective maintenance of the DH11 16 line asynchronous serial line multiplexer. It consists of 48 logically sequenced diagnostic tests designed to test and verify that the DH11 is operating in accordance with its design specifications.

The program is configurable by the autosizer or by console dialogue to enable it to automatically test and verify all 16 lines on up to 16 contiguous DH11s (with non-contiguous/contiguous vector assignments). Individual units and individual lines within a unit may be selected or deselected to facilitate fault isolation to a particular DH11 or a functional area of logic affecting a particular line within a unit. Whenever an error is detected, a comprehensive error report is typed that allows the user to isolate the fault to a functional area of logic. Extensive documentation is provided to permit the user to proceed from the error report to additional logic checks in order to isolate the problem to a replaceable unit.

In order to facilitate installation checkout, tests 101 and 105 through 107 (test group 1) of the modem control diagnostic, ZDHK, have been included in this program. In this way, all the level converters and cables can be checked with just one program using the H315 turnaround connector.

NOTE 1: The H315 turnaround connector must be installed on any line under test when running ZDHM. As described in Section B.2.1, lines may be selected and tested on an individual basis.

NOTE 2: The ZDHM diagnostic will not consistantly run error free if a distribution panel contains only one of the eight-line adaptor panels. The procedure for testing a distribution panel with this configuration is to temporarily place another eight-line adaptor in the panel. This problem is caused by the diagnostic's assumption that each DEC DH11 is equiped with 16 lines. The diagnostic expects certain modem status information from every line even though all of the lines might not be selected for testing.

B.2 LOADING PROCEDURES

There are several different methods for loading the DH11 diagnostics under the control of the XXDP diagnostic monitor. The following procedure is common to many DEC systems and similar to others.

1) Mount the appropriate medium (Dectape, disk, etc.) containing the XXDP monitor and ZDHM.

2) Boot the system to load the monitor.

3) Once loaded the XXDP monitor prints an introductory message and displays a period (.) to indicate that it is ready to accept commands.

4) Type "L ZDHMD0." This will cause the diagnostic to be loaded, but it will not be started.

B.3 STARTING PROCEDURES

The console switch register is used to select between DH11 diagnostic program options. The program can also be started at different locations to allow it to be rerun without having to reenter the DH11 parameters.

B.3.1 Program Options

The CPU switch register (SR) is used to allow the user to select between several program options. The 16 bits of the register represent different options during program start than they do during testing (SR = switch register).

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SR	SR	SR	SR	SR	SR	SR	SR	SR	SR	SR	SR	SR	SR	SR	SR

Switch Reg.	Start	Testing
Bit 15 = 1	No function.	Halt on error (after typing message).
Bit 14 = 1	No function.	Loop continuously on current test.
Bit 13 = 1	No function.	Inhibit error typouts.
Bit 11 = 1	No function.	Inhibit sub-test iterations (quick pass).
Bit 10 = 1	No function.	Inhibit modem control on abbreviated test.
Bit 09 = 1	No function.	Lock on hard errors.

Bit 08 = 1	Halts after configuration to permit dumping pre-configured copies of the program.	Search for and lock on test selected by the contents of SR <07:00>.
<07:00>	See below for <01:00>	Contains test number to search for when SR 08 = 1.
Bit 01 = 1	Types device map generated by the auto-sizer.	
Bit 00 = 1	Allows the user to input DH parameters manually. (inhibits the autosizer).	

B.3.2 Normal Program Start At 200

After loading diagnostic, start execution at 200_8. Set SR bit 0 OFF if autosizer is to be used and set it ON if the operator is to enter the parameters. The operator should respond as indicated to the following questons asked by the program:

- Number of addresses between vectors - Enter 10_8 for standard DH11's with contiguous vectors; enter 20_8 if the DM11 vectors are interleaved with the DH11 vectors. The default value is 20_8.
- Device address - Enter the octal address of the first DH11 in the system.
- Vector address - Enter the octal receiver vector address for the first DH11 in system.
- DH11 device selection - Type in a six digit octal number encoded as follows (setting bit 15 to one causes device 15 to be tested, setting bit 13 to one causes device 13 to be tested, setting bit 10 to zero causes device 10 to be ignored, etc.):

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DH	DH	DH	DH	DH	DH	DH	DH	DH	DH	DH	DH	DH	DH	DH	DH

A value of 177777_8 will test all DH11's. The default is 177777_8. (DH = Device)

- Line selection - Type in a six digit octal number encoded as follows (setting bit 15 to one causes line 15 of all selected devices to be tested, setting bit 13 to one causes line 13 of

all selected devices to be tested, setting bit 10 to zero causes line 10 to be ignored, etc.):

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN	LN

A value of 177777_8 will test all lines. The default is 177777_8. (LN = Line)

B.3.3 Default Parameter Start At 204

When starting at 204_8, the program will default to the parameters used in the previous execution. It should not be used for the first execution. The SR should be set for testing at the time the program is started.

B.3.4 Line and Device Parameter Change Start At 210

When the program is started at 210_8, it will ask the last two (parameter setting) questions of the input dialogue described above. Set the SR for testing.

B.3.5 Switchless CPU

If the diagnostic is run on a CPU without a Switch Register, then a software switch register (location 176) is used which allows the user the same switch options.

When SR values are needed the program types out the current value of the SR and asks for new values by typing NEW=. A control G will allow the user to change the contents of the software switch register.

Note: After typing control G, it may be necessary to wait up to 30 sec for the diagnostic to respond. This is because the diagnostic allows SR changes only after completion of each of the 48 subtests.

B.4 TEST SUMMARY

1	Check SSYN response from all DH11 registers.
2	Test that Master Clr can clear the SCR, LPR, BKR, SSR regs
3	Test SCR register R/W bits can set CLR (normal mode)
4	Test SCR register read-only bits (normal mode)
5	Test SCR register bits that can be Set/Clr in maint. mode
6	Test that all R/W bits in LPR can be set/clr
7	Test that all R/W bits in BKR can be set/clr
10	Test that all R/W bits in SSR can be set/clr
11	Test that Clr/Set bit N in LPR doesn't clear any other bits
12	Test that Clr/Set bit N in BKR doesn't clear any other bits
13	Test that Clr/Set bit N in SSR doesn't clear any other bits
14	CAR memory addressing test
15	BCR memory addressing test
16	CAR register test - all 1's / all 0's - all lines
17	BCR register test - all 1's / all 0's - all lines
20	CAR memory patterns test / 0's disturb
21	BCR memory patterns test / 0's disturb
22	CAR memory patterns test / 1's disturb
23	BCR memory patterns test / 1's disturb
24	Test that CAR memory ext bits Set/Clr properly
25	Test intr. enable bits - intr. condition disabled
26	Test char. available i.e., with intr. condition active
27	Test silo overflow i.e., with intr. condition active
30	Test NXM i.e., with intr. condition active
31	Test XMITTR done i.e., with intr. condition active
32	Transmitter NPR logic test 1
33	Transmitter NPR logic test 2
34	Test that character available can cause RCVR interrupt
35	Test that the silo status register counts up correctly
36	Test that silo status register down counts correctly
37	Test silo alarm level for counts 0,1,2,4,8,16, and 32
40	Transmitter timing test - all selected lines - all speeds
41	Receiver timing test - all selected lines - all speeds
42	Verify storage overflow-non maint mode-all selected lines
43	Basic data test - all selected lines/all character lengths
44	Single line data test - all selected lines
45	Basic parity logic test - all selected lines - odd parity
46	Multi-line parity data test - all selected lines
47	Auto-echo test 1 - all selected lines
50	Auto-echo test 2 - all selected lines
51	Auto-echo test 3 - all selected lines
52	Break bit test - all selected lines
53	Half-duplex test - all selected lines
54	Verify that overrun can set properly - all selected lines
55	Abbreviated modem control diagnostic (ZDHK T101)
56	Modem control diagnostic continued (ZDHK T105)
57	Modem control diagnostic continued (ZDHK T106)
60	Modem control diagnostic continued (ZDHK T107)

B.5 ERROR HEADER MNEMONIC DEFINITIONS

All numbers printed as error data are in octal

(PC)	Address of the error call (error PC)
(PS)	Contents of the PSW at the time of the error
(SP)	Contents of the stack pointer at the time of the error
TEST	Test number
DEVADR	Device address - lst address in the selected DH11
REGADR	Address of the DH11 register being tested
WAS	What the actual data read was (DH11 register or memory location)
S/B	What the data read should have been
SPEED	Speed code in the LPR register at the time of error
TIMEB	Contents of software counter used in timing tests
TIMEC	contents of software counter used in timing tests.
CHRLNG	Character length code in the LPR at the time of the error 00=5 bits, 01=6 bits, 02=7 bits, 03=8 bits
TRPPC	Contents of the PC (R7) at the time of a bus error or RSVD instruction trap
TRPPS	Contents of the PSW at the time of a bus error or RSVD instruction trap
(LPRG)	Contents of the LPR register at the time of the error
LINACT	Flags used by multi-line tests to indicate active lines
WASADR	Memory address of the WAS data (actual data read)
SBADR	Memory address of the S/B data (good data)
SCRWAS	Contents of the SCR register
SCRS/B	What the contents of the SCR register should have been
LINCHK	Line no. being checked during CAR and BCR memory tests
LINEWR	Line no. being written into during CAR and BCR tests
PATTRN	Test pattern being written into CAR or BCR memories

Appendix C

EXPANDED SILO OPTION

C.1 GENERAL DESCRIPTION

As described in Section 2.4.1.3, each DH11 contains a 16-bit wide by 64 word deep silo. The amount of storage in this silo may be doubled to 128 words by closing the Expanded Silo option switch SW2-7 (see Appendix A). Using this option has the advantage of doubling the latency time available before a receiver interrupt must be serviced.

The ZDHM diagnostic test program may be run with the Expanded Silo option selected if the program is patched as described below. All subtests which use the Silo Maintenance function to fill the silo are skipped, since there is no Silo Maintenance function for the expanded silo. Other tests are modified as appropriate to handle the increased depth of the silo.

C.2 ZDHM DIAGNOSTIC PATCHES

Location	From	To	Comment
10734	12737	4	Skip Tests 34, 35, 36, 37
10736	10756	4	
10740	1110	4	
10742	13703	137	
10744	27304	11676	
12550	177677	177577	Patch Test 42
12754	77	177	
17322	177674	177574	Patch Test 54
17434	101	201	
17450	101	201	
27672	100077	77	Modify SSR Mask for Read/Write Bits

BLANK

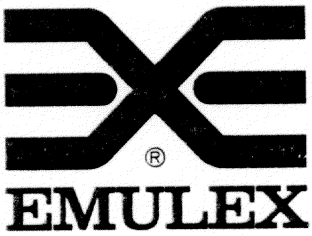
Appendix D

ZDHK PATCHES

The Modem Control Multiplexer Diagnostic requires a minor patch to allow it to run without error. The patch is shown below:

Location	Is	Should Be
3200	5077	137
3202	12332	3266

BLANK



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