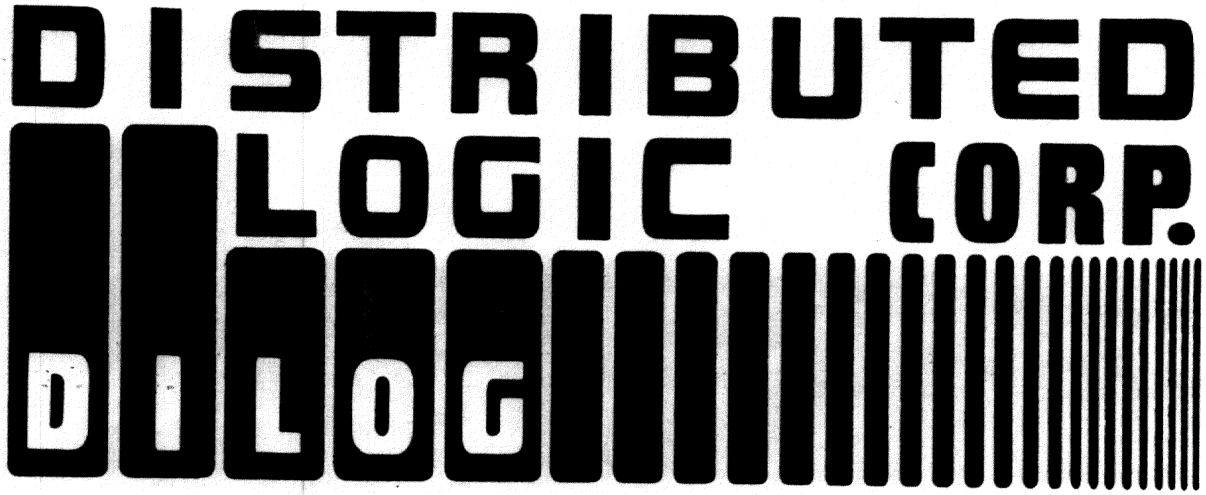
MODEL DQ215
DISC CONTROLLER
INSTRUCTION MANUAL



Part Number 30009-0

MODEL DQ215
DISC CONTROLLER
INSTRUCTION MANUAL

July 1983

DISTRIBUTED LOGIC CORP.
DILOG

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SECTION 1
DESCRIPTION

INTRODUCTION

This manual describes the installation, operation, programming, troubleshooting, and theory of operation of Distributed Logic Corporation (DILOG) Model DQ215 Disc Controller. The controller interfaces DEC* LSI-11 based computer systems to one or two SMD I/O disc drives, including 8- and 14-inch Winchester, SMD pack and CMD cartridge type drives. The complete controller occupies one quad module in the backplane. Full sector buffering in the controller matches the transfer rate of the disc drive and the CPU. The controller is compatible with RK06/RK07 software drivers in RT-11, RSX-11 and RSTS.

CONTROLLER CHARACTERISTICS

The disc controller links the LSI-11 computer to one or two disc storage units. Commands from the computer are received and interpreted by the controller and translated into a form compatible with the disc units. Buffering and signal timing for data transfers between the computer and the discs are performed by the controller.

A microprocessor is the sequence and timing center of the controller. The control information is stored as firmware instructions in read-only-memory (ROM) on the controller board. One section of the ROM contains a diagnostic program that tests the functional operation of the controller. This self-test is performed automatically each time power is applied. A green diagnostic indicator on the controller board lights if self-test passes.

Data transfers are directly to and from the computer memory using the DMA facility of the LSI-11 I/O bus. In addition, the controller monitors the status of the disc units and the data being transferred and presents this information to the computer upon request. An error correction code with a 56-bit checkword corrects error bursts up to 11 bits. To compensate for media errors, bad sectors are skipped and alternates assigned, and there is an automatic retry feature for read errors. The controller is capable of addressing four megabytes and controlling up to two disc drives in various configurations up to a total on-line formatted capacity of 220.32 megabytes. Figure 1-1 is a simplified diagram of a disc system.

*DEC, RSX and RSTS are registered trademarks of Digital Equipment Corporation.

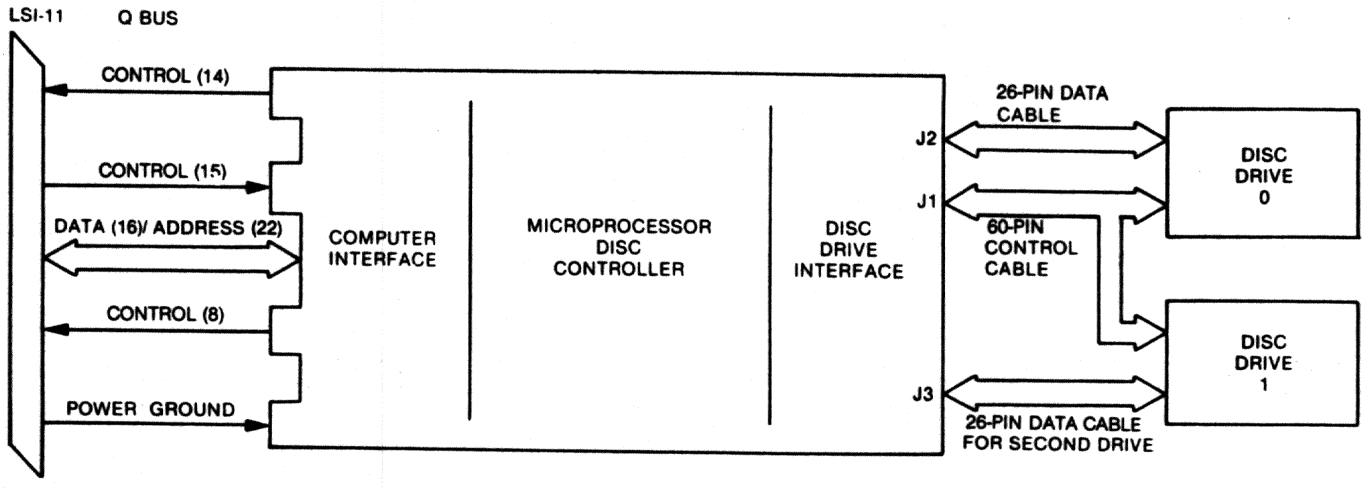

Figure 1-1. Disc Controller System Simplified Diagram

LSI-11 Q BUS INTERFACE

Commands, data and status transfers between the controller and the computer are executed via the parallel I/O bus (Q bus) of the computer. Data transfers are direct to memory via the DMA facility of the Q bus; commands and status are under programmed I/O. Controller/Q bus interface lines are listed in Table 1-1.

Table 1-1. Controller/Q-Bus Interface Lines

Bus Pin	Mnemonic	Controller Input/ Output	Description
AC2, AJ1, AM1, AT1, BJ1, BM1, BT1, BC2, CC2, CJ1, CM1, CT1, DC2, DJ1, DM1, DT1	GND	O	Signal Ground and DC return.
AN1	BDMR L	O	Direct Memory Access (DMA) request from controller: active low.
AP1	BHALT L	N/A	Stops program execution. Refresh and DMA is enabled. Console operation is enabled.
AR1	BREF L	N/A	Memory Refresh.
BA1	BDCOK H	I	DC power ok. All DC voltages are normal.
BB1	BPOK H	N/A	Primary power ok. When low activates power fail trap sequence.
BN1	BSACK L	O	Select Acknowledge. Interlocked with BDMGO indicating controller is bus master in a DMA sequence.
BR1	BEVNT L	O	External Event Interrupt Request. Real Time Clock Control.
AA2, BA2, BV1, CA2, DA2	+5	I	+5 volt system power.
AD2, BD2	+12	N/A	+12 volt system power.
AE2	BDOUT L	I/O	Data Out. Valid data from bus master is on the bus. Interlocked with BRPLY.
AF2	BRPLY L	I/O	Reply from slave to BDOUT or BDIN and during IAK.
AH2	BDIN L	I/O	Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY.
AJ2	BSYNC L	I/O	Synchronize: becomes active when master places address on bus; stays active during transfer.
AK2	BWTBT L	I/O	Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB.
AA1, AB1, AL2, BP1	BIRQ4L,5,6,7	O	Interrupt Request.
AM2 AN2 CM2 CN2	BIAK1I L BIAK1O L BIAK2I L BIAK2O L	I O I O	Serial Interrupt Acknowledge input and output lines routed from Q-Bus, through devices, and back to processor to establish and interrupt priority chain.
AT2	BINIT L	I	Initialize. Clears devices on I/O bus.
AU2, AV2, BE2, BF2, BH2, BH2, BK2, BL2, BM2, BN2, BP2, BR2, BS2, BT2, BU2, BV2	BDAL0 L through BDAL15 L	I/O	Data/address lines, 0-15
AR2 AS2 CR2 CS2	BDMG1I L BDMG1O L BDMG2I L BDMG2O L	I O I	DMA Grant Input and Output. Serial DMA priority line from computer, through devices and back to computer.
AP2	BBS7 L	I	Bank 7 Select. Asserted by bus master when address in upper 4K bank is placed on the bus.
AC1, AD1, BC1, BD1, BE1, BF1	BDAL 16 L -BDAL 21 L	O	Extended Address Bits 16-21

INTERRUPT

The interrupt vector address is factory set to address 210 (alternate 254). The vector address is programmed in a PROM on the controller, allowing user selection.

Interrupt requests are generated under the following conditions:

1. When the Controller Ready bit is set upon completion of a command.
2. When any drive sets an associated Attention Flag in the Attention Register and the Controller Ready bit is set.
3. When the controller or any drive indicates the presence of an error by setting the combined Error/Reset bit in the Control and Status Register.
4. When the Controller Ready bit is set by conventional initialization upon completion of a controller command or when an error condition is detected. For test purposes, a forced interrupt may be generated by the Controller Ready and Interrupt Enable bits.

DISC INTERFACE

The controller interfaces one or two disc drives through 60- and 26-pin cables. If two drives are used, the 60-pin control cable ("A" cable) is daisy chained to drive 0 and 1. The 26-pin cables ("B" cable) are connected separately from the controller to each drive. The maximum length of the 60-pin cable is 100 feet. The maximum length of the 26-pin cable is 50 feet. Table 1-2 lists the 60-pin interface signals, and Table 1-3 lists the 26-pin interface signals.

OPERATING SYSTEM COMPATIBILITY

RT-11: The emulation is transparent to the RT-11 version 4.0 operating system, using the standard device handler supplied by DEC.

RSX-11: The emulation is transparent to the RXS-11 version 4.0 operating system, using the standard device handler supplied by DEC.

RSTS: The emulation is transparent to the RSTS version 7.2 operating system, using the standard device handler supplied by DEC.

Table 1-2. Controller To Drive I/O Interface— "A" Cable

Signal Name (DILOG Term)	Pin Polarity (Active) –	Pin Polarity (Active) +	Source
DEVICE SELECT 0 (USEL0)	23	53	Controller
DEVICE SELECT 1 (USEL1)	24	54	Controller
DEVICE SELECT 2 (USEL2)	26	56	Controller
DEVICE SELECT 3 (USEL3)	27	57	Controller
SELECT ENABLE (USTAG)	22	52	Controller
SET CYLINDER TAG (TAG1)	1	31	Controller
SET HEAD TAG (TAG2)	2	32	Controller
CONTROL SELECT (TAG3)	3	33	Controller
BUS OUT 0 (BIT0)	4	34	Controller
BUS OUT 1 (BIT1)	5	35	Controller
BUS OUT 2 (BIT2)	6	36	Controller
BUS OUT 3 (BIT3)	7	37	Controller
BUS OUT 4 (BIT4)	8	38	Controller
BUS OUT 5 (BIT5)	9	39	Controller
BUS OUT 6 (BIT6)	10	40	Controller
BUS OUT 7 (BIT7)	11	41	Controller
BUS OUT 8 (BIT8)	12	42	Controller
BUS OUT 9 (BIT9)	13	43	Controller
BUS OUT 10 (BIT10)	30	60	Controller
DEVICE ENABLE (OCD)	14	44	Controller
INDEX (INDEX)	18	48	Drive
SECTOR MARK (SEC)	25	55	Drive
FAULT (FAULT)	15	45	Drive
SEEK ERROR (SERR)	16	46	Drive
ON CYLINDER (ONCYL)	17	47	Drive
UNIT READY (UNRDY)	19	49	Drive
WRITE PROTECTED (WPRT)	28	58	Drive
ADDRESS MARK (AMF)	20	50	Drive
BUS-DUAL-PORT ONLY	21	51	Drive
SEQUENCE IN (PICK)	29		Controller
HOLD (HOLD)	59		Controller

Table 1-3. Controller To Drive I/O Interface— "B" Cable

Signal (DILOG Term)	Pin Polarity (Active) –	Pin Polarity (Active) +	Pin Polarity (Active) Ground	Source
Ground			1	
Servo Clock (SCLOCK)	2	14		Drive
Ground			15	
Read Data (RDATA)	3	16		Drive
Ground			4	
Read Clock (RCLOCK)	5	17		Drive
Ground			18	
Write Clock (WCLOCK)	6	19		Controller
Ground			7	
Write Data (WDATA)	8	20		Controller
Ground			21	
Unit Selected (USEL)	22	9		Drive
Seek End (SEEK)	10	23		Drive
Ground			11	
Reserved for Index	12	24		
Ground			25	
Reserved for Sector	13	26		

CONTROLLER SPECIFICATIONS*

Mechanical—The Model DQ215 is completely contained on one quad module 10.44 inches wide by 8.88 inches deep, and plugs into and requires one slot in any DEC LSI-11 based backplane.

Computer I/O

Register Addresses (PROM selectable)

—Control/Status Register 1 (RKCS1) 777 440
—Word Count Register (RKWC) 777 442
—Bus Address Register (RKBA) 777 444
—Disc Address Register (RKDA) 777-446
—Control/Status Register 2 (RKCS2) 777 450
—Drive Status Register (RKDS) 777 452
—Error Register (RKER) 777 454
—Attention Summary/Offset Register (RKAS/OF) 777 456
—Desired Cylinder Register (RKDC) 777 460
—Extended Memory Address Register (RKXMA) 777 462
—Data Buffer Register (RKDB) 777 464
—Maintenance Register 1 (RKMR1) 777 466
—ECC Position Register (RKECPS) 777 470
—ECC Pattern Register (RKECPT) 777 472
—Maintenance Register 2 (RKMR2) 777 474
—Maintenance Register 3 (RKMR3) 777 476
—Enable Real Time Clock Control (RKERTC) 777 546

Data Transfer

—Method: DMA
—Maximum block size transferred in a single operation is 64K words.

Bus Load

—1 std unit load

Address Ranges

—Disc drive: up to 220.32 megabytes
—Computer Memory: to 2 megawords

Interrupt Vector Address

—PROM selectable, factory set at 210 (alternate 254) priority level BR5

Disc Drive I/O

Connector—one 60-pin type "A" flat ribbon cable mounted on outer edge of controller module Two 26-pin type "B" ribbon cables (1 for each drive interfaced with).

Signal—SMD A/B flat cable compatible

Power—+5 volts at 3.5 amps, +12 volts at 300 milliamps from computer power supply.

Environment—Operating temperature 40°F. to 140°F., humidity 10 to 95% non-condensing.

Shipping Weight—5 pounds, includes documentation and cables.

*Specifications subject to change without notice.

SECTION 2
INSTALLATION

INSPECTION

The padded shipping carton that contains the controller board also contains an instruction manual and cables to the first disc drive if this option is exercised. The controller is completely contained on the quad-size printed circuit board. Disc drives, if supplied, are contained in a separate shipping carton. Inspect the controller and cables for damage.

CAUTION

If damage to any of the components is noted, do not install. Immediately inform the carrier and DILOG.

Installation instructions for the disc drive are contained in the disc drive manual. Before installing any components of the disc system, read Sections 1, 2 and 3 of this manual. Figure 2-1 illustrates the configuration of the controller. Tables 2-1 and 2-2 describe switch and jumper settings.

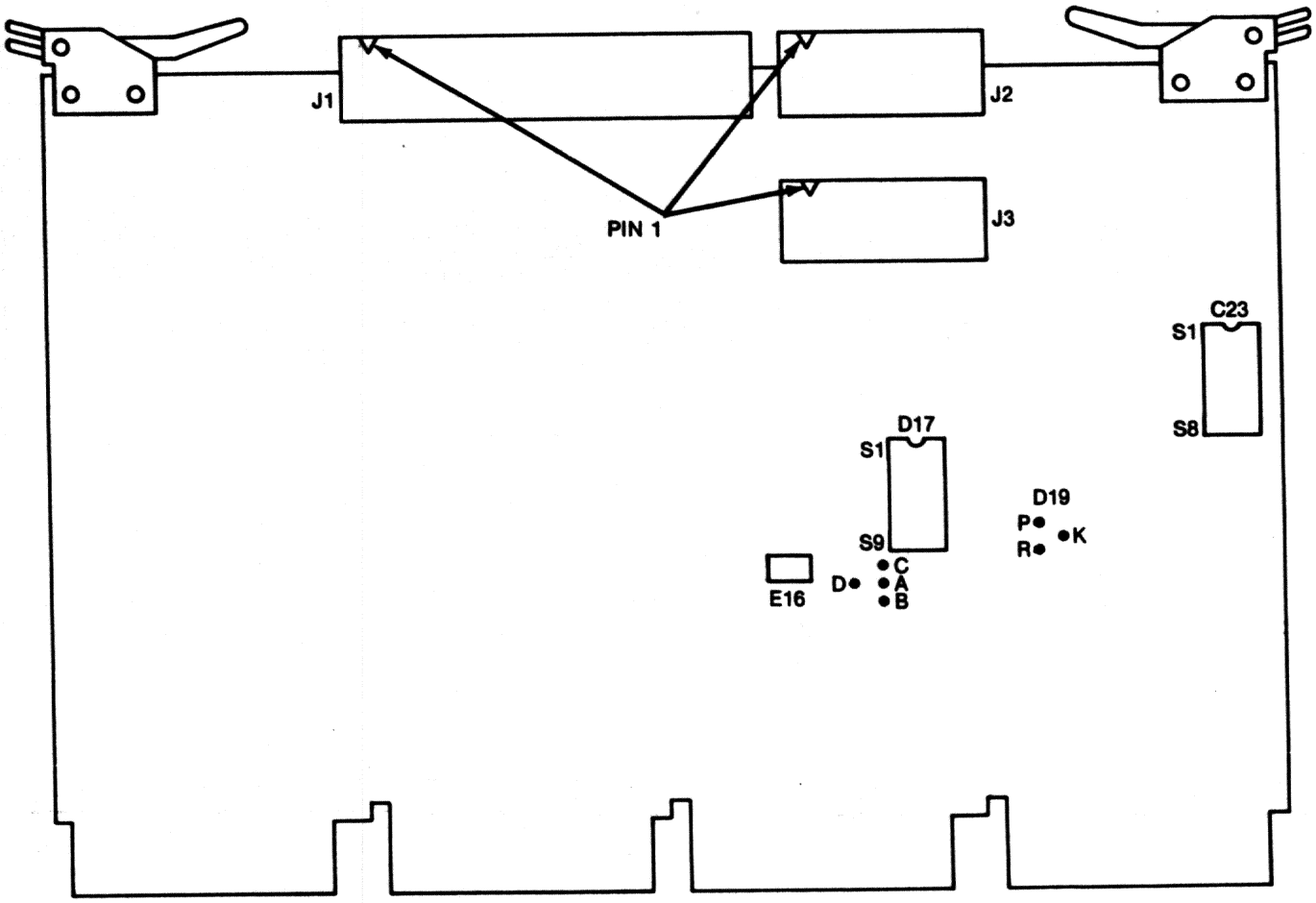

Figure 2-1. Controller Configuration

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TECHNICAL MANUAL CHANGE

MODEL: DQ215 MANUAL PART NUMBER: 30009-0 MANUAL DATE: July 1983

TMC NUMBER: 1 TMC DATE: 12 October 1983

PAGES AFFECTED: 2-2, 3-1

DESCRIPTION:

This TMC adds description of jumpers for priority of interrupt requests and changes the bootstrap procedure.

To Table 2-1, Page 2-2, add the following:

LOCATION E23

Jumpers Installed	Interrupt Level
JP1, JP2, JP3	BR4
JP2, JP3	BR5 (factory set)
JP1, JP3	BR6
JP1	BR7

Under the Bootstrap Procedure, page 3-1: "Definitions are as follows:"

Delete:

"RK=RK05 Disc"

Add:

"MS=TS-11 Tape"

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Table 2-1. Configuration Switches

LOCATION D17 SWITCHES

S1 (LSB) S2 S3 (MSB)

Binary Number of the first logical unit of the second physical drive.*

S4

ON = Bootstrap enable
OFF = Bootstrap disable

S5

ON = Controller error correction
OFF = CPU error correction

S6 (LSB) S7 S8 (MSB)

Binary number of last addressable logical unit.

S9

ON = Enable Real Time Clock Control. When enabled, emulates the real time clock register, address 777 546
OFF = Disables Real Time Clock Control.

*For example, if there are four logical units (numbered 0-3) in the first drive, set the switches for the fifth logical unit (number 4) as follows:

(LSB) S1	S2	(MSB) S3
0	0	1

Note

If S1, S2, and S3 are off (000), the controller will default to all logical units on the first physical drive (drive 0). Because of the characteristics of some operating systems, the switches should be set for two drives even if only one drive is present.

LOCATION C23 SWITCHES

Switch	Position	Logical Unit and Emulation
S1	ON	LU0 = RK07
	OFF	LU0 = RK06
S2	ON	LU1 = RK07
	OFF	LU1 = RK06
S3	ON	LU2 = RK07
	OFF	LU2 = RK06
S4	ON	LU3 = RK07
	OFF	LU3 = RK06
S5	ON	LU4 = RK07
	OFF	LU4 = RK06
S6	ON	LU5 = RK07
	OFF	LU5 = RK06
S7	ON	LU6 = RK07
	OFF	LU6 = RK06
S8	ON	LU7 = RK07
	OFF	LU7 = RK06

Table 2-2. Jumper Installation

BOOTSTRAP
ADDRESS JUMPERS E16

D . . C — *A to B (standard) 773 000
. A
. B — A to C (alternate) 775 000

DEVICE
ADDRESS JUMPERS D19

R to K (standard) 777 440
Interrupt Vector = 210

R to P (alternate) 776 700
Interrupt Vector = 254

*On an LSI-11/23 PLUS computer, bootstrap address 775 000 must be used.

PRE-INSTALLATION CHECKS

There are various LSI-11 configurations, many of which were installed before DEC made a hard disc available for LSI-11 based systems. Certain configurations require minor modifications before operating the disc system. These modifications are as follows:

A. If the system contains a REV11-C module, it must be placed closer to the processor module (higher priority) than the controller if the DMA refresh logic on the REV11-C is enabled.

B. If the 4K memory on the DK11-F is not used and the memory in the system does not require external refresh, the DMA refresh logic on the REV11-C should be disabled by removing jumper W2 on the REV11-C module.

C. If the system contains a REV11-A module, the refresh DMA logic must be disabled since the module must be placed at the end of the bus (REV11-A contains bus terminator).

D. If the REV11-C module is installed, cut the etch to pin 12 on circuit D30 (top of board) and add a jumper between pin 12 and pin 13 of D30.

E. If the system requires more than one backplane, place the REV-11 terminator in the last available location in the last backplane.

INSTALLATION

To install the controller module, proceed as follows:

CAUTION

Remove DC power from mounting assembly before inserting or removing the controller module.

Damage to the backplane assembly may occur if the controller module is plugged in backwards.

1. Select the backplane location into which the controller is to be inserted. Be sure that the disc controller is the lowest priority DMA device in the computer except if the DMA refresh/bootstrap ROM option module is installed in the system. The lowest priority device is the device farthest from the processor module. Note that the controller contains a bootstrap ROM.

   There are several backplane assemblies available from DEC and other manufacturers. Figure 2-2 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane or in the first location in the first backplane of multiple backplane systems.

   It is important that all option slots between the processor and the disc controller be filled to ensure that the daisy-chained interrupt (BIAK) and DMA (BDMG) signal be complete to the controller slots. If there must be empty slots between the controller and any option board, the following backplane jumpers must be installed:

FROM	TO	SIGNAL
C0 x NS	C0 x M2	BIAK1/L0
C0 x S2	C0 x R2	BDMG1/L0
↑ Last Full Option Slot	↑ Controller Slot	

2. Insert the controller into the selected backplane position. Be sure the controller is installed with the components facing row one, the processor.

   The controller module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

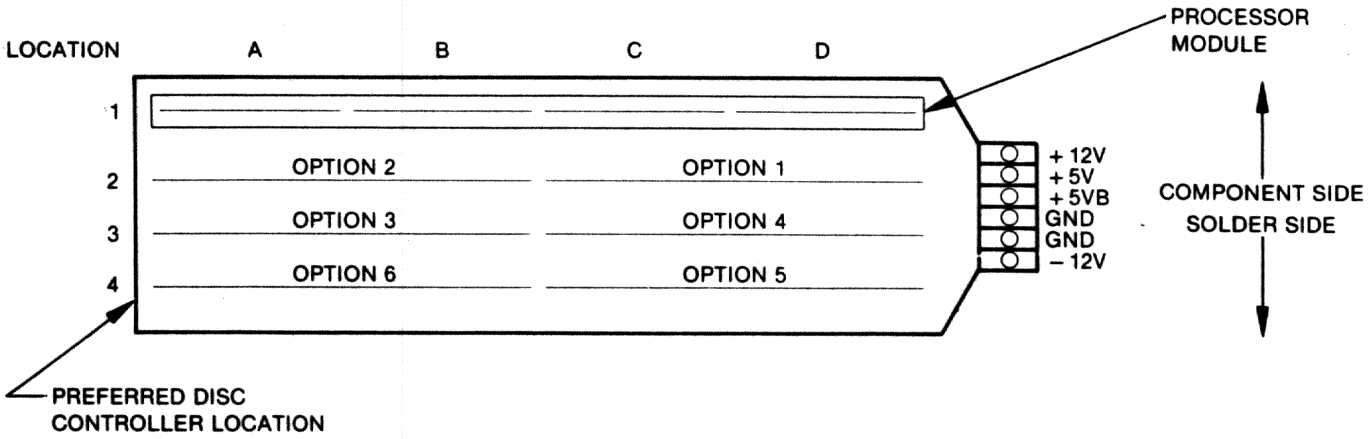
3. Feed the module connector end of the disc I/O cables into the controller module connectors. Ensure pin 1 is matched with the triangle on the connector as shown in Figure 2-1. Install the cable connectors into the module connectors. Verify that the connectors are firmly seated.

4. Connect the disc-end of the I/O cables to the disc I/O connectors. Be sure that the bus terminator is installed at the last disc in the system.

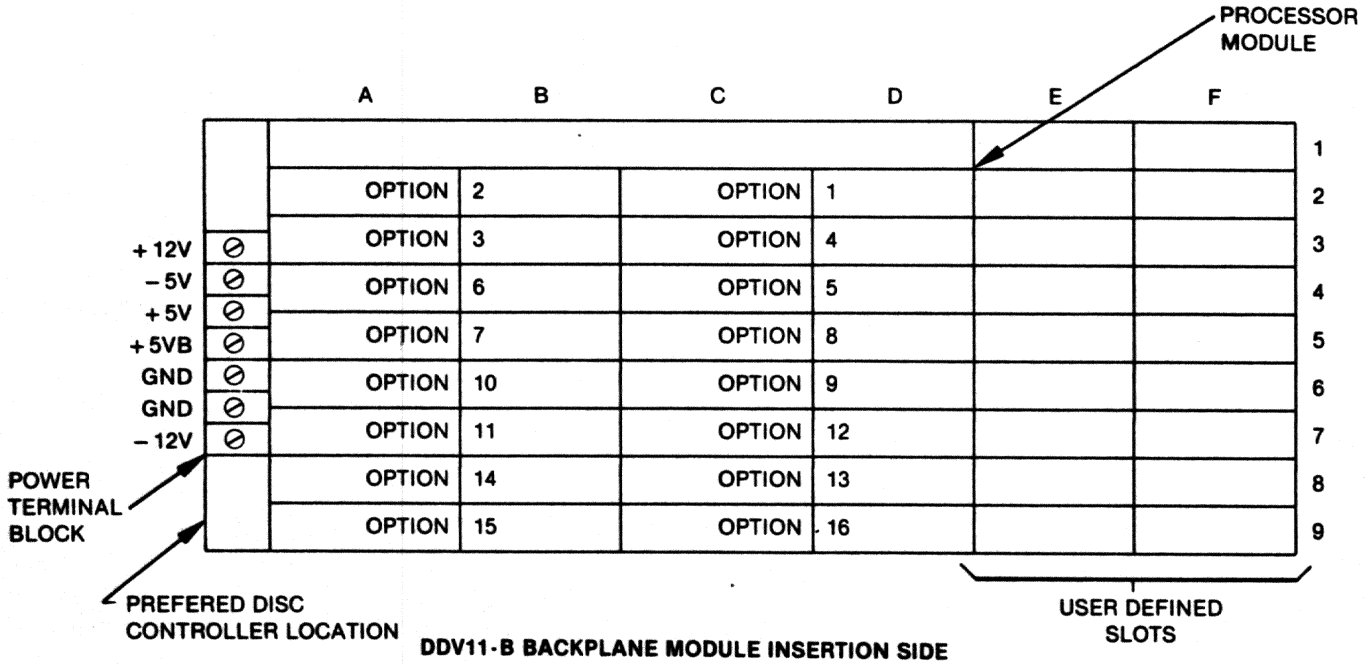
5. Refer to the disc manual for operating instructions and apply power to the disc and computer.

6. Observe that the green DIAGnostic LED on the controller board is lit.

7. The system is now ready to operate. Refer to Section 3 for operating instructions, diagnostics, and formatting.



H9270 MODULE INSERTION SIDE



DDV11-B BACKPLANE MODULE INSERTION SIDE

NOTE

MEMORY CAN BE INSTALLED IN ANY SLOT; IT IS NOT PRIORITY DEPENDENT AND DOES NOT NEED TO BE ADJACENT TO THE PROCESSOR.
CONTROLLERS ARE ALSO COMPATIBLE WITH H9273A MODULES.

Figure 2-2. Typical Backplane Configuration

GROUNDING

To prevent grounding problems, DILOG recommends standard ground braid be installed from the computer DC ground point to the disc drive DC ground point and also between disc drives at the DC ground points.

SECTION 4
PROGRAMMING

PROGRAMMING DEFINITIONS

Function—The expected activity of the disc system (write, seek, read, etc.)

Command—To initiate a function (halt, clear, go, etc.)

Instruction—One or more orders executed in a prescribed sequence that causes a function to be performed.

Address—The binary code placed in the BDAL0-15 lines by the bus master to select a register in a slave device. Note memory other than computer internal memory, i.e., peripheral device registers, the upper 4K (28-32K) address space is used.

Register—An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system. Classically, registers have been made up of groups of flip-flops. More and more often registers are the contents of addressed locations in solid-state or core memory.

DISC CONTROLLER FUNCTIONS

The disc controller performs 14 functions. A function is initiated by a GO command after the processor has issued a series of instructions that store function-control information into controller registers. To accept a command and perform a function, the controller must be properly addressed and the disc drive(s) must be powered up, be at operational speed, and be ready.

The functions performed by the controller are established by bits 01, 02, 03 and 04 of the control status register (RKCS1). The function and bit codings are given in Table 4-1. Descriptions of the functions are given in the following paragraphs.

Note that the controller automatically performs certain functions during each command. For example, the controller always performs the following steps:

1. Decodes instruction
2. Selects drive
3. Acknowledges pack (tests for RK06/RK07 drive type)
4. Executes one of the remaining nine functions

Table 4-1. Function Codes

Bit 4321	Command
0000	SELECT DRIVE
0001	PACK ACKNOWLEDGE
0010	DRIVE CLEAR (RESET ATTENTION STATUS)
0011	UNLOAD (NO OP)
0100	START SPINDLE (NO OP)
0101	RECALIBRATE (RESTORE DRIVE AND RESET FAULT)
0110	OFFSET
0111	SEEK
1000	READ DATA
1001	WRITE DATA
1010	READ HEADERS (1 TRACK OF HEADERS)
1011	WRITE HEADERS (FORMAT TRACK)
1100	WRITE CHECK

Select Drive

Performed automatically as part of all functions related to drive selection (connects drive).

Pack Acknowledge

Performed automatically to verify emulation (RK06/RK07) as part of all functions related to drive selection. Controls bit 08 in RKDS.

Drive Clear

Resets attention status in RKAS/0F.

Recalibrate

Relocates the heads to cylinder zero and clears the cylinder address register. Also resets all fault conditions. Sets attention bit in RKAS/0F.

Offset

Sets drive attention bit in RKAS/0F.

Seek

Performed automatically as part of all functions related to drive selection. Sets attention bit in

RKAS/0F. During Overlapped Seeks, loads cylinder address into RKMR3 (Maintenance Register 3).

Read Data

Causes the following sequence to be executed: A Seek to the cylinder in RKDC is performed. Headers are read and compared with the desired disc address until the correct sector is found. Transfer of data through the data buffer to memory is initiated. When the sector data transfer is complete, the ECC logic is checked to ensure that the data read from the disc was error-free. If a data error occurred, the ECC correction logic is initiated to determine whether the error is correctable; when finished, the command is terminated to allow software or hardware (as selected) to apply the correction information. Assuming no data errors, the word count in RKWC is checked; if non-zero, the data transfer operation is repeated into the next sector. The word count is checked at the end of each sector until it reaches zero, at which time the command is terminated by setting the Ready bit.

Write Data

Causes the following sequence to be executed: A Seek to the cylinder in RKDC is performed. Transfer of data from memory to the data buffer is begun, and headers are read and compared with the desired disc address until the correct sector is found. Preamble, Data (256 words), and ECC bits (56) are written on the disc. If the word count in RKWC goes to zero during the sector, the rest of the sector is zero-filled. After the sector transfer, the word count is RKWC is checked and, if non-zero, the data transfer operation is continued into the next sector. The word count in RKWC is checked at the end of each sector and, when it equals zero, the command is terminated by setting the Ready bit.

Read Headers

A Seek to the cylinder in RKDC is performed. This function causes the controller to read all headers starting at the Index mark. Each 5-word header is read in the order in which it appears on the disc. If an ECC error is detected in the header, the HRE bit of RKER is set.

Write Headers

A Seek to the cylinder in RKDC is performed. The controller then waits until Index is detected. When detected, zeros are written until Index is again detected. This "cleans" the track of potential spurious signals. After Index is detected a second time, 5 header words and a 32-bit ECC are written after each sector pulse. When Index is next detected, the command is terminated and the Ready bit is set.

Note

All five words and the ECC code are prepared by the format routine (software) and treated as data by the controller. Only one complete track can be formatted at a time.

Write Check

Causes the following sequence to be executed: A Seek to the cylinder in RKDC is performed. The selected drive provides data as in a Read command, and data is obtained from memory as in a Write command. The data are compared on a word-for-word basis until the word count reaches zero or until a failure to compare occurs. If the data fails to compare, the command is terminated immediately.

Mapping and Map Override

In a typical DEC disc subsystem, the method by which the disc drive finds the proper location to read data from or write data to is as follows:

1. The application software program running under the operating system sends a record number to the disc device driver software.
2. The device driver converts this record number into head, sector and cylinder numbers.
3. The driver then sends this information to dedicated hardware registers on the disc controller.
4. The controller in turn passes these parameters on to the disc drive over I/O interface cables.
5. The drive interprets these signals and activates electronics and electromechanics enabling it to seek to the exact physical location where information will be recorded or retrieved.

In a DEC subsystem which includes a DILOG controller, the above procedure is the same up to step 4. But instead of passing on the head, sector and cylinder information to the drive, the DILOG controller first takes that information sent by the device driver software and reconverts it to the original record number. Then by invoking a special algorithm, the controller develops a new head, sector and cylinder number. This is called mapping

and it is a necessary procedure whenever the disc drive that is attached to the CPU does not contain the same specifications as the drive supplied by the CPU manufacturer.

Map Override is nothing more than a special operating mode of the DILOG disc controller which allows it to transfer the disc address to the drive as described in steps 1-5, bypassing the DILOG mapping procedure. Typically, this feature is only used in an environment in which the user requires the entire disc drive to be formatted as one large logical unit. In other words, one logical unit would equal one physical unit. For example, consider a subsystem consisting of a DQ215 and a Fujitsu Eagle 474 Mbyte drive. Obviously, the controller is not a good match for a drive that large, considering that one RK07 logical unit equals 27.6 Mbytes. If, however, the user had a definite requirement for running an RK07 instruction set, he could invoke Map Override and format the Eagle as one very large RK07. One requirement is that the device driver software has to be modified.

ENABLE REAL TIME CLOCK CONTROL

The real time clock line is from the 60-cycle power supply in the LSI. The Operating System uses the clock for time and date. The line on the Q Bus, BEVNT, can be disabled by a switch on the controller, which when ON enables real time clock control or when OFF disables control. The register, address 777 546, is shown at the end of this section.

REGISTERS

A summary of the registers is shown in Figure 4-1, followed by a description of each register.

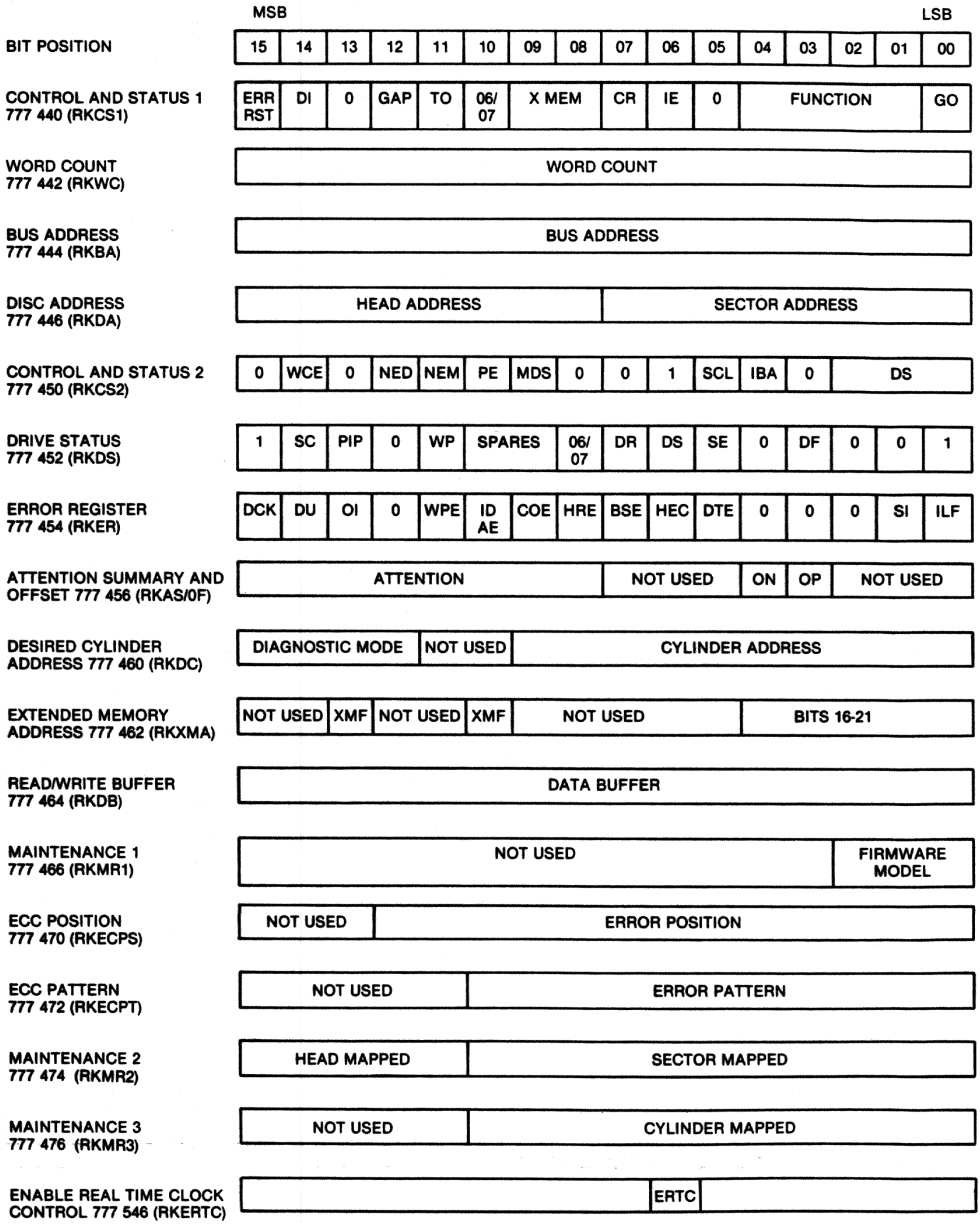
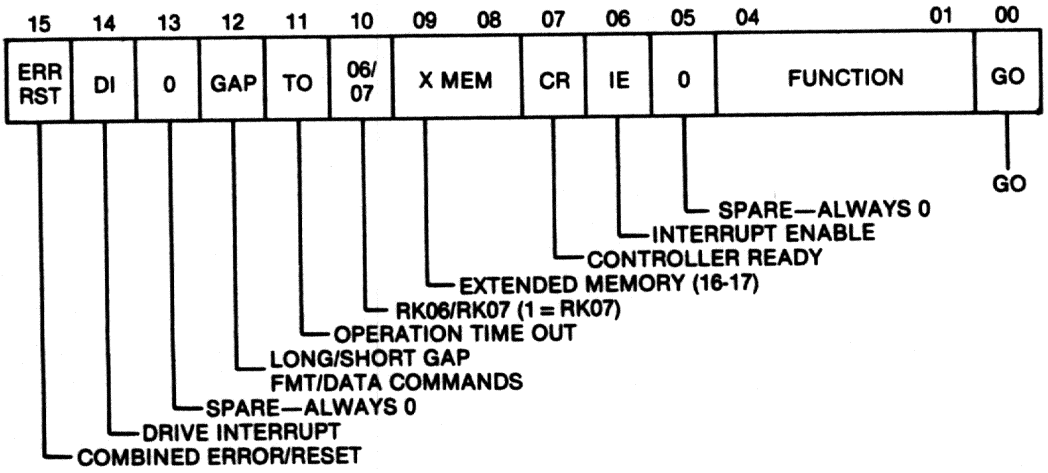


Figure 4-1. Controller Register Configuration

CONTROL AND STATUS REGISTER 1
777 440 (RKCS1)



BIT(S) DEFINITION

00 GO—When set this bit causes programmed commands (function codes) to be executed. When set, only two other bits can be set (except in the diagnostic mode); they are: Bit 15, CCLR, in RKCS1 and Bit 05, SCLR, in RKCS2.

01-04 FUNCTION CODE—

BIT 4321	0(GO)	OCTAL	COMMAND
0000	1	01	SELECT DRIVE
0001	1	03	PACK ACKNOWLEDGE
0010	1	05	DRIVE CLEAR (RESET DRIVE FAULT)
0011	1	07	UNLOAD (NO OPERATION)
0100	1	11	START SPINDLE
0101	1	13	RECALIBRATE (RESTORE DRIVE AND RESET FAULT)
0110	1	15	OFFSET
0111	1	17	SEEK (NO OPERATION)
1000	1	21	READ DATA
1001	1	23	WRITE DATA
1010	1	25	READ HEADERS (1 TRACK OF HEADERS)
1011	1	27	WRITE HEADERS (FORMAT TRACK)
1100	1	31	WRITE CHECK

05 SPARE—ALWAYS 0

06 INTERRUPT ENABLE—When this bit is set, the controller is allowed to interrupt the processor under any of the following conditions:

- When the Controller Ready bit (bit 07 in RKCS1) is set upon completion of a command.
- When any drive sets an associated Attention flag (ATN7-ATN0) in RKAS/0F, and the Controller Ready bit is set.
- When the controller or any drive indicates the presence of an error by setting the ERR/RST bit in RKCS1.

In addition, via program control, an interrupt can be forced by the simultaneous setting of the IE and RDY bits in RKCS1. The IE bit can be reset via program control as well as by conventional initialization (INIT, CCLR, SCLR).

07 CONTROLLER READY—This is a read-only bit. It is set via conventional initialization (INIT, CCLR, SCLR) upon completion of a controller command, or when an error condition is detected. The RDY bit is reset when the GO bit (bit 00 in RKCS1) is set.

08-09 EXTENDED BUS ADDRESS—These bits constitute an extension of the 16-bit Bus Address register (RKBA), which contains the memory address for the current data transfer.

10 RK06/RK07 SELECT—When set this bit selects RK07. When reset, RK06 is selected.

11 OPERATION TIME OUT—When set, this read-only bit indicates that the GO bit has been set for a specified time period and the current command has not been executed within that time period.

*12 GAP CONTROL—In the Write Header command (or write format) bit 12 will direct the controller to generate a long gap (24 bytes) or a short gap (16 bytes) between sector and header.

Bit 12 1 = Short Gap
0 = Long Gap

In the Write Data or Read Data command bit 12 will direct the controller to Write or Read a sector data field (512 bytes) with or without ECC (7 bytes) to or from memory.

Bit 12 1 = 512 Bytes + 7 Bytes
DATA ECC

0 = 512 Bytes

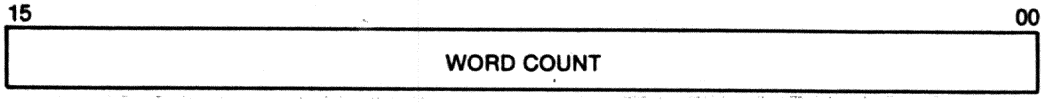
13 SPARE—ALWAYS 0

14 DRIVE INTERRUPT ENABLE (SEEK OR RESTORE)—This bit is set during a Seek or Restore operation or when any attention bit is set in the RKAS/OF register. The bit is reset by Bus Initialize (INIT), Subsystem Clear (SCLR) or by Drive Clear commands asserting attention.

15 COMBINED ERROR/RESET—When reading bit 15 via programmed control, a zero indicates an operation complete with good status; a one indicates an operation complete with an error.

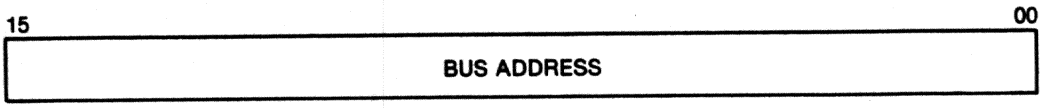
*NOTE: When bit 12 is set, the Word Count Register should be set for 520 bytes.

WORD COUNT REGISTER
777 442 (RKWC)



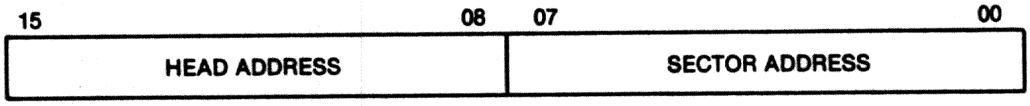
This is a Read/Write register. The bits of this register contain the 2's complement of the total number of words to be transferred during a Read, Write, or Write Check operation. The register is incremented by one after each transfer. When the register overflows (all WC bits go to zero), the transfer is complete and controller action is terminated at end of the present disc sector. Only the number of words specified in the RKWC are transferred. Cleared by INIT or RESET functions.

BUS ADDRESS REGISTER
777 444 (RKBA)



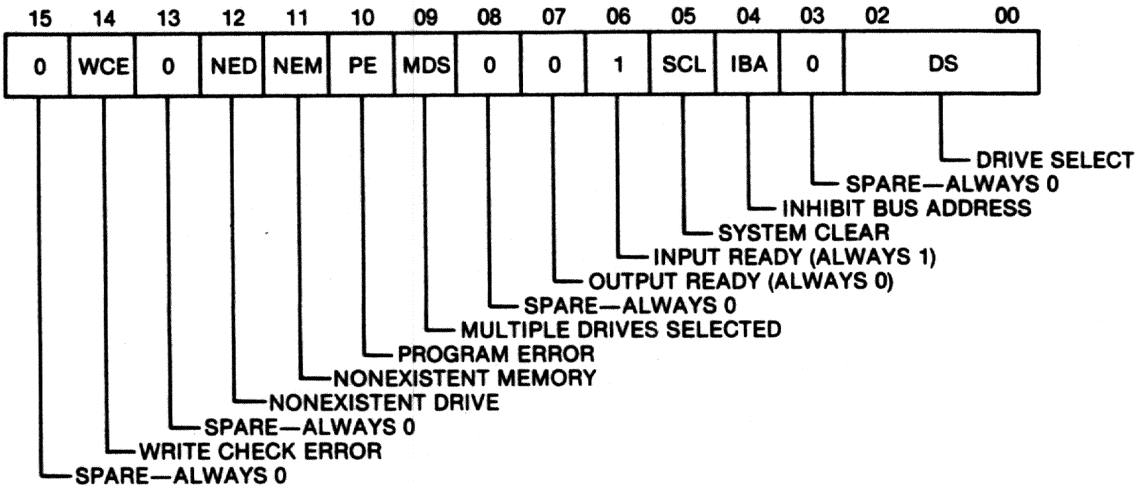
The Bus Address Register is initially loaded with the low-order sixteen bits of the bus address that reflects the main memory start location for a data transfer. With the low-order bit (bit 00) always forced to zero, the Bus Address Register bits are combined with bits 09 and 08 of the RKSC1 register (BA17, BA16) to form a complete even-numbered, 18-bit memory address. Following each data transfer bus cycle, the Bus Address Register is incremented to select the next even-numbered location.

DISC ADDRESS (TRACK AND SECTOR) REGISTER
777 446 (RKDA)



BIT(S)	DEFINITION
00-04 (00-07)	SECTOR ADDRESS—In the emulation mode, bits 00-04 select up to 20 sectors of 16-bit words. In the map override mode, bits 15, 14, 13, 12, in the Desired Cylinder Register 777 460, are set to 1000, respectively. The Sector Address then uses bits 00-07.
08-10 (08-15)	HEAD (TRACK) ADDRESS—In the emulator mode, bits 08-10 select heads 0, 1, 2. In the map override mode, bits 15, 14, 13, 12 and in the Desired Cylinder Address Register 777 460, are set to 1, 0, 0 and 0, respectively. The Head (TRACK) Address then uses bits 08-15.

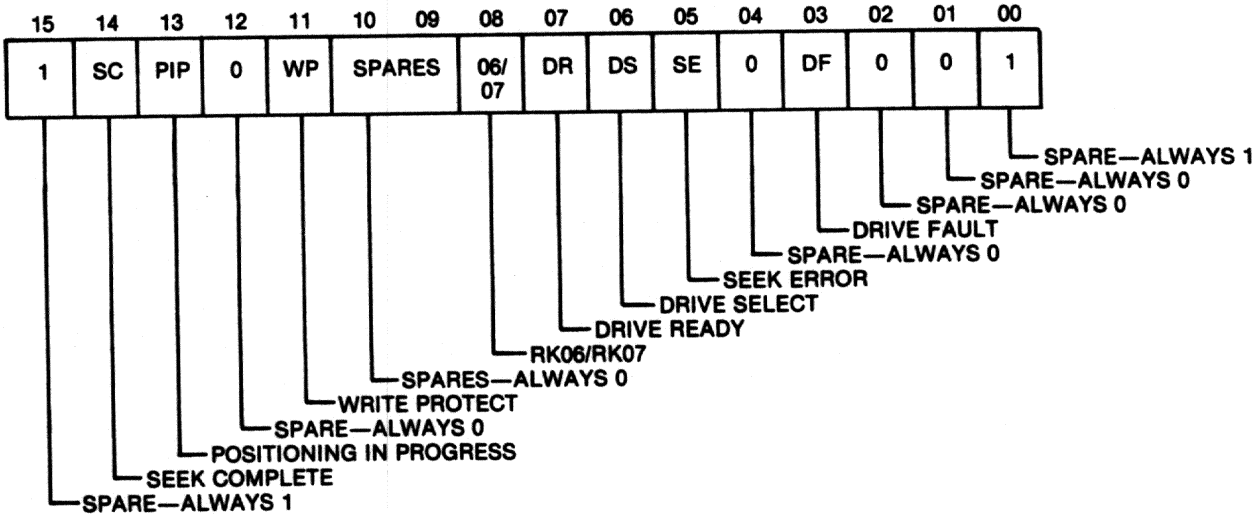
CONTROL AND STATUS REGISTER 2
777 450 (RKCS2)



BIT(S)	DEFINITION
00-02	DRIVE SELECT—These bits specify the drive to be selected.
03	SPARE—ALWAYS 0
04	INHIBIT BUS ADDRESS INCREMENT—When this bit is set, the Bus Address register is prevented from incrementing during data transfers.
05	SYSTEM CLEAR—When this bit is set the controller and drive are reset.
06	INPUT READY—ALWAYS 1
07	OUTPUT READY—ALWAYS 0
08	SPARE—ALWAYS 0
*09	MULTIPLE DRIVES SELECTED—This bit is set when more than one drive has been selected at the same time. This bit can only be cleared by INIT or SCLR.
*10	PROGRAM ERROR—This read-only error bit is set if any controller register is written (CCLR and SCLR excluded) while the GO bit in RKCS1 is set.
*11	NONEXISTENT MEMORY—This read-only error bit is set when the controller attempts to execute a bus cycle and SSYN is not returned within the specified time period.
*12	NONEXISTENT DRIVE—When set, this read-only error bit indicates that Select Acknowledge (SACK) has not been asserted by the selected drive in response to a Select Enable sent to the drive.
*13	SPARE—ALWAYS 0
*14	WRITE CHECK ERROR—When set, this read-only bit indicates that a data word read from the disc (during a Write Check command) did not compare with the data word in main memory. If a Write Check error is detected and the IBA bit (bit 04 of RKCS2) is cleared, the Bus Address register will contain the memory address of the mis-matched word plus two or plus four.
15	SPARE—ALWAYS 0

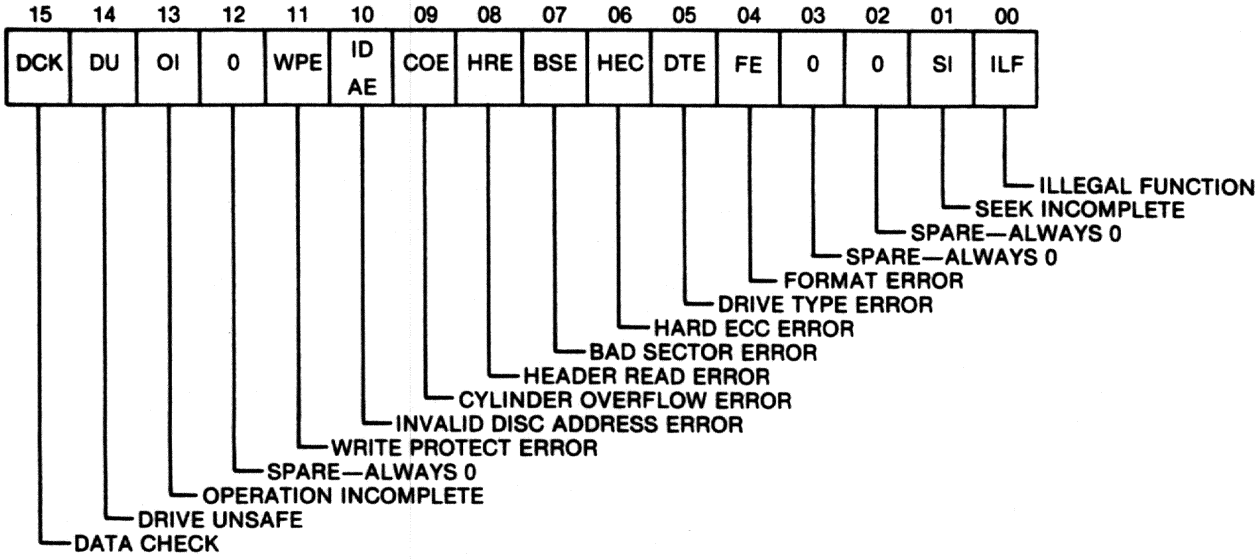
*Causes bit 15 in RKCS1 to set.

DRIVE STATUS REGISTER
777 452 (RKDS) Read Only Register



BIT(S)	DESCRIPTION
00	SPARE—ALWAYS 1
01	SPARE—ALWAYS 0
02	SPARE—ALWAYS 0
03	DRIVE FAULT—When set, indicates an error condition is detected within the drive and is prohibiting all operations. This bit is reset manually by clearing the fault condition within the drive.
04	SPARE—ALWAYS 0
05	SEEK ERROR—When set, indicates a seek was not completed within a specified time period after it was initiated.
06	DRIVE SELECTED—When set, the drive is selected and on line.
07	DRIVE READY—Drive Ready is a read-only bit which when set indicates the selected drive is up to speed, the heads are on cylinder and the drive is ready to accept commands. It is reset when these conditions are not met or when driving is seeking.
08	RK06/RK07—When set indicates RK07, when reset, RK06.
09-10	SPARES—ALWAYS 0
11	WRITE PROTECT—When set, the selected disc is write protected.
12	SPARE—ALWAYS 0
13	POSITIONING IN PROGRESS—When set, the selected disc is write protected.
14	SEEK INCOMPLETE—This read-only bit sets when the drive is ON CYLINDER. SEEK or RESTORE is completed.
15	ALWAYS 1

ERROR REGISTER
777 454 (RKER)



BIT(S) DEFINITION

00 ILLEGAL FUNCTION—When set, this read-only bit indicates that an illegal command has been loaded into the RKCS1 register.

01 SEEK INCOMPLETE—When set, this read-only bit indicates that a seek operation has not been completed by the selected drive.

02 SPARE—ALWAYS 0

03 SPARE—ALWAYS 0

04 FORMAT ERROR—When set in conjunction with bit 09, indicates that the sector pulses are too close together. Diagnostic message is "sector size too small."

05 DRIVE TYPE ERROR—This read-only bit is set when the drive type status does not compare with Control Drive Type bit (RKCS1, bit 10), i.e., RK06 instead of RK07 or vice versa.

06 HARD ECC ERROR—When set, this read-only bit indicates that a data error detected by the ECC logic cannot be corrected using ECC.

07 BAD SECTOR ERROR—When set, this read-only bit indicates that a data transfer was attempted to or from a sector and the sector is bad.

08 HEADER READ ERROR—When set, this read-only bit indicates that an uncorrectable ECC error was detected on a sector header during a data transfer. If bit 13 is also set, the error indication is header not found.

09 CYLINDER OVERFLOW ERROR—When set, the word count is not equal to zero and the operation is programmed to continue beyond the last logical sector on the disc. This will occur on a Read or Write data operation.

10 INVALID DISC ADDRESS ERROR—When set, this bit indicates that an invalid cylinder address or an invalid head address has been detected during a Seek command or Write/Read data command.

11 WRITE PROTECT ERROR—When set, this read-only bit indicates that the drive received assertion of Write Gate while in the write protect mode.

12 SPARE—ALWAYS 0

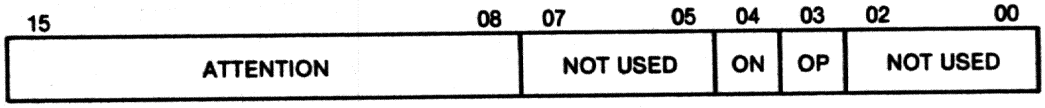
13 OPERATION INCOMPLETE—When set, this read-only bit indicates that during a data transfer, the desired header could not be found. This error can result from any one of the following:

- Head Misposition
- Incorrect Head Selection
- Read Channel Failure
- Improper Pack Formatting

14 DRIVE UNSAFE—When set, this read-only bit indicates that a Read/Write Unsafe condition has been detected.

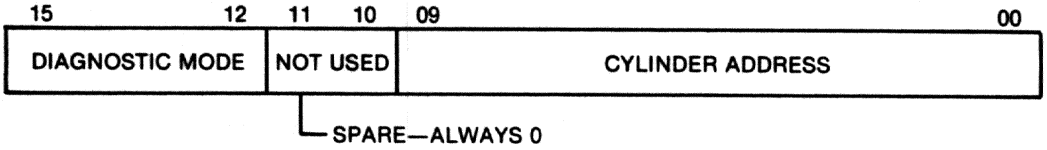
15 DATA CHECK—When set, this read-only bit indicates that a data error was detected when the current sector was read.

ATTENTION SUMMARY AND OFFSET REGISTER
777 456 (RKAS/0F)



BIT(S)	DEFINITION
00-02	SPARE—ALWAYS 0
03	OFFSET POSITIVE—Offsets the head in the positive direction from the centerline of the track (positive is from the lower cylinder number toward the higher cylinder number).
04	OFFSET NEGATIVE—Offsets the head in the negative direction from the centerline of the track (negative is from the higher cylinder number toward the lower cylinder number).
05-07	SPARE—ALWAYS 0
08-15	ATTENTION—The eight Attention bits, one for each drive, correspond to the logical unit number of each drive. Each bit indicates the state of the Drive Status Change flip-flop in the corresponding drive. All of the ATN bits are continuously scanned and updated (polled).

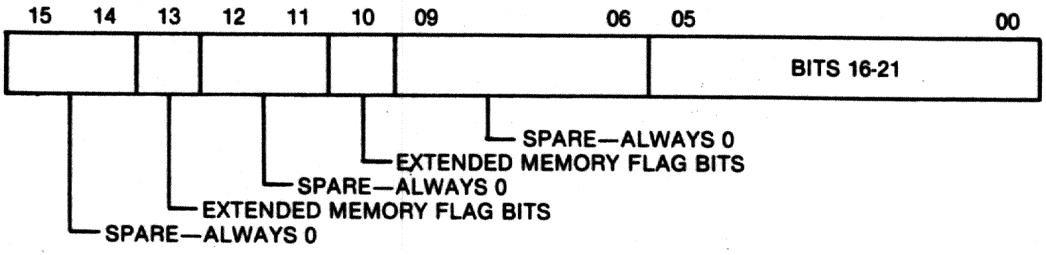
DESIRED CYLINDER ADDRESS REGISTER
777 460 (RKDC)



BIT(S)	DEFINITION
00-09	CYLINDER ADDRESS—The cylinder address in RKDC is the emulated address. The actual mapped address is contained in RKMR2. The cylinder number is written in octal in the register.
10-11	SPARE—ALWAYS 0
12-15	DIAGNOSTIC MODE—These bits are as follows:

15	14	13	12	
0	0	0	0	RK06/RK07 Emulation Mode
1	0	0	0	MAP OVERRIDE MODE—These bits can be set by the programmer to override the mapping algorithm. When set, the head, cylinder, and sector addresses supplied to the controller specify absolute address to the disc. Could be typically used to permit the device handler to be modified to take advantage of the head per track options available in some disc drives.
1	1	0	0	DMA BUFFER TEST MODE—Allows Reading/Writing of the controller data buffer using the computer DMA interface. The controller word count and memory address registers are used to set up the DMA transfer with a maximum transfer of 1024 bytes starting with location 0 of the data buffer. The write command, 23_8, will write from the buffer. The read command, 21_8, will read from the data buffer.
1	1	1	0	ECC TEST MODE
1	1	0	1	I/O BUS INTERFACE TEST MODE
1	1	1	1	I/O W/R INTERFACE TEST MODE

EXTENDED MEMORY ADDRESS REGISTER (22-Bit)
777 462 (RKXMA)

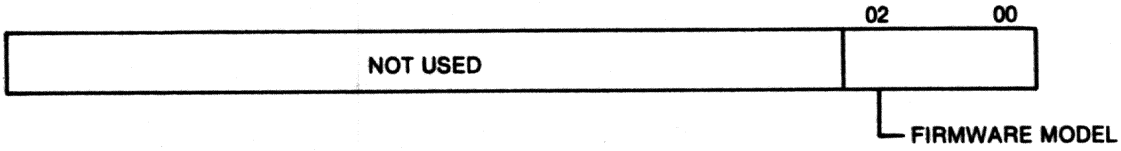


BIT(S)	DEFINITION
00-05	BITS 16-21—These bits, when set, define bits 16-21 of the 22-bit extended memory.
06-09	SPARE—ALWAYS 0
10, 13	EXTENDED MEMORY—When bits 10 and 13 are set, the 22-bit address is used.
11-12, 14-15	SPARE—ALWAYS 0

READ/WRITE BUFFER REGISTER
777 464 (RKDB)

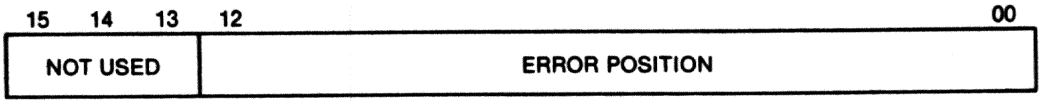
BIT(S)	DEFINITION
00-15	The Data Buffer Register is a Read/Write register. Writing into the register loads data into the controller data buffer, one word at a time. Reading the register reads data from the controller data buffer. The commands INIT, CLL and SRC clears the Data Buffer address allowing writing or reading of the Data Buffer starting at location 0. Reading from or writing into the buffer will increment the address register.

MAINTENANCE REGISTER 1
776 466



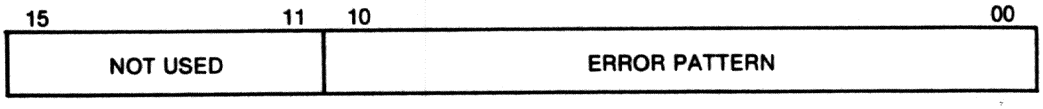
BIT(S)	DEFINITION
00-02	FIRMWARE MODEL—These three bits define the model number of the firmware used in the controller.
03-15	SPARE—ALWAYS 0

ECC POSITION REGISTER
777 470 (RKECPS)



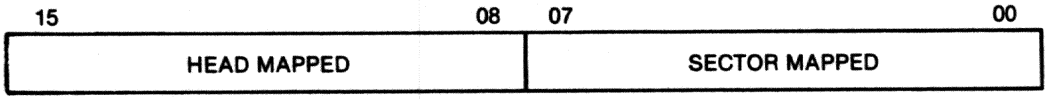
BIT(S)	DEFINITION
00-12	ERROR POSITION—These read-only bits define the start location of an error burst (containing from one to eleven error bits) within a 256-word data field, sequence. The position is valid if the error is ECC correctable.
13-15	SPARE—ALWAYS 0

ECC PATTERN REGISTER
777 472 (RKECPT)



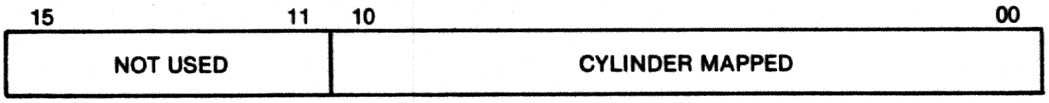
BIT(S)	DEFINITION
00-10	ERROR PATTERN—These are read-only bits that provide an 11-bit correction pattern for an error burst that does not exceed 11 error bits in length and is therefore ECC correctable.
11-15	SPARE—ALWAYS 0

MAINTENANCE REGISTER 2
777 474 (RKMR2)



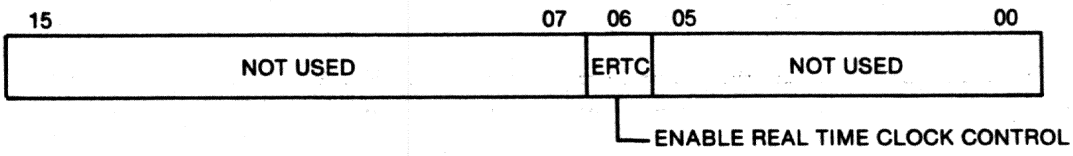
BIT(S)	DEFINITION
00-07	SECTOR MAPPED—These bits define the actual mapped sector address in the disc as opposed to the emulated address.
08-15	HEAD MAPPED—These bits define the actual mapped head address on the disc as opposed to the emulated address.

MAINTENANCE REGISTER 3
777 476



BIT(S)	DEFINITION
00-10	CYLINDER MAPPED—These bits define the actual mapped cylinder address on the disc as opposed to the emulated address.
11-15	SPARE—ALWAYS 0

ENABLE REAL TIME CLOCK CONTROL REGISTER
777 546



The Enable Real Time Clock Control register performs a separate function from the other registers. During a read operation, bit 06 is always reset. During a write operation bit 06 is set enabling the real time clock control. Switch S9 must be ON to enable this function.