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DILOG

INSTRUCTION MANUAL

FOR

MODEL DU130

MAGNETIC TAPE COUPLER

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INSTRUCTION MANUAL

FOR

MODEL DU130

MAGNETIC TAPE COUPLER

FORWARD

SECTIONS 1-4 of this Instruction Manual are intended to assist an operator in installing and operating a magnetic tape subsystem which includes a Distributed Logic Corporation magnetic tape coupler. The material assumes a knowledge of the instruction set and operating programs for the PDP-11 computer being used.

SECTION 5 contains a Theory of Operation. SECTION 6 contains Detailed Logic Drawings, and a Troubleshooting Guide. A second companion document entitled "Software Aids and Diagnostic" contains operating instructions and a listing for the DILOG-supplied diagnostic.

Prior to reading this guide, the user should become thoroughly familiar with the PDP-11 based hardware/software combination he is using, and be certain he has read the manuals on the tape formatter and transports with which the coupler is to be used.

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SECTION 1

GENERAL DESCRIPTION

1.0 INTRODUCTION

This material defines the functional characteristics of the Model DU130 magnetic tape coupler which, when used with any industry standard formatted magnetic tape drive, comprises a complete PDP-11 compatible 9 track magnetic tape subsystem. Magnetic tape drives from manufacturers other than DEC can be used while still retaining software and format compatibility with the DEC TM-11 tape system. The Model DU130 is completely contained on one quad module that occupy one SPC slot in the backplane. Data transfers are via the DMA facility of the PDP-11. Transfer rates vary, depending upon the density and speed of the drives included in the system, between 10,000 and 200,000 characters per second.

Up to two embedded-formatter tape drives or external stand-alone tape formatters may be connected to the Model DU130. Each embedded-formatter tape drive is capable of handling an additional three slave drives. All industry standard external stand alone formatters are capable of handling four drives. The Model DU130 can accommodate up to eight drives.

The optimal usage of the Model DU130 is in situations where 9 track, dual density, 800/1600 bpi tape recording capabilities are required; however, the Model DU130 is compatible with single density 800 or 1600 bpi embedded-formatter tape drives or stand alone external formatters. In cases where single density 800 bpi NRZI format is the only density required, the Model DU120 magnetic tape coupler should be considered.

The primary functions of the Model DU130 coupler in a magnetic tape subsystem are to buffer and interlock data and status transfers between the computer I/O bus and the tape formatter, and to translate CPU commands into tape formatter control signals such as START, STOP, REWIND, GENERATE IR GAP, GENERATE EOF GAP, etc. The primary function of the formatter, is to control tape motion, establish data format, and perform error checking. The overall tape control function is a combination of the coupler functions which are related to the PDP-11 and the formatter functions which are related to the tape drives.

A microprocessor is the sequence and timing center of the coupler. The control information is stored as firmware instructions in Read Only Memory (ROM) on the coupler board. One section of the ROM contains a diagnostic program that tests the functional operation of the coupler. This self test is performed automatically each time power is applied or whenever an INIT command is issued on the CPU I/O bus. A green diagnostic indicator on the board lights if self test passes.

Two additional indicators on the coupler board display dynamic operating conditions to an operator. The conditions displayed are Coupler Busy and Coupler Transferring Data (DMA Busy).

The coupler is connected to a tape formatter via a ribbon cable which plugs into two 50-pin 3M connectors located near the top at the center of the coupler.

1.1 General Description

The DU130 magnetic tape coupler links a PDP-11 computer to one or two tape formatters (embedded or stand alone). The formatter permits information to be read and written on tape between the PDP-11 system and other computers, either small or large scale, and of various manufacturers (DEC, IBM, Data General, Honeywell, etc.). The coupler performs the following major functions:

a. Buffers and interlocks data and status transfers across the computer I/O bus.

b. Translates computer command words into single commands or strings of commands to the tape formatter.

The formatter in a system performs the following major functions:

a. Controls the timing and the format of data transfers to the tape units.

b. Monitors the status of the tape units and the quality of the data transferred onto the tape and presents this information to the coupler.

c. Generates all discrete control signals to the tape units.

Each formatter can link up to four tape units to the computer in various configurations. Figure 1-1a illustrates a simplified system using embedding-formatter tape transports, and Figure 1-1b a system using stand along formatters.

A high-speed microprocessor is the control and timing center of the coupler. PROMs on the coupler board provide control instructions for the microprocessor, contain configuration-control information, and serve as general purpose logic elements. The microprocessor also permits an automatic self test of the coupler.

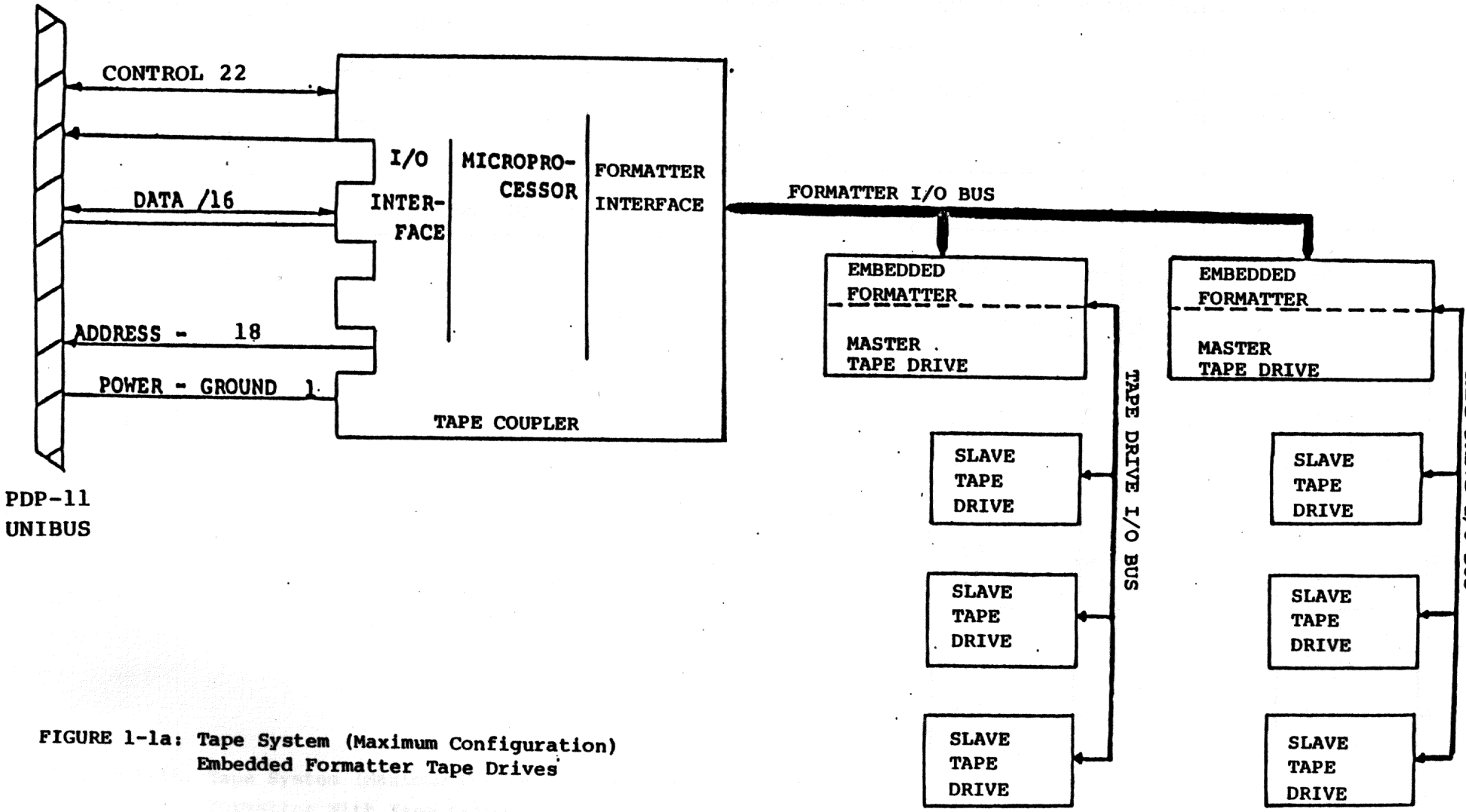


FIGURE 1-1a: Tape System (Maximum Configuration)
Embedded Formatter Tape Drives

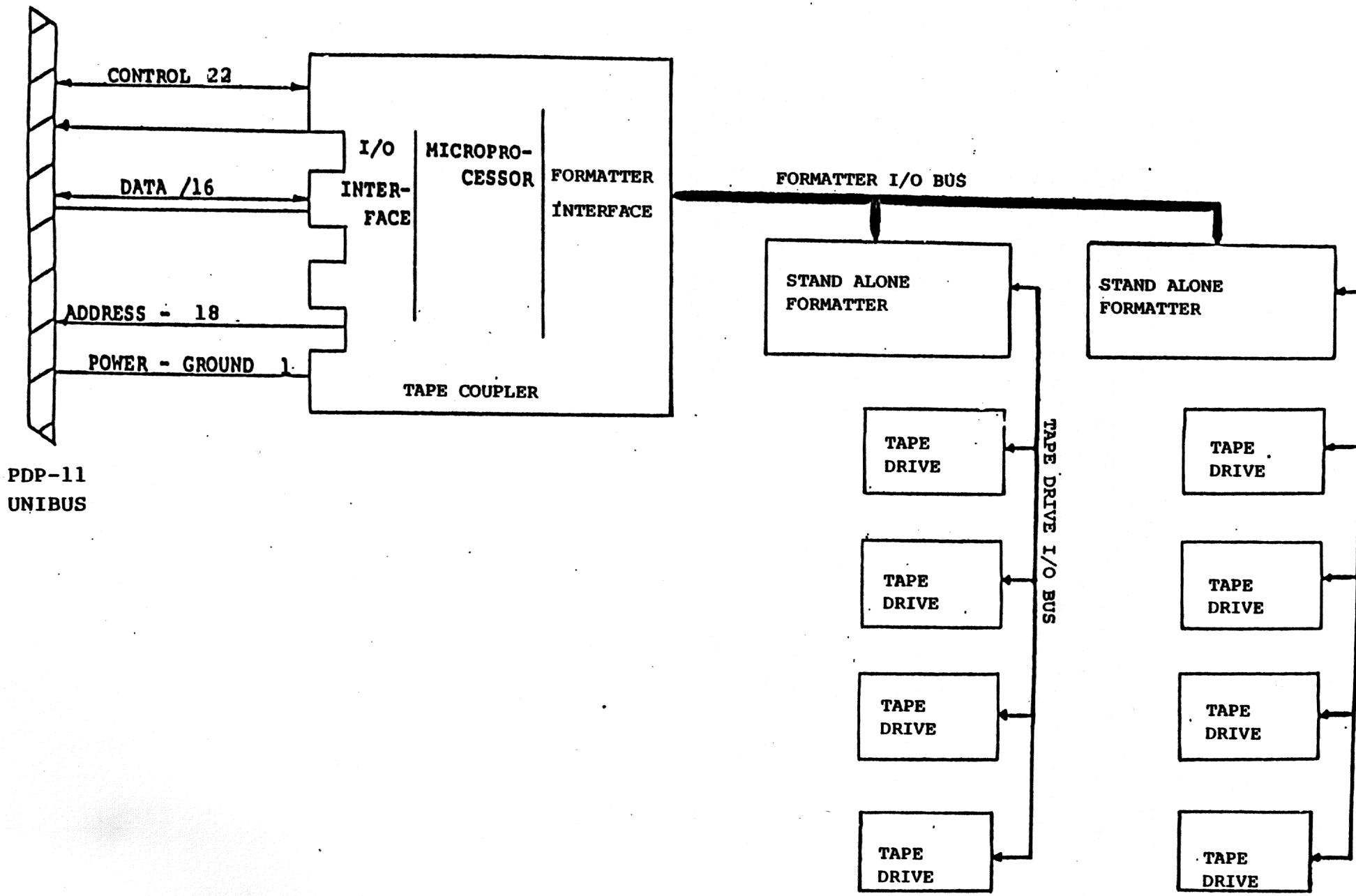


FIGURE 1-1b: Tape System (Maximum Configuration) Stand Alone Formatter With Tape Drives.

1.1.1 PDP-11 UNIBUS Interface

Commands, data, and status transfers between the coupler and the computer are executed via the parallel I/O bus (UNIBUS) of the computer. Data transfers are direct to memory via the NPR facility of the UNIBUS; commands and status are under programmed I/O interrupt control. Data transfer rates are from 5,000 to 100,000 16-bit words per second, depending upon tape packing density and tape drive speed. Coupler/UNIBUS interface lines are listed in Table 1-1.

1.1.2 Interrupt

The interrupt vector address is factory set to address 224, which is compatible with TM-11 software. Interrupts are generated when processor attention is required or when an error occurs.

1.1.3 Formatter Interface

The coupler interfaces with the tape formatter through two 50-pin 3M connectors at the top, center of the coupler board. Two formatters are connected to the coupler in a daisy-chain manner. The maximum cable length from the coupler to the last formatter in a string is 25 feet. Coupler to formatter interface lines are listed in Table 1-2.

TABLE 1-1: COUPLER/UNIBUS INTERFACE LINES

BUS PIN	MNEMONIC	DESCRIPTION
CA1	NPG IN	Non processor grant in
CB1	NPG OUT	Non processor grant out
CD2	D15L	Data line bit 15
CE2	D14L	Data line bit 14
CF2	D13L	Data line bit 13
CH2	D12L	Data line bit 12
CH1	D11L	Data line bit 11
CJ2	D10L	Data line bit 10
CK2	D09L	Data line bit 9
CL2	D08L	Data line bit 8
CM2	D07L	Data line bit 7
CN2	D04L	Data line bit 4
CP2	D05L	Data line bit 5
CR2	D01L	Data line bit 1
CS2	D00L	Data line bit 0
CT2	D03L	Data line bit 3
CU2	D02L	Data line bit 2
CV2	D06L	Data line bit 6
DD2	BR7L	Bus request 7
DE2	BR6L	Bus request 6
DF2	BR5L	Bus request 5
DH2	BR4L	Bus request 4
DJ2	BR OUT	Bus request out
DK2	BK17 (D01L2)	Bus grant dn 7
DL1	INIT L	Initiate
DL2	BG07	Bus grant bit 7 out
DM2	BG16	Bus grant bit 6 in
DN2	BG06	Bus grant bit 6 out
DP2	BGI5	Bus grant bit 5 in
DR2	BG05	Bus grant bit 5 out
DS2	BGI4	Bus grant bit 4 in
DT2	BG04	Bus grant bit 4 out

TABLE 1-1: COUPLER/UNIBUS INTERFACE LINES (continued)

BUS PIN	MNEMONIC	DESCRIPTION
DW2	BGIN	Bus grant in
DV2	BGOUT	Bus grant out
EC1	A12L	Address bit 12
ED2	A15L	Address bit 15
ED1	A17L	Address bit 17
EE1	MSYNL	Master sync
EE1	A16L	Address bit 16
EF1	A02L	Address bit 2
EH1	A016	Address bit 1
EH2	A00L	Address bit 0
EJ1	SSYNL	Slave sync
EK1	A14L	Address bit 14
EK2	A13L	Address bit 13
EL1	A11L	Address bit 11
EN2	A08L	Address bit 8
EP1	A10L	Address bit 10
EP2	A07L	Address bit 7
ER1	A09L	Address bit 9
EV1	A06L	Address bit 6
EV2	A04L	Address bit 4
EV1	A05L	Address bit 5
EV2	A03L	Address bit 3
EJ2	C0L	Control bit zero
EF2	C1L	Control bit one
FD1	BBSY	Bus busy
FJ1	NPR	Non processor request
FF1	ID05	Interrupt vector bit 5
FF2	ID06	Interrupt vector bit 6
FH1	ID07	Interrupt vector bit 7
FK1	ID08	Interrupt vector bit 8
FM1	INTR	Interrupt
FT2	SACK	Select acknowledge

TABLE 1-2A: COUPLER TO FORMATTER INTERFACE LINES

Coupler Connector J4 to P4 (Cipher, Pertec) to J124 (Tandberg, CDC) to J4 (Digi-Data), To J1 (F880)

J4 SIGNAL	J4 GROUND	MNENONIC	DESCRIPTION
2	1	FFBY	Formatter Busy
4	3	FLWD	Last Word
6	5	DWD4	Write Data 4
8	7	FGO	Initiate Command
10	9	FWDO	Write Data 0
12	11	FWD1	Write Data 1
14	13	FSGL	Not Used
16	15	FLOL	Load on Line
18	17	FREV	Reverse/Forward
20	19	FREW	Rewind
22	21	FWDP	Not Used
24	23	FWD7	Write Data 7
26	25	FWD3	Write Data 3
28	27	FWD6	Write Data 6
30	29	FWD2	Write Data 2
32	31	FWD5	Write Data 5
34	33	FWRT	Write/Read
36	35	FRTH2	Read Threshold 2
38	37	FEDIT	EDIT
40	39	FERASE	Erase
42	41	FWFM	Write File Mark
44	43	FRTH1	Read Threshold 1
45*		FPAR	Parity Select
46	45	FTADO	Transport Address 0
48	47	FRD2	Read Data 2
50	49	FRD3	Read Data 3

*Grounded except when working with 7 track formatter

TABLE 1-2B: COUPLER TO FORMATTER INTERFACE LINES

Coupler J5 to P5 (Pertec, Cipher) to J12-5 (Tandberg, CDC)to J3 (Digi-Data), J2 (F880)

J5 SIGNAL	J5 GROUND	MNEMONIC	DESCRIPTION
1		FRDP	Read Data Parity
2		FRD0	Read Data 0
3		FRD1	Read Data 1
4		FLDP	Loan Point
6	5	FRD4	Read Data 4
8	7	FRD7	Read Data 7
10	9	FRD6	Read Data 5
12	11	FHER	Hard Error
14	13	FFMK	File Mark
16	15	FCCG/ID	CCG/IDENT
18	17	FFEN	Formatter Enable
20	19	FRD5	Read Data 5
22	21	FEOT	End of Tape
24	23	FOFL	Off Line
26	25*	FNRZ	NRZI
25*		F7TR	7 Track
28	27		Ready
30	29	FRWD	Rewinding
32		FFPT	File Protect
34	33	FRSTR	Read Strobe
36	35	FDWDS	Demand Write Data Strobe
38	37	FDBY	Data Busy
40	39	FSPEED	Speed
42	41	FCER	Corrected Error
44	43	FONL	On-Line
46	45	FTAD1	Transport Address 1
48	47	FFAD	Formatter Address
50	49	FDEN	Density Select

*Grounded except for 7 track formatter

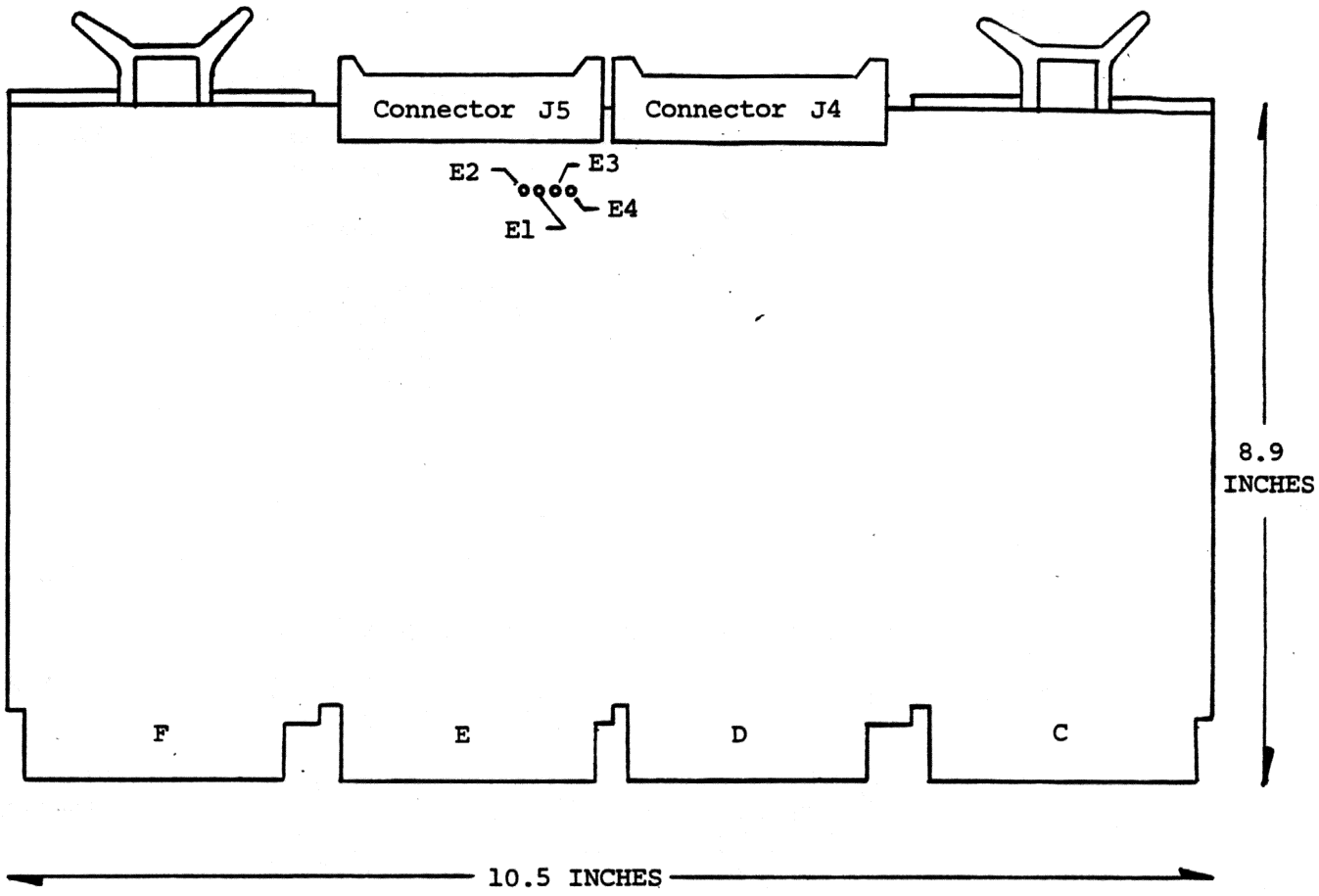


Figure 1-2: Coupler Board Configuration

1.2 Tape System General Specifications

DATA FORMAT

Industry standard non-return-to-zero (NRZ) or Phase Encoded (PE) recording.

9 tracks

Recording densities:
800 characters per inch
1600 characters per inch
800/1600 characters per inch

Interrecord gap 0.60 inch min.

Tape parity marks: LPC, CRC, LRC

MEDIA CHARACTERISTICS

TYPE

½" wide mylar base, oxide coated, magnetic tape.

REEL SIZE

7", 8½", or 10½" diameter tape reels containing 600, 1,200 and 2,400 feet of tape respectively.

DATA CAPACITY (megabytes)

Assumes approximate 80% recording efficiency:

		800 CPI	1600 CPI
600 Ft.	=	5.75	11.5
1,200 Ft.	=	11.5	23.0
2,400 Ft.	=	22.0	44.0

DATA TRANSFER RATE (Characters/Second)

		800 CPI	1600 CPI
12.5 ips	=	10,000	20,000
25.0 ips	=	20,000	40,000
37.5 ips	=	30,000	60,000
45.0 ips	=	36,000	72,000
75.0 ips	=	60,000	120,000
125.0 ips	=	100,000	200,000

REGISTER ADDRESS

Status (MTS) 772 520
Command (MTC) 772 522
Byte Record Counter (MTBRC) 772 524
Current Memory Address (MTCMA) 772 526
Data Buffer (MTD) 772 530
Tape Read Lines (MTRD) 772 532

COMPUTER I/O INTFC.

Interrupt Vector Address 224. NPR data transfer. 1 bus load.

COUPLER/FORMATTER INTERFACE	Coupler is compatible with formatters manufactured by Pertec, Kennedy, Tandberg, Cipher, CDC, Digi-Data.
PACKAGING	The coupler is completely contained on one quad module 10.44 inches wide by 8.88 inches deep.
DOCUMENTATION	One Instruction Manual is supplied with the coupler.
SOFTWARE	One diagnostic routine with object listing is supplied with a coupler (or the first of a series of couplers).
POWER	+5, $\pm$0.25 VDC at 3.6 amps, from computer backplane.
ENVIRONMENT	Operating temperature 50^{o}F to 140^{o}F* Operating humidity 0% to 90% non-condensing.*

*NOTE: The quality of recording and reading information on magnetic tape is affected by temperature and humidity. The area where the tape is used should be maintained within the following limits:

Temperature: 15^{o}C to 32^{o}C
Humidity: 20% to 80%

SHIPPING WEIGHT 5 pounds including documentation.

SECTION 2

INSTALLATION

2.0 INTRODUCTION

The padded shipping carton that contains the coupler board also contains an instruction manual and cable set to the first formatter (if this option is exercised). The coupler is completely contained on the quad-size printed circuit board. The formatter and/or tape drive, if supplied, is contained in a separate shipping carton.

CAUTION: IF DAMAGE TO ANY OF THE COMPONENTS IS NOTED, DO NOT INSTALL! IMMEDIATELY INFORM THE CARRIER AND DILOG.

Installation instructions for the formatter and tape drive are contained in the formatter or tape manuals.

2.1 Installation

To install the coupler module, proceed as follows:

CAUTION: REMOVE DC POWER FROM COMPUTER CHASIS BEFORE INSERTING OR REMOVING COUPLER MODULE!

DAMAGE TO THE BACKPLANE ASSEMBLY AND THE COUPLER MODULE WILL OCCUR IF THE COUPLER MODULE IS PLUGGED IN BACKWARDS!

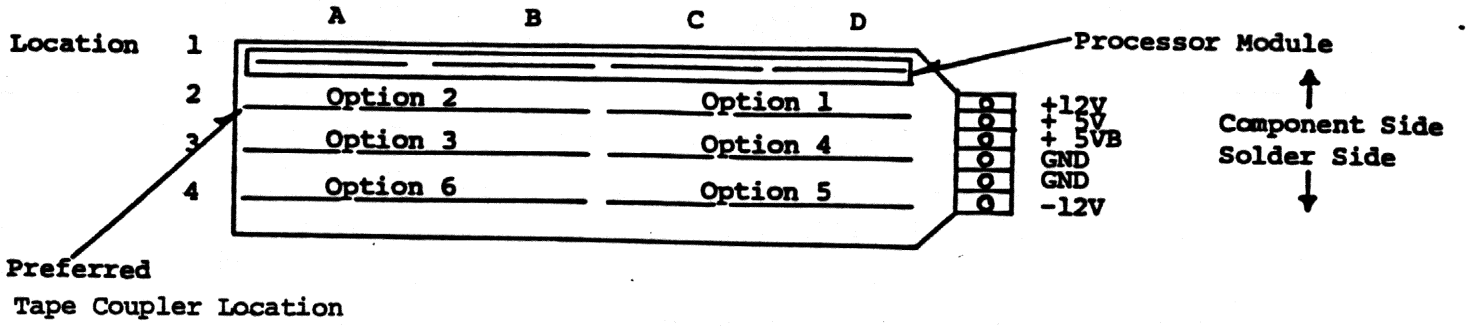
1. Select the backplane Small Peripheral Controller (SPC) location into which the coupler is to be inserted. SPC locations are connectors C, D, E, and F of slots 1 through 9 of the backplane assembly.

   Several backplane assemblies exist depending on the type of system. Note that the processor module is always installed in the first location of the backplane or the first location in the first backplane of multiple backplane systems.

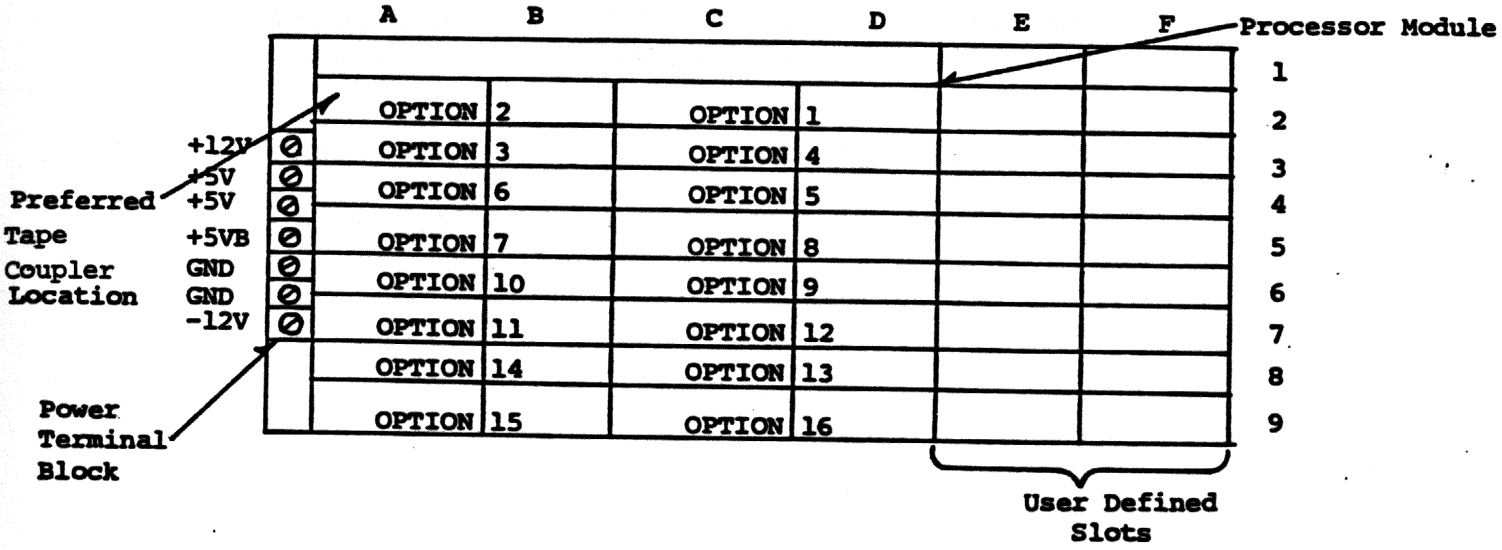
2. To use the NPR facility required with the coupler, the backplane wiring of the SPC slot must be modified. The modification is as follows:

   Remove the wire on the connector C between A1 and B1 of the slot into which the coupler is to be plugged. This allows the non-processor grant priority line to be carried through the coupler.

   Note that any connector rows which do not have a card installed, must have a bus grant jumper card installed in the D slot to continue the bus grants to other devices in the UNIBUS.



H9270 MODULE INSERTION SIDE



DDV11-B Backplane Module Insertion Side

NOTE: Memory can be installed in any slot; it is not priority dependent and does not need to be adjacent to the processor.

Figure 2-1 Typical Backplane Configurations

On older PDP-11 backplanes, the following additional wiring changes may be necessary if Pin 1 AU1 is directly connected to Pin 4 AU1 of the system unit into which the coupler is to be installed:

Remove wire between 1 AU1 and 4 AU1.

At the coupler slot, connect 1 AU1 to CA1 and 4 AU1 and CB1.

3. If a streamer type tape transport is to be used, cut the etch on the bottom side of the coupler between E1 to E2 and E3 to E4. Add a jumper from E2 to E3.

4. Insert the coupler into the selected backplane position. Be sure the coupler is installed with the components facing Row One (1).

   The coupler module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane, then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

5. Feed the module connector end of the formatter I/O ribbon cable set into the computer module area. Install the cable connectors into module connectors J4 and J5. Verify that the connector is firmly seated. NOTE that ribbon cable connectors are not keyed and therefore CAN be plugged in backwards. The connectors have a triangle marked on one end to identify Pin 1. These triangles on the cable and controller connectors MUST be lined up.

6. Connect the tape formatter end of the I/O ribbon cables to the formatter I/O connectors. Refer to Table 1-2.

7. If the formatter is equipped with a 100-pin connector, adapter Part No. ACC993A must be used to convert the 100-pin connector to two 50-pin connectors.

8. Apply power to the computer and verify that the green DIAGnostic LED indicator on the controller board is lighted. If the DIAG LED is not lighted, power is not applied to the coupler, the coupler board is bad, or the LED is bad.

9. Refer to the tape drive manual for operating instructions and apply power to the tape drive. Install a known good reel of tape on the tape drive and place the tape drive ON LINE.

10. Place the computer in the HALT mode to enable ODT. Using the computer terminal examine location 772 520. The contents of this location should be 000 141. These are the tape drive status bits signifying: ON LINE, BEGINNING OF TAPE, and TAPE READY.

11. Using the computer console device, deposit 60007 into location 772 522. The tape should move forward approximately 6 inches and stop. A file mark should have been written on the tape. Examine location 772 520. The contents of this location should be 040 101 signifying that a file mark has been written and detected.

12. Refer to the DILOG software manual and run the diagnostics.

13. The tape system is now ready for data transfer operations.

SECTION 3

OPERATION

3.0 INTRODUCTION

Prior to operating the system, the instruction manual sections describing the controls and indicators on the tape drive and procedures for mounting and removing tape reels should be given to handling and magnetic tape to prevent loss of data or damage to the tape handling equipment. The following precautions should be observed.

a. Always handle a tape reel by the hub hole. Squeezing the reel flanges can cause damage to the tape edges when winding or unwinding tape.

b. Never touch the portion of tape between the BOT and EOT markers. Oils from fingers attract dust and dirt. Do not allow the end of the tape to drag on the floor.

c. Never use a contaminated reel of tape. This spreads dirt to clean tape reels and can affect tape drive operation.

d. Always store tape reels inside their containers. Keep empty containers closed so dust and dirt cannot get inside.

e. Inspect tapes, reels, and containers for dust and dirt. Replace Take-up reels that are old or damaged.

f. Do not smoke near the tape drive or tape storage area. Tobacco smoke and ash are especially damaging to tape.

g. Do not place the tape drive near a line printer or other device that produces paper dust.

h. Clean the tape path frequently.

Note that tape drives permit off-line or on-line operation. The off-line mode is controlled by switches on the tape drive. The on-line mode is controlled by programmed commands from the computer via the coupler and formatter. When system operation is desired, be sure the tape drive on-line indicator is lit. On-line operation is a function of program commands described in SECTION 4 of this manual.

3.1 Tape Format

For detailed information on tape format characteristics see formatter and tape drive manuals.

3.2 Booting From Magnetic Tapes

1. Place the tape transport "ON LINE" and position the tape at "Beginning of Tape".

2. If the CPU is equipped with a hardware bootstrap, simply type "MTO" CR . If no hardware bootstrap is installed, proceed with the following steps.

3. Load Register location 772522_8 with 10000_8.

4. Load Register location 772524_8 with 177777_8.

5. Load Register location 772522_8 with 60011_8. The tape will jump forward and halt.

6. Load Register location 772522_8 with 60003_8. The tape will jump forward and halt.

7. Load PC (777707_8) with 0.

8. Start the CPU from location zero.

SECTION 4

PROGRAMMING

NOTE: For purposes of discussion in this section, whenever the tape "CONTROLLER" or "CONTROL UNIT" is referred to the terms "CONTROLLER" or "CONTROL UNIT" refer to the coupler/tape formatter functional combination.

4.1 Programming Definitions

FUNCTION: The expected activity of the tape system (read, write, rewind).

COMMAND: The instruction which initiates a function (GO, Select).

INSTRUCTION: One or more orders executed in a prescribed sequence that cause a function to be performed.

ADDRESS: The binary code placed on the BDAL0-15 lines by the bus master to select a register in a slave device. Note that "register" can be either discrete elements (flip-flops) or memory elements (core, solid state RAM or ROM). When addressing devices other than computer internal memory, i.e., peripheral device registers, the upper 4K (28-32K) address space is used.

REGISTER: An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system.

4.2 Tape Controller Functions and Registers

The tape controller performs eight functions. A function is initiated by a GO command after the processor has issued a series of instructions that store function-control information into controller registers. To accept a command, and perform a function, the controller must be properly addressed and the tape drives must be powered up, at operational speed, and be ready.

All software interaction between the tape controller, the processor, and processor memory is accomplished by six registers in the tape controller. These registers are assigned memory addresses and can be read or written into (except as noted) by instructions that reference respective register addresses. The six controller registers, their addresses, mnemonics, and their bit assignments are shown in Figure 4-1.

REGISTER	ADDRESS	MSB 15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	LSB 00
BIT POSITION																	
Status (MTS)	772 520	ILL COM	EOF		PRE	BGL	EOT	RLE		NX M	SE LR	BOT	7 CH	SD WN	WRL	RWS	TUR
Command (MTC)	772 522	ERR	DEN 8	DEN 5	PWR CLR	PE VN	US 2	US 1	US 0	CU R	INT ENB	XBA 17	XBM 16	FU 2	FU 1	FU 0	GO
Byte Record Counter (MTBRC)	772 524	15															00
Current Memory Address (MTCMA)	772 526	CM 15	CM 14	CM 13	CM 12	CM 11	CM 10	CM 09	CM 08	CM 07	CM 06	CM 05	CM 04	CM 03	CM 02	CM 01	CM 00
Data Buffer (MTD)	772 530								DB 08	DB 07	DB 06	DB 05	DB 04	DB 03	DB 02	DB 01	DB 00
Tape Read Lines (MTRD)	772 532	TIMER	CRC/ LPC		GS				P	CH 0	CH 1	CH 2	CH 3	CH 4	CH 5	CH 6	CH 7

FIGURE 4-1 Coupler Register Configuration

4.2.1 Status Register (MTS)

The address of the MTS register is 772 520. MTS is a read only register. The functions of the bits of this register are as follows:

BIT 15 - ILLEGAL COMMAND: Set by any of the following illegal commands:

1. Any DATO or DATOB to the command register during the tape operation period.

2. A write, write EOF, or write with extended IRG operation when the File Protect bit is a 1.

3. A command to a tape unit whose Select Remote bit is 0.

4. The Select Remote (SELR) bit becoming a 0 during an operation.

In error conditions 1 through 3, the command is loaded into the MTC, but the GO Pulse to the tape unit is not generated. In addition, the CU ready bit remains set.

BIT 14 - END OF FILE (EOF): Set when an EOF character is detected during a read, space forward, or space reverse operation. During the read or space forward operation, the EOF bit is set when the LPC (longitudinal parity check) character following the EOF character is read. During a space reverse operation, the EOF bit is set when the EOF character following its LPC character is read. The ERR bit sets when the LPC character strobe is generated with the File Mark signal upon EOF detection.

BIT 13 - NOT USED

BIT 12 - HARD ERROR (HE): Set as the result of an error being detected on tape.

For all errors, the ERR bit sets at the end of the record. Both lateral and longitudinal parity errors are detected during a read, write, write EOF and write with extended IRG operations. The entire record is checked including the CRC and LOC characters. During a write operation a correctable error in the PE (1600 bpi) mode will set this bit.

BIT 11 - BUS GRANT LATE (BGL): Set when the control unit, after issuing a request for the bus, does not receive a bus grant before the controller receives the bus request for the following tape character. The condition is tested only for NPR (non-processor request) operations. The ERR bit sets simultaneously with BGL, thus terminating the operation. If the BGL occurred during a write or write with extended IRG operation, the control unit does not send the signal WDS to the master, while the master writes the CRC character (if required) and LPC character onto the tape, terminating the record.

BIT 10 - END OF TAPE (EOT): Set when the EOT marker is read while the tape is moving in the forward direction. The bit is cleared as soon as the same point is read while the tape is moving in the reverse direction. The ERR bit, as a result of the EOT bit at a 1, sets only in the tape forward direction and coincidentally with the reading of an LPC character.

BIT 9 - RECORD LENGTH ERROR (RLE): Detected only during a read operation. It occurs for long records only and is indicated as soon as MTBRC increments beyond 0, at which time both data transfer into memory and incrementing of the MTCMA and MTBRC stop.

However, the control unit reads the entire record and sets the ERR bit when the LPC character is read. CU ready remains at 0 until the LPC character is read.

BIT 8 - BAD TAPE ERROR (BTE): NOT USED

BIT 7 - NON-EXISTENT MEMORY (NXM): Set during NPR operations when the control unit is bus master, and is performing data transfers into and out of the bus when the control unit does not receive a slave SYNC signal within 10 microseconds after it had issued a master sync signal. The operations which occur when the error is detected are identical to those indicated for the BGL error.

BIT 6 - SELECT REMOTE (SELR): Cleared when the tape unit addressed does not exist, is offline, or has its power turned off.

BIT 5 - BEGINNING OF TAPE (BOT): Set when the BOT marker is read, and cleared when the BOT marker is not read. BOT at a 1 does not produce a 1 in the ERR bit.

BIT 4 - SEVEN CHANNEL (7CH): Set to indicate a 7-channel tape unit; cleared to indicate a 9-channel unit.

BIT 3 - TAPE SETTLE DOWN (SDWN): Set whenever the tape unit is slowing down. The master will accept and execute any new command during the SDWN period except if the new command is to the same tape unit as the one issuing SDWN and if the direction implied in the new command is opposite to the present direction.

BIT 2 - WRITE LOCK (WRL): Set to prevent the control unit from writing information on tape. Controlled by presence or absence of the write protect ring on the tape reel.

BIT 1 - REWIND STATUS (RWS): Set by the master as soon as it receives a rewind command from the control unit. Cleared by the master as soon as the tape arrives at the BOT marker in the forward direction. (It overshoots BOT in the reverse direction)

BIT 0 - TAPE UNIT READY (TUR): Set when the selected tape unit is stopped and when the SELECT REMOTE is false. Cleared when the processor sets the GO bit and the operation defined by the function bit occurs.

4.2.2 Command Register (MTC)

The address of MTC is 772 522. The functions of the bits of this register are as follows:

BIT 15 - ERROR (ERR): Set as a function of bits 7-15 of the Status Register MTS. Cleared on INIT or on the GO command to the tape unit.

BITS 14-13 - DENSITY (DEN 8, DEN 5): NOT USED. Not applicable on 9 track tape.

BIT 12 - POWER CLEAR (PCLR): Provides the means for the processor to clear the control unit and tape units without clearing any other device in the system. The PCLR bit is always read back by the processor as 0.

BIT 11 - LATERAL PARITY (PEVN): Not applicable for 9 track tape.

BIT 10 - UNIT SELECT 2: Specifies one of two possible formatters. Selects the high-speed streaming mode on streamer type tape transport.

BITS 9-8 - UNIT SELECT 1: Specifies one of the four possible magnetic tape units. All operations defined in the MTC and all status conditions defined in the MTS pertain to the unit indicated by these bits. Cleared on INIT.

BIT 7 - CU READY (CUR): Cleared at start of a tape operation, and set at end of tape operation. The control unit accepts as legal, all commands it receives while the CU Ready bit is 1.

BIT 6 - INTERRUPT ENABLE (INT ENB): When set, an interrupt occurs whenever either the CU ready bit or the ERR bit change from 0 to 1 or whenever a tape unit that was set into rewind has arrived at the beginning of tape. In addition, an interrupt occurs on an instruction that changes the INT ENB from 0 to 1 and does not set the GO bit i.e., CU READY or ERROR = 1.

BITS 5-4 - ADDRESS BITS: Extended memory bits for an 18-bit bus address. Bit 5 corresponds to XBA17, and bit 4 to XBA16. They are an extension of the MTCMA, and increment during a tape operation if there is a carry out of MTCMA.

BITS 3-1 - FUNCTION BITS: Selects 1 of 8 functions (programmable commands).

BIT 3	BIT 2	BIT 1	
0	0	0	Off line
0	0	1	Read
0	1	0	Write
0	1	1	Write EOF
1	0	0	Space Forward
1	0	1	Space Reverse
1	1	0	Write with Extended Interrecord Gap
1	1	1	Rewind

BIT 0 - GO: When set, begins the operation defined by the function bits.

4.2.3 Byte Record Counter (MTBRC) (The address of MTBRC is 722 524)

The MTBRC is a 16-bit binary counter which is used to count bytes in a read, write, or write with extended IRG operation, or records in a space forward of space reverse operation. When used in a write or write with extended IRG Operation, the MTBRC is initially set by the program to the 2's complement of the number of bytes to be written on tape. The MTBRC becomes 0 after the last byte of the record has been read from memory. Thus, when the next WDS (Write Data Strobe) signal occurs from the master, the control unit will not send the WDR (Write Data Request) to the master indicating that there are no more data characters in the record.

When the MTBRC is used in a read operation, it is set to a number equal or greater than the 2's complement of the number of bytes to be loaded into memory. A record length error (RLE) occurs for long records only, and is indicated when a read pulse for data (RDS occurring when CRCS or LPCS does not occur) occurs when the MTBRC is 0. The MTBRC increments by 1 immediately after each memory access.

When the MTBRC is used in a space forward or space reverse operation, it is set to the 2's complement of the number of records to be spaced. It is incremented by a 1 at LPC time, whether the tape is moving in the forward or reverse direction. A new GO pulse is sent to the tape unit during the SDWN time if the MTBRC is not 0 during that time. When the tape unit is moving in reverse, the LPC character is detected before SDWN, but before the entire record has been traversed. Thus, both SDWN and LPC character appear to be in different positions on tape from those when the tape unit is moving forward.

4.2.4 Current Memory Address Register (MTCMA) (The address of MTCMA is 772 526).

The MTCMA contains 16 of the possible 18 memory address bits. It is used in NPR operations to provide the memory address for data transfers in read, write, and write with extended IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation, or from which the first byte is read in a write, or write extended IRG operation. The MTCMA is incremented by 2 immediately after each memory access. Thus, at any instant of time, the MTCMA points to the next higher address than the one which had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address plus 2 of the last characters in the record. In the error conditions Bus Grant Late (BGL) and Non-Existent Memory (NXM), the MTCMA contains the address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI except bit 0 which always reads as a zero under program control. Bit 0 can be asserted during NPR's to determine the selected byte. The bits are set or cleared on a processor DATO. INIT clears all bits in the MTCMA.

4.2.5 Data Buffer (MTD) (The address of MTD is 772 530).

The data buffer is an 9-bit register which is used during a read, write, or write with extended IRG operation. In a read operation, the data buffer is a temporary storage register for characters read from tape before being stored into memory. In a processor read, all nine bits are stored into memory. Bits 0 through 7 in memory correspond to channels 7 through 0 respectively from tape, and bit 8 corresponds to the parity bit. In a DMA operation only the data bits are read into memory, and are alternately stored into the low and high bytes. In a write or write with extended IRG operation, the data buffer is a temporary storage register for characters read from core memory before they are written on tape.

In a read operation, the LPC character enters the data buffer when bit 14 of MTRD is a 1, and inhibited from doing so when bit 14 is a 0. Thus, after reading a nine-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the CRC character when bit 14 is 0. After reading an EOF character, the data buffer contains all 0's when bit 14 is a 1 and the LPC character when bit 14 is 0. The MTD is available to the processor on a DATI. Bits 9 through 15 are read identically to bits 1 through 8 respectively. Bits 0 through 7 are set or cleared on a processor DATA. Bits 8 through 15 are not affected by a processor DATO. INIT clears all bits in the MTD.

4.2.6 Tape Read Lines (MTRD) (The address of MTRD is 772 532)

The memory locations allocated for the tape read lines are:

Bits 0-7 for the channels 7-0 respectively.
Bit 8 for the parity bit.
Bit 12 for the gap shutdown bit.
Bit 13 not used.
Bit 14 for the CRC, LPC character selector.
Bit 15 for the timer.

For correct longitudinal parity, bits 0-8 are 0 after writing a record or reading a record from tape. For a longitudinal parity error, one or more of the bits 0-8 remains at a 1, the bit(s) are at a 1 indicating the channel(s) containing the error which sets the CU ready bit. Thus, if the pulse is set during a tape operation, CU ready sets prematurely thus producing the gap shutdown period when characters are still being read. Bits 0-8 are set and cleared by the tape unit. Bit 14 is set and cleared by the processor and cleared by INIT. Bit 15 is uniquely controlled by the 100 microsecond timer. The MTRD is available to the processor on a DATO except that bit 13 reads back as a 0.

4.2.7 Timer

TIMER is a a 10 kHz signal with a 50% duty cycle. The signal is used for diagnostic purposes in measuring the time duration of the tape operations. The timer is read as bit 15 in the MTRD.

SECTION 5

TECHNICAL DESCRIPTION

5.0 INTRODUCTION

This section contains the theory of operation of the DU130 tape coupler The text references block and timing diagrams interspersed with text, a Glossary of Terms in Appendix B, and detailed logic diagrams in SECTION 6. The material begins with a General Description followed by a Functional Description.

The General Description describes the interconnection of the major logic elements that make up the coupler. The principal reference is the simplified block diagram. The Functional Description describes the individual logic elements within the coupler. The text is referenced to the detailed block diagram. The numbers in the corner of the boxes in the detailed block diagram refer to the schematic sheet showing the circuit. The description assumes an understanding of the PDP-11 I/O bus and a basic understanding of digital computer theory.

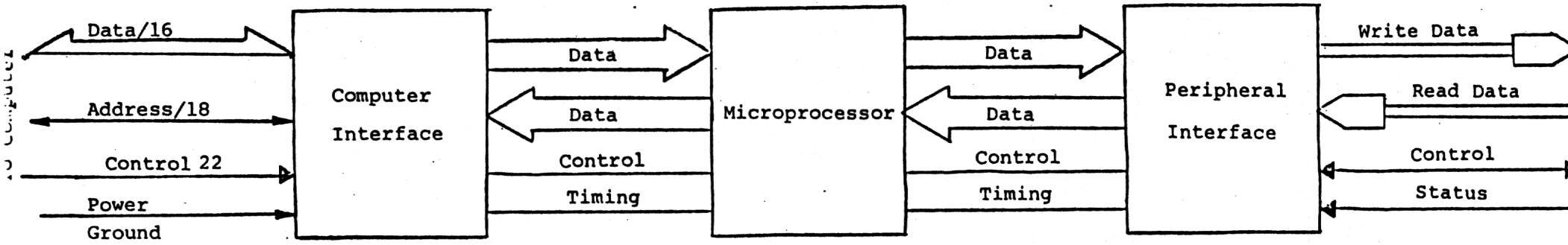
5.1 General Description

Figure 5-1 is a simplified block diagram of the coupler. The coupler comprises three logical sections:

a. Computer interface
b. Microprocessor
c. Formatter interface

The three sections function together to transfer data between the I/O bus of the computer and up to eight tape drives. The two interface sections match the voltage levels and load/drive characteristics of the computer I/O bus and tape I/O lines to the logic levels of the coupler. The microprocessor is the control, timing, and data conversion section of the coupler.

The microprocessor functions under control of firmware instructions stored in solid state, programmable, Read Only Memory (PROM). The microprocessor is implemented with AM2900-series bit-slice microprocessor chips. Refer to "MICROPROGRAMMING HANDBOOK" from Advanced Micro Devices, Inc., 1901 Thompson Place, Sunnyvale, California 94086 for introductory material on microprogramming a bipolar microprocessor.



- Buffer I/O Lines
- Bus Sequence (State processor)
- Address Decode

- Timing Source
- Control Center
- Error Checking
- Register Storage
- Data Buffering

- Buffer I/O Lines
- Set Tape Configuration
- Clock Synchronization

FIGURE 5-1: Simplified Block Diagram
Peripheral Controller

5.1.1 Computer Interface

The purpose of the computer interface is to (1) buffer lines between the UNIBUS of the computer and the controller and (2) synchronize information transfers. There are three major classes of lines connected to the computer interface:

a. Data lines
b. Address lines
c. Control lines

There are 16 bidirectional data lines between the UNIBUS and the controller, and 18 bidirectional address lines between the UNIBUS and the controller. The control lines request information transfers, select the type and direction of transfers, and synchronize the transfers. The control lines are unidirectional and originate either at the UNIBUS or at the controller.

Information transfers are initiated by a bus master placing an address on the address lines. The bus master then either received data from, or outputs data to, the addressed slave device (controller or memory). During initialization and status transfer sequences, the controller is a slave and is selected by address 224_8. During data transfer sequences, the controller is bus master and either receives data from or outputs data to the processor memory via the NPR facility.

The computer interface controls the synchronization or "bus arbitration" sequence. Bus synchronization is done by a state processor separate from the microprocessor to minimize bus use by the controller. This permits other devices to use the NPR facility on a time multiplexed basis with the tape controller.

5.1.2 Microprocessor

The microprocessor is the timing and control center of the controller. The microprocessor is controlled by instructions stored in programmable read only memory (PROM). These instructions, called firmware, cause the microprocessor to operate in a prescribed manner during each of the computer-selected functions. The functions are established by a series of instructions issued by the computer. The instruction operands are stored in registers within the microprocessor.

When a GO command is issued by the computer, the firmware microinstructions cause the registers to be examined and either a data transfer sequence or a rewind sequence to be performed. Note that rewind functions can be performed on any tape drive not involved in a data transfer operation simultaneous with data transfers.

The microprocessor contains an eight word RAM memory dedicated to buffering data between the UNIBUS and the microprocessor. This allows several NPR cycle requests to be missed without missing data words being transferred between the tape and computer memory.

The rate and order (format) at which data is transferred to the tape is controlled by the microprocessor. Within the microprocessor, data is handled in 8-bit parallel bytes. Error check bits are calculated (LRCC, CRCC) and supplied to the tape during a write function. During a read function, the microprocessor monitors the error check bits and the data being read. Discrepancies are flagged as errors to the computer. The microprocessor detects other types of errors during the transfer functions (data late, programming error, etc.) and monitors status lines from the tape for malfunctions within this assembly. All errors are assembled into a status word for access by the processor.

5.1.3 Peripheral Interface

The purpose of the peripheral interface is to match the characteristics of the tape drive to the characteristics of the microprocessor. The peripheral interface:

a. Contains line drivers and receivers that buffer the information lines between the coupler and the tape drives over cable lengths up to 20 feet.

b. Contains the PROM and switches that permit configuring the coupler to match the different tape subsystem configurations.

5.2 Functional Description

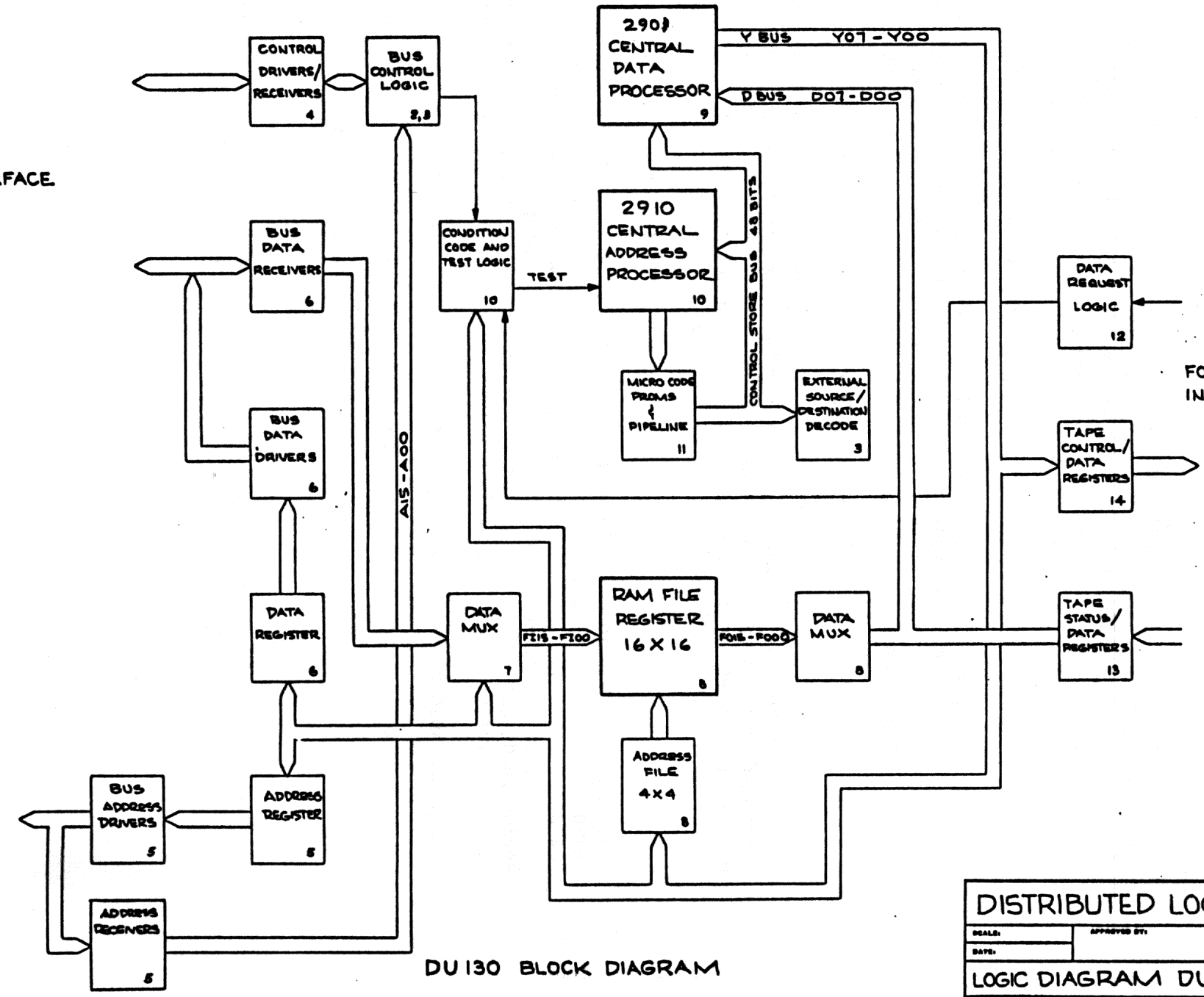
The detailed block diagram (Figure 5-2) shows the functional elements of the tape controller. A number within the blocks of the diagram references the sheet or the detailed logic drawing represented by the block. The detailed logic drawings are in SECTION 6. A Glossary of Terms, in Appendix B, defines the mnemonics used in this text and on the logic drawings.

5.2.1 Computer Interface

The computer interface comprises the following elements:

a. Data receiver/drivers
b. Control receiver/drivers
c. Address receiver/drivers
d. Bus and arbitration sequence

The computer interface is a hard-wired logic section that buffers and synchronizes information transfers between the I/O bus and the controller.



DU 130 BLOCK DIAGRAM

FIGURE 5-2

DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM DU130		SHT 1 OF 14
		DRAWING NUMBER 853019

5.2.1.1 Data Receiver/Drivers

The tristate receiver/driver circuits F15, F16, F17, and F18, shown on sheet 6, buffer data lines BUS DØØL - BUS D15L between the UNIBUS and the controller. Received data lines are identified as DBØØ-DB15, transmitted data lines are identified as TDØØ-TD15. The received data lines connect to the microdata file multiplexer (sheet 7).

5.2.1.2 Control Receiver/Drivers

The control lines between the I/O bus and the controller are buffered by circuits E6, E7, F3, F4, and F5 shown on sheet 4. The receivers are always connected to the bus. Most of the circuits are permanently enabled but circuit E7 is enabled by Address Control Enable $\overline{\text{ACEN}}$.

5.2.1.3 Address Receiver/Drivers (See sheet 5)

Tri-state receiver/driver circuits F6, F7, F8, and F9 buffer addresses between the UNIBUS and the controller. Addresses are enabled to the bus by Address Control Enable ($\overline{\text{ACEN}}$). Addresses to the bus are from the microdata file output latch (F10, F11). Addresses from the bus are routed to the bus and arbitration sequence logic on sheets 2 and 3.

5.2.1.4 Bus and Arbitration Sequence

To ensure fastest response time, the synchronization of I/O bus transfers is done by hard-wired state logic illustrated on sheets 2 and 3. Information transfers are of two kinds; programmed I/O and non processor request (NPR). During programmed I/O transfers, the processor is bus master. During NPR transfers, the controller is bus master. Distinguishing between the two transfer types is the function of the arbitration logic.

The bus sequence logic synchronizes master/slave transfers over the I/O bus.

Transfers between the I/O bus and the controller are of two types:

a. Register transfers via programmed I/O
b. Data transfers via NPR

During programmed I/O transfers, the seven controller registers are accessed, initialization information is transferred to the registers, and status information is accessed from the registers. The registers are located in the microdata file on sheet 8. Address information from the processor is decoded by circuits D10 and D11.

The bus and arbitration sequence logic comprises PROMs, used as decoders, and flip-flops that temporarily store control information. The storage elements for the DMA light, the BUSY light, and the DIAGNOSTIC light are contained in this logic. Monostable multivibrators in device C3 monitor bus activity to ensure responses to the bus master occur within 10 microseconds. Circuit D2 establishes the crystal-controlled time base for the controller. The 10 megabit output of D2 is divided by two by flip-flop D8 to generate 200 nano-second clock PCLK buffered to become PPCLK, PPCLK, and CLK*. Figures 5-3, 5-4, 5-5, 5-6 and 5-7 are timing diagrams that illustrate bus control sequences.

5.2.2 Microprocessor

The microprocessor comprises the following major elements:

a. Data file
b. Data file address register
c. Data file multiplexer
d. 2901A array and status register
e. Control memory and register
f. Control store address programmer and test multiplexer
g. D bus multiplexer

The preceding elements are interconnected to perform the control, timing, error checking, and data manipulation functions of the controller. Information is transferred among the elements over internal buses defined by Table 5-1.

A microprocessor functions under control of instructions stored in read only memory (ROM or PROM). These instructions are called microinstructions because most often a series of them is required to perform a function. All of the microinstructions are called firmware since, once stored in PROM, they cannot be altered. To understand the function of a microprocessor, please refer to "The Microprogramming Handbook" from Advanced Micro Devices, Inc., 901 Thompson Place, Sunnyvale, California 94086. Detailed technical descriptions of the 2901A four-bit bipolar microprocessor slice and of the 2901 microprogram controller are given in Advanced Micro Devices "AM2900 Family Data Book". These two elements are the major components of the controller.

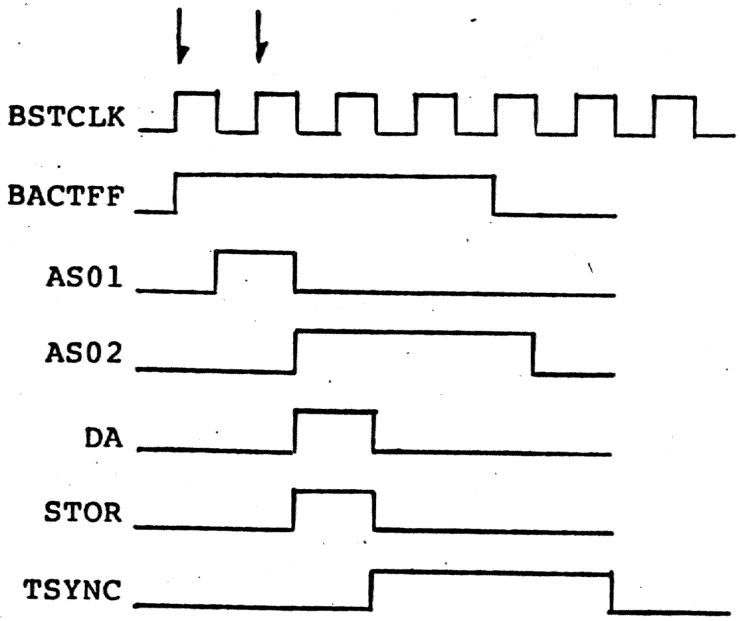


FIGURE 5-3: SLAVE DATO TRANSFERS (C1=1, C0=1)

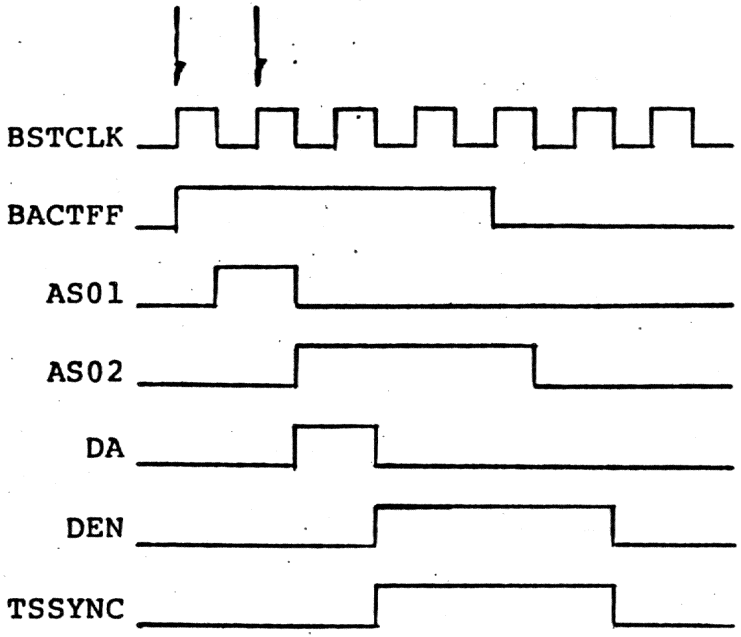


FIGURE 5-4: SLAVE DATI TRANSFERS (C1, C0=0)

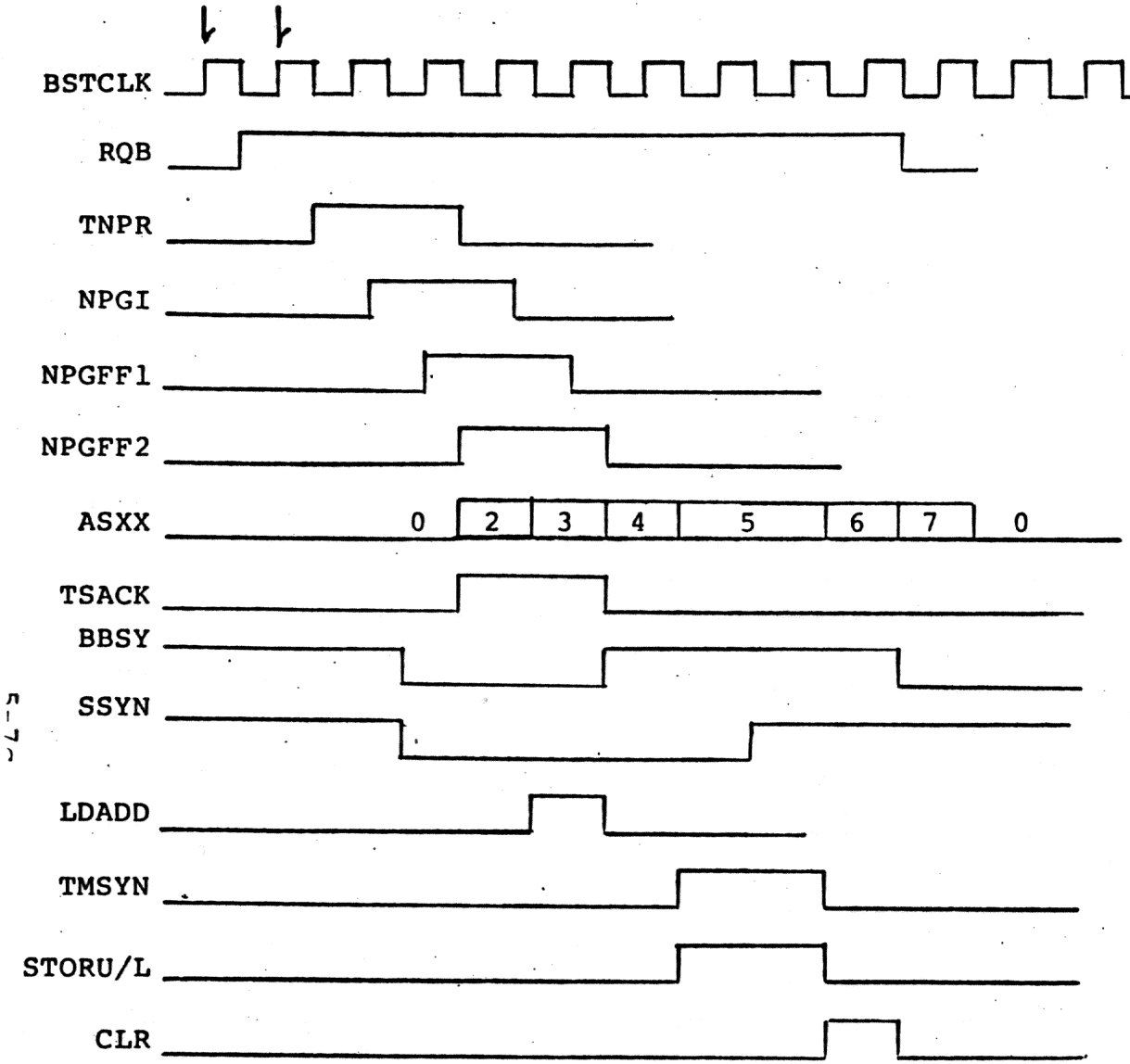


FIGURE 5-5: NPR DATI

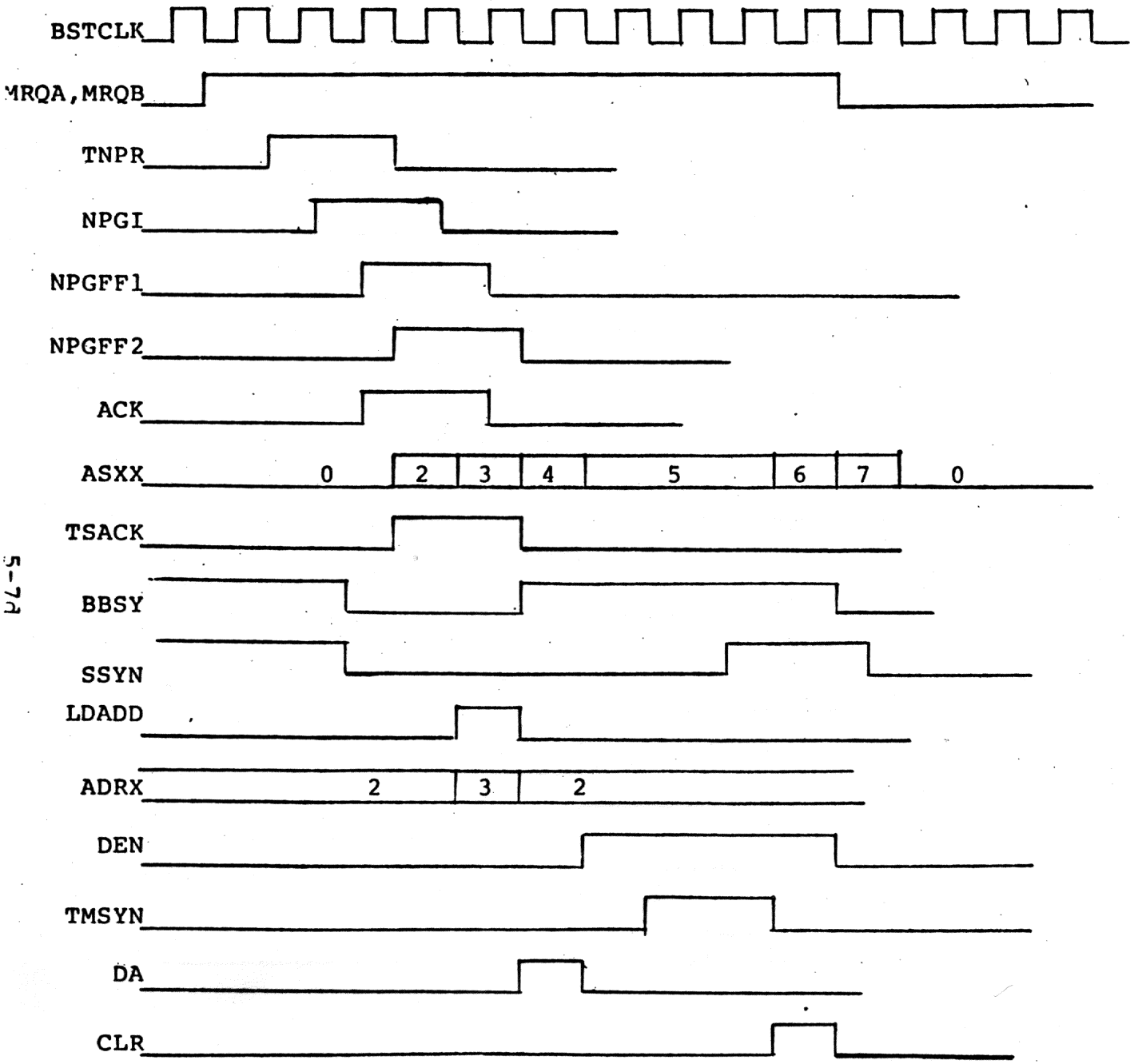


FIGURE 5-6: NPR DATO

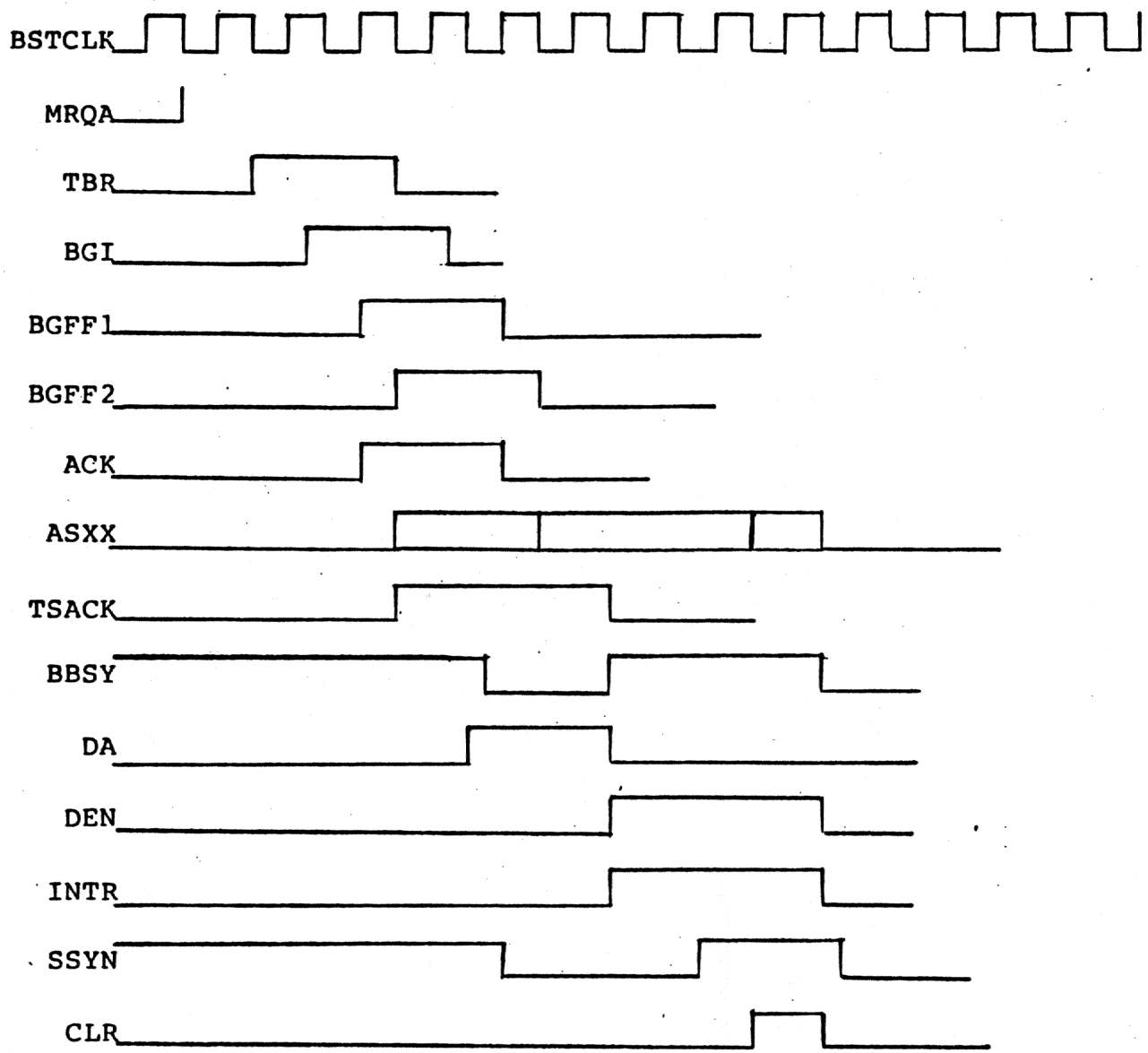


FIGURE 5-7: INTERRUPT

TABLE 5-1: CONTROLLER BUSES

DESIGNATION	FUNCTION
B	PDP-11 I/O bus; Data and Address lines are bidirectional, most control lines are unidirectional.
DB	Data bus FROM I/O bus receivers into controller
D	Input Data bus to 2901A supplied with information from multiplexer 5D, 10D, 11D, 8 bits wide.
P	Peripheral Bus: Data and Control signals.
T	Transmit data or control signals from controller to PDP-11 I/O bus.
Y	Output data bus from 2901A array.
FO	Output of 16 x 16 data file.

5.2.2.1 Micro Data File (sheet 8)

This data file stores sixteen 16-bit words (16 x 16) and has two functions:

a. Storage for the seven controller registers in locations 9_{16} through F_{16} as shown in Table 5-2.

b. Buffer storage for data words being transferred via NPR between memory and tape in locations Ø through 7.

TABLE 5-2: CONTROLLER REGISTER STORAGE

REGISTER	FILE LOCATION (HEX)
MTRD	A
MTD	B
MTCMA	C
MTBRC	D
MTC	E
MTS	F

Sheet 8 shows the data file. Data inputs to the file are from the data file multiplexer on lines FIØØ - FI15. Outputs from the data file are on lines FOØØ - FO15 to the microdata bus. Data file locations are accessed by the address file and by the DS2 portion of the control register word. Note that the data file is separated into 8-bit bytes and that the upper byte (FOØ8 - FO15), the lower byte (FOØØ - FOØ7), or both bytes can be written into or read from independently.

5.2.2.2 Micro Data File Addressing

The microdata file address logic is shown on sheet 8. Two sources address the data file:

a. The bus and arbitration sequence logic (circuit D10).
b. The 4 x 4 address file (circuit D11).

Address control from the bus and arbitration sequence logic is address lines AØ1 - AØ3, which select specific controller registers.

The 4 x 4 address file is capable of storing up to four addresses. The source of address information to the address file is bit 03 of field three of the control register word and bits 00, 01, and 02 or the Y bus. Information can be read from and written into different locations of the address file simultaneously. When addresses are being buffered through circuit D10, circuit D11 is disabled from supplying addresses. Write and read addresses to the address file are from field three of the control register word directly, and indirectly via PROM C10 (sheet 3).

5.2.2.3 Micro Data File Multiplexer

The microdata file multiplexer, shown on sheet 7, switches the input to the microdata file between two sources: the contents of the Y bus, and the contents of the data bus (DB). The contents of field three of the control register word control the selection.

5.2.2.4 2901A Array and Status Register

The 2901A array is shown on sheet 10. The 2901A array comprises two AM2901A four-bit bipolar microprocessor slice integrated circuits connected in cascade to perform data manipulation on 8-bit bytes. The major sections of the AM2901 are shown within dashed lines on the detailed block diagram in Figure 5-2. A description of the operation of this device is given in the "AM2900 Family Data Book".

The D bus supplies external data to the 2901A. Data from the 2901A is on the Y bus. Control inputs to the 2901A are given in Table 5-3.

TABLE 5-3: CONTROL INPUTS TO 2901A

MNEMONIC	SIGNAL SOURCE	DEFINITION
AØ-3	Control Register	Address inputs: selects the A file register contents to be connected to the 2901A, A bus (S1)
BØ-3	Control Register	Address inputs: selects the A file register contents to be connected to the 2901A, B bus (S2)
IØ-8	Control Register	Instruction control lines: lines Ø-2 select the data sources to be applied to the ALU; lines 3-5 select the ALU function to be performed; lines 6-8 determine the routing of the output of the ALU within the ALU and the source of data supplied to the Y (output) bus. (ALU, ALU SRC, DST)
CN	Control Register	Carry input of ALU. Used during arithmetic operations.
CP	Crystal Oscillator	200 nanosecond clock to 2901A.

The status register is updated on a controller clock with the ALU status. The register stores the conditions shown in Table 5-4.

TABLE 5-4: 2901 STATUS REGISTER BITS

MNEMONIC	DEFINITION
Z_s	Indicates result of ALU operation is Zero
C_s	Indicates a "carry out" of ALU
N_s	The most significant ALU bit (sign of result)

5.2.2.5 Control Memory and Register

The control memory stores the firmware that controls the operation of the controller. It comprises six 512 x 8 bit programmable read-only-memories (PROMs) identified as B12, B14, B15, B16, B17, and B18 on sheet 11. The PROMs have a pipeline register at the output identified as the Control Register (CR). The six PROMs produce a 48-bit instruction word divided into six 8-bit fields. Figure 5-8 depicts the instruction word.

The contents of the control memory are accessed by the Control Store Address Processor and strobed into the control register by the PPCLK clock. The contents of the control register (CR1-ØØ-Ø7 through CR5-ØØ--Ø7 and literal DØØ-DØ7) are routed throughout the logic of the controller.

5.2.2.6 Control Store Address Programmer

The Control Store Address Programmer (CSAP) is an AM2910 microprogram control circuit and is described in "The AM2900 Family Data Book". It controls the sequence of execution of microinstructions stored in the control memory. The CSAP is shown on sheet 10.

Control store output address lines CSAØØ through CSAØ8 select one of 512 locations in control memory and are also routed to test five of the control register and the $\overline{\text{TEST}}$ output of test conditions multiplexer A17 (shown on sheet 10). Bits ØØ through Ø7 (LSB) of field five (CR5) supply instruction codes to the CSAP. Any one of 16 instructions can be selected. The instructions can be modified by the state of the $\overline{\text{TEST}}$ input. The instructions select the next source of addresses to the control memory. The primary sources of addresses are as follows:

a. A program counter/register within the CSAP.
b. A five word stack within the CSAP.
c. Branch addresses directly from bits ØØ-Ø7 of field five (CR-5)

Note that bits Ø4 through Ø6 of field four (CR4) control test condition multiplexer A17. This multiplexer connects one of eight selected conditions to the $\overline{\text{TEST}}$ line when specified by the current microinstruction being executed. The conditions tested for are shown in A17, Table 5-5.

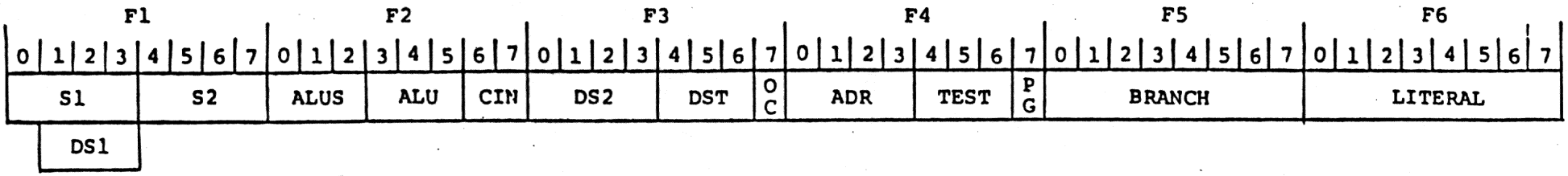


FIGURE 5-8 Microinstruction Word

TABLE 5-5: ADDRESS MODIFICATION CONDITIONS

MNEMONIC	CONDITION
C	No carry from 2901A ALU
Z	ALU result is zero
C	Carry from ALU
N	ALU sign bit logical true
P	Parity true
D	Data reg flag
INIT	System reset
T	True

Note that bus signal DCLØ, if ever low, disables the output of the CSAP and generates a Reset (RST) signal.

5.2.2.7 D Bus Multiplexer

The D bus multiplexer, shown on sheets 8 and 13 is the information source to the 2901A array processor. The multiplexer comprises circuits E12 and F12 on sheet 8 and circuits B6, B7, and B8 on sheet 13. Circuits E12 and F12 also function as storage registers. Additional information sources for the D bus are PROM B12, shown on sheet 11, which supplies the literal (LIT) and PROM D12 on sheet 10.

Field one, bits ØØ through Ø3, and bit Ø2 of field two, via circuit B10 (sheet 3) gate the selected source to the D bus. Information sources to the D bus are as shown in Table 5-6.

TABLE 5-6: INFORMATION SOURCES TO D BUS

CIRCUIT	SHEET	SOURCE
B12	11	Literal from control memory
E12, F12	8	Microdata bus upper and lower bytes
D12	10	Controller status
B7	13	Data from tape
B8	13	Tape status

5.2.3 Peripheral Interface

The peripheral interface comprises the following elements:

a. Peripheral input output registers
b. Tape timing and configuration logic
c. Cable driver/receivers and control buffers

5.2.3.1 Peripheral Input Output Registers

There are two registers which temporarily store information being transferred between the tape and the other elements of the coupler; an input register shown on sheet 13, and an output register shown on sheet 14.

The input register stores status information and data received from the tape and comprises circuits B6, B7, and B8. The outputs of these circuits are gated to the D bus as described in paragraph 5.2.2.7. Timing is controlled by signals POA, POB, and POC generated on sheet 3.

The output register stores information to be sent to the tape and comprises circuits A13, A14, and A15. These circuits make up a 32-bit register that receives information from tne Y bus in 8-bit segments. Y bus information is stored in the register under control of the PIA, PIB and PIC clocks.

TABLE 5-7: GLOSSARY OF TERMS

TERM	DESCRIPTION	ORIGIN SHEET
A00-A15	Address bus bit 0 through bit 15	5
A16, A17	Address bus bits 16 & 17 (MSB)	4
$\overline{\text{ACEN}}$	Address and control enable	4
ACK	Acknowledge	2
ADRA	Address A	3
ADRB	Address B	3
A00FF	Address bit 0 flip-flop	2
AS00	A sequencer bit 00	2
AS01	A sequencer bit 01	2
AS02	A sequencer bit 02	2
BACT FF	Bus activity flip-flop	2
$\overline{\text{BG}}$	Bus Grant	4
BBSY	Bus busy	4
$\overline{\text{BGFF1,2}}$	Bus grant flip-flop	2
$\overline{\text{BGO}}$	Bus grant out	2
BOT	Beginning of tape mark	14
BSY	Busy	3
BSYS	Busy Set	2
BSYFF	Busy flip-flop	2
BUSA00L- BUSA15L	Data address bus lines (16)	5
C0C1	Control zero, one	4
C0FF/C1FF	Control zero/one flip-flops	2
CN+2	Carry output of 2901	9
$\overline{\text{CLRB}}$	Clear bus	3
$\overline{\text{CLR}}$	Clear	2
CR1-07	Control register one output bits 0-7	11
CR2-00-- CR2-07	Control register two output bits 0-7	11
CR3-00-- CR3-07	Control register three output bits 0-7	11
CR4-00-- CR4-07	Control register four output bits 0-7	11

GLOSSARY OF TERMS (continued)

TERM	DESCRIPTION	ORIGIN SHEET
CR5-00--		
CR5-07	Control register five output bits 0-7	11
CS	Carry signal out of second 2901	9
CSA08	Control store address bits 0 through 08 (9 bits)	10
D00--	Data bus bits 0-7 to 2901	8,10,11,12
D07		
DA	Data enable	
DA16, DA17	Data address bits 16 and 17	3
DB00-	Data bus bits 00-15 from UNIBUS	6
DB15	Bit 15 is MSB, bit 00 is LSB	6
DB8M	Data bit 8, multiplexes	7
DB15M	Data bit 15, multiplexed	
DCLO	DC Voltage low	4
$\overline{\text{DEN}}$	Device enable	2
$\overline{\text{EOT}}$	End of tape from tape	14
$\overline{\text{FLPT}}$	File protect from tape	14
DRQFLG	Data request flag	12
FI00-FI15	File in bits 0-15	7
FUNC	Function	3
F000	File out bits 0-15	8
F015		
$\overline{\text{FL-D}}$	File lower data	3
$\overline{\text{FU-D}}$	File upper data	3
$\overline{\text{FLCLK}}$	File lower byte clock	3
$\overline{\text{FUCLK}}$	File upper byte clock	3
INIT	Initialize	4
LDADD	Load address	2
$\overline{\text{LIT}}$	Literal	2
MRST	Master reset	2
MRQA	Memory request A	3
MRQB	Memory request B	3
MSYN	Master sync	4
MTC	Magnetic tape control	2
$\overline{\text{MTR}}$	Magnetic tape request	2

GLOSSARY OF TERMS (continued)

TERM	DESCRIPTION	ORIGIN SHEET
MTS	Magnetic tape status	2
NS	Most significant output bit of 2901 ALU (sign)	9
$\overline{\text{NPG}}$	Non processor grant	4
$\overline{\text{NPGFF1,2}}$	Non processor grant flip-flops	2
NXM	Non existent memory	3
OFC	Off line command to tape	14
$\overline{\text{ONL}}$	On line status from tape	14
PARS	Parity status from tape	11
PBSY	Peripheral busy set	3
$\overline{\text{PIACLK}}$	Peripheral in A byte clock	3
$\overline{\text{PIBCLK}}$	Peripheral in B byte clock	3
$\overline{\text{PICCLK}}$	Peripheral in C byte clock	3
$\overline{\text{PIDCLK}}$	Peripheral in D byte clock	3
$\overline{\text{PØA-D}}$	Peripheral out A byte data	3
$\overline{\text{PØB-D}}$	Peripheral out B byte data	3
$\overline{\text{PØC-D}}$	Peripheral out C byte data	3
$\overline{\text{PØD-D}}$	Peripheral out D byte data	3
PUP	Pull up voltage	
PPCLK	Processor clock (controller clock)	3
PIAØØ-Ø7	Peripheral in A byte bits (8)	12
PIBØØ-Ø7	Peripheral in B byte bits (8)	12
PICØØ-Ø7	Peripheral in C byte bits (8)	12
RDØ-RD7	Read data lines from tape	14
RDP	Read data parity from tape	14
RDQ	Read data request	13
RDS	Read data strobe from tape	14
RSTS	Reset tape status	2
RWC	Rewind command to tape	14
RWS	Rewind status from tape	14
$\overline{\text{7TRK}}$	7 or 9 track status from tape	14
SEL1-SEL4	Select tapes 1,2,3, or 4	14
SFC	Synchronous forward command to tape	14
SWS	Set write status	14

GLOSSARY OF TERMS (continued)

TERM	DESCRIPTION	ORIGIN SHEET
SRC	Syhchronous reverse command to tape	14
STORL,U	Store lower, upper byte	2
SSYN	Slave sync	3
$\overline{STA}$	Status	3
SYNFF	Synchronize flip-flop	2
TA00-TA15	Transmit address bits 00-15	5
$\overline{TA}$	Transmit address	3
TBBSY	Transmit bus busy	2
TBR	Transmit bus request	2
TD00-TD15	Transmit data bits 00-15	6
TD00G	Transmit D bus bit 00 gated	2
TO	Time out	3
TOD	Time out delay	3
TINTR	Transmit interrupt	2
TMSYN	Transmit master sync	2
TNPR	Transmit non processor request	2
TSACK	Transmit select acknowledge	2
TSSYN	Transmit slave sync	2
$\overline{TRDY}$	Tape ready from tape	14
WARS	Write amplifier reset to tape	14
WDS	Write data strobe to tape	14
WDP	Write data parity to tape	14
WD0-WD7	Write data lines (8) to tape	14
$\overline{WRL}$	Write load	3
$\overline{WRU}$	Write unload	3
Y00- Y07	Y bus bits 0 through 7 from 2901	9

SECTION 6

TROUBLESHOOTING GUIDE

6.0 INTRODUCTION

The purpose of this section is to assist the maintenance engineer in isolating malfunctions to specific assemblies of the tape based computer system. Normally, once a malfunctioning assembly (tape drive, memory, controller CPU board, etc.) is located, a known good assembly should be substituted while the malfunctioning unit is returned to a repair depot. Be sure to read this entire section carefully before beginning to troubleshoot the system.

6.1 General

System malfunctions come under two major classifications; intermittent and continuous. Intermittent failures are normally very difficult to isolate and usually require step-by-step substitution of equipment over a period of time until the intermittent assembly is isolated. This section will primarily discuss continuous failure isolation.

When troubleshooting electronic equipment, certain basic items should always be checked:

a. Is power properly applied to all system assemblies - switches on, fuses good, AC power cords plugged in, area power circuit breakers on, etc.

b. Check DC power at backplane terminals of computer - +5V DC, +12V DC. If DC voltages are low, verify AC line voltage is within tolerance:

   100 - 127 Vrms, 50±1 Hz or 60±1 Hz
   200 - 254 Vrms, 50±1 Hz or 60±1 Hz

c. Verify system generates proper response when system is powered-up (refer to operation instructions for the processor).

d. Verify all modules are properly plugged in. No empty slots should exist between modules.

e. Verify all signal cables (tape, console terminal) are properly plugged in. Check each end of cables.

f. Can the console be operated in "Local" mode? If not, console is defective.

g. Is the tape drive ON LINE light on?

h. Are the computer panel switches set correctly (ENA/HALT, LTC, etc.)?

i. Is green DIAG light on tape controller board on?

6.2 Operating Instructions

While troubleshooting the system, the engineer should check the following items:

a. Is the tape clean? Dirty tape or tape read/write heads cause bit dropouts.

b. If tape produces a high-pitched whine or metal-to-metal sound, immediately power down the tape; a bad bearing is possible.

c. Was any module pulled out or plugged in while power was applied? Shorting connector pins together can cause integrated circuit to fail.

d. Has ribbon cable connector been plugged in upside down at controller? This connector is not keyed. Be sure the arrows on the female connector line up with arrows on male connector.

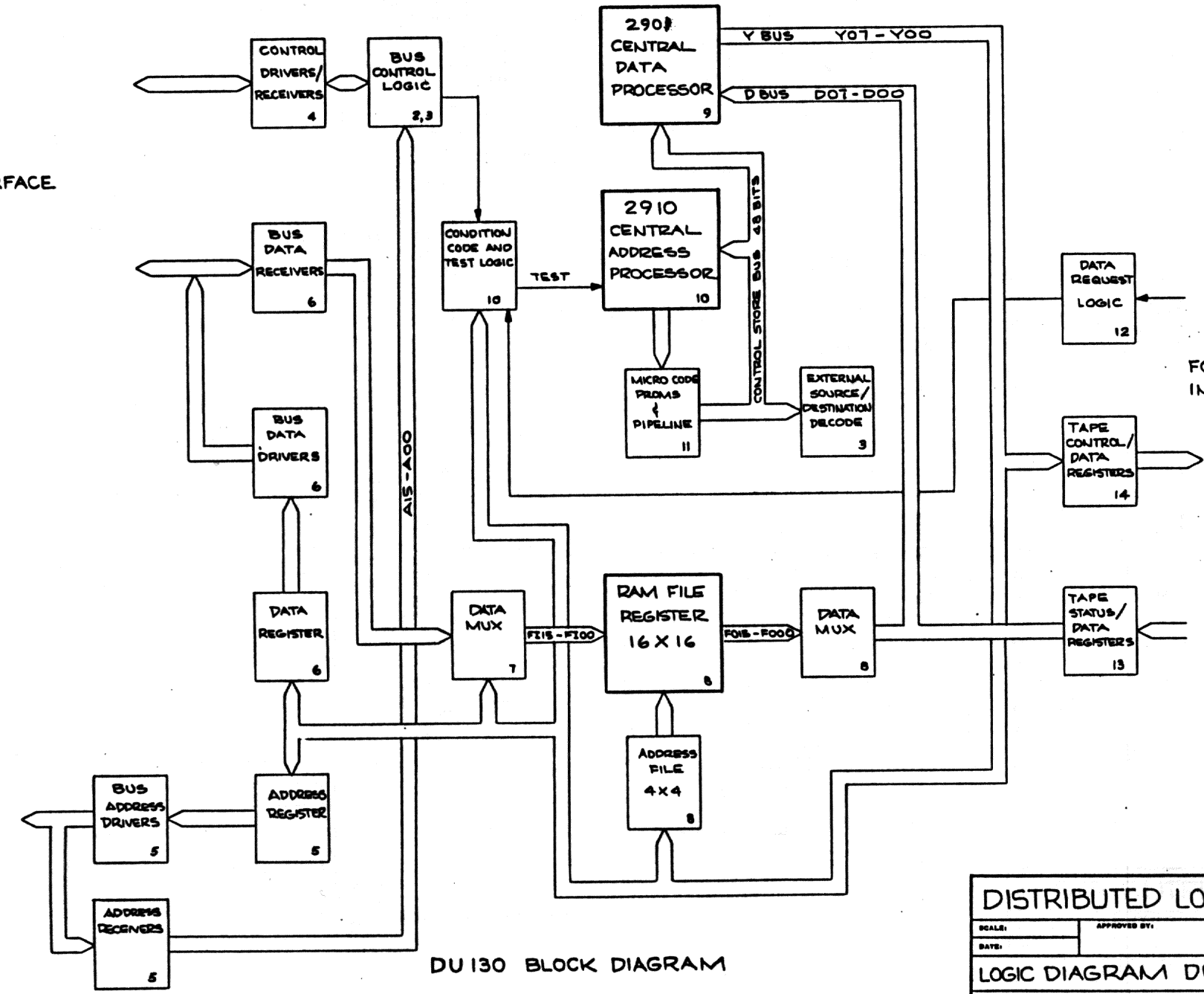
6.3 Possible Troubles

This paragraph provides possible malfunction locations based on either visual indications or tests and assumes the basic items in paragraph 6.2 have been checked and found normal.

NOTE: Before troubleshooting the system be sure proper operating procedures are being followed and the system is properly configured. Refer to SECTIONS 2 and 3 of this manual or the the USER'S GUIDE.

The following pages contain a trouble chart. Space is left on the chart for field failures not in the chart to be noted.

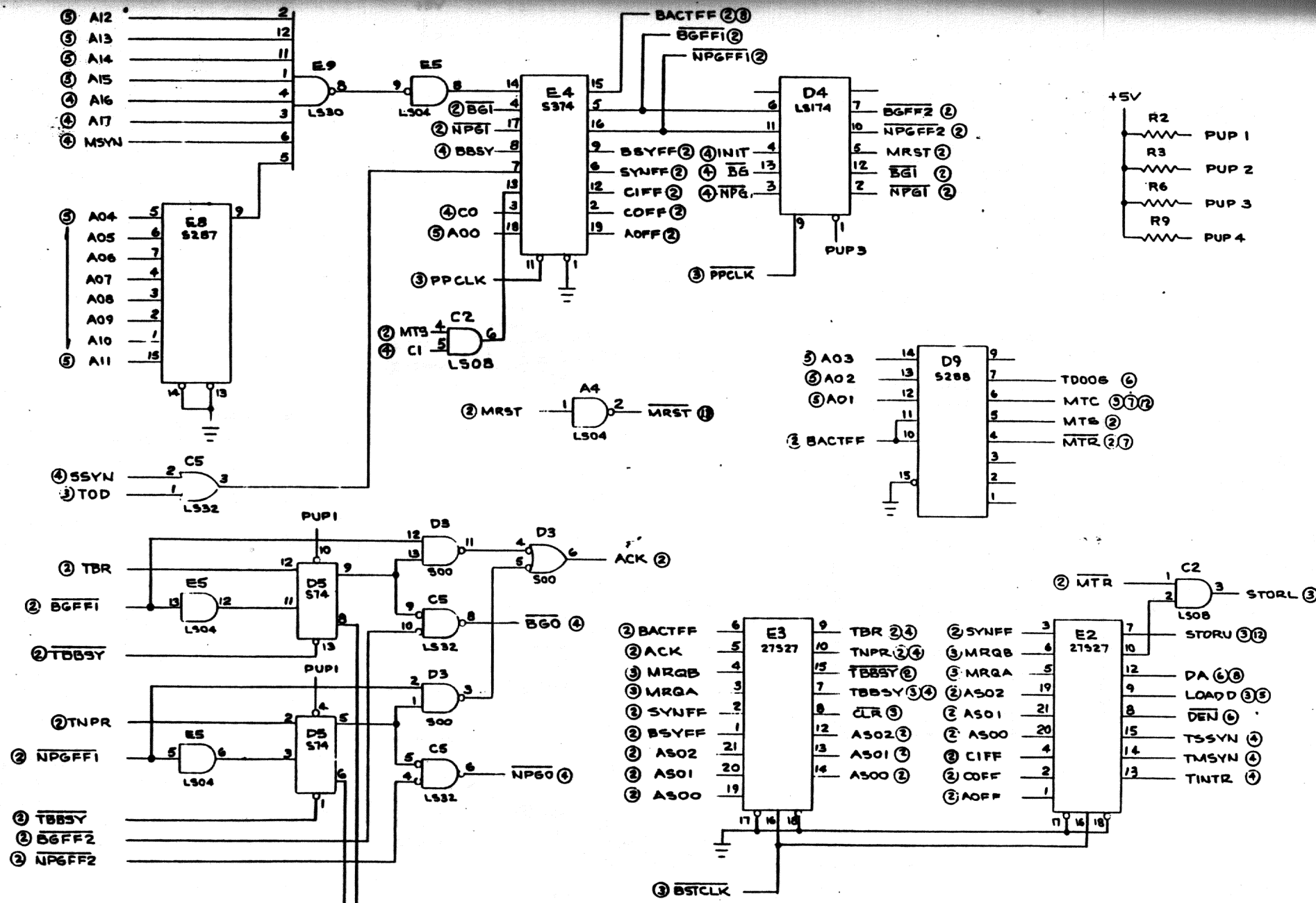
TROUBLE	POSSIBLE CAUSE	CHECK/REPLACE
1. GREEN DIAGnostic light on coupler is OFF.	1. Microprocessor section of coupler inoperative.	1. Coupler.
	a. Crystal not seated in socket or in wrong.	Put board on extender. With scope look at pins of 2901. All pins except power and ground should be switching. Look for "stuck high", or "stuck low", or half-amplitude pulses. If no switching, either power or crystal bad.
	b. Short or open on board.	
	c. Bad integrated circuit.	
	d. No DC power.	
2. No communication between console and computer.	2. I/O section of coupler "handing up" QBus.	2. Computer interface logic of coupler.
	a. $\overline{\text{DEN}}$ always low.	a. Check signal DEN for constant assertion.
	b. Shorted bus transceiver IC.	b. Check I/O IC's. Remove coupler board to see if trouble goes away.
	c. Bad CPU board	c. Run CPU diagnostics.
3. No data transfers to/from tape. BSY light never lights.	3. Tape not ready or bad cable connection.	3. Check tape switches and cable connector.
	a. Improper communication with tape registers on coupler or bad IC in register section of coupler.	a. Load and read tape registers from console with processor halted; i.e., RKDS, RKDA, RKER. Verify bits loaded can be read.
4. Data transferred to/from tape inccorrect. DMA and BSY lights blink to indicate transfers.	4. Bad memory board in backplane.	4. Run memory diagnostic.
	a. Noise or intermittent source of DC power in computer.	a. Check AC and DC power.
	b. Bad IC in tape I/O section of coupler.	b. While operating, check lines from coupler to tape with a 'scope for short or open.
	c. Run tape diagnostic, set console to make system "Halt On Error."	c. Analyze error halt.
	d. Bad area on tape.	d. Errors should always occur in same sector of tape.
	e. Head worn.	e. Replace head.
	f. Crystal in coupler wrong frequency.	f. Check characteristics of tape drive.
	g. Configuration switch J4 not set properly.	g. Check configuration paragraph of Installation Section.



DU130 BLOCK DIAGRAM

DISTRIBUTED LOGIC CORP.

SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM DU130		SHT 1 OF 14
		DRAWING NUMBER 853019



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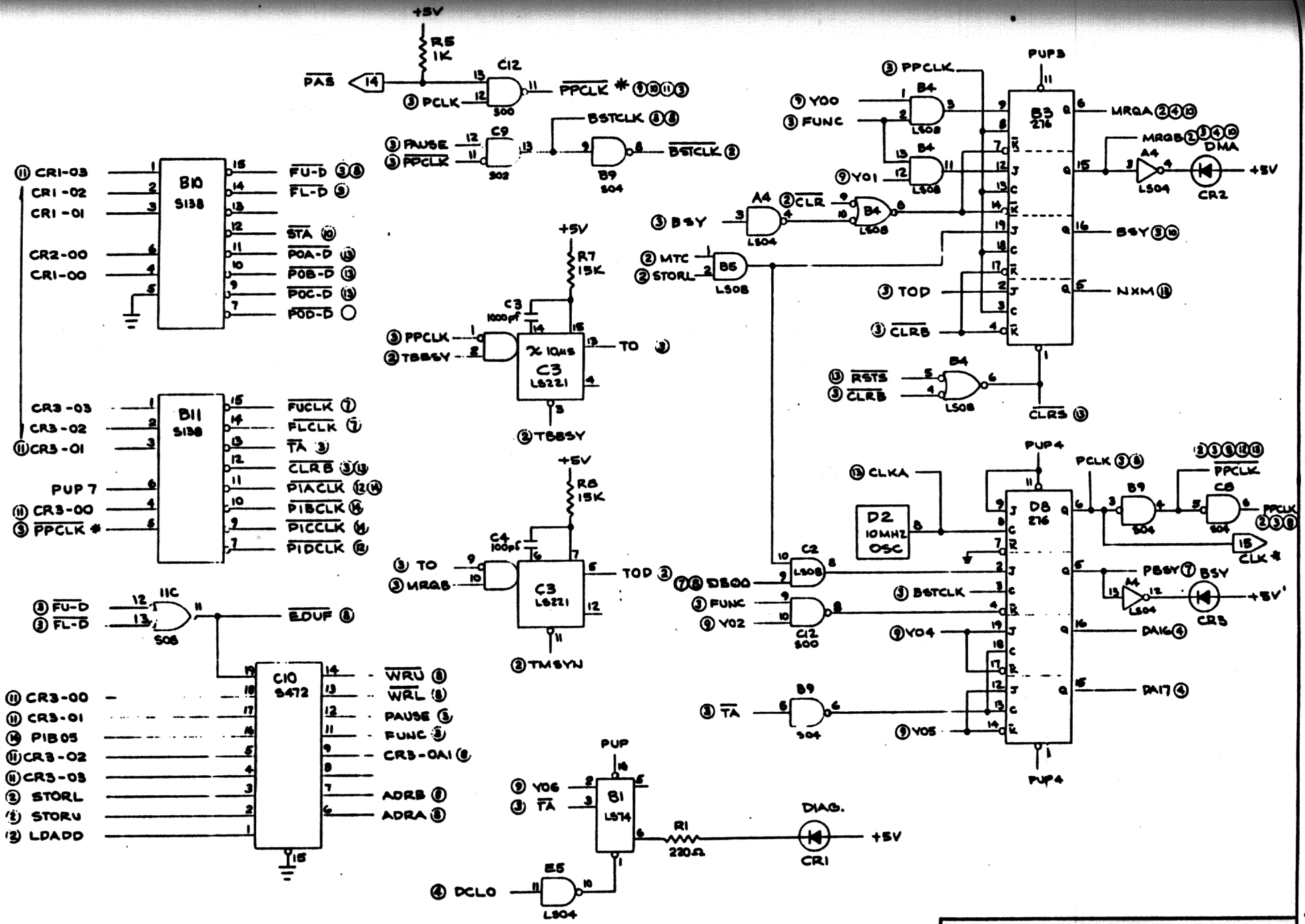

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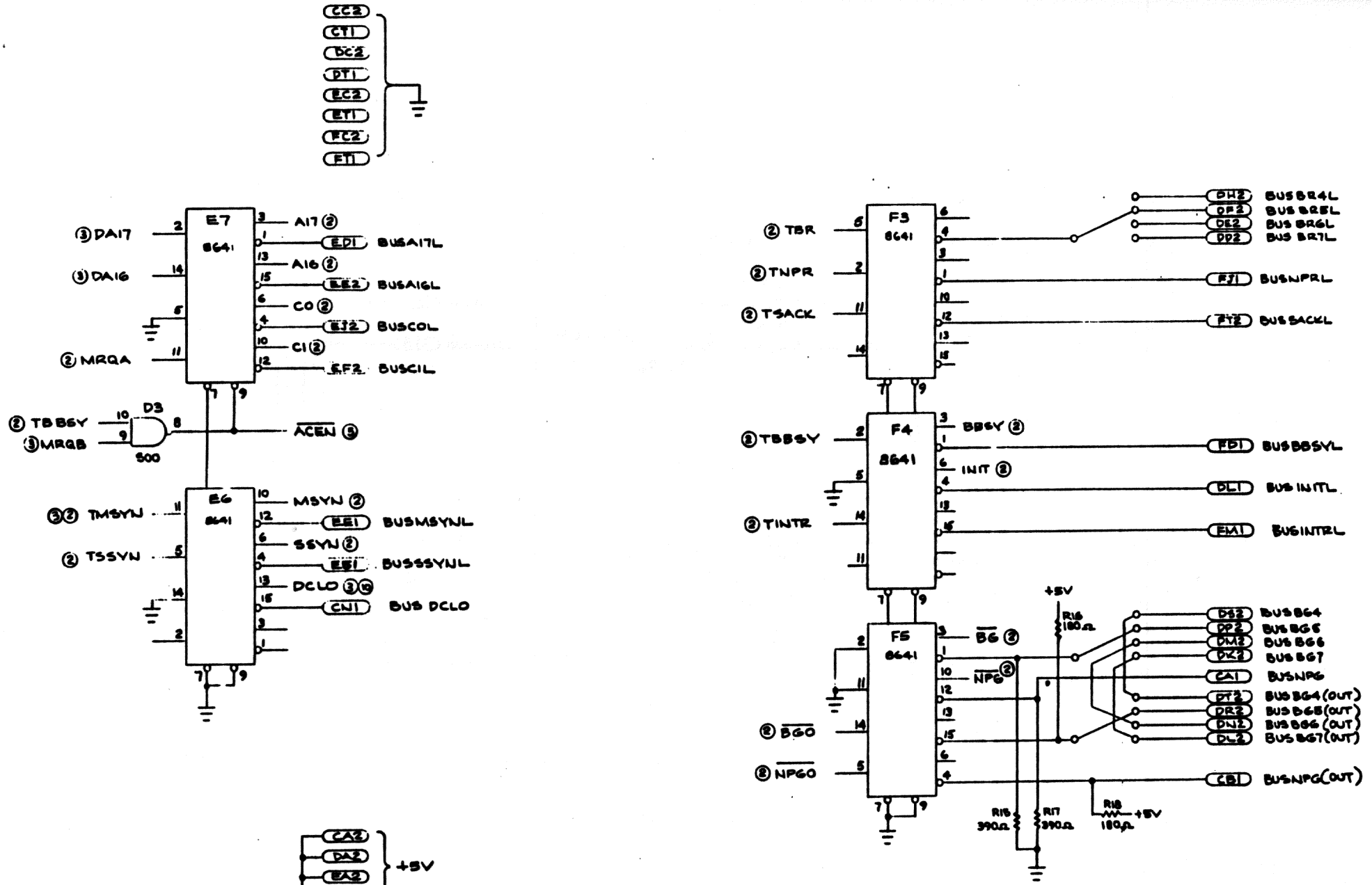

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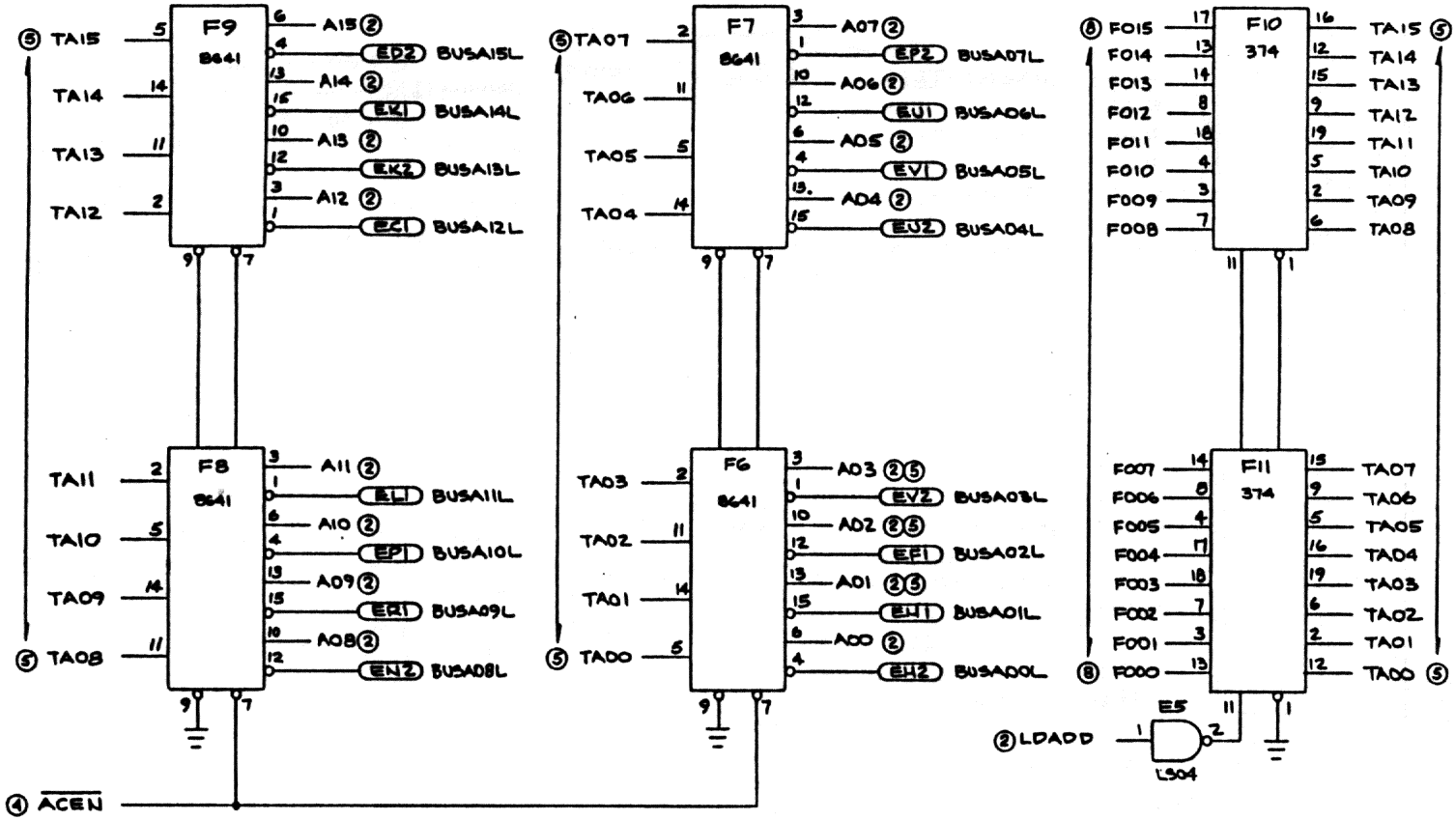

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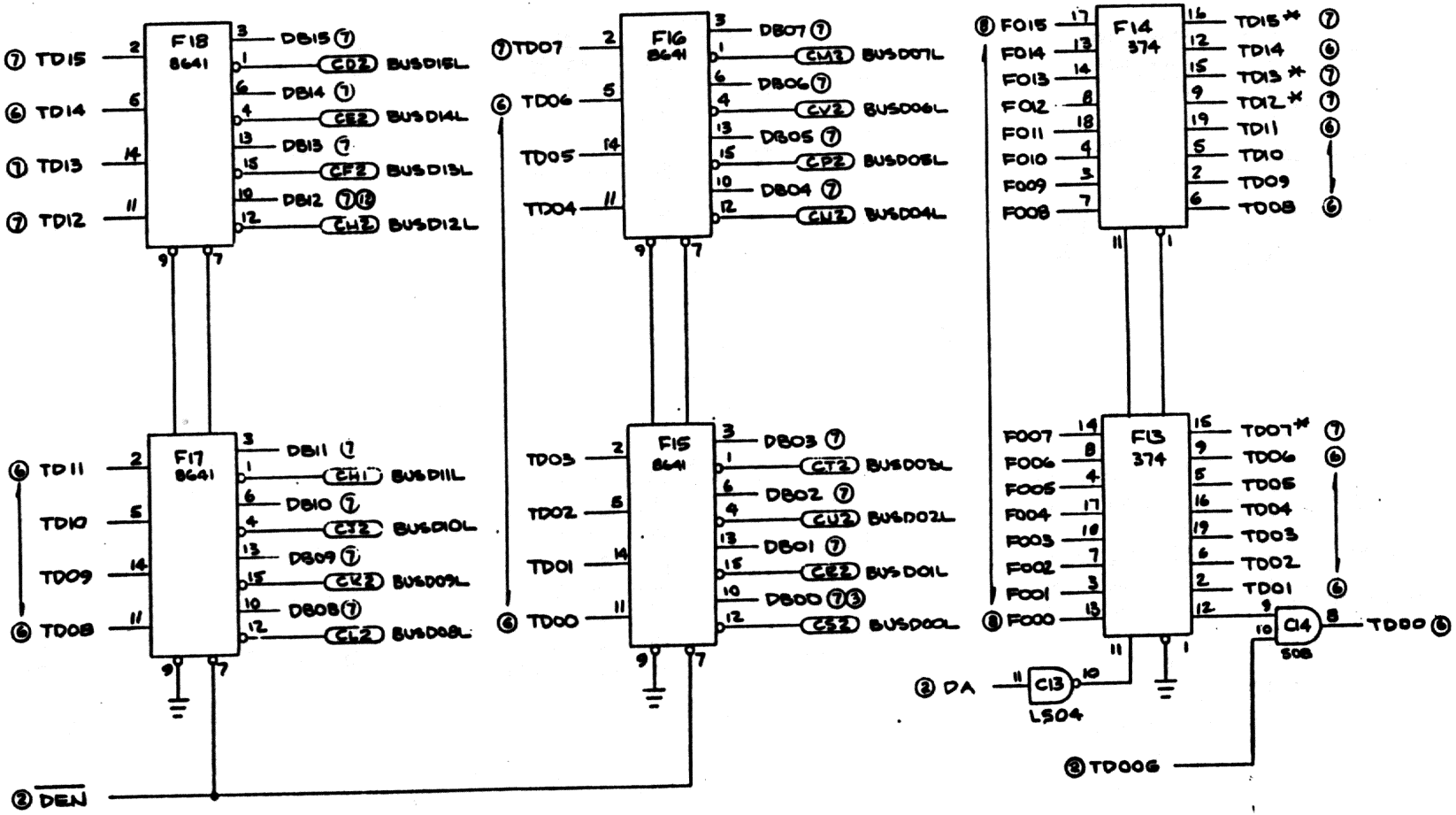

DATA BUS RCVR/DVR

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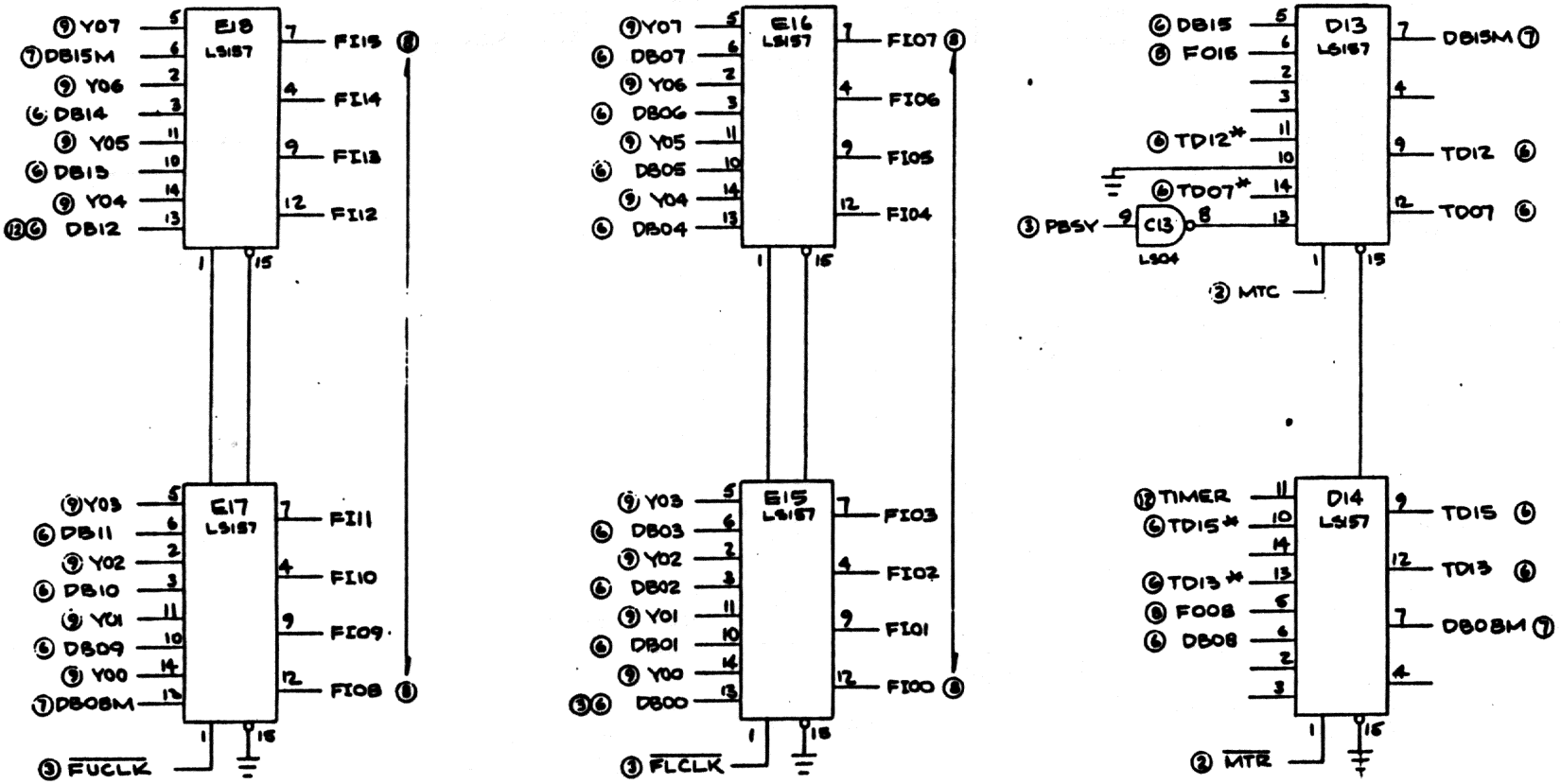

U FILE DATA INPUT MUX

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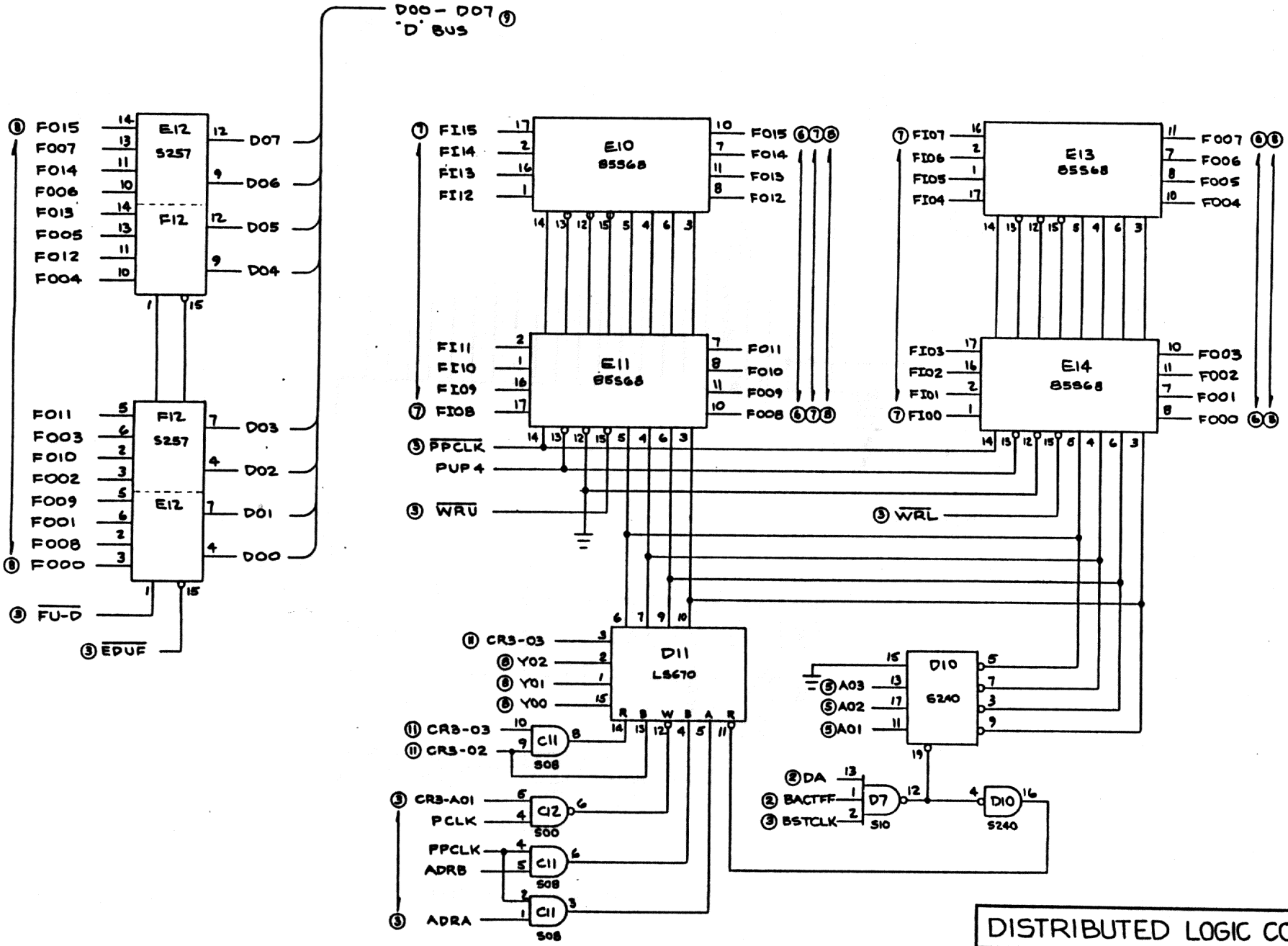

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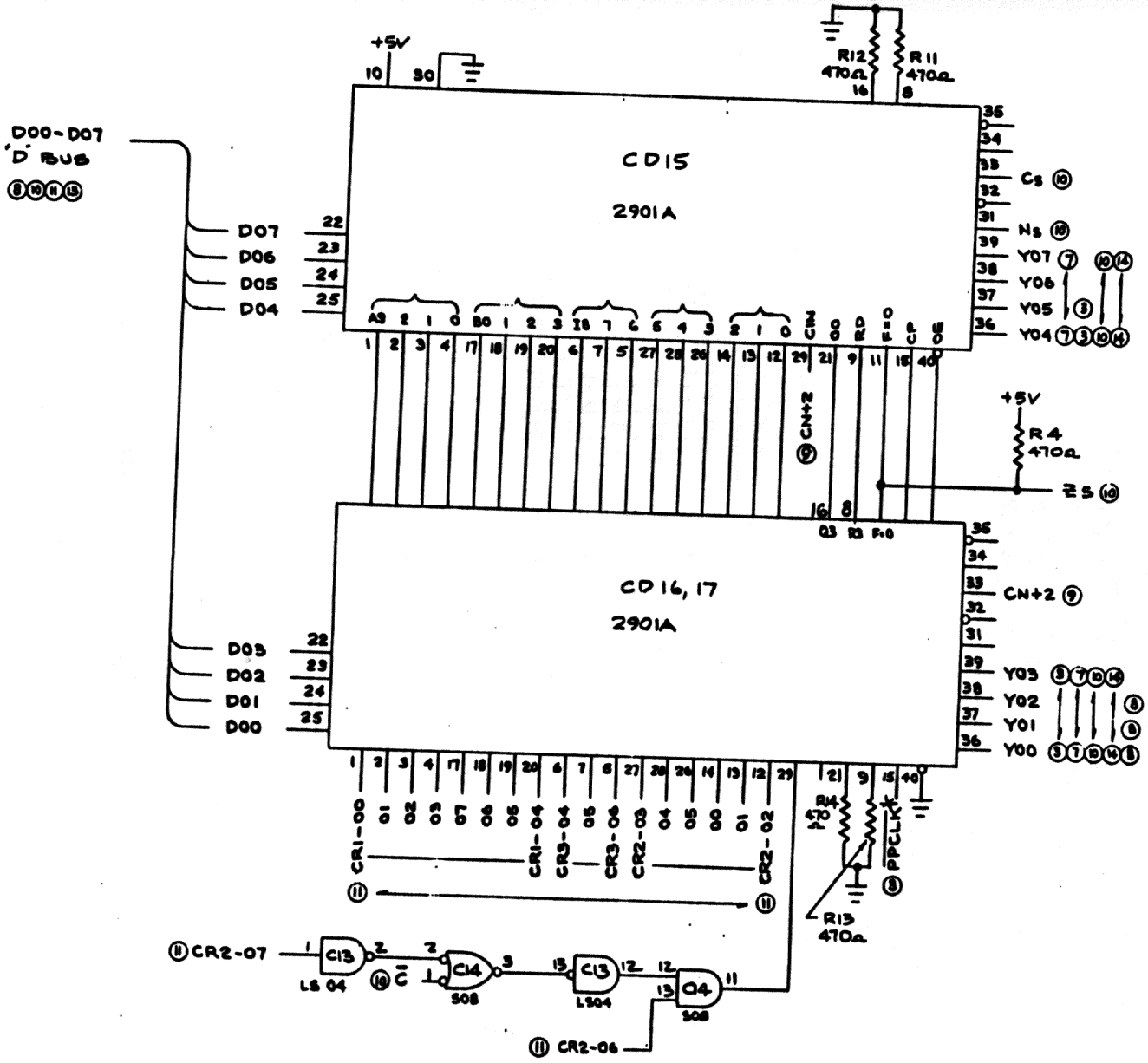

MICRO PROCESSOR

1. RESISTORS ARE 470Ω ±5%, ¼W

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LOGIC DIAGRAM, DU130		SHT 9 OF 14
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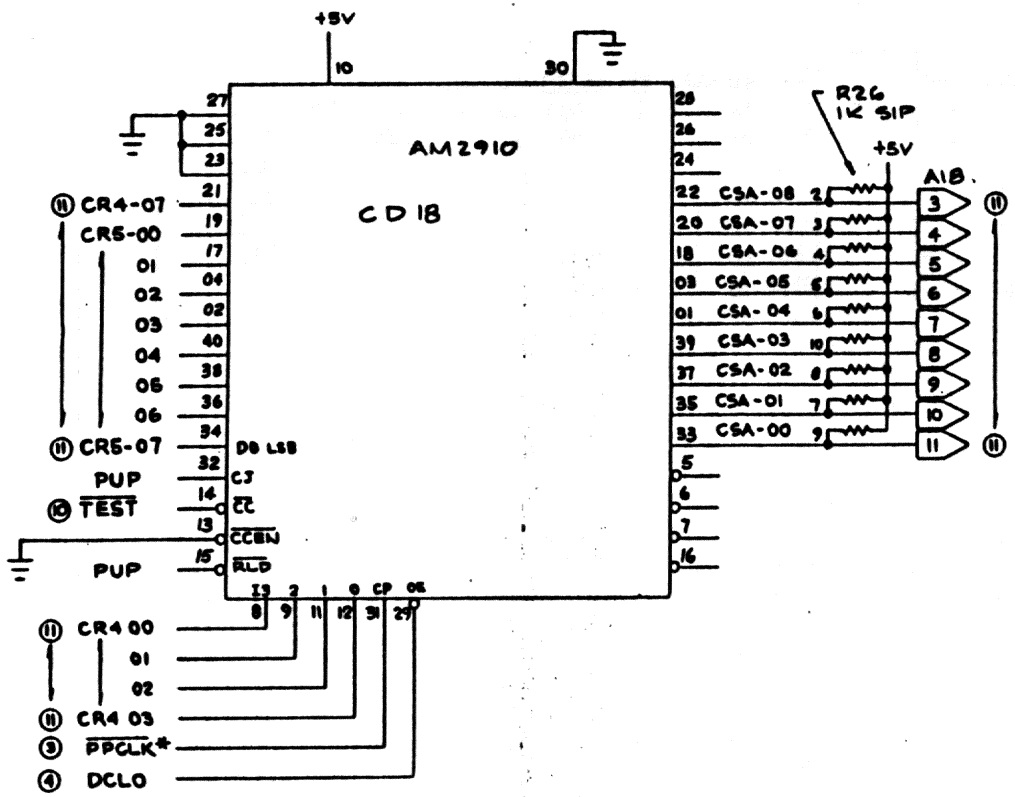
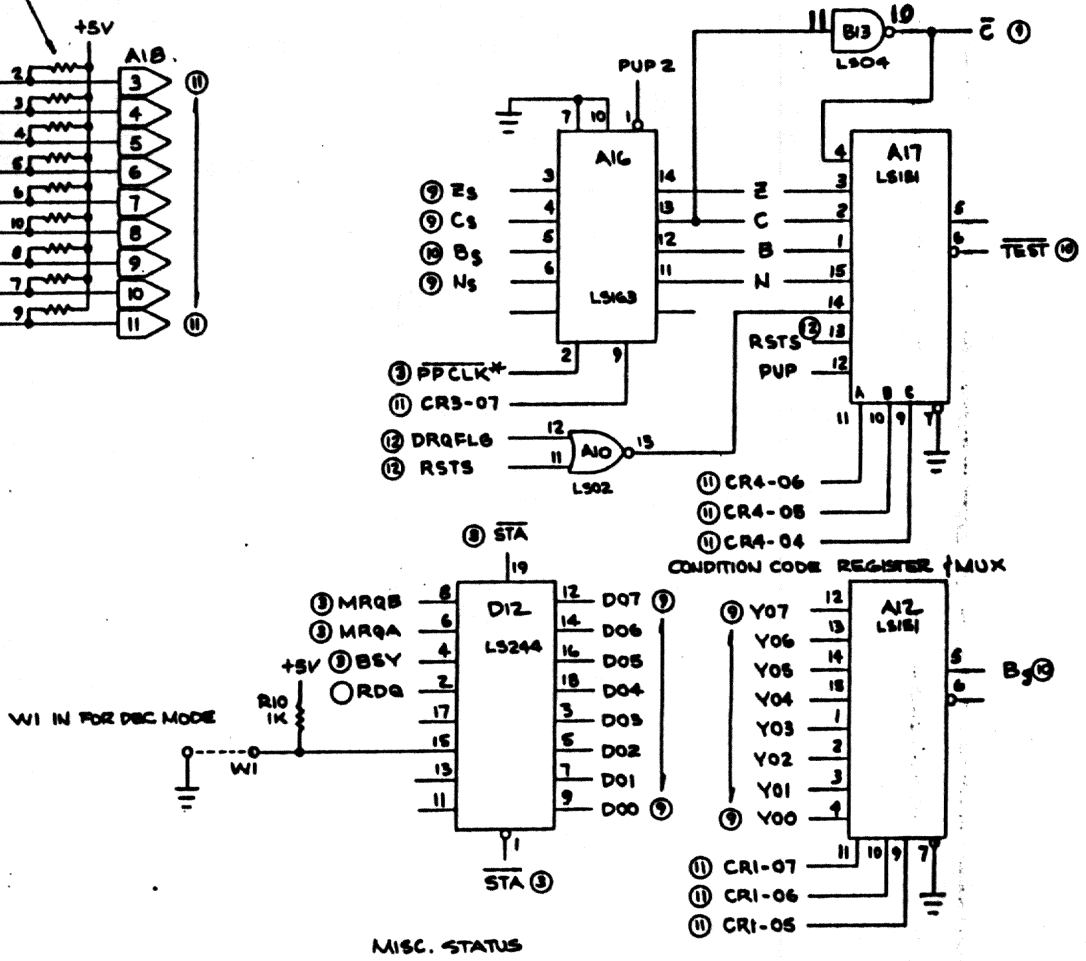


CONTROL STORE ADDRESS PROCESSOR



1. SYMBOL: (X) INDICATES 16 PIN "DIP" CONNECTOR LOCATED AT A18.

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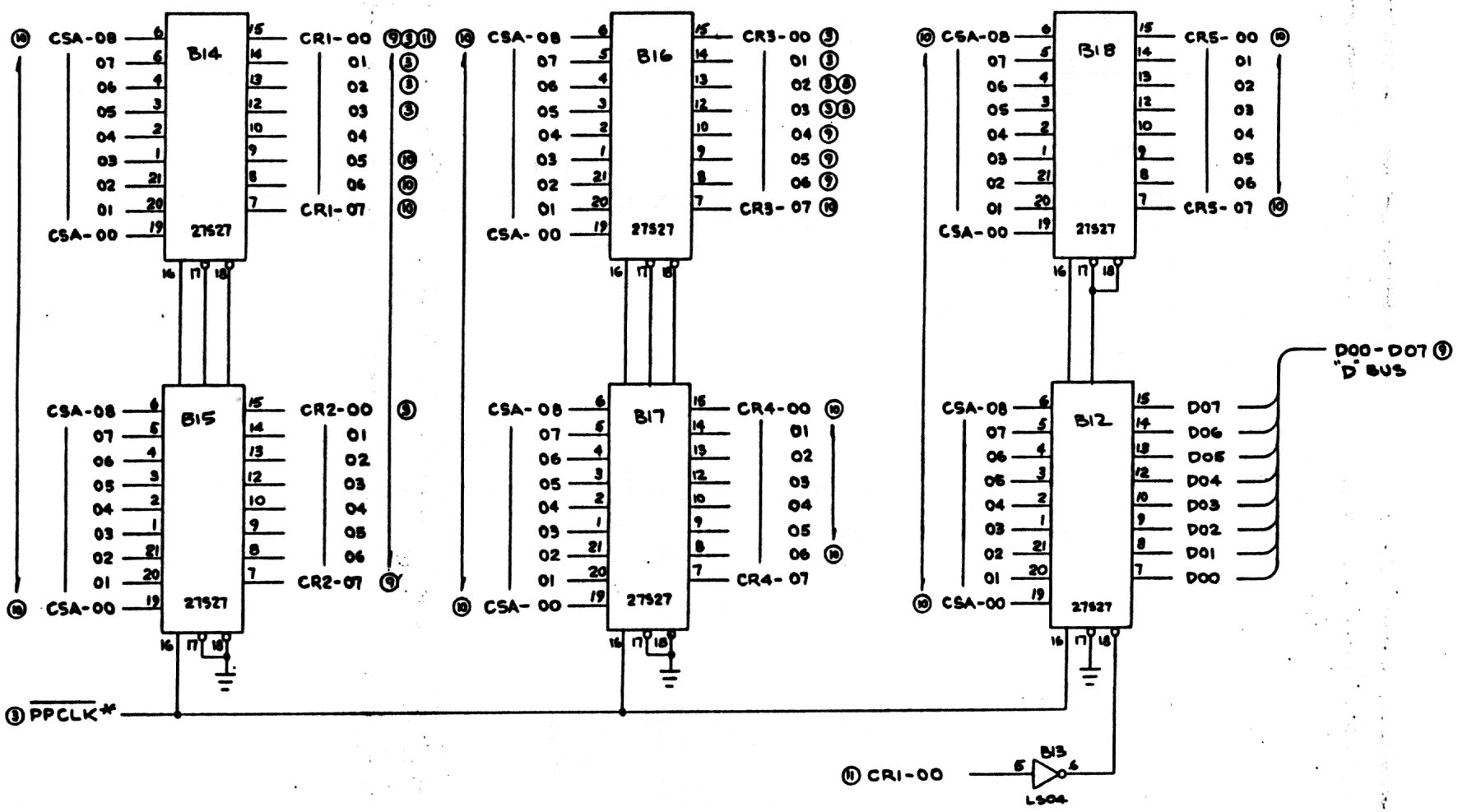

CONTROL STORE & PIPELINE

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LOGIC DIAGRAM, DU130		SHT 11 OF 14
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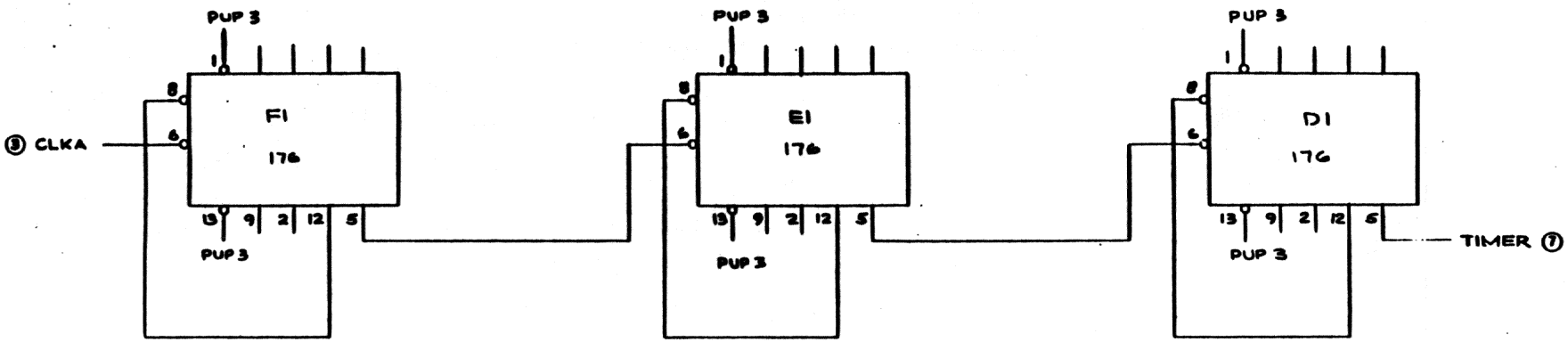

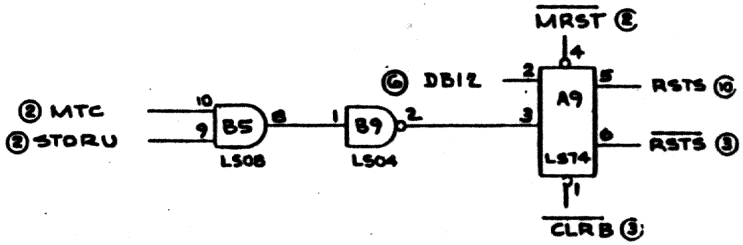

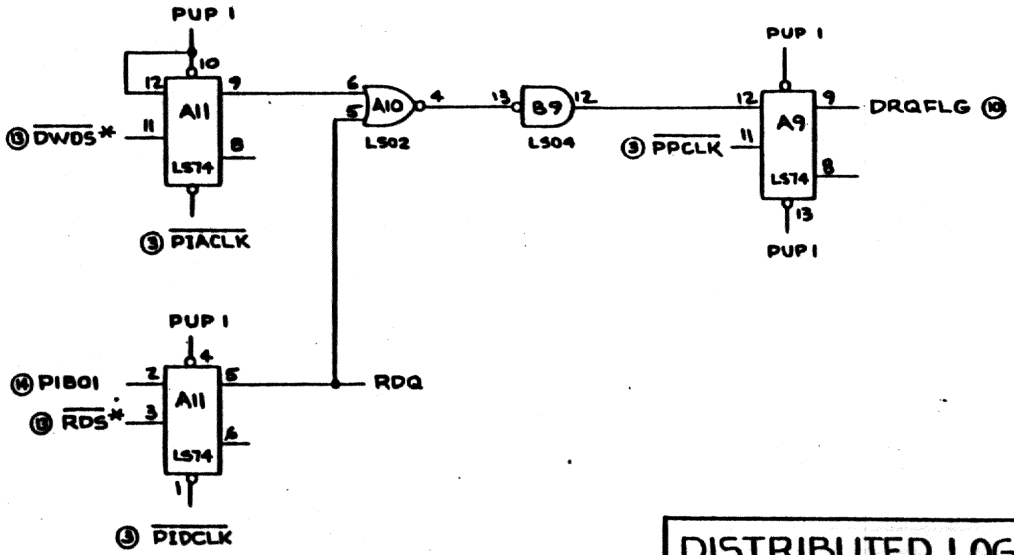

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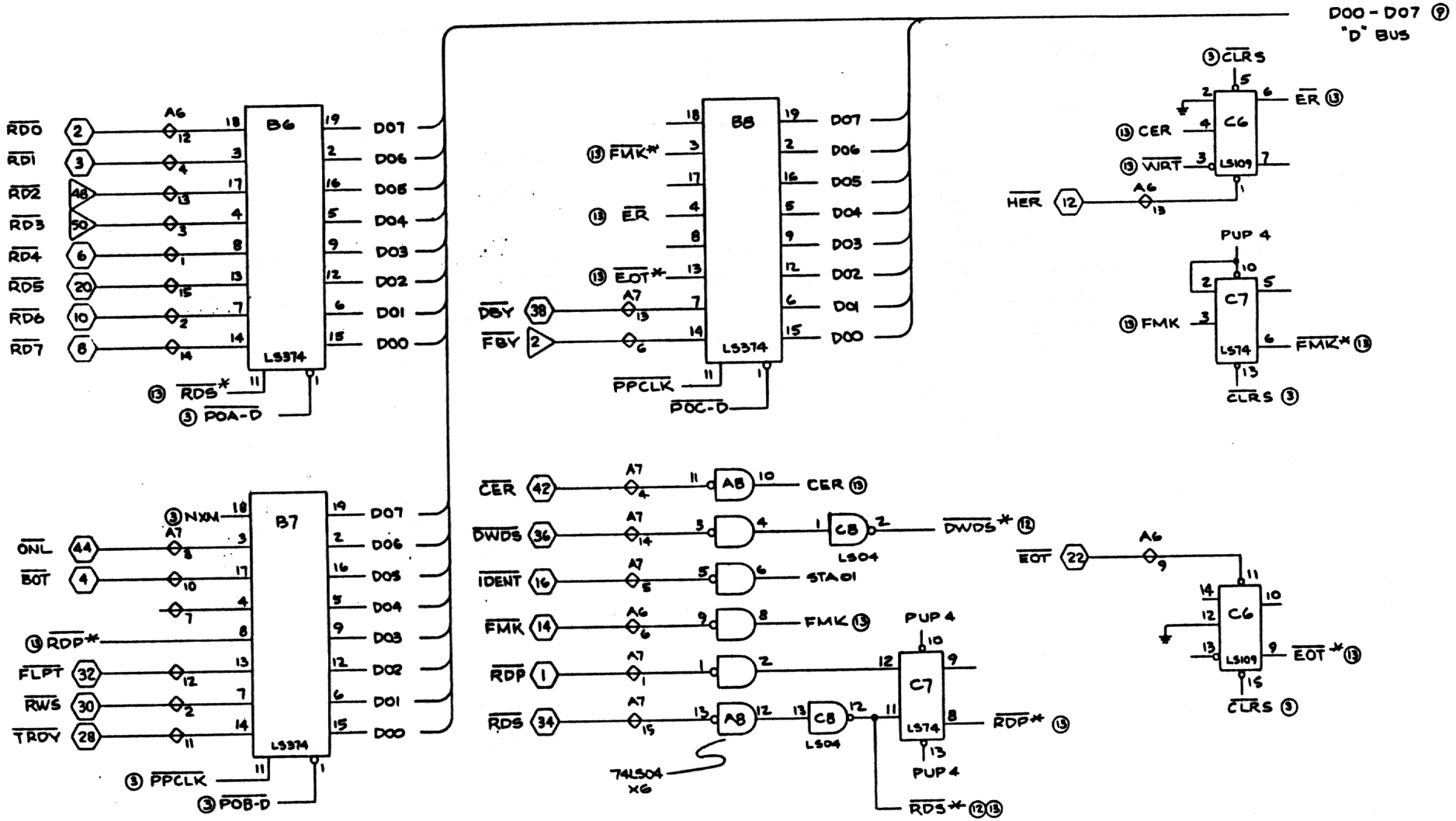

SYMBOL ▷ INDICATES "J4", 50 PIN CONNECTOR (ALL ODD PINS ARE GND.)

SYMBOL ⬡ INDICATES "J5", 50 PIN CONNECTOR (ODD PINS EXCEPT 1 & 3 ARE GND.)

NOTE: SYMBOL —◇— INDICATES 220Ω/330Ω TERMINATOR

DISTRIBUTED LOGIC CORP.		
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DATE:		REVISED
LOGIC DIAGRAM, DU130		SHT 13 OF 14
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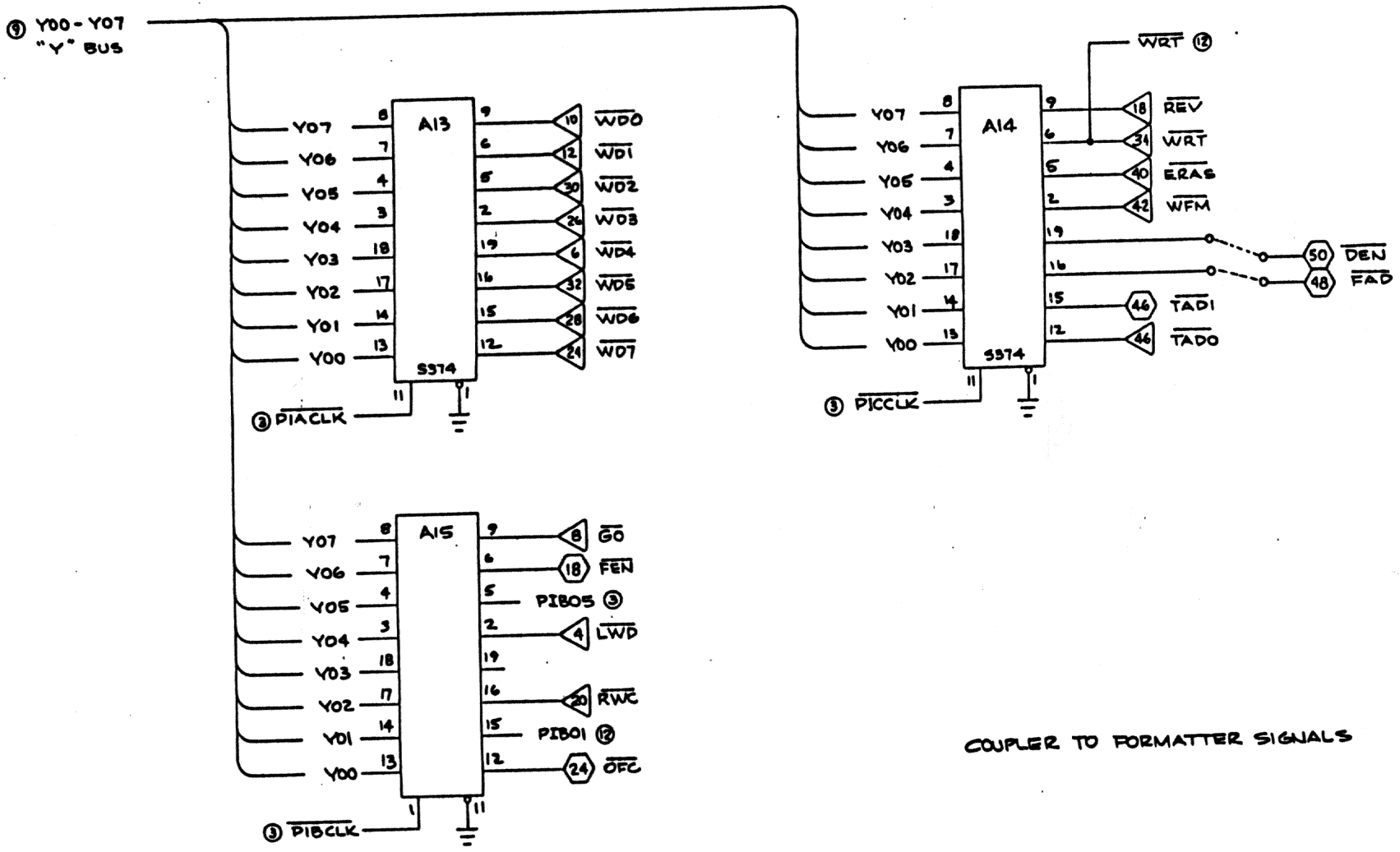

COUPLER TO FORMATTER SIGNALS

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LOGIC DIAGRAM, DU130		SHT 14 OF 14
		DRAWING NUMBER 853019

APPENDIX A

CABLE LIST

TABLE 1-2A: COUPLER TO FORMATTER INTERFACE LINES

Coupler Connector J4 to:
- A) Cipher F100X, F900X, Pertec; Connector P4
- B) Cipher F880; Connector P1
- C) CDC, Tandberg; Connector J125
- D) Digi-Data; Connector J4
- E) Kennedy Streamer; J1
- F) Kennedy Formatted drive; J1

J4 SIGNAL	J4 GROUND	MNENONIC	DIRECTION	DESCRIPTION
2	1	FFBY	IN	Formatter Busy
4	3	FLWD	0	Last Word
6	5	FWD4	0	Write Data 4
8	7	FGO	0	Initiate Command
10	9	FWDO	0	Write Data 0
12	11	FWD1	0	Write Data 1
13	13	F5GL	---	Not Used
16	15	FLOL	---	Load on Line
18	17	FREV	0	Reverse/Forward
20	19	FREW	0	Rewind
22	21	FWDP	---	Write Data Parity
24	23	FWD7	0	Write Data 7
26	25	FWD3	0	Write Data 3
28	27	FWD6	0	Write Data 6
30	29	FWD2	0	Write Data 2
32	31	FWD5	0	Write Data 5
34	33	FWRT	0	Write/Read
---	35	FRTh2	---	Read Threshold 2
---	37	FEDIT	---	EDIT
40	39	FERASE	OUT	Erase
42	41	FWFM	OUT	Write File Mark
44	43	FRTH1	---	Not Used
45*	---	FPAR	---	Not Used
46	45	FTADO	OUT	Transport Address 0
48	47	FRD2	IN	Read Data 2
50	49	FRD3	IN	Read Data 3

---

* Grounded except when working with 7 track formatter.

TABLE 1-2B: COUPLER TO FORMATTER INTERFACE LINES

Coupler Connector J1 to:
A) Cipher F100X, F900X, Pertec; Connector P5
B) Cipher F880; Connector P2
C) CDC, Tandberg; Connector J124
D) Digi-Data; Connector J3
E) Kennedy Streamer; J2
F) Kennedy Formatted drives; J5

J5 SIGNAL	J5 GROUND	MNEMONIC	DIRECTION	DESCRIPTION
1		FRDP	I	Read Data Parity
2		FRDO	I	Read Data 0
3		FRD1	I	Read Data 1
4		FLDP	I	Load Point
6	5	FRD4	I	Read Data 4
8	7	FRD7	I	Read Data 7
10	9	FRD6	I	Read Data 6
12	11	FHER	I	Hard Error
14	13	FFMK	I	File Mark
16	15	FCCG/ID	I	CCG/IDENT
18	17	FFEN	0	Formatter Enable
20	19	FRD5		Read Data 5
22	21	FEOT		End of Tape
24	23	FOFL		Off Line
26	25*	FNRZ		NRZI
25*		F7TR		7 Track
28	27			Ready
30	29	FRWD		Rewinding
32		FFPT		File Protect
34	33	FRSTR		Read Strobe
36	35	FDWDS		Demand Write Data Strobe
38	37	FDBY		Data Busy
40	39	FSPEED		Speed
42	41	FCER		Corrected Error
44	43	FONL		On-Line
47	45	FTAD1		Transport Address 1
48	47	FFAD		Formatter Address
50	49	FDEN		Density Select

* Grounded except for 7 track formatter.

APPENDIX B

GLOSSARY OF TERMS

APPENDIX B: GLOSSARY OF TERMS

TERM	DESCRIPTION
A00	Q bus Address bit 0, LSB
A01	Q bus Address bit 1
A02	Q bus Address bit 2
A03	Q bus Address bit 3, MSB
ACK	Acknowledge
ACKFF	Acknowledge Flip-Flop
ADRA	Address A
ADRB	Address B
A00FF	Address bit 0 Flip-Flop
As00	A State Sequencer bit 00
AS01	A State Sequencer bit 01
As02	A State Sequencer bit 02
BACT FF	Bus Activity Flip-Flop
BBS7 L	Q bus Bank Seven Select
BDAL00 L-	Q bus Data Address Lines (16)
BDAL15 L	
BDCOKH	Q bus DC power OK
BDOUT L	Q bus Data Out from master
BDIN L	Q bus Data In from master
BDMGI L	Q bus DMA Grant In
BDMGO L	Q bus DMA Grant Out
BIAKI L	Q bus Interrupt Acknowledge Input
BIAKO L	Q bus Interrupt Acknowledge Output
BINIT L	Q bus Initialize
BIRQ L	Q bus Interrupt Request
BDMR L	Q bus Direct Memory Request
$\overline{\text{BOT}}$	Beginning of Tape Mark
BRPLY L	Q bus Reply from slave
BSACK L	Q bus Select Acknowledge
$\overline{\text{BSTCLK}}$	Q bus Clock
BSYNK L	Q bus Synchronize
BWTBT L	Q bus Write Byte
BR^{O}FF	Bus Reply Flip-Flop
BSS7	Bank 7 Select
BSY	Busy

TERM	DESCRIPTION
CLKA	Clock 10 megahertz
$\overline{\text{CLK 1}}$	Clock one to the tape drive
CN+2	Carry output of 2901
$\overline{\text{CLRB}}$	Clear Bus
$\overline{\text{CLR}}$	Clear
CR1-00-- CR1-07	Control Register one output bits 0-7
CR2-00-- CR2-07	Control Register two output bits 0-7
CR3-00-- CR4-07	Control Register three output bits 0-7
CR4-00-- CR4-07	Control Register four output bits 0-7
CR5-00-- CR5-07	Control Register five output bits 0-7
CS	Carry signal out of second 2901
CSA00-- CSA08	Control Store Address bits 0 through 08 (9)
D00-- D07	2901 Data bus bits 0-7
DA	Data Enable
DA16,DA17	Data Address bits 15 and 17
DB00- DB15	Data bus bits 00-15 from A bus Bit 15 is MSB, bit 00 is LSB
DB16,DB17	Data bus bits 16 and 17 (Address extension)
$\overline{\text{DEN}}$	Device Enable
DIN	Data In
DINFF	Data In Flip-Flop
DMG	Direct Memory Grant Delayed
DMGFF	Direct Memory Grant Flip-Flop
DMGI	Direct Memory Grant in from Q bus
+DMR	Direct Memory Request
DOUT	Data Out
DOUTFF	Data Out Flip-Flop
DRQFLG	Data Request Flag
DSL	Density Select to Tape
$\overline{\text{EOT}}$	End of Tape from Tape

TERM	DESCRIPTION
$\overline{\text{FLPT}}$	File Protect from tape
FI00	File In bits 0-15
FI15	
FUNC	Function
FØ0O--	File Out bits 0-15
FØ15	
$\overline{\text{FL-D}}$	File Lower Data
$\overline{\text{FU-D}}$	File Upper Data
$\overline{\text{FLCLK}}$	File Lower Byte Clock
FUCLK	File Upper Byte Clock
LDADD	Load Address
LIT	Literal
$\overline{\text{MRST}}$	Master Reset
MRQA	Memory Request A
MRQB	Memory Request B
MTC	Magnetic Tape Control
$\overline{\text{MTR}}$	Magnetic Tape Request
MTS	Magnetic Tape Status
NXM	Non Existant Memory
OFC	Off Line Command to Tape
$\overline{\text{ONL}}$	On Line Status from Tape
PAUSE	
PBSYS	Peripheral Bus Set
PARS	Parity Status from Tape
$\overline{\text{PIACLK}}$	Peripheral In A byte clock
$\overline{\text{PIBCLK}}$	Peripheral In B byte clock
$\overline{\text{PICCLK}}$	Peripheral in C byte clock
$\overline{\text{PØA-D}}$	Peripheral Out A Byte Data
$\overline{\text{PØB-D}}$	Peripheral Out B Byte Data
PPCLK	Processor Clock
PIA00-07	Peripheral In A
PIB00-07	Peripheral In B
PIC00-07	Peripheral In C

TERM	DESCRIPTION
PPCLK*	Processor Clock
RDO-AD7	Read Data bits 0-7 from Tape
$\overline{\text{RDP}}$	Read Data Parity from Tape
$\overline{\text{RDS}}$	Read Data Strobe from Tape
RSYNC	Synchronize From Q bus
RWC	Rewind Command to Tape
7TRK	7 of 9 Track Status from Tape
SEL1-SEL4	Select Tapes 1, 2, 3, or 4
SFC	Synchronous Forward Command to Tape
SWS	Set Write Status
SRC	Synchronous Reverse Command to Tape
$\overline{\text{STA}}$	Status
STORL,U	Store Lower, Upper Byte
TA	Tag clock for extended address bits
TDIN	Transmit D Bus In
TDOUT	Transmit D Bus Out
TDOOG	Transmit D Bus bit 00 Gated
TDMR	Transmit Direct Memory Request
TDMG	Transmit Direct Memory Grant
TIAK	Transmit Interrupt Acknowledge
TIRQ	Transmit Interrupt Request
TRPLY	Transmit Reply
TSACK	Transmit Select Acknowledge
TO	Time Out
TOD	Time Out Delay
TSYNC	Transmit Sync
$\overline{\text{TRDY}}$	Tape Ready from Tape
TWTBT	Transmit Write Byte
VS	Overflow from 2901
WARS	Write Amplifier Reset to Tape
WDS	Write Data Strobe to Tape
WDP	Write Data Parity to Tape
WDO-WD7	Write Data Lines (8) to Tape
$\overline{\text{WRL}}$	Write Load
$\overline{\text{WRU}}$	Write Unload
WTBTFF	Write Byte Flip-Flop
YOO--	Write Byte Flip-Flop
YO7	Y Bus bits 0 through 7