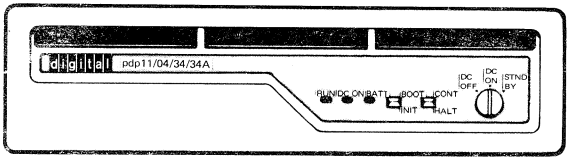
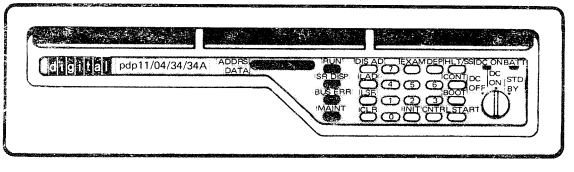
Dick Wilds BST

digital

PDP-11/04/34/34A

Maintenance Card





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EK-11034-MC-003

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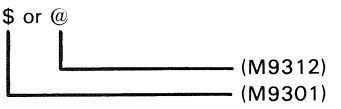
CONSOLE EMULATOR

Sequence of events for standard* M9301/M9312 configuration on power up,

When boot switch depressed or return of ac power:

1. Primary CPU tests are executed (loop on error).
2. Register printout and prompt character.

(R0)	(R4)	(SP)	(PC)
XXXXXX	XXXXXX	XXXXXX	XXXXXX



3. User can now exercise console functions provided by console emulator routine.
4. On bootstrap command, secondary CPU and memory tests are executed. These will halt on error, or if successful will boot device.

Console Functions	Keyboard Strokes
Load Address	L <SB> XXXXXX <CR>
Examine	E <SB>
Deposit	D <SB> XXXXXX <CR>
Start	S <CR>
Bootstrap	<Code> n <CR>

<SB> = Space bar
<CR> = Carriage return

n = Unit number (optional; defaults to 0)

*For standard configuration, see page: 23, M9301; 26, M9312.

CONSOLE EMULATOR – continued

Device	Code	M9301			M9312
		YA	YB	YF	
PC05	PR	X	X	X	X
DL11-A/W	TT	X	X	X	X
TU55/56	DT	X	X	X	X
TU/TE10, TS03	MT	X	X	X	X
TU/TE16, TM02/03	MM		X	X	X
TU60	CT	X	X		X
TU58	DD				X
TS04	MS				X
RX01	DX	X	X	X	X
RX02	DY				X
RK03/05/05J	DK	X	X	X	X
RP02/03	DP	X	X	X	X
RP04/05/06, RM02/03	DB		X	X	X
RL01	DL				X
RK06/07	DM			X	X
RS03/04	DS		X	X	X

Cross Reference: Device to Controller

Device	Controller
PC05 (hi spd rdr)	PC11/R11
ASR-33 (lo spd rdr)	DL11-A/W
TU55/56	TC11
TU/TE10, TS03	TM11/A11/B11
TU/TE16, TM02,03	RH11
TU60	TA11
RX01	RX11
RX02	RXC11
RK03/05/05J	RK11-C/D
RP02/03	RP11-C/E
RP04/05/06, RM02/03	RH11
RL01	RL11
RK06/07	RK611
RS03/04	RH11

CONSOLE EMULATOR – DIAGNOSTICS

If M9301/M9312 is configured to run diagnostics and a halt occurs when booting a device:

1. Obtain register printout and prompt by rebooting.
2. Address in PC will indicate type of halt (processor or memory).
3. If a memory halt, contents of R0, R4, and SP are interpreted as shown below.

PROCESSOR HALTS

PC = 165316, 165346, 165370 → YA
173450, 173470, 173512 → YB
165646, 165662, 165676 → YF, M9312

MEMORY HALTS

	YA,YB	YF,M9312
R0 =	Expected Data	Failing address
R4 =	Received data	Received data
SP =	Failing address	Expected data

PC = 165334 → YA
173762 → YB
165776 → YF
165772 → M9312

KY11-LB PROGRAMMER'S CONSOLE

|KEY| = Function

|LAD| = (Display) → Address Reg*
|DIS AD| = Address Register → Display
|EXAM| = (Address) → Display
|DEP| = (Display) → (Address)
|CLR| = CLR TDB
|LSR| = (Display) → Switch Reg
|CNTRL-HLT/SS| = Halt/PC → Display
|HLT/SS| (While Halted) = Inst. Step
|CNTRL-CONT| = Continue
|CNTRL-BOOT| = M9301/M9312 Program
|CNTRL-START| = Start
|CNTRL-INIT| = Init
|CNTRL-#1| = Enter maintenance mode
See KY11-LB User's Guide for setup and use of maintenance mode

(Display) = TDB = Temp Data Buffer

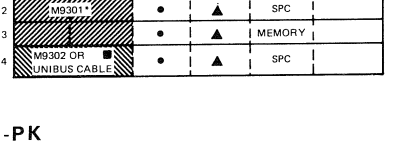
LED INDICATORS

DC ON	All dc power +5 V to logic is on
BATT	Battery monitor IND (operative if BBU option present) OFF – No battery present or battery failure ON – Battery present and charged Flashing (slow)– AC power OK and battery is charging. Flashing (fast) – Loss of ac power; battery is discharging while maintaining MOS memory contents
RUN	State of processor, running or halted
SR disp	Contents of switch register being displayed
MAINT	Console in maintenance mode
BUS ERR	Examine or deposit resulted in a SSYN timeout or a HALT REQ from the console failed to receive a HALT GRANT

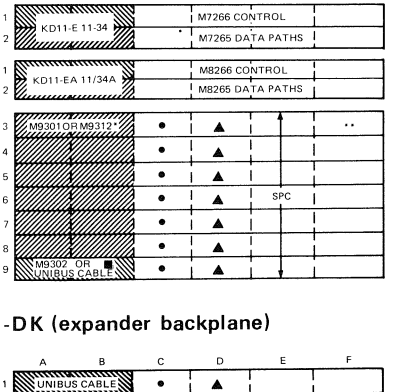
* An 18-bit number is stored in Temp register.

DD11-CK/DK/PK BACKPLANES

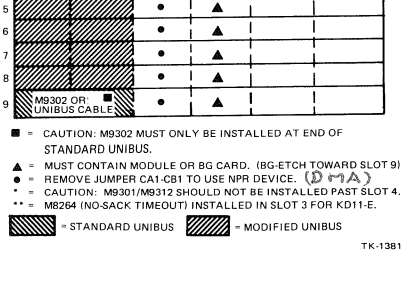
DD11-CK



DD11-PK



DD11-DK (expander backplane)



■ = CAUTION: M9302 MUST ONLY BE INSTALLED AT END OF STANDARD UNIBUS.

▲ = MUST CONTAIN MODULE OR BG CARD. (BG-ETCH TOWARD SLOT 9).

● = REMOVE JUMPER CA1-CB1 TO USE NPR DEVICE. (DMA)

* = CAUTION: M9301/M9312 SHOULD NOT BE INSTALLED PAST SLOT 4.

** = M8264 (NO-SACK TIMEOUT) INSTALLED IN SLOT 3 FOR KD11-E.

= STANDARD UNIBUS = MODIFIED UNIBUS

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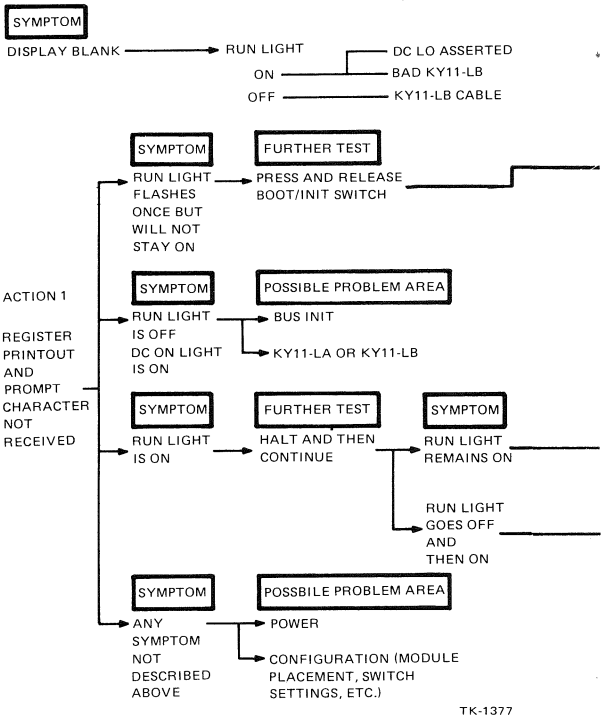
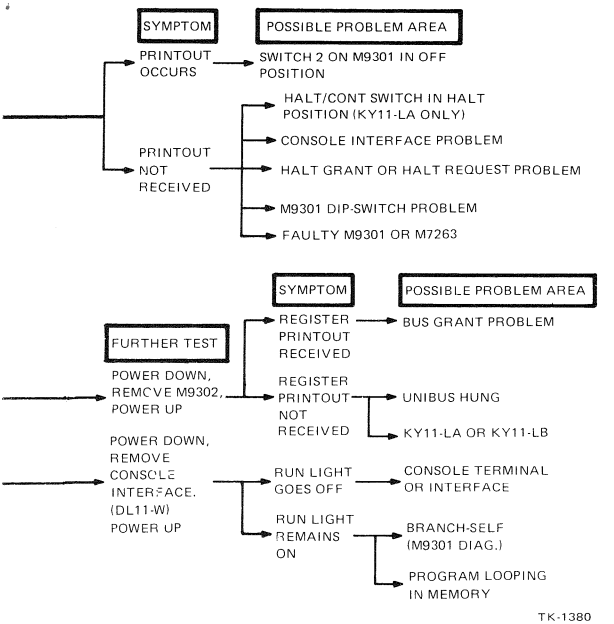
TROUBLESHOOTING



NOTE

For a detailed explanation of these troubleshooting actions, refer to PDP-11/34 Systems User Manual, Section 6.

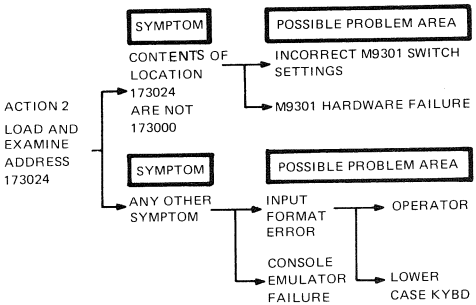
TROUBLESHOOTING – continued

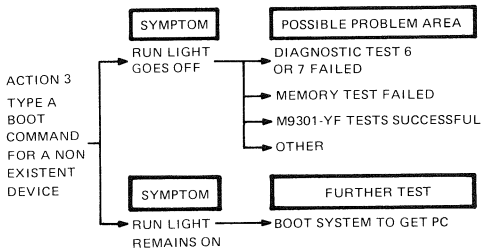


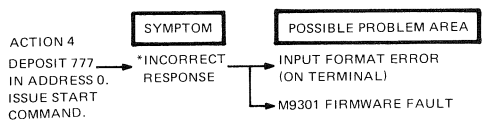
NOTE

DC on light does not necessarily indicate that dc power is within the required levels.

TROUBLESHOOTING – continued







*KEY BOARD SHOULD NO LONGER RESPOND AND THE RUN LIGHT SHOULD BE ON.

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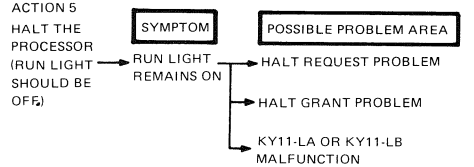
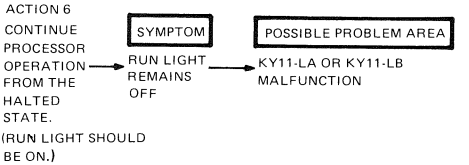
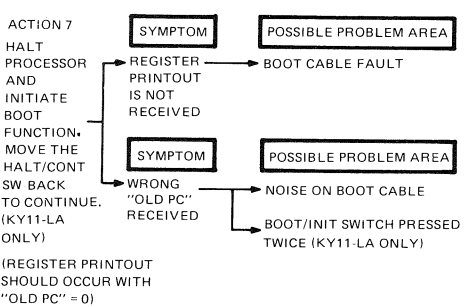
TROUBLESHOOTING – continued







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PROCESSOR JUMPERS

KD11-EA **11/34A**

M8265 (Data Paths)
W1, W2 – IN

M8266 (Control)
Enable parity detection – W1-IN
Disable parity detection – W1-OUT

KD11-E **11/34**

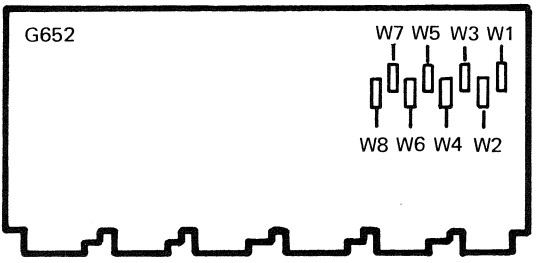
M7265 (Data Paths)
W1, W2 – IN

M7266 (Control)
Enable parity detection – W1-OUT, W2-IN
Disable parity detection – W1-IN, W2-OUT

KD11-D **11/04**

M7263
Enable parity detection – W1-IN, W2-OUT
Disable parity detection – W1-OUT, W2-IN

MM11-DP



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NOTE

Jumpers W9-W11 are factory set and not shown.

(NON-INTERLEAVED) W5, W6 OUT

STARTING ADDRESS ASSIGNMENT

Address					
Decimal	Octal	W1	W2	W3	W4
0K	000000	OUT	OUT	OUT	IN
8K	040000	OUT	OUT	IN	OUT
16K	100000	OUT	OUT	IN	IN
24K	140000	OUT	IN	OUT	OUT
32K	200000	OUT	IN	OUT	IN
40K	240000	OUT	IN	IN	OUT
48K	300000	OUT	IN	IN	IN
56K	340000	IN	OUT	OUT	OUT
64K	400000	IN	OUT	OUT	IN
72K	440000	IN	OUT	IN	OUT
80K	500000	IN	OUT	IN	IN
88K	540000	IN	IN	OUT	OUT
96K	600000	IN	IN	OUT	IN
104K	640000	IN	IN	IN	OUT
112K	700000	IN	IN	IN	IN

W7 and W8 – OUT for PDP-11/04/34/34A.

INTERLEAVED MEMORY OPERATION

- One memory is assigned the odd addresses and the other the even addresses within the same 32K block.
  W5-IN, W6-OUT – assigns even addresses
  W5-OUT, W6-IN – assigns odd addresses
- Both memories must be assigned the same starting address.

STARTING ADDRESS ASSIGNMENT
(Interleaved-Memory Operation)

Address					
Decimal	Octal	W1	W2	W3	W4
0K	000000	OUT	OUT	IN	IN
8K	040000	OUT	IN	OUT	OUT
16K	100000	OUT	IN	OUT	IN
24K	140000	OUT	IN	IN	OUT
32K	200000	OUT	IN	IN	IN
40K	240000	IN	OUT	OUT	OUT
48K	300000	IN	OUT	OUT	IN
56K	340000	IN	OUT	IN	OUT
64K	400000	IN	OUT	IN	IN
72K	440000	IN	IN	OUT	OUT
80K	500000	IN	IN	OUT	IN
88K	540000	IN	IN	IN	OUT
96K	600000	IN	IN	IN	IN

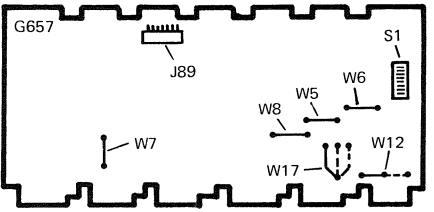
BACKPLANE INSTALLATION

DD11-PK – Slots 2–8 (11/04)
DD11-PK – Slots 3–8 (11/34,34A)
DD11-DK – Slots 2–8
DD11-CK – Slots 2 and 3

NOTE

A grant continuity card (G727) must be installed in slot D of the overhanging memory module.

MM11-YP CORE



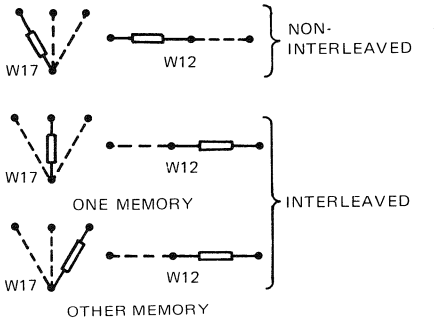
NOTE: JUMPERS NOT SHOWN ARE FACTORY SET AND SHOULD NOT BE ALTERED IN THE FIELD.

JUMPERS

W5 W6
OUT OUT – Out for PDP-11/04/34/34A

W7 W8
IN IN – For parity operation

INTERLEAVED/NON-INTERLEAVED OPERATION



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J89 – Provides connection for the field service memory margining device. P/N 70-11459.
S1 – Starting address selection.

STARTING ADDRESS ASSIGNMENT

Address		S1 Switch Selection				
		S1-1	S1-2	S1-3	S1-4	S1-5
0K	000000	ON	ON	ON	ON	ON
4K	020000	ON	ON	ON	ON	OFF
8K	040000	ON	ON	ON	OFF	ON
12K	060000	ON	ON	ON	OFF	OFF
16K	100000	ON	ON	OFF	ON	ON
20K	120000	ON	ON	OFF	ON	OFF
24K	140000	ON	ON	OFF	OFF	ON
28K	160000	ON	ON	OFF	OFF	OFF
32K	200000	ON	OFF	ON	ON	ON
36K	220000	ON	OFF	ON	ON	OFF
40K	240000	ON	OFF	ON	OFF	ON
44K	260000	ON	OFF	ON	OFF	OFF
48K	300000	ON	OFF	OFF	ON	ON
52K	320000	ON	OFF	OFF	ON	OFF
56K	340000	ON	OFF	OFF	OFF	ON
60K	360000	ON	OFF	OFF	OFF	OFF
64K	400000	OFF	ON	ON	ON	ON
68K	420000	OFF	ON	ON	ON	OFF
72K	440000	OFF	ON	ON	OFF	ON
76K	460000	OFF	ON	ON	OFF	OFF
80K	500000	OFF	ON	OFF	ON	ON
84K	520000	OFF	ON	OFF	ON	OFF
88K	540000	OFF	ON	OFF	OFF	ON
92K	560000	OFF	ON	OFF	OFF	OFF
96K	600000	OFF	OFF	ON	ON	ON
100K	620000	OFF	OFF	ON	ON	OFF
104K	640000	OFF	OFF	ON	OFF	ON
108K	660000	OFF	OFF	ON	OFF	OFF
112K	700000	OFF	OFF	OFF	ON	ON
116K	720000	OFF	OFF	OFF	ON	OFF
120K	740000	OFF	OFF	OFF	OFF	ON

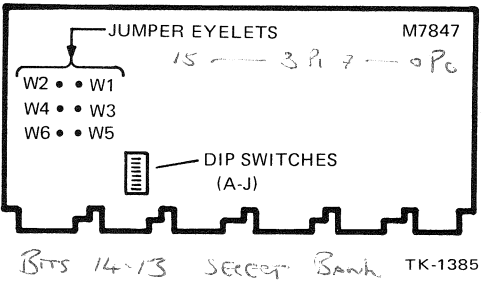
NOTE

For interleaved operation, both memories must have the same starting address.

BACKPLANE INSTALLATION

DD11-PK – Slots 2–8 (11/04)
DD11-PK – Slots 3–8 (11/34,34A)
DD11-DK – Slots 2–8
DD11-CK – Slots 2 and 3

MS11-EP/FP/JP – MOS



MEMORY SIZE JUMPERS/SWITCHES

Size	W3–W4	W1–W2	W5–W6	F	H	J
4K	IN	OUT	OUT	OFF	OFF	OFF
8K	IN	IN	OUT	OFF	OFF	OFF
12K	IN	IN	IN	OFF	OFF	OFF
16K	IN	IN	IN	OFF	ON	OFF

BACKPLANE INSTALLATION

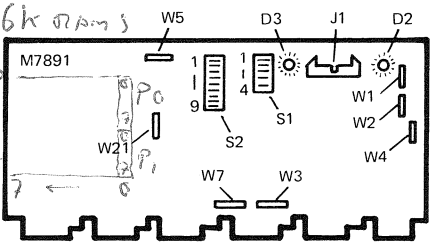
DD11-PK – Slots 2–8 (11/04)
DD11-PK – Slots 3–8 (11/34,34A)
DD11-DK – Slots 2–8
DD11-CK – Slots 2 or 3

SW2
SWITCHES 1 2 3 4 5

STARTING ADDRESS ASSIGNMENT

Address		Switch Selection				
Decimal	Octal	A	B	C	D	E
0K	000000	OFF	OFF	OFF	ON	ON
4K	020000	OFF	OFF	ON	OFF	OFF
8K	040000	OFF	OFF	ON	OFF	ON
12K	060000	OFF	OFF	ON	ON	OFF
16K	100000	OFF	OFF	ON	ON	ON
20K	120000	OFF	ON	OFF	OFF	OFF
24K	140000	OFF	ON	OFF	OFF	ON
28K	160000	OFF	ON	OFF	ON	OFF
32K	200000	OFF	ON	OFF	ON	ON
36K	220000	OFF	ON	ON	OFF	OFF
40K	240000	OFF	ON	ON	OFF	ON
44K	260000	OFF	ON	ON	ON	OFF
48K	300000	OFF	ON	ON	ON	ON
52K	320000	ON	OFF	OFF	OFF	OFF
56K	340000	ON	OFF	OFF	OFF	ON
60K	360000	ON	OFF	OFF	ON	OFF
64K	400000	ON	OFF	OFF	ON	ON
68K	420000	ON	OFF	ON	OFF	OFF
72K	440000	ON	OFF	ON	OFF	ON
76K	460000	ON	OFF	ON	ON	OFF
80K	500000	ON	OFF	ON	ON	ON
84K	520000	ON	ON	OFF	OFF	OFF
88K	540000	ON	ON	OFF	OFF	ON
92K	560000	ON	ON	OFF	ON	OFF
96K	600000	ON	ON	OFF	ON	ON
100K	620000	ON	ON	ON	OFF	OFF
104K	640000	ON	ON	ON	OFF	ON
108K	660000	ON	ON	ON	ON	OFF
112K	700000	ON	ON	ON	ON	ON
116K	720000	OFF	OFF	OFF	OFF	OFF
120K	740000	OFF	OFF	OFF	OFF	ON

MS11-L



NOTE: JUMPERS W10-W16 AND W20 ARE FACTORY SET AND NOT SHOWN.

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JUMPERS

W5 **W21**
OUT IN – for PDP-11/04/34/34A

W3 **W7**
OUT IN – +5 V and +5 V BBU (Normal Configuration)
IN OUT – +5 V only

W1 **W2**
OUT IN – ±15 V (PDP-11/04/34/34A)
IN OUT – ±12 V

W4
OUT – ~~Unibus~~/MUD operation (PDP-11/04/34/34A)
IN – Special bus operation

SWITCHES/LEDS

S1 – Selects CSR address
S2 – Assigns MS11-L starting address
D2 – Indicates +5 V or +5 V BBU power is being supplied to refresh logic (green).

NOTE

MS11-L should not be extracted while D2 is ON.

D3 – Indicates a parity error has occurred (red).

MS11-L – continued

STARTING ADDRESS ASSIGNMENT

Address		S2 Switch Selection				
Decimal	Octal	S2-5	S2-6	S2-7	S2-8	S2-9
0K	000000	ON	ON	ON	ON	ON
4K	020000	ON	ON	ON	ON	OFF
8K	040000	ON	ON	ON	OFF	ON
12K	060000	ON	ON	ON	OFF	OFF
16K	100000	ON	ON	OFF	ON	ON
20K	120000	ON	ON	OFF	ON	OFF
24K	140000	ON	ON	OFF	OFF	ON
28K	160000	ON	ON	OFF	OFF	OFF
32K	200000	ON	OFF	ON	ON	ON
36K	220000	ON	OFF	ON	ON	OFF
40K	240000	ON	OFF	ON	OFF	ON
44K	260000	ON	OFF	ON	OFF	OFF
48K	300000	ON	OFF	OFF	ON	ON
52K	320000	ON	OFF	OFF	ON	OFF
56K	340000	ON	OFF	OFF	OFF	ON
60K	360000	ON	OFF	OFF	OFF	OFF
64K	400000	OFF	ON	ON	ON	ON
68K	420000	OFF	ON	ON	ON	OFF
72K	440000	OFF	ON	ON	OFF	ON
76K	460000	OFF	ON	ON	OFF	OFF
80K	500000	OFF	ON	OFF	ON	ON
84K	520000	OFF	ON	OFF	ON	OFF
88K	540000	OFF	ON	OFF	OFF	ON
92K	560000	OFF	ON	OFF	OFF	OFF
96K	600000	OFF	OFF	ON	ON	ON
100K	620000	OFF	OFF	ON	ON	OFF
104K	640000	OFF	OFF	ON	OFF	ON
108K	660000	OFF	OFF	ON	OFF	OFF
112K	700000	OFF	OFF	OFF	ON	ON
116K	720000	OFF	OFF	OFF	ON	OFF
120K	740000	OFF	OFF	OFF	OFF	ON
124K	760000	OFF	OFF	OFF	OFF	OFF

NOTE

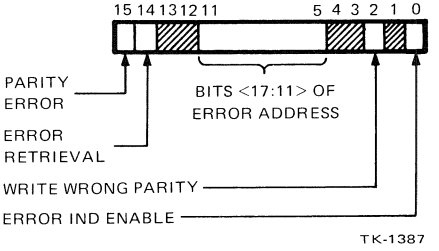
Switch positions S2-1 through S2-4 should be set to the ON position for PDP-11/04/34/34A.

CSR ADDRESS SELECTION

Address	S1-1	S1-2	S1-3	S1-4
772100	ON	ON	ON	ON
772102	ON	ON	ON	OFF
772104	ON	ON	OFF	ON
772106	ON	ON	OFF	OFF
772110	ON	OFF	ON	ON
772112	ON	OFF	ON	OFF
772114	ON	OFF	OFF	ON
772116	ON	OFF	OFF	OFF
772120	OFF	ON	ON	ON
772122	OFF	ON	ON	OFF
772124	OFF	ON	OFF	ON
772126	OFF	ON	OFF	OFF
772130	OFF	OFF	ON	ON
772132	OFF	OFF	ON	OFF
772134	OFF	OFF	OFF	ON
772136	OFF	OFF	OFF	OFF

The MS11-L memory does not require a parity controller (M7850) but it can be installed in the same backplane as other memories utilizing an M7850.

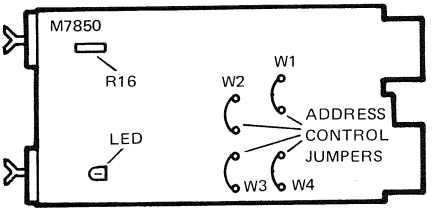
CSR



MS11-L BACKPLANE INSTALLATION

DD11-PK – Slots 3–8
DD11-DK – Slots 2–8
DD11-CK – Slots 2 and 3

M7850 PARITY CONTROLLER

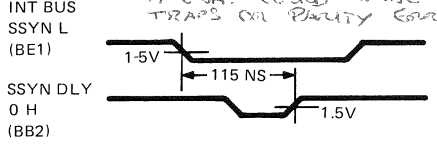


W5 IS FACTORY SET AND NOT SHOWN

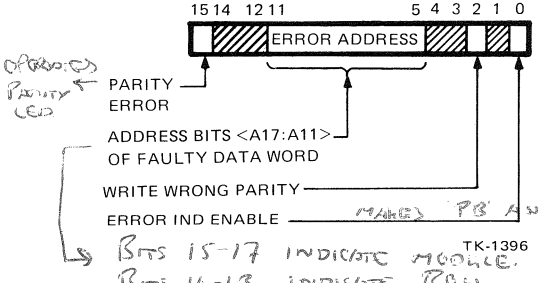
- One M7850 will generate and check parity for all memory in its backplane.
- The M7850 does not differentiate between core or MOS.
- When a parity error is detected, the parity error LED is latched ON. If error IND ENABLE (CSR bit 0) is set, the processor traps to 114.
- When installed, the M7850 intercepts MEMORY SSYN and asserts BUS SSYN after checking parity.

SSYN DELAY (Adjustable via R16)

IF ONA. COULD CAUSE SPURIOUS TRAPS ON PARITY ERRORS.



CSR



TK-1396

BITS 15-17 INDICATE MODULE.
BITS 14-13 INDICATE ROW.

M7850 PARITY CONTROLLER – continued

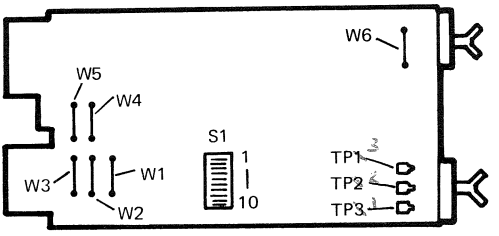
M7850 CSR address is factory set at 772100. Jumpers W1–W4 allow selection of a unique address between 772100–772136.

CSR ADDRESS SELECTION

Address	W4	W3	W2	W1
772100*	IN	IN	IN	IN
772102	IN	IN	IN	OUT
772104	IN	IN	OUT	IN
772106	IN	IN	OUT	OUT
772110	IN	OUT	IN	IN
772112	IN	OUT	IN	OUT
772114	IN	OUT	OUT	IN
772116	IN	OUT	OUT	OUT
772120	OUT	IN	IN	IN
772122	OUT	IN	IN	OUT
772124	OUT	IN	OUT	IN
772126	OUT	IN	OUT	OUT
772130	OUT	OUT	IN	IN
772132	OUT	OUT	IN	OUT
772134	OUT	OUT	OUT	IN
772136	OUT	OUT	OUT	OUT

*Standard CSR address.

M9301-YA/YB/YF



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JUMPERS

W1–W6 – out for PDP-11/04/34/34A

FAST ON CONNECTIONS

TP1 *	Black wire to	Boot ENA
TP2	Red wire to	Boot SW
TP3	Shield	NC

*Connect with battery backup only.

SWITCH S1 FUNCTIONS

S1-1 **Low ROM Enable**

YA Must be on to enable diagnostics.

YB,YF Must be on to enable console emulator and diagnostics.

S1-2 **Power-up Reboot Enable**

YA,YB,YF

ON S1-1, 3-10 determine power-up function.

OFF Normal user power-up routine. Trap to 24. (S1-1, 3-10 are ignored.)

S1-3-10 **ROM Address Switches**

YA,YB,YF Switch values determine device that is booted, with or without diagnostics, on power up.

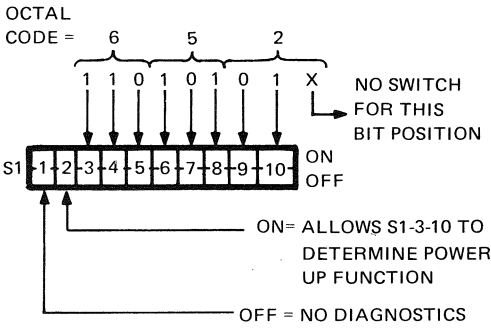
S1 SWITCH SETTINGS

Function On Power Up	Diagnostics	Octal Code S1-3 – S1-10 YA	YB	YF
Vector through 24	YES	002	002	644
	NO	▲	▲	▲
Console emulator	YES *	000	000	000
	NO	030	226	002
Boot DL11	YES	650		364
	NO	652		366
Boot PC11	YES	660		704
	NO	662		706
Boot RK11	YES	440		144
	NO	442		146
Boot RP11	YES	466		040
	NO	470		042
Boot RX11	YES	636		544
	NO	640		546
Boot TA11	YES	624		
	NO	626		
Boot TM11	YES	524		474
	NO	526		476
Boot RK611	YES			662
	NO			664
Boot RH11				
RP04/05/06	YES			224
	NO			226
RS03/04	YES			440
	NO			442
TU16	YES			054
	NO			056

▲ S1-2 OFF – Normal user power up through 24.
(S1-3–10 are ignored.)

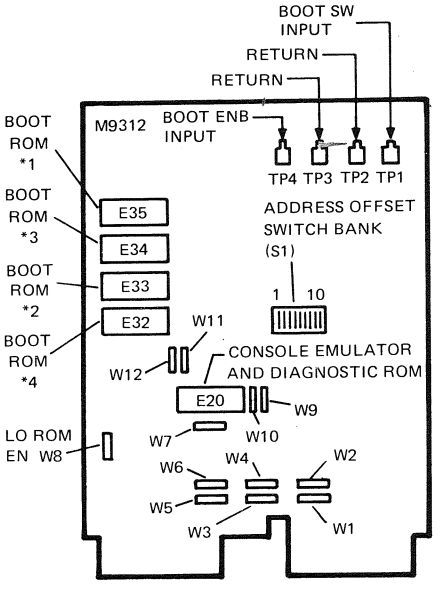
*Standard M9301 configuration.

EXAMPLE: Boot DL11 (YA) with no diagnostics



1 = Switch OFF

0 = Switch On.



JUMPER CONFIGURATION FOR PDP-11/04/34/34A

W1–W6 – OUT
W7 – IN
W8 – OUT
W9–W10 – IN
W11–W12 – OUT

M9301 TO M9312 FAST ON CONVERSION

From M9301	To M9312
Blk TP1	Blk TP4
Red TP2	Red TP1
NC TP3	NC TP3

NC = NOT COLOURED.

CONFIGURATION FOR POWER-UP/BOOT SWITCH FUNCTION

Console Emulator/Diagnostic ROM (P/N 23-248F1)

ROM Location	Diagnostics	S1-3 through 10
E20	NO	144
	YES*	020

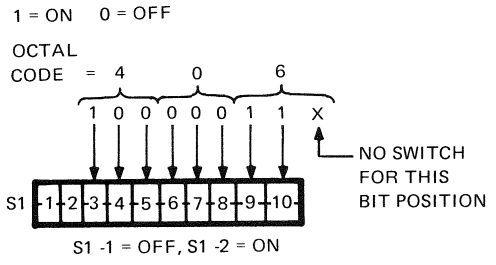
*Standard M9312 configuration.

BOOTSTRAP ROMS

ROM Location	Diag-nostics	Octal Code in S1-3 – 10		
		First Device All ROMS	Second Device 23-755A9 Only	Second Device 23-756A9 and 23-760A9 Only
1 (E35)	NO	004	050	034
1	YES	006	052	036
2 (E33)	NO	204	250	234
2	YES	206	252	236
3 (E34)	NO	404	450	434
3	YES	406	452	436
4 (E32)	NO	604	650	634
4	YES	606	652	636

ALL ROMS MUST BE CONTIGUOUS. IE. NO GAPS.
(CONSOLE EMULATOR WILL FAIL WITH GAPS, ODT WILL NOT)

EXAMPLE: Boot ROM location 3; first device; with diagnostics and power-up boot enabled.



S1-1 ON – Console emulator/diagnostic ROM is addressed on a boot function.
OFF – A device bootstrap ROM is addressed on a boot function.

S1-2 ON – Enables power-up boot.
OFF – Disables power-up boot.

S1-3–10 – The value in these switch positions controls which ROM location is addressed on power-up or boot SW functions.

S1 Configuration Identification Without Removing M9312

1. Load and examine 773024.
2. Display = 165XYZ – indicates S1-1 ON
   = 173XYZ – indicates S1-1 OFF
3. Remaining octal digits (XYZ) are converted to bits and associated to the on/off condition of S1-3 through S1-10.

	XXX	YYY	Z Z	Z 1 = ON
S1-345	678	910		0 = OFF

ROM Identification Without Removing M9312

Perform one of the following two operations.

1. Run MAINDEC CZM9B.
2. Load and examine the following and compare data to table below.

   (E20) 775774 – XXXXXX
   (E35) 773000 – XXXXXX
   (E33) 773200 – XXXXXX
   (E34) 773400 – XXXXXX
   (E32) 773600 – XXXXXX

XXXXXX	Code	P/N
040460	A0	23-248F1
041524	CT	23-761A9
042113	DK	23-756A9
042114	DL	23-751A9
042115	DM	23-752A9
042120	DP	23-755A9
042123	DS	23-759A9
042130	DX	23-753A9
042131	DY	23-811A9
046515	MM	23-757A9
046524	MT	23-758A9
050122	PR	23-760A9
177776	Continuation ROM of a multiple boot ROM	
XXX777	Bad ROM or no ROM present	

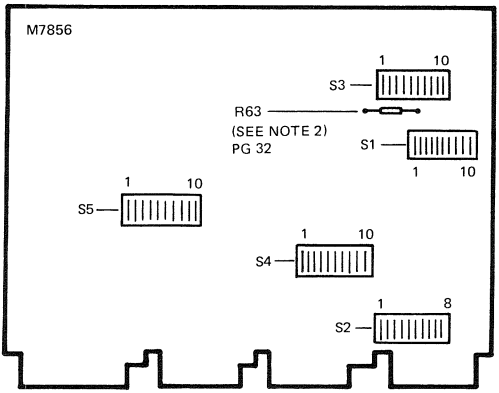
M9312 – continued

ROM IDENTIFICATION

First Device	P/N	Second Device
Console Emulator	23-248F1	
RL01	23-751A9	
RK06/07	23-752A9	
RX01	23-753A9	
RP02/03	23-755A9	RP04/05/06, RM02/03
RK03/05	23-756A9	TU55/56
TU16/E16	23-757A9	
TU10/E10,TS03	23-758A9	
RS03/04	23-759A9	
PC05	23-760A9	DL11-A/W
TU60	23-761A9	
RX02	23-811A9	
TS04	23-764A9	
*		
*		

*Intentionally left blank. Can be used to document new ROMs as they become available.

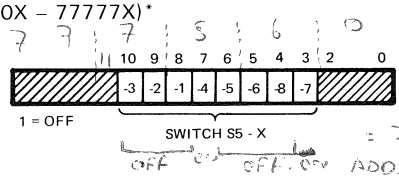
DL11-W



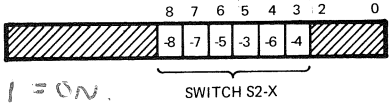
ADDRESS AND VECTOR SELECTION

For standard console device address = 77756X
vector = 06X

ADDRESS:
(77400X – 77777X)*



VECTOR:
(007 – 77X)*



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*The last digit is not determined by the switches.

DL11-W – continued

DATA FORMAT

No. Bits	S4-4	S4-3
5	ON	ON
6	ON	OFF
7	OFF	ON
8	OFF	OFF

No. Stop Bits	S4-5
1	ON
2	OFF*

PARITY

Enable: S4-6 ON
Disable: S4-6 OFF

Odd: S4-2 ON
Even: S4-2 OFF

TRANSMITTER

	S1-1	S1-2	S1-3	S1-6	S1-7
20 mA loop active**	ON	ON	OFF	OFF	ON
20 mA loop passive	OFF	OFF	ON	ON	OFF

RECEIVER

	S3-6	S3-7	S3-8	S3-9	S3-10
Active**	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF

PAPER TAPE READER ENABLE

	S1-4	S1-5	S1-8	S1-9	S1-10
Active**	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF

RCVR Error Bits

Enable: S4-7 ON
Disable: S4-7 OFF

Break

Enable: S4-1 ON
Disable: S4-1 OFF

* 1.5 with five data bits.

** The most common configuration is with the DL11-W active and the terminal passive.

DL11-W – continued

BAUD RATE	XMIT		
	S4-10	S3-1	S3-4
110	ON	ON	ON
150	OFF	ON	ON
300	ON	OFF	OFF
600	ON	OFF	ON
1200	ON	ON	OFF
2400	OFF	OFF	OFF
4800	OFF	OFF	ON
9600	OFF	ON	OFF

BAUD RATE	RECEIVE		
	S3-2	S3-3	S3-5
110	OFF	OFF	OFF
150	ON	OFF	OFF
300	OFF	ON	ON
600	OFF	ON	OFF
1200	OFF	OFF	ON
2400	ON	ON	ON
4800	ON	ON	OFF
9600	ON	OFF	ON

LINE CLOCK

Address set for 777546

S5-9	S5-10		
OFF	ON	–	Enable (SLU and LTC)
ON	OFF	–	Disable (SLU only)
ON	ON	–	DL11-W is line clock only. SLU does not respond to any address.

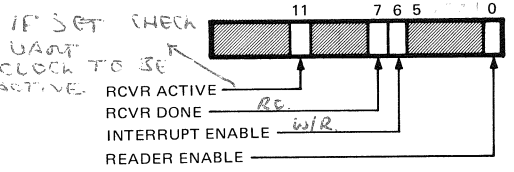
NOTES

1. **LTC must be disabled if SLU is other than console interface.**
2. **When using multiple DL11-W's, only one should have LTC enabled. R63 should be removed on all others.**

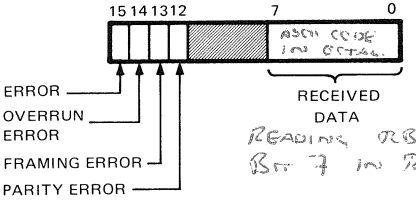
LTC. VECTOR = 100

DL11-W – continued

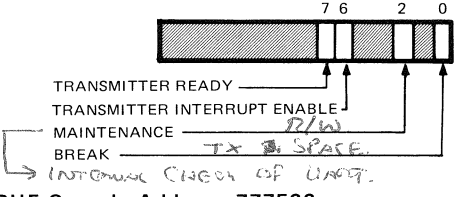
RCSR Console Address: 777560



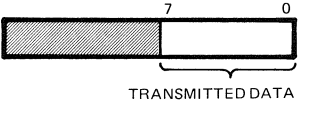
RBUF Console Address: 777562



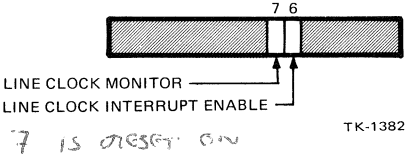
XCSR Console Address: 777564



XBUF Console Address: 777566



LKS Console Address: 777546



KK11-A CACHE M 8268 -11/34A-

- Direct mapping, 1K words
- Cache is installed in slot 3 if FP11-A is not present. If FP11-A is present, cache is installed in slot 5.

NOTE

Memory should be located between cache and all NPR devices.

CACHE RESPONSES TO HIT/MISS OPERATIONS

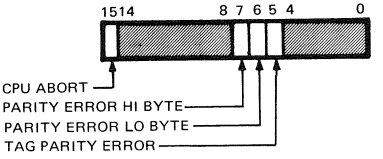
Mode	DMA Miss	DMA Hit	CPU Hit	CPU Miss
Read	Not Affected	Not Affected	Cache Read	Write Data Write Tag Write Valid
Read Bypass	Not Affected	Invalidate	Invalidate	Not Affected
Write Bypass	Not Affected	Invalidate	Invalidate	Not Affected
Write	Not Affected	Invalidate	Write Data Write Valid	Not Affected

When installing cache, compute +5 Vdc consumption for system modules to prevent overloading regulator capacity.

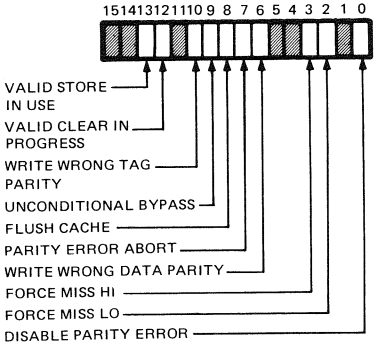
NOTE

Total +5 Vdc consumption for the modules housed in the CPU backplane must not exceed 32 A.

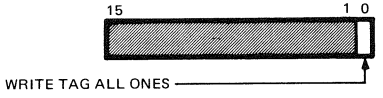
CACHE MEMORY ERROR REGISTER 777744



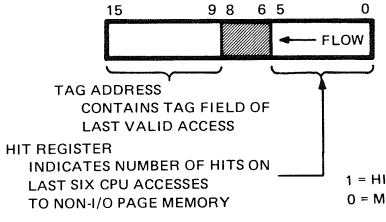
CACHE CONTROL REGISTER 777746



CACHE MAINTENANCE REGISTER 777750



CACHE HIT REGISTER 777752



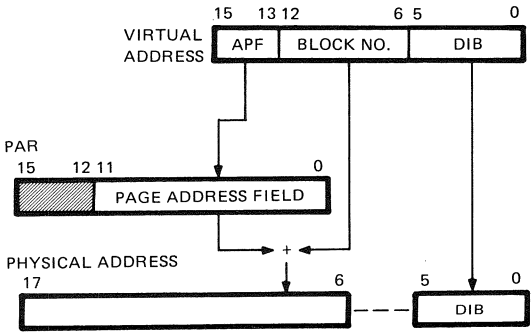
TK-1383

MEMORY MANAGEMENT

CAPABILITIES PROVIDED BY MEMORY MANAGEMENT

• Memory Size (words)	124K max (plus 4K for I/O)
• Address Space	Virtual (16 bits) Physical (18 bits)
• Modes of Operation	Kernel and user
• Stack Pointers	2 (one per mode)
• Memory Relocation	
Block	32_{10} words
Page Length	1 to 128 blocks (32 to 4096 words)
No. of Pages	16 (8 per mode)
• Size of Relocatable Memory	32,768 words max (8 × 4096)
• Memory Protection	No access Read only Read/write

CONSTRUCTION OF A PHYSICAL ADDRESS



APF = ACTIVE PAGE FIELD
DIB = DISPLACEMENT IN BLOCK
PAR = PAGE ADDRESS REGISTER.

TK-1391

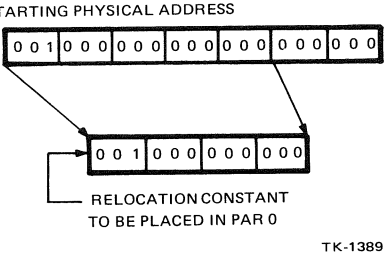
Virtual Address Range	Kernel Addresses PAR	PDR	User Addresses PAR	PDR
0–17776	772340	772300	777640	777600
20000–37776	772342	772302	777642	777602
40000–57776	772344	772304	777644	777604
60000–77776	772346	772306	777646	777606
100000–117776	772350	772310	777650	777610
120000–137776	772352	772312	777652	777612
140000–157776	772354	772314	777654	777614
160000–177776	772356	772316	777656	777616

To calculate a relocation constant:

1. A page may start on any 32_{10} word boundary.
2. Take desired starting physical address.
3. Shift right six places.
4. The remaining 12 bits are the relocation constant used in the PAR.

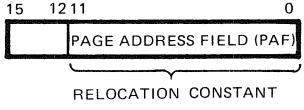
Example:

If PAR 0 (virtual address range 000000–017776) should point to physical address 100000, then:

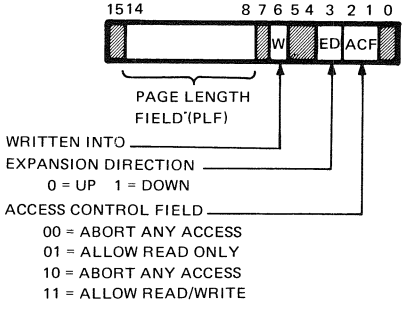


TK-1389

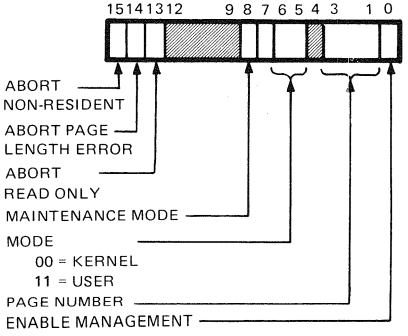
PAGE ADDRESS REGISTER (PAR)



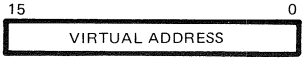
PAGE DESCRIPTOR REGISTER (PDR)



STATUS REGISTER 0 (SR0) 777572



STATUS REGISTER 2 (SR2) 777576



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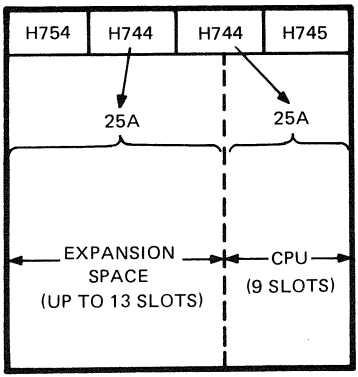
Physical Bank		Physical Address	Relocation Constant
PAGE-0	(4K)	000000–07776	0000
1	(8K)	020000–27776	0200
2	(12K)	040000–47776	0400
3	(16K)	060000–67776	0600
4	(20K)	100000–117776	1000
5	(24K)	120000–137776	1200
6	(28K)	140000–157776	1400
7	(32K)	160000–177776	1600
10	(36K)	200000–217776	2000
11	(40K)	220000–237776	2200
12	(44K)	240000–257776	2400
13	(48K)	260000–277776	2600
14	(52K)	300000–317776	3000
15	(56K)	320000–337776	3200
16	(60K)	340000–357776	3400
17	(64K)	360000–377776	3600
20	(68K)	400000–417776	4000
21	(72K)	420000–437776	4200
22	(76K)	440000–457776	4400
23	(80K)	460000–477776	4600
24	(84K)	500000–517776	5000
25	(88K)	520000–537776	5200
26	(92K)	540000–557776	5400
27	(96K)	560000–577776	5600
30	(100K)	600000–617776	6000
31	(104K)	620000–637776	6200
32	(108K)	640000–657776	6400
33	(112K)	660000–677776	6600
34	(116K)	700000–717776	7000
35	(120K)	720000–737776	7200
36	(124K)	740000–757776	7400
37	(128K)	760000–777776	7600

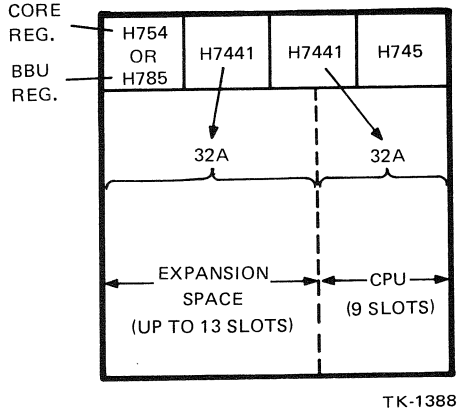
11/34. PS4 - Bin 31166. H777AB
SYSTIME H777 -11- 55089
(SYS 1000/5000 11/34A)

CURRENT DISTRIBUTION
-10-1/2 Inch Box-

BA11-K



10-1/2 INCH BOX FOR PDP-11/34A



TK-1388

NOTE

Any time H7441's are in the system, you must use power distribution board 54-10864-YA-1.

MOUNTING BOX TYPE	CPU BACKPLANE JUMPERS			EXPANDER BACKPLANE JUMPERS		
	+15 B	−15 B	+5 B	+15 B	−15 B	+5 B
BA11-L with BBU	OUT	OUT	OUT	---	---	---
BA11-L without BBU	OUT	OUT	OUT	---	---	---
▲ BA11-K without BBU	IN	IN	IN	IN	IN	IN
■ BA11-KA with BBU	OUT	OUT	OUT	OUT	OUT	OUT
■ BA11-KA without BBU	IN	IN	IN	IN	IN	OUT
■ 11/34's with FP11-AU	IN	IN	IN	IN	IN	OUT

▲ With power distribution board 54-10864.

■ With power distribution board 54-10864-YA-1.

NOTE

For more detailed information on backplane jumper configuration, refer to Section 2 of PDP-11/34A Power System Description Manual (EK-1134A-TM-003).

MODIFIED UNIBUS PIN ASSIGNMENTS

Pin	Signal
AA1	BUS INIT L
AA2	POWER (+5 V)
AB1	BUS INTR L
AB2	TEST POINT
AC1	BUS D00 L
AC2	GROUND
AD1	BUS D02 L
AD2	BUS D01 L
AE1	BUS D04 L
AE2	BUS D03 L
AF1	BUS D06 L
AF2	BUS D05 L
AH1	BUS D08 L
AH2	BUS D07 L
AJ1	BUS D10 L
AJ2	BUS D09 L
AK1	BUS D12 L
AK2	BUS D11 L
AL1	BUS D14 L
AL2	BUS D13 L
AM1	BUS PA L
AM2	BUS D15 L
AN1	P1
AN2	BUS PB L
AP1	P0
AP2	BUS BBSY L
AR1	BAT BACKUP +15 V
AR2	BUS SACK L
AS1	BAT BACKUP –15 V
AS2	BUS NPR L
AT1	GROUND
AT2	BUS BR 7 L
AU1	+20 V
AU2	BUS BR 6 L
AV1	+20 V
AV2	+20 V

MODIFIED UNIBUS PIN ASSIGNMENTS – continued

Pin	Signal
BA1	CACHE HIT L
BA2	POWER (+5 V)
BB1	SPARE
BB2	TEST POINT
BC1	BUS BR 5 L
BC2	GROUND
BD1	BAT BACKUP +5 V
BD2	BR 4 L
BE1	INT SSYN
BE2	PAR DET
BF1	BUS ACLO L
BF2	BUS DCLO L
BH1	BUS A01 L
BH2	BUS A00 L
BJ1	BUS A03 L
BJ2	BUS A02 L
BK1	BUS A05 L
BK2	BUS A04 L
BL1	BUS A07 L
BL2	BUS A06 L
BM1	BUS A09 L
BM2	BUS A08 L
BN1	BUS A11 L
BN2	BUS A10 L
BP1	BUS A13 L
BP2	BUS A12 L
BR1	BUS A15 L
BR2	BUS A14 L
BS1	BUS A17 L
BS2	BUS A16 L
BT1	GROUND
BT2	BUS C1 L
BU1	BUS SSYN L
BU2	BUS CO 1
BV1	BUS MSYN L
BV2	–5 V

NOTES

NOTES

Typical System Component	Current Required at +5 Vdc
KD11-EA (M8266 and M8265)	11.5 A
KD11-E (M7266 and M7265)	10.5 A
KD11-D (M7263)	5 A
KY11-LB (M7859)	3 A
DL11-W (M7856)	2 A
FP11-A (M8267)	7 A
KK11-A (M8268)	4 A
MM11-C/CP (G651)	3 A
MM11-D/DP (G652)	4 A
MM11-YP (G657)	5 A
MS11-E–J (M7847)	2 A
MS11-L (M7891)	1.5 A
Parity Controller (M7850)	1 A
No-Sack Timeout (M8264)	1 A
Terminators (M9312)	1.5 A
(M9301)	2 A
(M9302)	1.3 A
*	

*Intentionally left blank, for users own use.