digital PDP-11/44

Maintenance Card

CONTENTS

EK-PDP44-MC-001

Printed in U.S.A.

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CONSOLE COMMANDS

CONSOLE MODE

Entered by:

1. CPU halting.
2. User typing the console break character (CTRL-P).

Exited by:

1. Continue command.
2. Start command.
3. Boot command.

PROGRAM I/O MODE

Entered by:

1. Continue command.
2. Start command.
3. Boot command.

Exited by:

1. CPU halting.
2. CTRL-P.

CONSOLE COMMAND SYNTAX EXPRESSIONS

<SP>	One space
<COUNT>	Numeric count in octal
<ADDRESS>	Address argument in octal
<DATA>	Data argument in octal
<QUALIFIER>	Command modifier
<INPUT-PROMPT>	Console prompt string (>>>)
<CR>	Carriage return
<LF>	Line feed

CONSOLE COMMANDS – continued

ADDRESS MODIFIERS

+	Increment last address used by two
–	Decrement last address used by two
*	Address last used
@	Last data used becomes address
SW	Hardware switch register

CONTROL CHARACTERS

CTRL-C	Cancels command processing before a terminal session.
CTRL-O	Alternately suppresses and continues display of data at the terminal.
CTRL-P	Initiates console mode.
CTRL-Q	Restarts terminal output that was suspended by CTRL-S.
CTRL-S	Suspends terminal output until CTRL-Q is pressed.
CTRL-U	Cancels current line and discards it.

QUALIFIERS

/G	Specifies general register space.
/N	Permits multiple examines or deposits for one command.
/M	Specifies a machine-dependent register. The address of each machine-dependent register is:

CONSOLE COMMANDS – continued

Address	Register
0 (Read only)	Floating-point data
1 (Read only)	CIS Micro PC (CPC)
2 (Read only)	CIS data
3 (Read only)	CPU data
4 (Read/Write)	CPU Micro PC (MPC)
5 (Read only)	Cache data
6 (Read only)	CPU error register
7 (Read only)	MFM data
10 (Read only)	UNIBUS data
11 (Read only)	Signal register

/TB Take bus, maintenance feature if bus is hung.

/CB Cache bypass, do not read cache.

/E Specifies test-extensive, used with (T) command.

/A Specifies test-extensive-apt, used with (T) command.

CONSOLE COMMANDS

Adder A<CR>

Boot B[<SP><DEVICE-IDENTIFIER>]<CR>

Continue C<CR>

Deposit D[<QUALIFIER-LIST>]
<SP><ADDRESS><SP>
<DATA><CR>

Examine E[[<QUALIFIER-LIST>]
<SP><ADDRESS>]<CR>

Fill F[<SP><COUNT>]<CR>

CONSOLE COMMANDS – continued

Halt H<CR>

Initialize I<CR>

Microstep M[<SP><COUNT>]<CR>

Repeat R<SP>(COMMAND)<CR>

Single-Instruction Step N[<SP><COUNT>]<CR>

Start S[<SP><DATA>]<CR>

Self-Test T[<QUALIFIER>]<CR>

CONSOLE ERRORS

?01 SYN	Illegal command.
?11 IPR ERR	Illegal internal processor register. Applies to the use of the /M qualifier.
?15 HLT CPU	Command illegal while CPU is running.
?20 TRAN ERR	Console tried to examine or deposit but failed due to memory timeout or parity error.
?20 MPC=15	An examine was attempted while the CPU was halted and at micro PC 015.
?21 HLT ERR	Console tried to halt the processor, but failed.
?22 HUNG	Console initiated a CPU transfer, but it was never started.

CONSOLE COMMANDS – continued

?30	Checksum error was found while executing a binary load/unload command.
?81	Checksum error was found in PROM 1 of console control store (while running self-test).
?82	Checksum error was found in PROM 2 of console control store (while running self-test).
?85	Error in read/write test for console RAM.
?A7	Halt/continue test of T/E failed.
?A8	PAX data bus test of T/E failed.
?A9	PAX address test of T/E failed.
?AA	Switch register test of T/E failed.

MODULE UTILIZATION

KD11–Z PROCESSOR BACK PLANE

	A	B	C	D	E	F
1	CIM ▲	M7090	CIS	M7091		
2			CIS	M7092		
3			FP	M7093		
4			DATA PATHS	M7094		
5			CONTROL	M7095		
6			MFM	M7096		
7			CACHE	M7097		
8			UBI	M7098		
9			MS11–M	M8722		
10			MS11–M	M8722		
11			MS11–M	M8722		
12			MS11–M	M8722		
13			SPC* ■			
14	M9302 OR UNIBUS CABLE		SPC* ■			

* MUST CONTAIN MODULE OR BG CARD

■ REMOVE JUMPER CA1–CB1 TO USE NPR DEVICE

▲ CAUTION: DO NOT PLACE A MULTI–LAYER EXTENDER BOARD IN ROWS A & B OF SLOT #1

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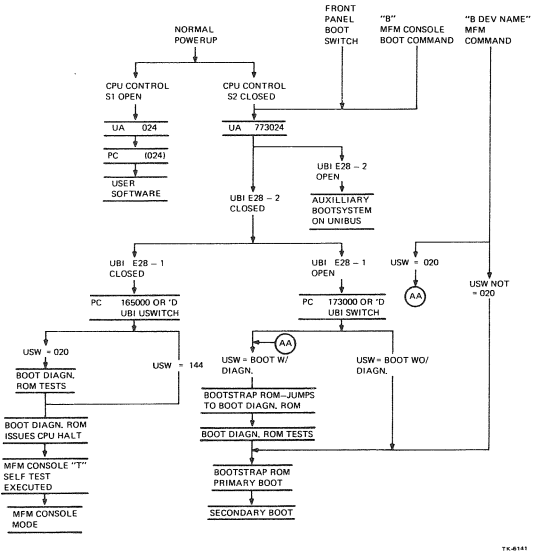
Module Utilization

POWERUP/BOOT FLOW



Powerup/Boot Flow

REGISTER ADDRESSES

PDP-11/44 CPU AND I/O DEVICE REGISTER ADDRESSES

Address	Register
17 777 776	Processor status word (PSW)
17 777 772	Program interrupt request (PIRQ)
17 777 766	CPU error
17 777 707 – 17 777 700	CPU general registers
17 777 676 – 17 777 660	User data PAR, registers 0-7
17 777 656 – 17 777 640	User instruction PAR, registers 0-7
17 777 636 – 17 777 620	User data PDR, registers 0-7
17 777 616 – 17 777 600	User instruction PDR, registers 0-7
17 777 576	MM status register 2 (SR2)
17 777 574	MM status register 1 (SR1)
17 777 572	MM status register 0 (SR0)
17 777 566 – 17 777 560	Console terminal SLU
17 7XX XX6 – 17 7XX XX0	TU58 DECtape SLUs (normally 17 776 500)

REGISTER ADDRESSES – continued

Address	Register
17 777 570	Switch register
17 772 516	MM status register 3 (SR3)
17 772 376 – 17 772 360	Kernel data PAR, registers 0-7
17 772 356 – 17 772 340	Kernel instruction PAR, registers 0-7
17 772 336 – 17 772 320	Kernel data PDR, registers 0-7
17 772 316 – 17 772 300	Kernel instruction PDR, registers 0-7
17 772 276 – 17 772 260	Supervisor data PAR, registers 0-7
17 772 256 – 17 772 240	Supervisor instruction PAR, registers 0-7
17 772 236 – 17 772 220	Supervisor data PDR, registers 0-7
17 772 216 – 17 772 200	Supervisor instruction PDR, registers 0-7
17 770 372 – 17 770 200	Map registers

FRONT PANEL OPERATION

KEYSWITCH POSITIONS

DC Off	Logic and fan power off. AC and DC power still present in power supply.
Local	Normal ON position. Logic and fans have power. Console can be used in either program I/O or console mode.
Local Disable	Locks out console mode. Program I/O is still available. Locks out RD interface if W21 is installed on the M7090.
Standby	Shuts off main +5 V, +15 V, and −15 V power. Memory voltage and fans remain on.

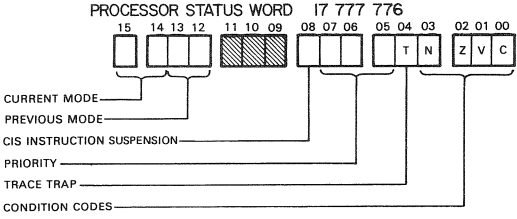
THREE-POSITION TOGGLE SWITCH

Boot	Momentary position.
Continue	Normal operating position.
Halt	Halts CPU.

LIGHT-EMITTING DIODES (LEDs)

Run Light	ON: CPU executing instructions. OFF: CPU halted.
DC On Light	ON: DC power within tolerance. Blinking: DC power out of tolerance.
Battery Light	ON: >90% charged. Slow Blinking: < 90% charged and charging. Fast Blinking: Discharging. OFF: Fully discharged or not present.
Remote Light	ON: CPU under RD control. OFF: CPU not under RD control.

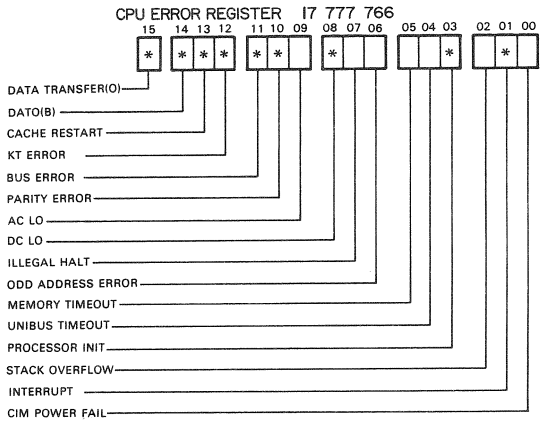
PROCESSOR STATUS WORD REGISTER



* BIT <08> IS SET WHEN A CIS INSTR. IS ENTERED AND CLEARED WHEN THE INSTRUCTION IS COMPLETED. IF SET WHEN AN INTERRUPT OCCURS, IT INDICATES THAT THE CIS INSTRUCTION WAS NOT COMPLETED AND MUST BE CONTINUED UPON RETURN FROM THE INTERRUPT. WHEN SET IT PREVENTS THE SETTING OF THE T-BIT.

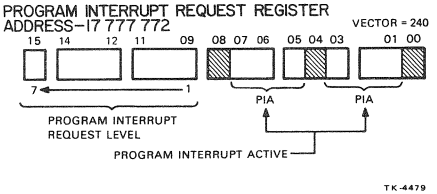
Processor Status Word 17 777 776

CPU ERROR REGISTER



CPU Error Register 17 777 776

PIRQ REGISTER



Program Interrupt Request Register

PDP-11/44 MAINDEC DIAGNOSTICS

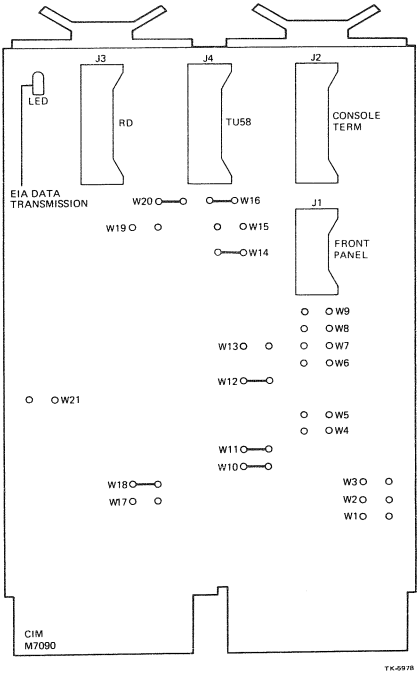
PDP-11/44 MAINDEC DIAGNOSTICS

NOTE
Items should be executed in the order they are listed.

1.	KKFA??	11/44 Diagnostic ROM*
2.	KKAA??	11/44 CPU/EIS
3.	KKAB??	11/44 Traps
4.	KKTA??	11/44 Memory Management, Part A
5.	KKTB??	11/44 Memory Management, Part B
6.	ZM9B??	M9312/11/44 UBI Boot
7.	KKUA??	11/44 UBI MAP
8.	KKKA??	11/44 KK11-B Cache
9.	ZMSD??	MS11/M/L Memory
10.	ZDLD??	DL11-W/11/44 MFM SLU
11.	KKAC??	11/44 Power Fail
12.	KFPA??	FP11-F, Part A
13.	KFPB??	FP11-F, Part B
14.	KFPC??	FP11-F, Part C
15.	ZKEE??	PDP-11 CIS Instruction Exerciser
16.	ZKUA??	UNIBUS Systems Exerciser
17.	ZKUB??	UNIBUS Exerciser Module

* Diagnostic ROM is on the M7098 module.

CIM (M7090)



CIM Jumper Lead Locations, Connectors, and LED Indicator

CIM CONFIGURATION

20 mA Configuration

Mode	Jumper Leads				
Transmitter	**W4**	**W5**	**W6**	**W7**	**W13**
Active	OUT	IN	IN	OUT	IN
Passive	IN	OUT	OUT	IN	OUT
EIA Device	OUT	OUT	OUT	OUT	OUT

CIM (M7090) – continued

Mode	Jumper Leads						
Receiver	**W1**	**W2**	**W3**	**W8**	**W9**	**W17**	**W18**
Active	IN	OUT	IN	OUT	IN	IN	OUT
Passive	OUT	IN	OUT	IN	OUT	IN	OUT
EIA Device	OUT	OUT	OUT	OUT	OUT	OUT	IN

Jumper W11 should always be installed. Jumpers W12, W15, W16, W19, and W20 may remain installed for 20 mA operation.

EIA Configuration

Mode	Jumper Leads			
	W12	**W15**	**W16**	**W17**
RS-232-C	IN	OUT	IN	OUT
RS-423	OUT	OUT	IN	OUT
RS-422	OUT	OUT	IN	OUT

Mode	Jumper Leads			
	W18	**W19**	**W20**	**W1-9 W13**
RS-232-C	IN	OUT	IN	OUT
RS-423	IN	OUT	IN	OUT
RS-422	IN	IN	OUT	OUT

CIM (M7090) – continued

TU58 Configuration

Mode	Jumper Lead W14
RS-232-C	IN
RS-423	OUT

Connector J4 should have a test connector (74-22428-00) when there is no TU58 for diagnostics. In order to run operating software, this turn-around plug must be removed.

Remote Diagnosis Configuration

W21

IN: RD disabled if in local disable.
OUT: RD enabled if in either local disable or local enable.

Voltage Monitoring

W10

IN: Enables +12 V monitoring.
OUT: Disables +12 V monitoring.

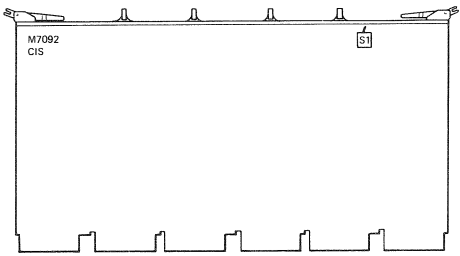
LED Indicator

The LED is lit when EIA data transmission to the console terminal occurs in both directions. The 20 mA operation has no effect on this LED.

CIM

The CIM (M7090) can not be extended on multi-layer extenders. A multi-layer extender can not be inserted into slot 1, rows A and B.

CIS (M7091 and M7092)



M7092 CIS

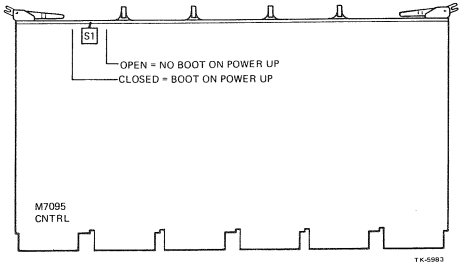
KE44-A (CIS)

1. CIS instructions are clocked in.
2. The CPU addresses MPC 000 in order to process an illegal instruction trap. However, the KE44-A asserts the signal CIS ENAB L. This forces an MPC value of 740 onto the KD11-Z MPC lines.

   NOTE
   KD11-Z microcode addresses 740-776 are utilized for CIS instructions.

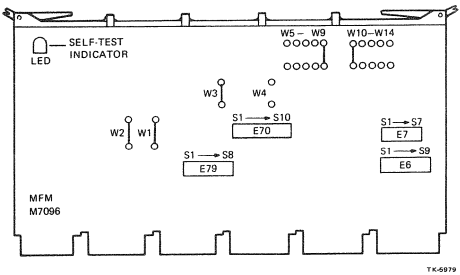
3. During execution of the CIS instruction, the CIS processor controls the next MPC generation for the KD11-Z.
4. Upon completion of the CIS instruction, the KE44-A stops controlling the KD11-Z's next MPC lines. It also drops the signal CIS ENAB L.
5. The KD11-Z attempts to address MPC 000 in order to process the illegal instruction trap. When CIS ENAB L is dropped, it makes the signals serve IR L and serve IR H on K2-2. This forces a no OP (BR2) to be clocked into the IR which removes the trap condition. Instead of processing an illegal instruction trap, the KD11-Z fetches a new instruction.

CONTROL (M7095)



M7095 CPU Control

MFM (M7096)



MFM Jumper Lead Locations, Switches, and LED Indicator

MFM CONSOLE TERMINAL BAUD RATE SELECTION

	Switch Pack E6			
Receiver Switch Locations	**2**	**3**	**4**	**5**
Transmitter Switch Locations	**6**	**7**	**8**	**9**
Baud Rate				
50	ON	ON	ON	ON
75	ON	ON	ON	OFF
110	ON	ON	OFF	ON
134.5	ON	ON	OFF	OFF
150	ON	OFF	ON	ON
200	ON	OFF	ON	OFF
300	ON	OFF	OFF	ON
600	ON	OFF	OFF	OFF
1200	OFF	ON	ON	ON
1800	OFF	ON	ON	OFF
2000	OFF	ON	OFF	ON

MFM (M7096) – continued

	Switch Pack E6			
Receiver Switch Locations	**2**	**3**	**4**	**5**
Transmitter Switch Locations	**6**	**7**	**8**	**9**
Baud Rate				
2400	OFF	ON	OFF	OFF
3600	OFF	OFF	ON	ON
4800	OFF	OFF	ON	OFF
9600	OFF	OFF	OFF	ON
19200	OFF	OFF	OFF	OFF

MFM CONSOLE TERMINAL JUMPERS

W1 — IN: Enable address decode.
OUT: Disable address decode.

W4 — IN: Enable receiver error bits (15:12).
OUT: Disable receiver error bits (15:12).

W5 — IN: Enable terminal break.
OUT: Disable terminal break.

W6 — IN: Enable parity.
OUT: Disable parity.

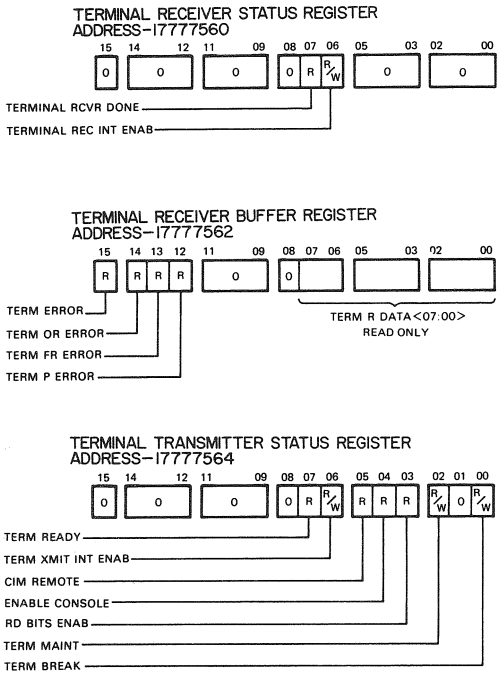
W7 & W8 — Character length for console UART.

Jumper	5 Bits	6 Bits	7 Bits	8 Bits
W7	IN	IN	OUT	OUT
W8	IN	OUT	IN	OUT

MFM (M7096) – continued

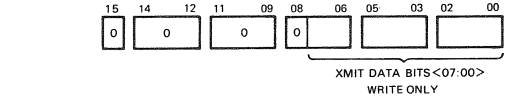
W9 IN: Odd parity.
OUT: Even parity.

S1 (E6) ON: 1 stop bit.
OFF: 2 stop bits.
OFF: 1.5 stop bits if W7 and W8 are in.

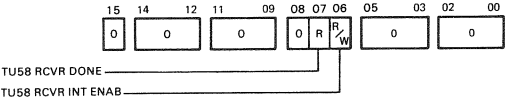


MFM Registers

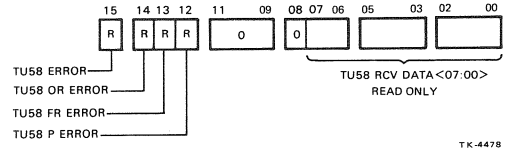
TERMINAL TRANSMITTER BUFFER REGISTER
ADDRESS–17 777 566



TU58 RECEIVER STATUS REGISTER
ADDRESS–17 7XX XX0



TU58 RECEIVER BUFFER REGISTER
ADDRESS–17 7XX XX2



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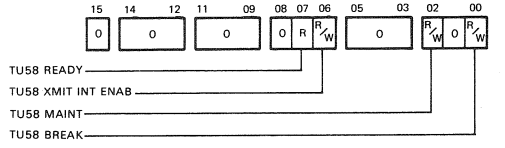
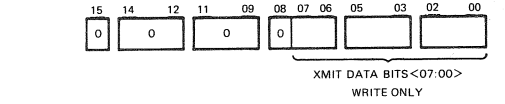
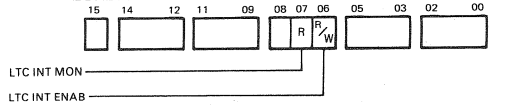
TU58 TRANSMITTER STATUS REGISTER
ADDRESS–17 7XX XX4



TU58 TRANSMITTER BUFFER REGISTER
ADDRESS–17 7XX XX6



LINE CLOCK STATUS REGISTER
ADDRESS–17 777 546



TK-4507

CACHE (M7097)

KK11-B

- 4K words (8K bytes).
- Single set, direct mapped caches with write through features.
- Can be removed without affecting overall KD11-Z operation.
- Switch S1:

  ON: Force miss upper 2K words of cache.

  OFF: Enable upper 2K words of cache.
- Switch S2:

  ON: Force miss lower 2K words of cache.

  OFF: Enable lower 2K words of cache.
- Jumpers W1 and W2:

  W1:IN, W2:OUT – Single port memory and force miss only (cache not affected).

  W1:OUT, W2:IN – Multiport memory and force miss only (cache invalidated).

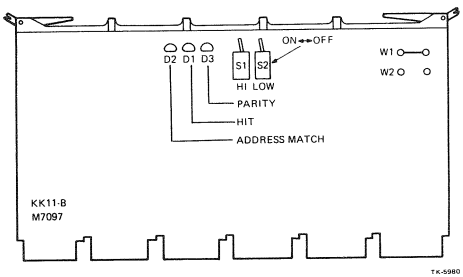
  NOTE
  This is for CPU read hit with bypass.

CACHE (M7097) – continued

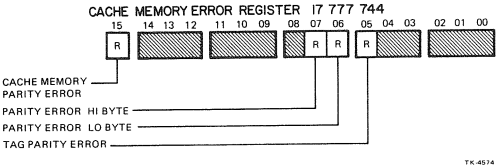
CACHE RESPONSES TO HIT/MISS OPERATIONS

	DMA Hit	DMA Miss	CPU Hit	CPU Miss
Read	Not Affected	Not Affected	Cache Read	Write Data Write Tag Write Valid
Read Bypass	Invalid	Not Affected	Invalid * or Not Affected	Not Affected
Write	Invalid	Not Affected	Write Data	Not Affected
Write Bypass	Invalid	Not Affected	Invalid	Not Affected

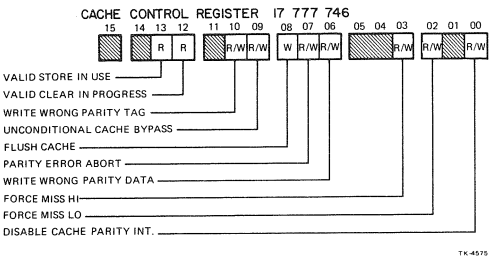
* Depends on jumpers W1 and W2.



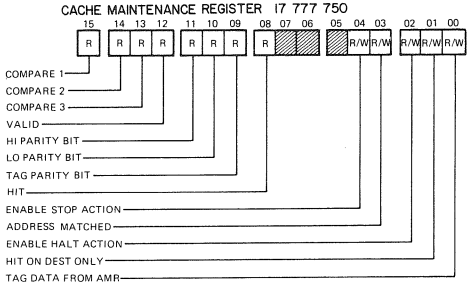
Cache Memory Module, Switches, LED Indicators, and Jumper Lead Locations



Cache Memory Error Register 17 777 744



Cache Control Register 17 777 746



NOTE:

THE CACHE MAINTENANCE REGISTER CAN ALSO BE REFERENCED AS THE ADDRESS MATCH REGISTER. WHEN WRITING TO BITS <15:10> OF THE CACHE MAINTENANCE REGISTER IT CONTAINS BITS <21:16> OF THE ADDRESS MATCH REGISTER.

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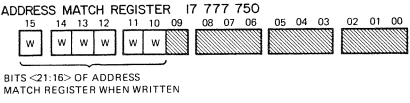
Cache Maintenance Register 17 777 750



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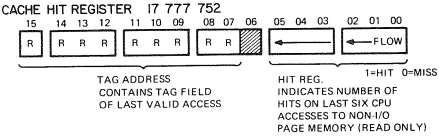
Address Match Register 17 777 750



NOTE:

THE CACHE HIT REGISTER CAN ALSO BE REFERENCED AS THE ADDRESS MATCH REGISTER. WHEN WRITING TO BITS <15:00> OF THE CACHE HIT REGISTER IT CONTAINS BITS <15:00> OF THE ADDRESS MATCH REGISTER.

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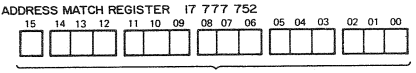
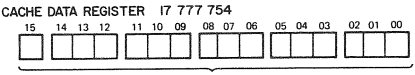
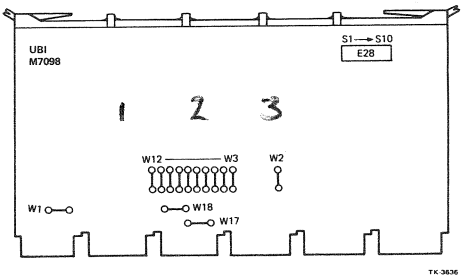
Cache Hit Register 17 777 752



Address Match Register 17 777 752



Cache Data Register 17 777 754



UBI Module, Switch and Jumper Lead Locations

UBI DIAGNOSTIC AND BOOTSTRAP ROMS

Switch Pack E28

- Switch S1:

  ON: 765 XXX device bootstrap program.

  OFF: 775 XXX CPU diagnostic program.

- Switch S2:

  ON: Bootstrap/diagnostic enabled.

  OFF: Bootstrap/diagnostic disabled.

- Switches S3-S10 are bits (08:01) of the starting address (ON = 1, OFF = 0).

- Device ROM identification:

  To identify the device bootstrap ROMS that are installed, initiate the diagnostic program MAINDEC CZM9B?? or examine the following five addresses and compare the response with the bootstrap ROM identifiers listed.

  1. 775774 (CPU diagnostic ROM)
  2. 773000 (Device ROM #1) — RL01
  3. 773200 (Device ROM #2) — RP04, 5, 6

4. 773400 (Device ROM #3) ✓ TS04

5. 773600 (Device ROM #4)

A 177 776 response indicates the continuation of a ROM diagnostic program to an additional ROM.

A XXX 777 response indicates a ROM failure or no ROM present at the addressed location.

- The position of the bootstrap ROM on the module must be sequential, starting with device #1 through device #4.

IC Location	Bootstrap ROM
E 48	Device #1
E 49	Device #2
E 50	Device #3
E 51	Device #4

- W1: IN – Enable parity error abort.
  OUT – Disable parity error abort.

- W2: IN – Enable diagnostic ROM.
  OUT – Disable diagnostic ROM.

- W17,W18 – Always installed.

BOOTSTRAP ROM IDENTIFIERS

Octal ID Number	Device ROM
041524	TA11
042104	TU58
042113	RK03/05/05J
042113	TU55/56
042114	RL01
042115	RK06/07
042120	RP02/03
042120	RP04/05/06

UBI (M7098) – continued

Octal ID Number	Device ROM
042120	RM02/03
042123	RS03/04
042130	RX01
042131	RX02
046515	TU16/45/77/TE16
046523	TS04
046524	TU10, TE10, TS03
050122	PC05
050122	ASR 33
054115 177776 177776	DL11
054115 177776 177776	DMC-11
054125 177776 177776	DU11
054127 177776 177776	DUP-11

PDP-11/44 UBI DIAGNOSTIC ROM

- Tests 1-14 loop ON error.
- Tests 15-16 halt ON error.

Loop/Halt Address	Test Numbers	Description
165070	1	Unconditional branch
165106	2	CIR, Mode 0, BMI, BVS, BHI, BLT, BLOS

UBI (M7098) – continued

Loop/Halt Address	Test Numbers	Description
165122	3	DEC, Mode 0, BBPL, BEQ, BGE, BLE
165134	4	ROR, Mode 0, BUC, BHIS, BNE
165172	5	Register data path
165202	6	ROL, BCC, BLK
165220	7	ADD, INC, COM, BCS, BLE
165240	10	BOR, DEC, BIS, ASS, BLO
165246	11	COM, BLOS
165260	11	BIC, BGT, BLE
165302	12	SWAB, CMP, BIT, BNE, BGT
165312	13	MOVB, BPL
165334	13	SOB, CIR, TST, BNE
165346	14	JSR
165356	14	Push onto stack failed
165366	14	RTS
165400	14	RTI
165406	14	JMP
165526	15	Main memory data error without cache
165550	15	Main memory data error without cache
165634	16	No hit in cache
165652	16	No hit in cache
165664	15 or 16	Parity error
165702	Any Test	Hardware trap to 4 (check stack)

DEVICE ROM PART NUMBERS

Device	ROM Part Number
ASR 33	23-760A9
DL11	23-926A9 23-927A9 23-928A9
DMC-11	23-862A9 23-863A9 23-864A9

UBI (M7098) – continued

Device	ROM Part Number
DU11	23-868A9 23-869A9 23-870A9
DUP-11	23-865A9 23-866A9 23-867A9
PC05	23-760A9
RK03/05	23-756A9
RK06/07	23-752A9
RL01	23-751A9
RP02/03	23-755A9
RP04/05/06	23-755A9
RS03/04	23-759A9
RX01	23-753A9
RX02	23-811A9
TS04	23-764A9
TU10, TE10, TS03	23-758A9
TU16, 45, 77, TE16	23-757A9
TU55, 56	23-756A9
TU58	23-765A9
TU60	23-761A9

UBI (M7098) – continued

DEVICE BOOTSTRAP IDENTIFIERS

CT	TA11
DB	RP04/05/06, RM02/03
DD	TU58
DK	RK03/05/05J
DL	RL01
DM	RK06/07
DP	RP02/03
DS	RS03/04
DT	TU55/56
DX	RX01
DY	RX02
MM	TU16/TE16 (TM02/03)
MT	TU10/TE10/TS03
PR	PC05
TT	ASR 33
XM	DMC-11
XW	DUP-11
XU	DU11
XL	DL11

UNIBUS MAP REGISTERS

Register	UNIBUS Address LO	HI	Mapping Address Page
0	770200,	02	000000 - 017777
1	770204,	06	020000 - 037777
2	770210,	12	040000 - 057777
3	770214,	16	060000 - 077777
4	770220,	22	100000 - 117777
5	770224,	26	120000 - 137777
6	770230,	32	140000 - 157777
7	770234,	36	160000 - 177777
10	770240,	42	200000 - 217777

UBI (M7098) – continued

Register	UNIBUS Address LO	HI	Mapping Address Page
11	770244,	46	220000 - 237777
12	770250,	52	240000 - 257777
13	770254,	56	260000 - 277777
14	770260,	62	300000 - 317777
15	770264,	66	320000 - 337777
16	770270,	72	340000 - 357777
17	770274,	76	360000 - 377777
20	770300,	02	400000 - 417777
21	770304,	06	420000 - 437777
22	770310,	12	440000 - 457777
23	770314,	16	460000 - 477777
24	770320,	22	500000 - 517777
25	770324,	26	520000 - 537777
26	770330,	32	540000 - 557777
27	770334,	36	560000 - 577777
30	770340,	42	600000 - 617777
31	770344,	46	620000 - 637777
32	770350,	52	640000 - 657777
33	770354,	56	660000 - 677777
34	770360,	62	700000 - 717777
35	770364,	66	720000 - 737777
36	770370,	72	740000 - 757777
* 37	770374,	76	

* Register 37 is not used for relocation as the corresponding mapping address is the I/O page.

UNIBUS ADDRESS SPACE JUMPERS, UPPER LIMIT

Defines the last address which will not pass to main memory.

UNIBUS ADDRESS SPACE JUMPERS, LOWER LIMIT

Defines the first address which will not pass to main memory.

UNIBUS Address Space Jumpers, Upper Limit

Last UNIBUS Address	Decimal Kw	Octal Bank	W7	W6	W5	W4	W3
0	0	0	IN	IN	IN	IN	IN
17777	4	1	OUT	IN	IN	IN	IN
37777	8	2	IN	OUT	IN	IN	IN
57777	12	3	OUT	OUT	IN	IN	IN
77777	16	4	IN	IN	OUT	IN	IN
117777	20	5	OUT	IN	OUT	IN	IN
137777	24	6	IN	OUT	OUT	IN	IN
157777	28	7	OUT	OUT	OUT	IN	IN
177777	32	10	IN	IN	IN	OUT	IN
217777	36	11	OUT	IN	IN	OUT	IN
237777	40	12	IN	OUT	IN	OUT	IN
257777	44	13	OUT	OUT	IN	OUT	IN
277777	48	14	IN	IN	OUT	OUT	IN
317777	52	15	OUT	IN	OUT	OUT	IN
337777	56	16	IN	OUT	OUT	OUT	IN

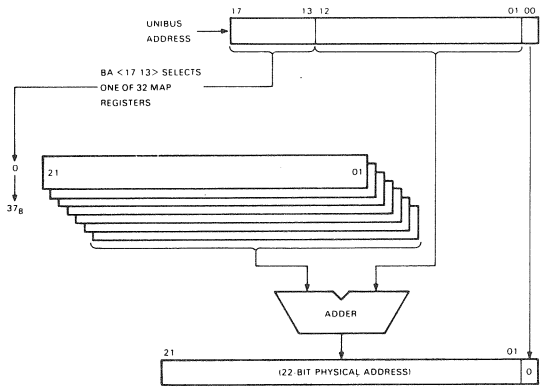
Last UNIBUS Address	Decimal Kw	Octal Bank	W7	W6	W5	W4	W3
357777	60	17	OUT	OUT	OUT	OUT	IN
377777	64	20	IN	IN	IN	IN	OUT
417777	68	21	OUT	IN	IN	IN	OUT
437777	72	22	IN	OUT	IN	IN	OUT
457777	76	23	OUT	OUT	IN	IN	OUT
477777	80	24	IN	IN	OUT	IN	OUT
517777	84	25	OUT	IN	OUT	IN	OUT
537777	88	26	IN	OUT	OUT	IN	OUT
557777	92	27	OUT	OUT	OUT	IN	OUT
577777	96	30	IN	IN	IN	OUT	OUT
617777	100	31	OUT	IN	IN	OUT	OUT
637777	104	32	IN	OUT	IN	OUT	OUT
657777	108	33	OUT	OUT	IN	OUT	OUT
677777	112	34	IN	IN	OUT	OUT	OUT
717777	116	35	OUT	IN	OUT	OUT	OUT
737777	120	36	IN	OUT	OUT	OUT	OUT
757777	124	37	OUT	OUT	OUT	OUT	OUT

UNIBUS Address Space Jumpers, Lower Limit

First UNIBUS Address	Decimal Kw	Octal Bank	W12	W11	W10	W9	W8
0	0	0	IN	IN	IN	IN	IN
20000	4	1	OUT	IN	IN	IN	IN
40000	8	2	IN	OUT	IN	IN	IN
60000	12	3	OUT	OUT	IN	IN	IN
100000	16	4	IN	IN	OUT	IN	IN
120000	20	5	OUT	IN	OUT	IN	IN
140000	24	6	IN	OUT	OUT	IN	IN
160000	28	7	OUT	OUT	OUT	IN	IN
200000	32	10	IN	IN	IN	OUT	IN
220000	36	11	OUT	IN	IN	OUT	IN
240000	40	12	IN	OUT	IN	OUT	IN
260000	44	13	OUT	OUT	IN	OUT	IN
300000	48	14	IN	IN	OUT	OUT	IN
320000	52	15	OUT	IN	OUT	OUT	IN
340000	56	16	IN	OUT	OUT	OUT	IN

First UNIBUS Address	Decimal Kw	Octal Bank	W12	W11	W10	W9	W8
360000	60	17	OUT	OUT	OUT	OUT	IN
400000	64	20	IN	IN	IN	IN	OUT
420000	68	21	OUT	IN	IN	IN	OUT
440000	72	22	IN	OUT	IN	IN	OUT
460000	76	23	OUT	OUT	IN	IN	OUT
500000	80	24	IN	IN	OUT	IN	OUT
520000	84	25	OUT	IN	OUT	IN	OUT
540000	88	26	IN	OUT	OUT	IN	OUT
560000	92	27	OUT	OUT	OUT	IN	OUT
600000	96	30	IN	IN	IN	OUT	OUT
620000	100	31	OUT	IN	IN	OUT	OUT
640000	104	32	IN	OUT	IN	OUT	OUT
660000	108	33	OUT	OUT	IN	OUT	OUT
700000	112	34	IN	IN	OUT	OUT	OUT
720000	116	35	OUT	IN	OUT	OUT	OUT
740000	120	36	IN	OUT	OUT	OUT	OUT
760000	124	37	OUT	OUT	OUT	OUT	OUT

UBI (M7098) – continued



Constructing a Physical Address from a UNIBUS Address

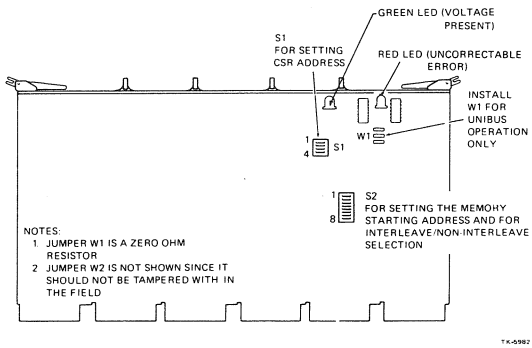
MS11-M MEMORY

- MS11-M can accommodate battery backup (H7750). The module is partitioned for +5 V, +12 V, and −12 V battery backup voltages.

  WARNING:
  The green LED indicates +5 V BBU is present, in which case the module should not be removed until such voltages are powered off.

- The red LED on the module indicates that an uncorrectable error has occurred.
- When the MS11-M is used with a PDP-11/44, the memory should be inserted into one of the designated extended UNIBUS slots 9-12 in the processor's backplane. Jumper W1 must be out.
- Power voltage checks:

Voltage	Tolerance	Backplane
+5 V Maximum ripple = .2 VP–P	(.25 V)	AA2, BA2, CA2
+5 V BBU Maximum ripple = .2 VP–P	(.25 V)	BD1
+12 V Maximum ripple = 1.0 VP–P	(.60 V)	AR1
−12 V Maximum ripple = 1.0 VP–P	(1.2 V)	AS1



Switch and Jumper Locations

STARTING ADDRESS CONFIGURATION

Decimal	Octal	SW2-5 (A21)	SW2-4 (A20)	SW2-3 (A19)	SW2-2 (A18)	SW2-1 (A17)
0K	00000000	ON	ON	ON	ON	ON
64K	00400000	ON	ON	ON	ON	OFF
128K	01000000	ON	ON	ON	OFF	ON
192K	01400000	ON	ON	ON	OFF	OFF
256K	02000000	ON	ON	OFF	ON	ON
320K	02400000	ON	ON	OFF	ON	OFF
384K	03000000	ON	ON	OFF	OFF	ON
448K	03400000	ON	ON	OFF	OFF	OFF
512K	04000000	ON	OFF	ON	ON	ON
576K	04400000	ON	OFF	ON	ON	OFF
640K	05000000	ON	OFF	ON	OFF	ON
704K	05400000	ON	OFF	ON	OFF	OFF
768K	06000000	ON	OFF	OFF	ON	ON
832K	06400000	ON	OFF	OFF	ON	OFF
896K	07000000	ON	OFF	OFF	OFF	ON
960K	07400000	ON	OFF	OFF	OFF	OFF

Decimal	Octal	SW2-5 (A21)	SW2-4 (A20)	SW2-3 (A19)	SW2-2 (A18)	SW2-1 (A17)
1024K	10000000	OFF	ON	ON	ON	ON
1088K	10400000	OFF	ON	ON	ON	OFF
1152K	11000000	OFF	ON	ON	OFF	ON
1216K	11400000	OFF	ON	ON	OFF	OFF
1280K	12000000	OFF	ON	OFF	ON	ON
1344K	12400000	OFF	ON	OFF	ON	OFF
1408K	13000000	OFF	ON	OFF	OFF	ON
1472K	13400000	OFF	ON	OFF	OFF	OFF
1536K	14000000	OFF	OFF	ON	ON	ON
1600K	14400000	OFF	OFF	ON	ON	OFF
1664K	15000000	OFF	OFF	ON	OFF	ON
1728K	15400000	OFF	OFF	ON	OFF	OFF
1792K	16000000	OFF	OFF	OFF	ON	ON
1856K	16400000	OFF	OFF	OFF	ON	OFF

Decimal	Octal	SW2-5 (A21)	SW2-4 (A20)	SW2-3 (A19)	SW2-2 (A18)	SW2-1 (A17)
1920K	17000000	OFF	OFF	OFF	OFF	ON
1984K	17400000	OFF	OFF	OFF	OFF	OFF

OFF = 1, ON = 0

UNIBUS or extended UNIBUS operation of the MS11-M is selected by W1.

W1	OUT	= Extended UNIBUS
W1	IN	= Modified UNIBUS

INTERLEAVE CONFIGURATIONS

Mode	SW2-6	SW2-7	SW2-7
Non-interleaved	OFF	OFF	OFF
1st Interleaved MEM/EVEN	ON	ON	OFF
2nd Interleaved MEM/ODD	ON	OFF	ON

NOTE

The five remaining switch configurations should never be used.

PARITY CST ADDRESS CONFIGURATIONS

UNIBUS Address	Extended UNIBUS Address	SW1-1 (A04)	SW1-2 (A03)	SW1-3 (A02)	SW1-4 (A01)
772100	17772100	ON	ON	ON	ON
772102	17772102	ON	ON	ON	OFF
772104	17772104	ON	ON	OFF	ON
772106	17772106	ON	ON	OFF	OFF
772110	17772110	ON	OFF	ON	ON

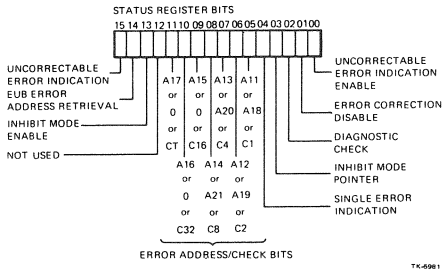
UNIBUS Address	Extended UNIBUS Address	SW1-1 (A04)	SW1-2 (A03)	SW1-3 (A02)	SW1-4 (A01)
772112	17772112	ON	OFF	ON	OFF
772114	17772114	ON	OFF	OFF	ON
772116	17772116	ON	OFF	OFF	OFF
772120	17772120	OFF	ON	ON	ON
772122	17772122	OFF	ON	ON	OFF
772124	17772124	OFF	ON	OFF	ON
772126	17772126	OFF	ON	OFF	OFF
772130	17772130	OFF	OFF	ON	ON
772132	17772132	OFF	OFF	ON	OFF
772134	17772134	OFF	OFF	OFF	ON
772136	17772136	OFF	OFF	OFF	OFF

OFF = 1, ON = 0

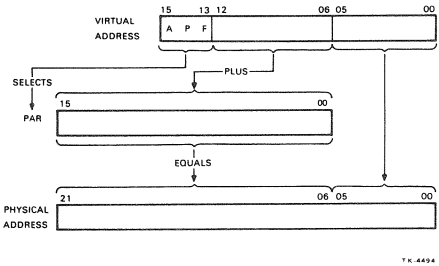
MEMORY MANAGEMENT

MEMORY MANAGEMENT RELOCATION CONSTANTS

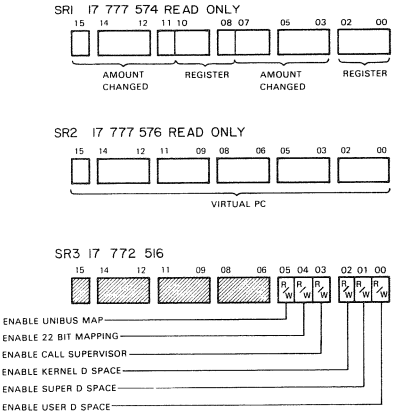
Physical Bank	Physical Address	Relocation Constant
0 (4K)	000000 - 017776	0000
1 (8K)	020000 - 037776	0200
2 (12K)	040000 - 057776	0400
3 (16K)	060000 - 077776	0600
4 (20K)	100000 - 117776	1000
5 (24K)	120000 - 137776	1200
6 (28K)	140000 - 157776	1400
7 (32K)	160000 - 177776	1600
10 (36K)	200000 - 217776	2000
11 (40K)	220000 - 237776	2200
12 (44K)	240000 - 257776	2400
13 (48K)	260000 - 277776	2600
14 (52K)	300000 - 317776	3000
15 (56K)	320000 - 337776	3200
16 (60K)	340000 - 357776	3400
17 (64K)	360000 - 377776	3600
20 (68K)	400000 - 417776	4000
21 (72K)	420000 - 437776	4200
22 (76K)	440000 - 457776	4400
23 (80K)	460000 - 477776	4600
24 (84K)	500000 - 517776	5000
25 (88K)	520000 - 537776	5200
26 (92K)	540000 - 557776	5400
27 (96K)	560000 - 577776	5600
30 (100K)	600000 - 617776	6000
31 (104K)	620000 - 637776	6200
32 (108K)	640000 - 657776	6400
33 (112K)	660000 - 677776	6600
34 (116K)	700000 - 717776	7000
35 (120K)	720000 - 737776	7200
36 (124K)	740000 - 757776	7400
37 (128K)	760000 - 777776	7600



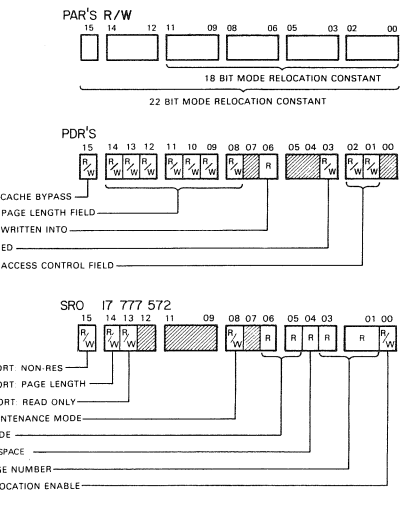
Control and Status Register



Physical Address Generation, 22-Bit Mapping



Memory Management Registers



Memory Management Registers

MEMORY MANAGEMENT – continued

TU58 JUMPER CONFIGURATIONS

W3 IN: Enable receiver error bits (15:12).
OUT: Disable receiver error bits (15:12).

W10 IN: Enable break bit.
OUT: Disable break bit.

W11 IN: Enable parity.
OUT: Disable parity.

W12 & W13 Character length for TU58 UART.

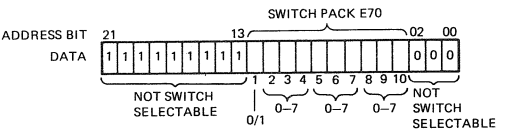
Jumper	5 Bits	6 Bits	7 Bits	8 Bits
W12:	IN	IN	OUT	OUT
W13:	IN	OUT	IN	OUT

W14 IN: Odd parity.
OUT: Even parity.

TU58 BAUD RATE SELECTION

	Switch Pack E7		
Receiver Switch	**1**	**2**	**3**
Transmitter Switch	**4**	**5**	**6**
Baud Rate			
38,400	ON	OFF	OFF
9600	OFF	ON	OFF
Console RCLK	OFF	OFF	ON

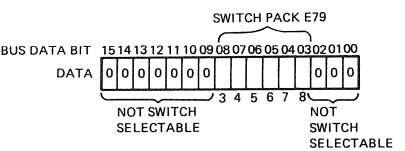
Switch S7 is not used



SWITCH ON= LOGICAL 1, OFF= LOGICAL 0

TK-3637

TU58 Device Address Selection Switch Pack E70



SWITCH ON = LOGICAL 1, OFF = LOGICAL 0

NOTE: DATA BIT # 2 IS 0 FOR RECEIVER VECTOR AND 1 for TRANSMITTER VECTOR

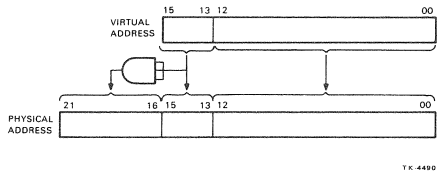
TK-3638

TU58 Vector Address Selection Switch Pack E79

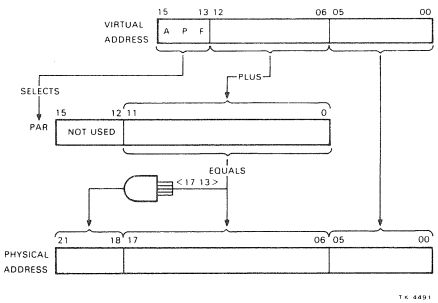
LINE TIME CLOCK

W2 IN: Enabled
OUT: Disabled

MEMORY MANAGEMENT – continued



Physical Address Generation, 16-Bit Mapping



Physical Address Generation, 18-Bit Mapping

POWER SUPPLY

H7140 POWER SUPPLY

1. The dc LED on the front panel must be lit. If the dc LED is blinking check the following:

   a. All dc voltages. Replace H7140.

   b. Battery backup jumpers on DD11-CK or DD11-DK backplanes. The jumpers should be out. No voltages on the backplane should be jumpered together. The jumpers are usually #20 insulated bus wire.

   c. D25 on the M7090 module is in backwards. Replace the M7090.

2. H7140 provides the following voltages:

   +5.1 Vdc at 120 amperes

   +15.0 Vdc at 3 amperes

   -15.0 Vdc at 3 amperes

   +12.0 Vdc at 5 amperes

   -12.0 Vdc at 1 ampere

   +5.0 Vdc at 10 amperes

3. Battery backup option (if applicable)

   The BAT LED on the front panel indicates battery backup status. If the "BAT" LED is:

   a. Continuously ON – battery backup is present and greater than 90% charged.

   b. OFF – no battery backup is present or it is fully discharged.

   c. Pulsing at a slow rate (1 Hz) – battery backup is present and less than 90% charged.

   d. Pulsing at a fast rate (10 Hz) – battery backup is present and being discharged.

POWER SUPPLY – continued

CPU MODULE CURRENT REQUIREMENTS

Option (Modules)	DC Current			
	+5.1 V	+12 V	-12 V	+5.1 BB
KD11-Z				
M7090	0.5 A			
M7094	7.5 A			
M7095	7.5 A			
M7096	5.0 A			
M7098	7.0 A			
KK11-B				
M7097	6.5 A			
FP11-F				
M7093	7.0 A			
KE11-A				
M7091	3.1 A			
M7092	6.0 A			
MS11-MB				
M8722-BA	4.8 A	1.0 A	50 mA	1.5 A
M9302	1.5 A			

NOTES

Digital Equipment Corporation • Bedford, MA 01730