EK-KMS1P-TM-002

KMS11-P Synchronous Communication Processor Technical Manual

Prepared by Educational Services
of
Digital Equipment Corporation

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PREFACE

This manual describes in detail the installation requirements, programming considerations and servicing procedures, including diagnostic support, for the KMS11-P Synchronous Controller. A series of appendices is also provided.

Other documents which support the KMS11-P Synchronous Controler are:

- KMS11 Synchronous Communications Processor Pocket Service Guide (EK-KMS11-PS)-001)
- M8206 Microprocessor option description (YM-C093C-00)
- M8203 Line Unit Technical Manual (EK-M8203-TM-001)
- KMS11-P Print Set (MP 01175)
- Electronic Industries Association (EIA) Specifications

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This chapter presents a short introduction to KMS11-P operation. The term KMS11-P, as used in this manual, means the communication series which has a microprocessor module and a line unit module.

1.2 GENERAL DESCRIPTION

The KMS11-P is designed to be used in a network link for a high performance connection between a VAX-11 or a PDP-11 computer. It is a microprocessor based intelligent programmable synchronous communications controller.

Features of the KMS11-P:

1. Error reporting
2. Modem control
3. Diagnostic tests
4. Support for local or remote, full-duplex or half-duplex configurations
5. 18-bit non-processor request (NPR), direct memory access (DMA) transfers

The KMS11-P basic unit (KMS1P-M) is made up of a M8206 microprocessor (also named KMC11-B) and a M8203 line unit. The microprocessor operates as a parallel data interface between the central processor (VAX-11 or PDP-11) and the M8203 line unit. This line unit/microprocessor combination permits remote computer applications. (For remote operations, computers are connected through external modems that use common carrier facilities.) See Figure 1-1 for typical applications.

When associated with different types of cabinet kits (CK-KMS1P-XX) the KMS1P-M can operate within a range of speeds from 2.4 Kbits per second to 56 Kbits per second (see table 1-1 and refer to Appendix F-2 for a complete description of the different types of cabinet kits).

The KMS11-P system is made up of a basic subsystem and three options which allow it to have standard and special interface configurations. With these options, KMS11-P systems can operate within a range of speeds from 2.4K bits/s to 56K bits/s (see Table 1-1).

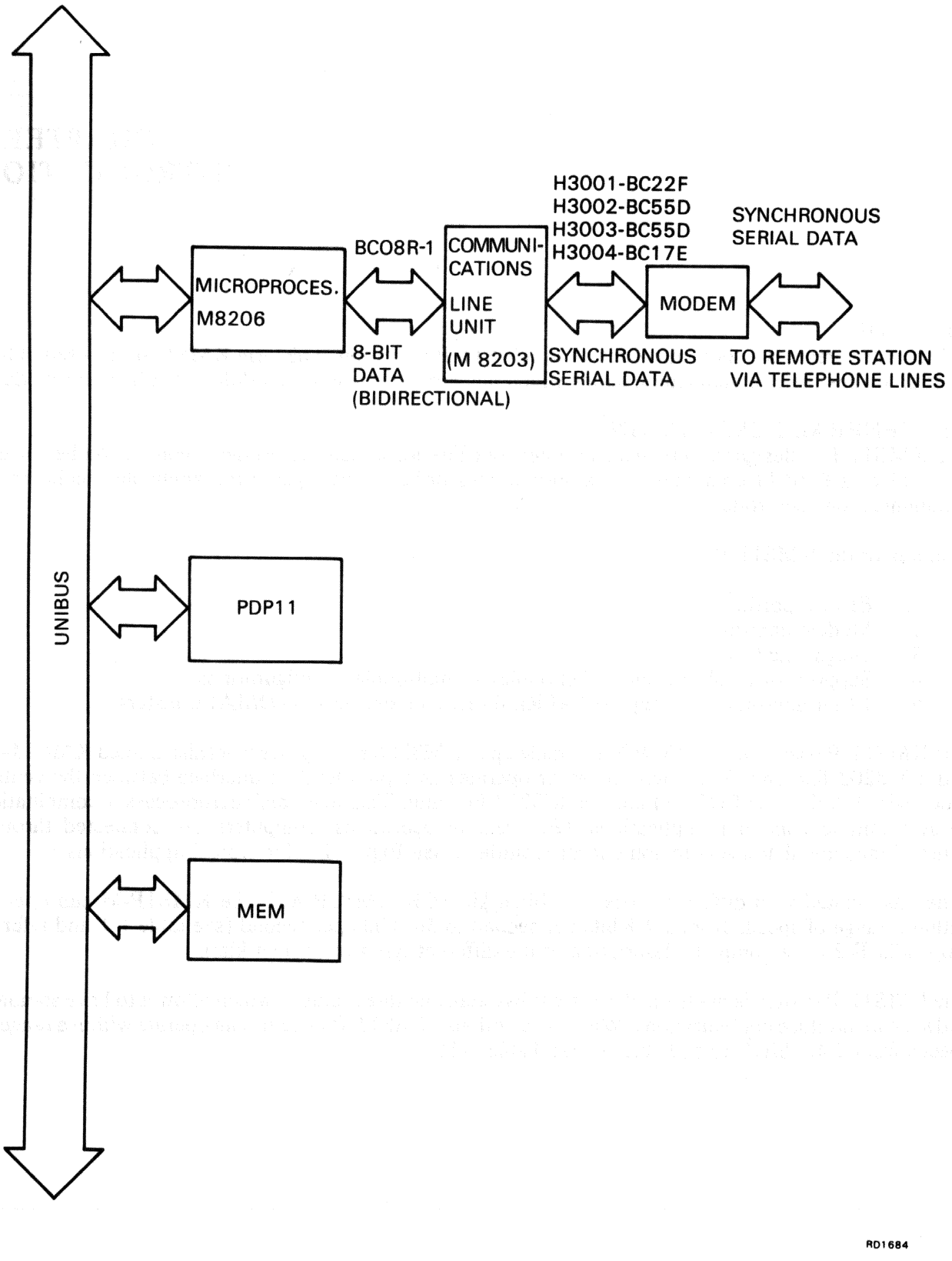

Figure 1-1 Typical Applications

Table 1-1 KMS11-P Options

Option	Description	Line Speed
KMS1P-M	Basic Unit	
CK-KMS1P-Ax CK-KMS1P-Fx	EIA RS-232-C* EIA RS-423-A CCITT V.10	Up to 19.2K bits/s Up to 56K bits/s**
CK-KMS1P-Bx	ISO 2593/CCITT V.35***	Up to 56K bits/s
CK-KMS1P-Ex	EIA RS-422-A/CCITT V.11	Up to 56K bits/s

* EIA – Electronic Industries Association

** Limited to 20K bits/s by RS-449 and 9600 bits/s by ISO 4902

*** ISO International Standards Organization CCITT (Comite Consultatif International de Telegraphie et Telephone)

x Cabinet Family Dependent (Refers to Appendix F)

1.3 KMS11-P SYSTEM OPERATION

Operation of the KMS11-P is started and controlled by a user program residing in the memory of the central processor (CPU). A user program is made up of an application program and a device driver routine that interfaces with the KMS11-P. Communication between the user program and the KMS11-P is done by four 16-bit Control and Status Registers (CSRs) integrated in the microprocessor. These CSRs are used for:

1. Loading the microprocessor firmware
2. Initializing
3. Selecting the mode of operation
4. Assigning receive or transmit buffers to the KMS11-P
5. Getting receive and transmit buffer returns from the KMS11-P
6. Error reporting.

1.4 GENERAL SPECIFICATIONS

The following paragraphs contain performance, electrical and environmental specifications for all KMS11-P configurations.

1.4.1 Power Requirements

The M8206 and M8203 line unit power requirements are listed below:

Module	Voltage Rating (Approximate Values)
M8206 M8203	+ 5 volts at 7.5 amperes + 5 volts at 3.0 amperes + 15 volts at 0.15 amperes – 15 volts at 0.2 amperes

1.4.2 Environmental Requirements

The KMS11-P is designed to operate in a class B environment as described in DEC Standard 102.B.

1. Operating temperature range 10 degrees C to 40 degrees C (50 degrees F to 104 degrees F)

2. Relative humidity 10 to 90 percent with a maximum wet bulb of 28 degrees C (82 degrees F) and a minimum dewpoint of 2 degrees C (36 degrees F)

1.5 EIA STANDARDS OVERVIEW (RS-449 VS RS-232-C)

The most common interface standard used in the past few years has been the RS-232-C. It does, however, have serious limitations for use in modern data communications systems; the most important being speed and distance. For this reason, the RS-449 has been developed to replace the RS-232-C. It maintains a degree of compatibility with RS-232-C to allow an upward change to RS-449.

The most significant difference between RS-449 and RS-232-C is the electrical characteristics of signals used between the data communication equipment (DCE) and the data terminal equipment (DTE). The RS-232-C standard uses only unbalanced circuits while the RS-449 uses both balanced and unbalanced electrical circuits.

The specifications for these different types of electrical circuits supported by RS-449 are contained in EIA Standard RS-422-A for balanced circuits and RS-423-A for unbalanced circuits. These new standards permit much faster transmission speeds and will allow larger distances between the DTE and DCE. The maximum transmission speeds supported by RS-422-A and RS-423-A circuits vary with circuit length; the normal speed limits being 20K bits/s for RS-423-A at 61 meters (200 ft) and 2M bits/s for RS-422-A at 61 meters (200 ft). These speeds or distances can be exceeded in special applications by using lower speeds for long distances, and the reverse.

Another major difference between RS-232-C and RS-449 is that two new connectors have been specified, to allow for the additional pins needed to support new circuit functions and the balanced interface circuits. One connector is a 37-pin cinch used to accept most data communications applications. The other is a nine-pin cinch used in applications needing secondary channel functions. These are typically some of the new circuits that have been added in RS-449, to support local and remote loopback testing and standby channel selection.

The change from RS-232-C to RS-449 will take some time. Therefore, any applications that are interconnected between RS-232-C and RS-449 must follow the limitations of RS-232-C, which has a normal speed of 20K bits/s at a maximum distance of 15 meters (50 ft).

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter provides all the necessary information for installing and testing the KMS11-P microprocessor subsystem. A checklist, which can be used to verify the installation process, is also included.

2.2 UNPACKING AND EXAMINATION

The KMS11-P is packed according to commercial practices. When unpacking, remove all packing material and check the equipment against the shipping list (Table 2-1 contains a list of the items provided for each configuration). Examine all parts and carefully examine the module for obvious damage. Report damages or shortage to the shipper and inform the local DIGITAL office.

2.3 INSTALLATION CONSIDERATIONS

Installation of the KMS11-P microprocessor/line unit subsystem should be done in four phases:

Phase 1 – Preinstallation Considerations

Verify system requirements, system position, and configuration requirements.

Phase 2 – Microprocessor Installation

Configure, install and verify microprocessor module via the appropriate diagnostics.

Phase 3 – Line Unit Installation

Configure the line unit module for the customer application and install the cable, and verify it via appropriate diagnostics.

Phase 4 – KMS11-P System Testing

Verify the KMS11-P microprocessor subsystem operation with the functional diagnostics and system exerciser programs.

2.4 PREINSTALLATION CONSIDERATIONS

The following list (Table 2-1) should have been considered before ordering a KMS11-P communications interface, to make sure that the system can accept the KMS11-P, and that it can be installed correctly. These steps should also be verified at installation time.

Table 2-1 Option Packing List

Option	Part List	Description
KMS1P-M	M8206	Microprocessor module
	M8203	Line unit module
	BC08S-1	Module interconnect cable
	H3254	V.35 module test connector
	H3255	RS232-C/RS422-A/RS423-A test connector
	EK-KMS11-IN	KMS11-P Installation Manual
	EK-KMS11-TM	KMS11-P Technical Manual
	MP 01175	Customer print set
		Diagnostic Package (as applicable)
CK-KMS1P-xx		Cabinet Kits (Refer to Appendix F.2)

2.4.1 System And Device Positioning

2.4.1.1 System Positioning – On systems that contain many high speed Direct Memory Access (DMA) devices, there is a chance of unacceptable bus latency. To help prevent this from occurring the nearer the physical position of the KMS11-P to the memory and CPU, the higher the DMA device priority.

2.4.1.2 Device Positioning – The KMS11-P needs two hex-height, Small Peripheral Controller (SPC), backplane slots (two adjacent slots are best). A DD11-C or a DD11-D backplane can accept the KMS11-P.

CAUTION

Each KMS11-P needs approximately 10.5 amperes from the +5 Volt source. Check to make sure that the supply is capable of providing 10.5 amperes per KMS11-P.

2.4.2 System Requirements

1. UNIBUS loading

   M8206 microprocessor — 1 UNIBUS dc load, 5 UNIBUS ac loads

   M8203 line unit — No UNIBUS loads

2. Power Requirements

   Check the power supply before and after installation to make sure the supply is not overloaded. The microprocessor/line unit total current requirement for the +5 volt supply is approximately 10.5 amperes. Also, the modules need plus and minus 15 volts. Power requirements for the microprocessor/line units are listed in Table 2-2.

Table 2-2 Voltages

Module	Voltage Rating (Approximate values)	Maximum Voltage	Minimum Voltage	Backplane Pin
M8206	+ 5 volts at 7.5 A	+ 5.25	+ 5.0	C1A2
M8203	+ 5 volts at 3.0A	+ 5.25	+ 5.0	C1A2
	+15 volts at 0.15A	+15.75	+14.25	C1U1
	- 15 volts at 0.2A	- 15.75	- 14.25	C1B2

2.5 MICROPROCESSOR INSTALLATION

2.5.1 Backplane Considerations

Perform the following on the SPC slot that will contain the KMS11-P, M8206 microprocessor module (selected at pre-installation).

1. Verify that backplane voltages are within the specified tolerances listed in Table 2-2.

2. Turn system power off and remove the NPR Grant (NPG) wire that runs between CA1 and CB1 on that backplane slot for the M8206 module.

NOTE

Make sure this jumper is replaced, if the microprocessor is removed from the system.

2.5.2 M8206 Considerations

Perform the following on the KMS11-P M8206 microprocessor module:

1. Make sure that the priority plug (level 5 provided) is correctly seated in its socket.

2. Verify that jumper W1 (M8206) is installed (Figure 2-1). This jumper should not be removed in the field; it is removed only during automated module testing at the factory to inhibit the oscillator in the microprocessor clock logic.

3. Set the switches at location E129, so that the module will respond to its assigned address. When a switch is OFF (open), a binary 1 is decoded; when ON (closed), a binary 0 is decoded. Note that the switch indicated '1' (Figure 2-2) controls address bit 3, '2' to address bit 4, '3' to address bit 5, and so on.

E 31 VECTOR SELECT (7-POLE SWITCH)
E129 ADDRESS SELECT (10-POLE SWITCH)
E82-18 PROGRAM TIMER SELECT (8-POLE SWITCH)
W1 ALWAYS IN
W3 NORMALLY IN (OUT TO DISABLE KMC11-B CONTROL OF AC LO)

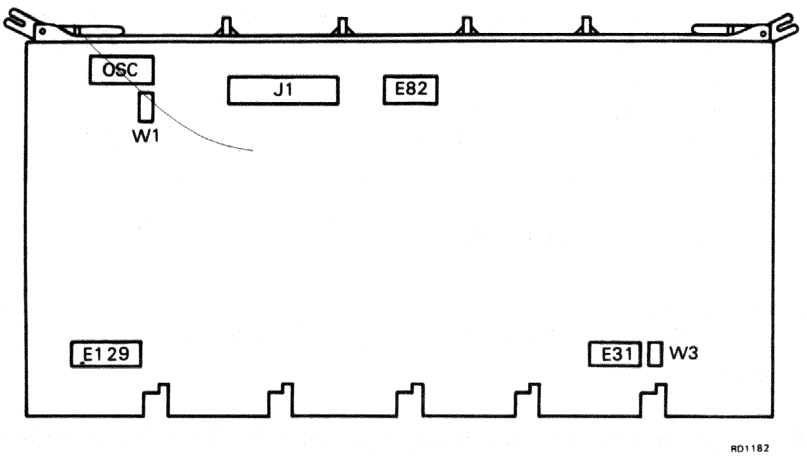

Figure 2-1 M8206 (KMC11-B) Switch and Jumper Locations

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	1	1	SWITCH PACK E 129										0	0	0	
SWITCH NB			S10	S9	S8	S7	S6	S5	S4	S3	S2	S1				DEVICE ADD.
												OFF				760010
											OFF					760020
											OFF	OFF				760030
										OFF						760040
										OFF		OFF				760050
										OFF	OFF					760060
										OFF	OFF	OFF				760070
									OFF							760100
								OFF								760200
								OFF	OFF							760300
							OFF									760400
							OFF		OFF							760500
							OFF	OFF								760600
							OFF	OFF	OFF							760700
						OFF										761000
					OFF											762000
					OFF	OFF										763000
				OFF												764000

NOTE : Switch off responds to logical one on the UNIBUS

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Figure 2-2 M8206 (KMC11-B) Address Selection

SWITCH PACK E129

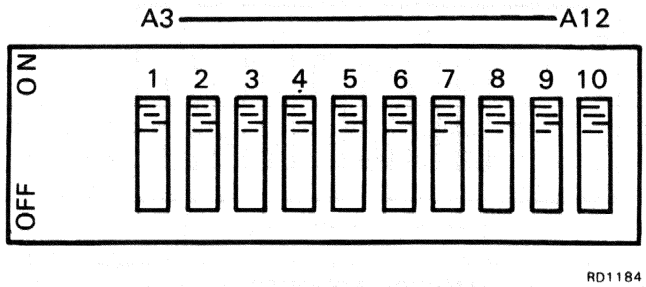

Figure 2-3 M8206 (KMC11-B) Device Address Switch Pack Layout

4. Vector selection is done using switches one to six, at location E31 (see Figure 2-4). When a switch is OFF (open) a binary 0 is decoded ; when ON (closed), a binary 1 is decoded. Note that switch '1' controls vector bit 3, '2' bit 4, and so on.

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	SWITCH PACK E31						1	0	0

SWITCH NB	S6	S5	S4	S3	S2	S1	VECTOR ADD.
		ON	ON				300
		ON	ON			ON	310
		ON	ON		ON		320
		ON	ON		ON	ON	330
		ON	ON	ON			340
		ON	ON	ON	ON		360
		ON	ON	ON	ON	ON	370
	ON						400
							—
	ON		ON				500
							—
	ON	ON					600
							—
	ON	ON	ON				700

NOTE : Switch ON produces logical 1 on the UNIBUS

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Figure 2-4 M8206 (KMC11-B) Vector Address Selection

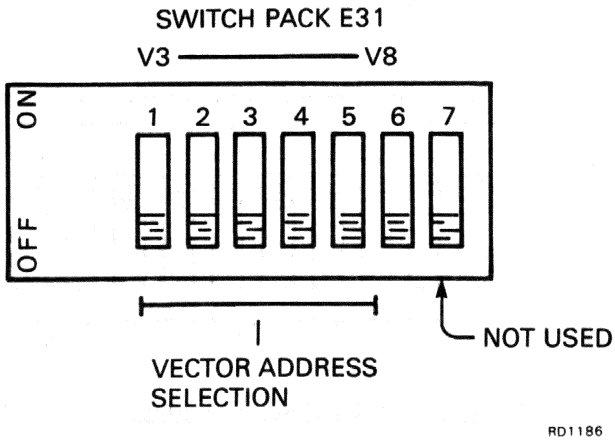


Figure 2-5 M8206 (KMC11-B) Vector Address Switch Pack Layout

5. Jumper W3 is normally IN and should only be removed if the KMC11-B is not to control ACLO.

6. The microprocessor contains a timer to run certain protocol firmware. It is important that timer values are set accurately before installation.

   The M8206 REV J microprocessor contains a switch pack at location E82, which is used to select the value of the program timer. E82-8 ON provides a timeout value of 115 milliseconds; OFF is 75 microseconds (E82 1-7 are not used).

NOTE

Make sure that the program timer selected is 115 millisecond when used with the KMS11-P option (E82-8 is ON).

2.5.3 M8206 Insertion

1. Carefully insert the M8206 microprocessor module into the selected SPC slot and perform the following tasks.

2. Turn system power ON and verify that the backplane voltages are within the specified tolerances listed in Table 2-2.

3. Load and execute the M8206 static diagnostics, parts one and two (no test connectors are needed).

   a. PDP-11 system

M8206 Static Test 1	CZKMB
M8206 Static Test 2	CZKMC

   b. VAX-11 systems

Microprocessor Repair Level Diagnostic	EVDHA
Microprocessor Level 2 Diagnostic	ESDHB

Chapter 4 provides additional information on these diagnostics. On getting a minimum of five error-free end passes, proceed to the M8203 line unit installation section.

2.6 LINE UNIT INSTALLATION

The M8203 line unit is a universal module with various types of interface capabilities. The M8203 line unit does not present any ac or dc loads to the UNIBUS system and takes power only from the backplane slot in which it resides. All data and control signals flow into and out of the line unit via a BC08R cable to the microprocessor. Because of the various M8203 applications, the configurations for each may be different, and are selected via switches, jumpers and different cables. To provide a better understanding of these variations, a number of tables describing each switch pack, jumper and cable function (as listed in Table 2-7) have been created for reference. Table 2-3 lists the normal M8203 line unit configuration for the different types of KMS11-P options. Refer to the following eight points as a guide.

1. Table 2-4 Jumper functions – These jumpers are used to select various interface standard parameters and modem interface signals, depending on application and modem type. Additional DIP switches are available on the RS232-C Bulkhead Panels for additional interface signal selection. (Refer to Appendix F3.)

2. Table 2-5 Switch Pack E39 functions – This switch pack allows correct selection of interface driver and receiver control logic and different line speeds for various applications.

3. Table 2-6 Switch Pack E121 functions – This switch pack is not used in the KMS11-P application.

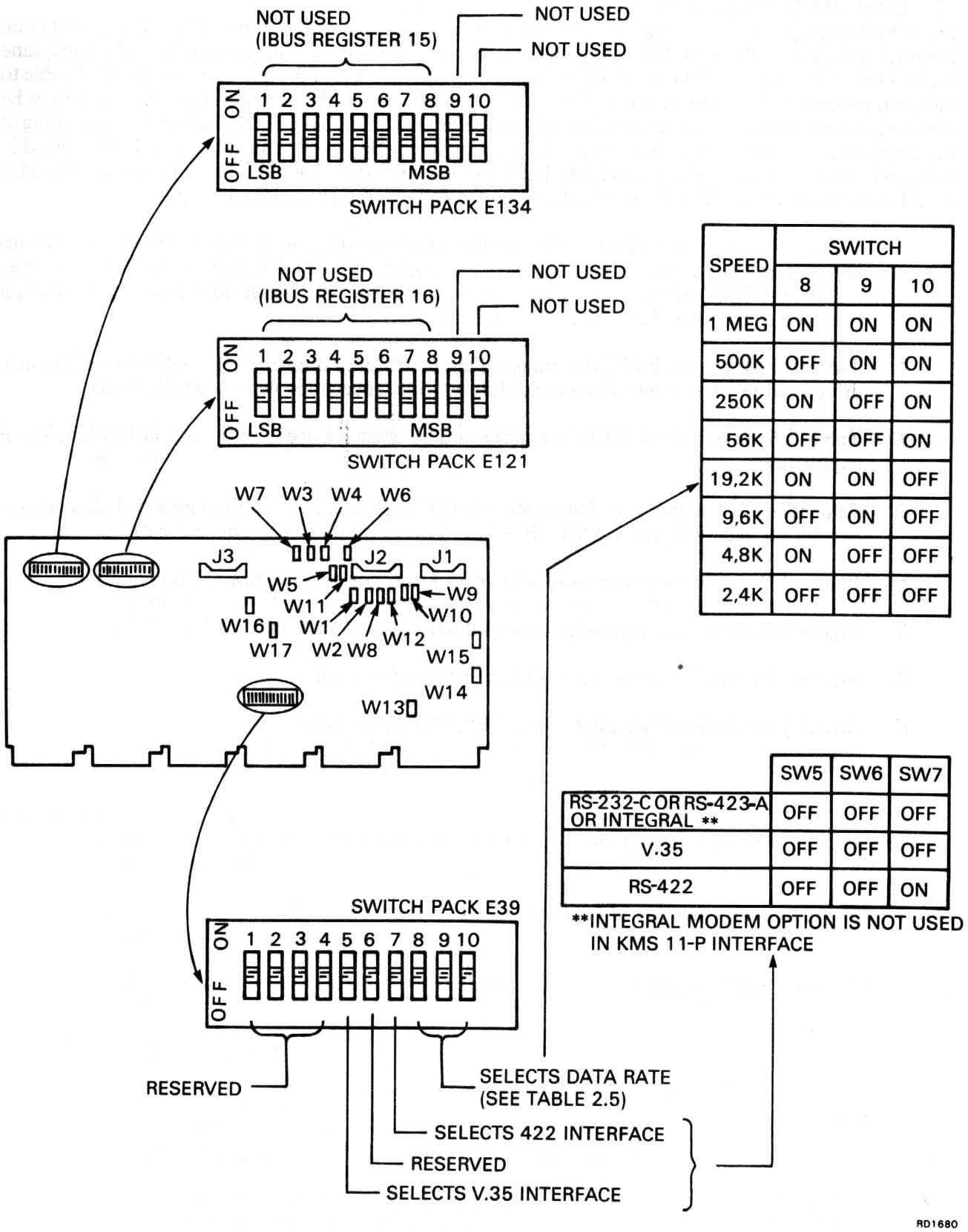
4. Appendix F2. Cabinet Kits Description – This appendix lists the functions and uses of each cabinet kit used with the KMS11-P. (Shows the cables and test connectors.)

5. Figure 2-6 shows the jumper and switch pack positions on the M8203 line unit.

6. Figure 2-7 shows the microprocessor and line unit installation.

7. Figures 2-8 and 2-9 show the module turnaround test connectors.

8. Switch pack E134 is not used in the KMS11-P application.



SPEED	SWITCH		
	8	9	10
1 MEG	ON	ON	ON
500K	OFF	ON	ON
250K	ON	OFF	ON
56K	OFF	OFF	ON
19,2K	ON	ON	OFF
9,6K	OFF	ON	OFF
4,8K	ON	OFF	OFF
2,4K	OFF	OFF	OFF

	SW5	SW6	SW7
RS-232-C OR RS-423-A OR INTEGRAL **	OFF	OFF	OFF
V.35	OFF	OFF	OFF
RS-422	OFF	OFF	ON

**INTEGRAL MODEM OPTION IS NOT USED IN KMS 11-P INTERFACE

Figure 2-6 M8203 Line Unit Switch and Jumper Locations

Table 2-3 Normal M8203 Configuration

M8203 Config.	Interface Type	EIA RS-232-C	CCITT V.35	EIA RS-422-A	EIA RS-423-A
Jumper config.* Table 2-4	W1-W6, W11 W14-W17	OUT	OUT	OUT	OUT
	W7-W10 W12, W13	IN	IN	IN	IN
Switch Pack E39 Table 2-5	S1-4	OFF	OFF	OFF	OFF
	S5	OFF	ON	OFF	OFF
	S6	OFF	OFF	OFF	OFF
	S7	OFF	OFF	ON	OFF
	S8	ON	ON	ON	ON
	S9	ON	ON	ON	ON
	S10	OFF	OFF	OFF	OFF
Switch Pack E121 Table 2-6	S1-8	NOT USED	NOT USED	NOT USED	NOT USED
	S9	NOT USED	NOT USED	NOT USED	NOT USED
	S10	NOT USED	NOT USED	NOT USED	NOT USED
Switch Pack E134 Table 2-7	S1-8	OFF	OFF	OFF	OFF
	S9	OFF	OFF	OFF	OFF
	S10	NOT USED	NOT USED	NOT USED	NOT USED
Cabinet Kit required		CK-KMS1P-A*x***	CK-KMS1P-B*x***	CK-KMS1P-E*x***	CK-KMS1P-F*x***
Module Turnaround		H3254 IN J1 AND H3255 in J2	H3254 IN J1 AND H3255 in J2	H3254 IN J1 AND H3255 in J2	H3254 IN J1 AND H3255 in J2

* Modem dependent

** *x* Cabinet family dependent -
For a complete description of the cabinet kits refer to Appendix F.2.

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Table 2-4 M8203 Jumper Functions

Jumper	Normal Config.	Function
W1	OUT	Clear to Send EIA/V.35
W2	OUT	Data Mode EIA/V.35
W3	OUT	Receive Data EIA
W4	OUT	Receive Clock EIA
W5	OUT	Receive Ready EIA
W6	OUT	Transmit Clock EIA
W7	IN	Signal Rate Indicate – When removed, opens signal to interface in RS-422-A and RS-232-C configurations.
W8	IN	Data Mode (Data Set Ready) – When removed, opens signal to interface in RS-422-A/423-A configurations. It has no effect in RS-232-C.
W9	IN	Null Modem Clock – When removed the signal amplitude is lowered below the interface standards so as not to create interference in some modems.
W10	IN	Terminal Ready – When removed, it opens the signal to modem in RS-422-A/423-A configurations.
W11	OUT	Receiver Ready (Carrier Detect) – When installed, it allows this signal to be on at all times. This could cause a problem with the microcode since the Universal Synchronous Receiver/Transmitter (USYRT) will be enabled all the time.
W12	IN	Terminal in Service (Make Busy) – When removed, it opens this signal to the modem. Some modems will not answer the phone and will be put in Analog Loopback when this signal is asserted.
W13	IN	Oscillator Enable – To be removed only for factory automatic testing. Jumper should always be installed.

Table 2-4 M8203 Jumper Functions (Cont)

Jumper	Normal Config.	Function
W14 and W15	OUT OUT	56K Bandpass Filter Enable – With these jumpers installed, the bandpass filter is limited to 56K b/s. Used in special applications only.
W16	OUT	Switched RTS-CTS Enable – When this jumper is installed, it enables the Request To Send interlock in the M8203 line unit which inhibits asserting RTS, until CTS is dropped. This jumper should never be installed when the KMS11-P is operating with a modem that has the constant CTS option installed.
W17	OUT	Half-Duplex Lockout Enable – When this jumper is installed, it enables the M8203 line unit half-duplex lockout feature when half-duplex mode is selected. The lockout feature disables the transmitter or receiver when the other is active. This jumper applies only to half-duplex applications. It must not be installed for full-duplex applications.

NOTE

Jumpers W16 and W17 are mutually exclusive. Only one or the other may be installed, not both. Also, these jumpers are provided only on M8203 modules REV E or later. For modules up to REV D, refer to ECO-M8203-MK-007 for details of jumpers.

Table 2-5 Switch Pack E39 (Z) Selections

Switches	Function			
1-4	Not used in KMS11-P			
5-7	Interface Selection – Selects correct drivers and receivers for each interface type.			
	Interface Type	SW5	SW6	SW7
	RS-232-C,RS-423-A	OFF	OFF	OFF
	V.35	ON	OFF	OFF
	RS-422-A	OFF	OFF	ON

Table 2-5 Switch Pack E39 (Z) Selections (Cont)

Switches	Function
8-10	Line Speed Selection – Selects modem speed for null modem applications, and diagnostic testing.

	Switch				Switch		
Speed	8	9	10	Speed	8	9	10
Not used	ON	ON	ON	19.2K	ON	ON	OFF
Not used	OFF	ON	ON	9.6K	OFF	ON	OFF
Not used	ON	OFF	ON	4.8K	ON	OFF	OFF
56K	OFF	OFF	ON	2.4K	OFF	OFF	OFF

NOTE

Switch OFF equals a logical one (1).

Table 2-6 Switch Pack E121 (Y) Selections

Switches	Function
1-8	These switches are not used in the KMS11-P option. They are physically connected to Register 16 with switch 1 being the least significant bit (LSB) and switch 8 the most significant bit (MSB).
9-10	These switches are physically connected to IBUS Register 11, bit 2 and 1. They must be off for a diagnostic purpose only.

NOTE

Switch OFF equals a logical one (1).

Table 2-7 Switch Pack E134 (X) Selections

Switches	Function
1-8	Not used in the KMS11-P option – These switches are physically connected to IBUS Register 15 with switch 1 being the least significant bit and switch 8 the most significant bit.
9	Auto-Answer Enable – When the switch is in the ON position, auto-answer is disabled. When the switch is in the OFF position, auto-answer is enabled. This allows the KMS11-P to monitor ring indicator (RI) and data set ready (DSR) to answer and control incoming calls. Control is established using a 20 second call set up timer. This switch must be OFF for the KMS11-P option.

Table 2-7 Switch Pack E134 (X) Selections (Cont)

Switches	Function
10	Not used in the KMS11-P option – Switch is physically connected to IBUS Register 11, bit 5.

NOTE

1. **Switch OFF equals a logical one (1).**

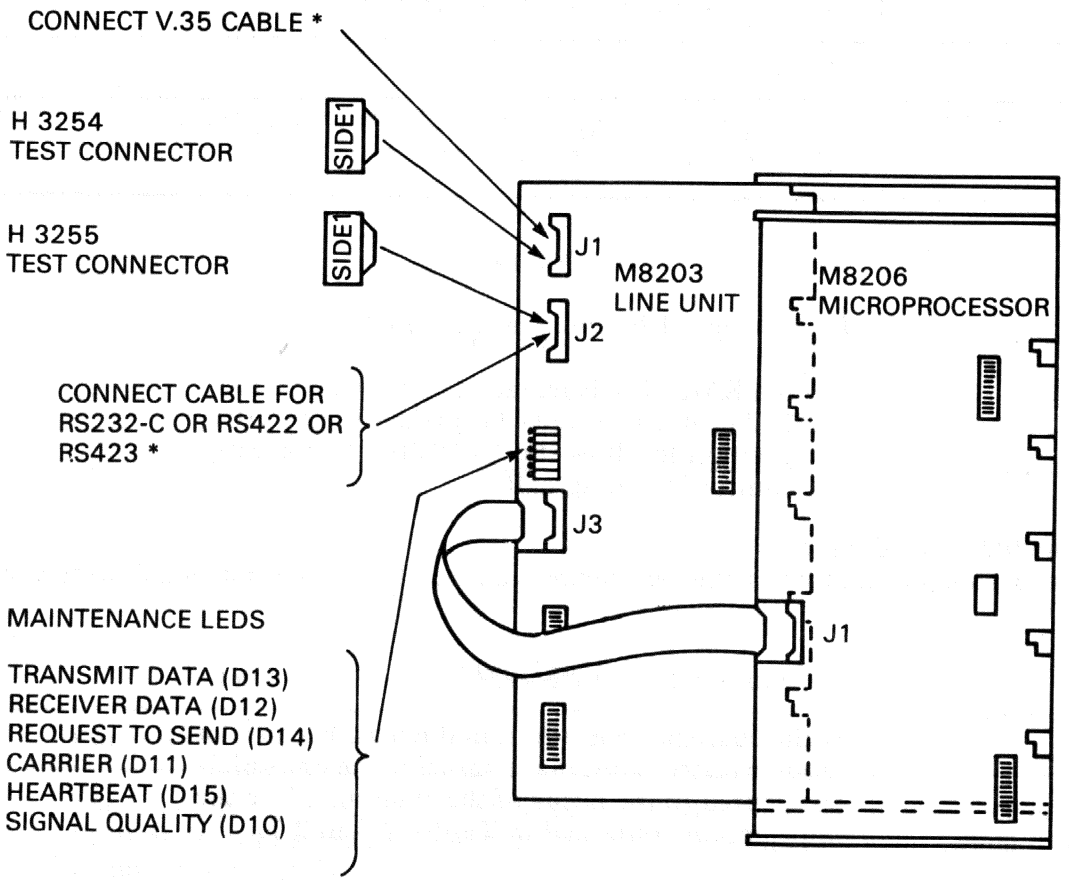
2. **If a KMS11-P is installed on a switched line, E134 switch 9 must be placed in the OFF position to allow the KMS11-P to correctly control incoming calls.**

2.6.1 M8203 Considerations

Configure all appropriate switch setting and jumpers on the M8203 line unit module as recommended in Table 2-7.

CAUTION

If the customer has additional needs, because of modem restrictions, make sure that the line unit is configured to the needs of the customer. Use the information contained in Tables 2-4 to 2-7.



* REFER TO APPENDIX F.2 FOR DETAILS

DESIGNATION	DESCRIPTION
D13	ON INDICATES UNIT IS TRANSMITTING A STEADY STREAM OF 1's
D12	ON INDICATES UNIT IS RECEIVING A STEADY STREAM OF 1's
D14	ON INDICATES THE USYRT IS READY TO TRANSMIT WHEN CTS IS DETECTED
D11	ON INDICATES CARRIER IS PRESENT AT THE RECEIVER
D15	HEARTBEAT
D10	ON INDICATES CARRIER PRESENCE AND OFF INDICATES CARRIER ABSENCE

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Figure 2-7 Microprocessor/Line Unit Installation

2.6.2 M8203 Insertion

1. With system power OFF, carefully insert the M8203 line unit module into the correct backplane slot (usually adjacent to the microprocessor) and perform the following.

2. Interconnect the line unit and the microprocessor using the BC08R-1 cable. One end of the cable is connected to J1 of the M8206 microprocessor module and the other end to J3 of the M8203 line unit module. Carefully bend the cable back to the right, close against the component side of either the microprocessor or line unit module, so as to fit it into the mounting box. Refer to Figure 2-7 for connector layouts.

3. Insert the appropriate module test connector into the correct line unit connector, as specified in Table 2-3. Make sure that the test connector is inserted with 'SIDE 1' (etched on the test connector) visible from the component side of the line unit. See Figure 2-7 for test connector layout.

   Schematics and outline drawings of each module turnaround test connector used with the KMS11-P are provided in Figures 2-8 and 2-9.

4. Turn system power ON and perform voltage checks on the line unit backplane slot. Make sure that the voltages are within the specified tolerances, as listed in Table 2-2.

5. Load and execute the M8203 static diagnostics, parts one and two, with external maintenance mode selected.

   b. PDP-11 System

      CZDMR – M8203 Static Diagnostic 1
      CZDMS – M8203 Static Diagnostic 2

   b. VAX-11 Systems

      EVDMA – M8203 Level 3 Diagnostics

   Chapter 4 provides detailed information on these diagnostic routines. On getting a minimum of five error-free end passes, with the module turnaround test connector installed, proceed with step 6.

6. Remove the module turnaround test connector and connect the appropriate cable to the correct Berg connector for the KMS11-P option selected. Refer to Appendix F for detailed information on cable requirements and to Figures 2-10 and 2-11 for system cable configurations.

CAUTION

Make sure that all cables mounted in the M8206 and M8203 are correctly installed and seated in the Berg connectors.

7. Insert the appropriate cable turnaround test connector in the end of the cable. Refer to Figures 2-10 and 2-11 for the specific test connector. Load and execute the M8203 static diagnostics specified in step 4, using the external maintenance mode, selected to verify the module and cable. On getting a minimum of five error-free passes, proceed to the KMS11-P System Test Procedures.

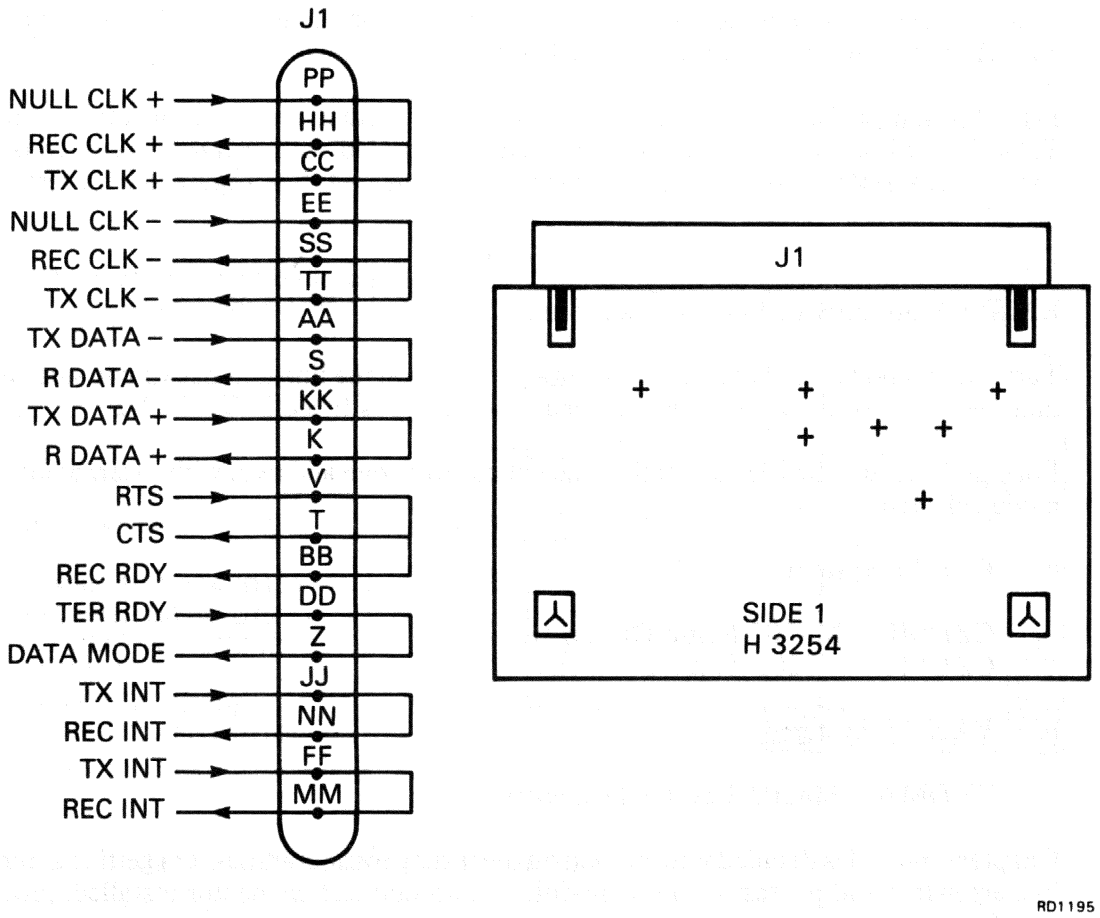


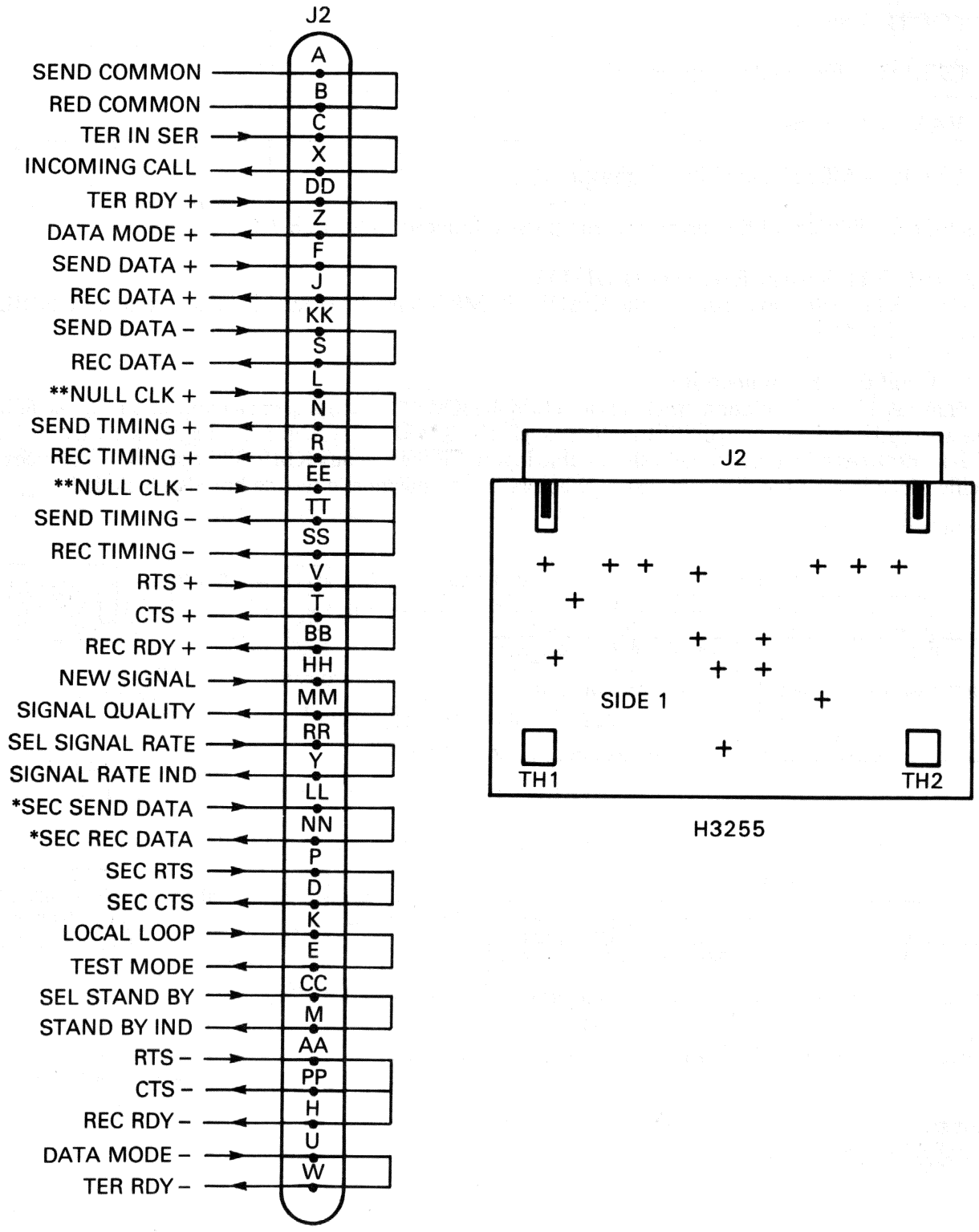
Figure 2-8 H3254 Module Test Connector

2.7 KMS11-P SYSTEM TESTING

The final step in the installation of a KMS11-P subsystem is to exercise the microprocessor and line unit, as one complete unit on the UNIBUS system, and over the communications link. This is the first testing that will use microcode loaded into the microprocessor.

2.7.1 Functional Diagnostic Testing

Make sure that the specific cable turnaround test connector, for the selected KMS11-P option, stays installed at the end of the cable. Load and execute the KMS11-P functional diagnostics with the External Mode selected. See Chapter 4 for details of this diagnostic test.



* NOT REQUIRED FOR KMS 11-P

** RS 449 SIGNAL – TERMINAL TIMING

RD1196

Figure 2-9 H3255 Module Test Connector

1. PDP-11 Systems

   CZKMR – Functional diagnostics

2. VAX-11 Systems

   EVDIG – M8203 Level 2R diagnostic

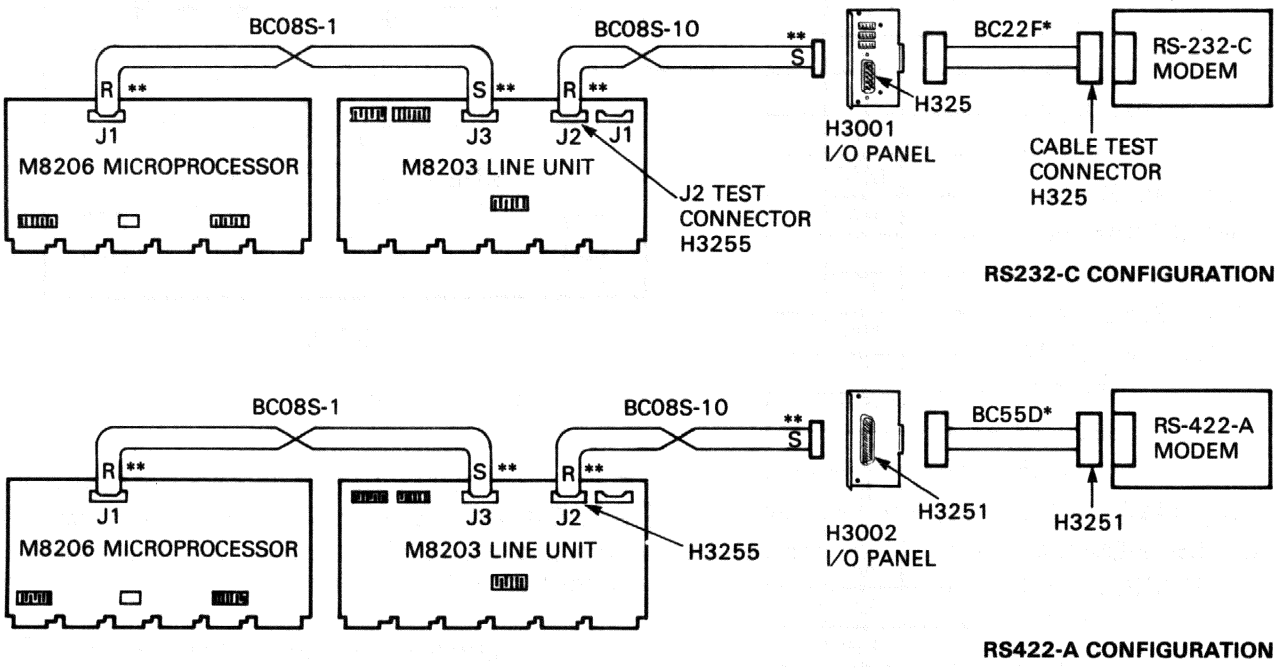
On getting a minimum of five error-free end passes, proceed to Section 2.7.2.

2.7.2 DEC/X11 System Exerciser (PDP-11)

The DEC/X11 system exerciser for the KMC11-B (M8206 module) can be run to check the UNIBUS activity (CXKMA).

2.7.3 Final Cable Connections

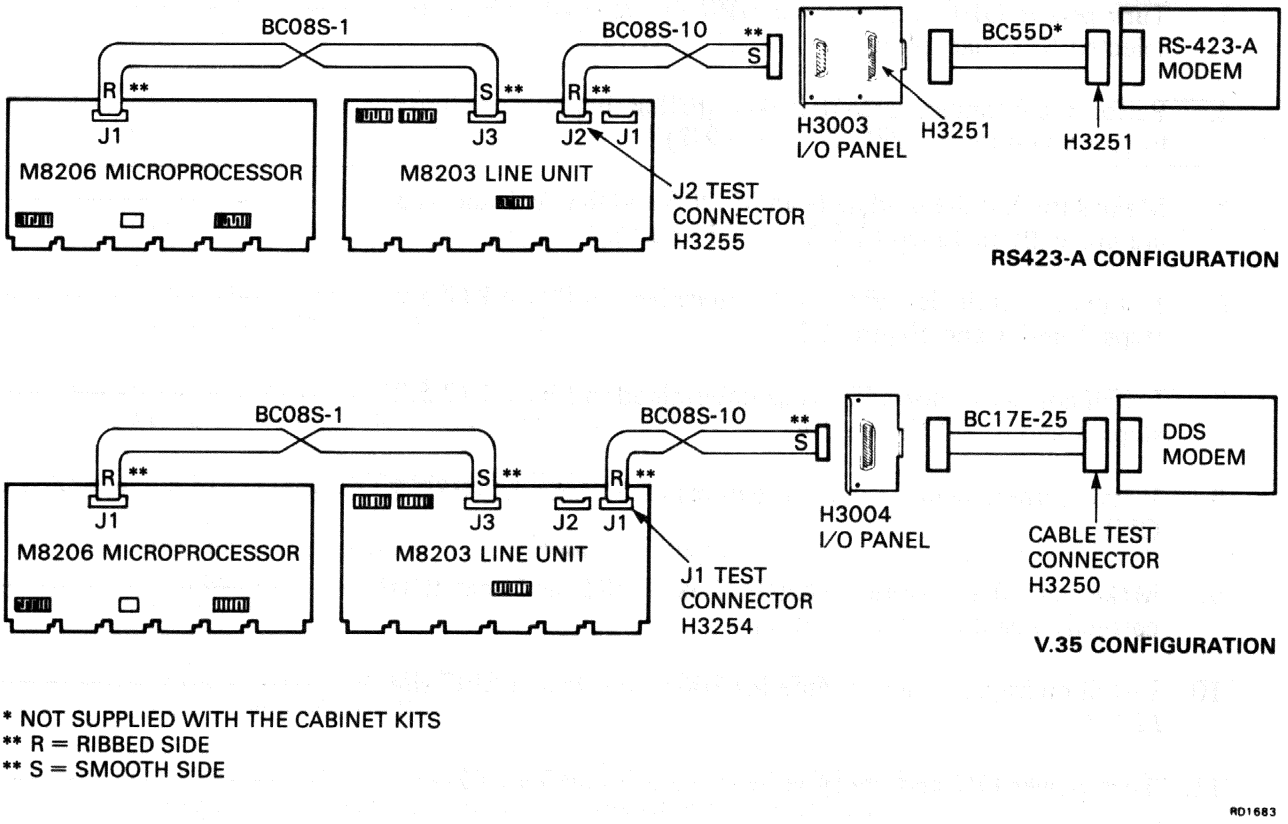
The final step in the installation process is to return the KMS11-P to its normal cable connections, either to the appropriate modem or to the distribution panel. The KMS11-P system cable diagrams in Figures 2-10 and 2-11 have been included to help show cable layout for the various KMS11-P options. References to specified locations of the different test connectors during diagnostic testing are also included.



* NOT SUPPLIED WITH THE CABINET KITS
** R = RIBBED SIDE
** S = SMOOTH SIDE

RD1682

Figure 2-10 Remote System Cable Diagram for RS-232 and RS-422



* NOT SUPPLIED WITH THE CABINET KITS
** R = RIBBED SIDE
** S = SMOOTH SIDE

RD1683

Figure 2-11 Remote System Cable Diagram for RS-423 and V.35

2.8 KMS11-P INSTALLATION CHECK-OFF LIST

PHASE 1 – PREINSTALLATION CONSIDERATIONS

Date Completed

1. System positioning (2.4.1.1) _____
2. Device positioning (2.4.1.2) _____
3. System requirements (2.4.2)

   UNIBUS loading
   b. Power requirements
   c. Interrupt priority level is 5
   d. KMS11-P device address
   e. KMS11-P vector address _____

PHASE 2 – MICROPROCESSOR INSTALLATION

1. Unpack KMS11-P option and verify that all components are present (Table F-1 and Appendix F-2.) _____
2. With power ON, verify selected SPC backplane voltages (2.5.1 and Table 2-2). _____

3. Turn power OFF and remove NPR Grant (NPG) wire on selected SPC backplane slot – CA1, CB1 (2.5.1). _____

4. Perform resistance checks to make sure that there are no shorts to ground on the backplane (Table 2-2). _____

5. Make sure that the module is an M8206 and that W1 and W3 are correctly installed (2.5.2 steps 2 and 5). _____

6. Install correct device address as determined in Phase 1 (2.5.2 steps 3 and 4 and Figure 2-3). _____

7. Install correct vector address as determined in Phase 1 (2.5.2 steps 3 and 4 and Figure 2-4). _____

8. Install correct switch selected features (2.5.2 step 6) (E82-8 ON). _____

9. Make sure that Priority Plug E77 is a BR5 and that it is correctly installed (2.5.2 step 1). _____

10. Install microprocessor module M8206 into selected SPC slot (2.5.3). _____

11. Turn power ON and verify voltages (2.5.3 and Table 2-2). _____

12. Load and execute M8206 Static Diagnostics (2.5.3 and Chapter 4). _____

PHASE 3 – LINE UNIT INSTALLATION

1. Install the correct jumpers and switch selection for the appropriate KMS11-P option. Use Table 2-3 to first set up the line unit and if additional features are needed, refer to Tables 2-4 to 2-7 (2.6.1, Figure 2-6 and Table 2-3). _____

   Also refer to:

   Table 2-4 Jumper Function
   Table 2-5 Switch Pack E39 Functions
   Table 2-6 Switch Pack E121 Functions
   Table 2-7 Switch Pack E134 Functions

2. Important switch/jumper verifications

   Be sure that E121 switch 9 and 10 are OFF (Table 2-6). _____

3. With power OFF, carefully install the M8203 line unit adjacent to the microprocessor, with interconnecting cable BC08R-01 in J3. The other end is installed in J1 of the M8206 microprocessor (2.6.2). _____

4. Correctly insert the correct module test connector in J1 and J2 of the M8203 line unit (2.6.2, Figure 2-7). _____

5. Turn power ON, perform voltage checks, and adjust if necessary (2.6.2 and Table 2-2). _____

6. Load and execute the M8203 static diagnostics, with module test connectors H3254 and H3255 installed (2.6.2 and Chapter 4). _____

7. Remove module test connectors and install the appropriate option cable to either J1 or J2, as needed. (Table 1-1 and Appendix F-2 and F-3). Insert the appropriate turnaround test connector at the end of the cable. _____

8. Load and execute the M8203 static diagnostics in External Mode to verify cable connections (2.6.2, Table 2-3). _____

PHASE 4 – KMS11-P SYSTEM TESTING

1. With cable turnaround test connectors installed, load and execute the KMS11-P functional diagnostic test (2.7.1 and Chapter 4). _____

2. Configure and execute the DEC/X11 System exerciser to include the KMC11-B. _____

3. Remove all cable test connectors, if installed, and connect appropriate cables to the modem or distribution panel (2.7.3 Figures 2-10 and 2-11). _____

CHAPTER 3
PROGRAMMING

3.1 INTRODUCTION

This chapter gives an introduction to the logical structure of the programmable Control and Status Registers (CSRs) and their operation and bit assignments. It also provides information useful for developing firmware programs compatible with the KMS11-P hardware.

The M8206 Microprocessor (KMC11-B) registers, and the M8203 Line Unit registers are completely detailed in this chapter. Before trying to program the KMC11-B, refer to the programming manual for this device – document number YM-P093C-00.

3.2 LOGICAL ORGANIZATION OF REGISTERS

Figure 3-1 shows the general logical organization of the various registers of the KMS11-P and the CPU (PDP-11 or VAX-11), and their interaction. It is important to understand that the data paths named OBUS*/IBUS* and OBUS/IBUS are not necessarily separate physical buses, but only logical assignments needed because the micro-P (microprocessor) has only a limited addressing capability of four bits (16 addresses). It is also important to understand that the various registers referred to are physically a mixture of actual memory registers, discrete hardware registers (flip-flops), and registers internal to integrated circuits.

The registers described in this chapter are called CSRs (Control and Status Registers) because they contain control and status information needed for correct operation of the hardware. They are also called micro-P CSRs because they can be accessed by the micro-P under program control. Some of these registers are also accessible to the CPU (PDP-11 or VAX-11), for interaction between the micro-P and the CPU UNIBUS system. When viewed from the CPU, these registers are called UNIBUS CSRs. Registers that need simultaneous access from more than one source have their physical location in the M8206 multiport RAM.

NOTE

OUTBUS* and INBUS* are also truncated to OBUS* and IBUS*; they are the same. OUTBUS and INBUS are also truncated to OBUS and IBUS; they are the same.

The description that follows will first cover the CPU CSRs, then the IBUS*/OBUS* CSRs, then the IBUS/OBUS CSRs and finally the CSRs of the Line Unit (M8203).

3.3 KMC11-B (M8206) REGISTERS

3.3.1 UNIBUS Control and Status Registers

Four 16-bit CSRs are used for the exchange of information between the CPU UNIBUS system and the KMC11-B microprocessor (micro-P). These CSRs are assigned the following addresses within the CPU floating address space in the I/O page:

76XXX0, 76XXX2, 76XXX4, and 76XXX6

They are word addressable or byte addressable by the CPU program. When word addressed, they are referred to as SEL 0, SEL 2, SEL 4 and SEL 6. When byte addressed, they are referred to as BSEL 0, BSEL 1, through to BSEL 7.

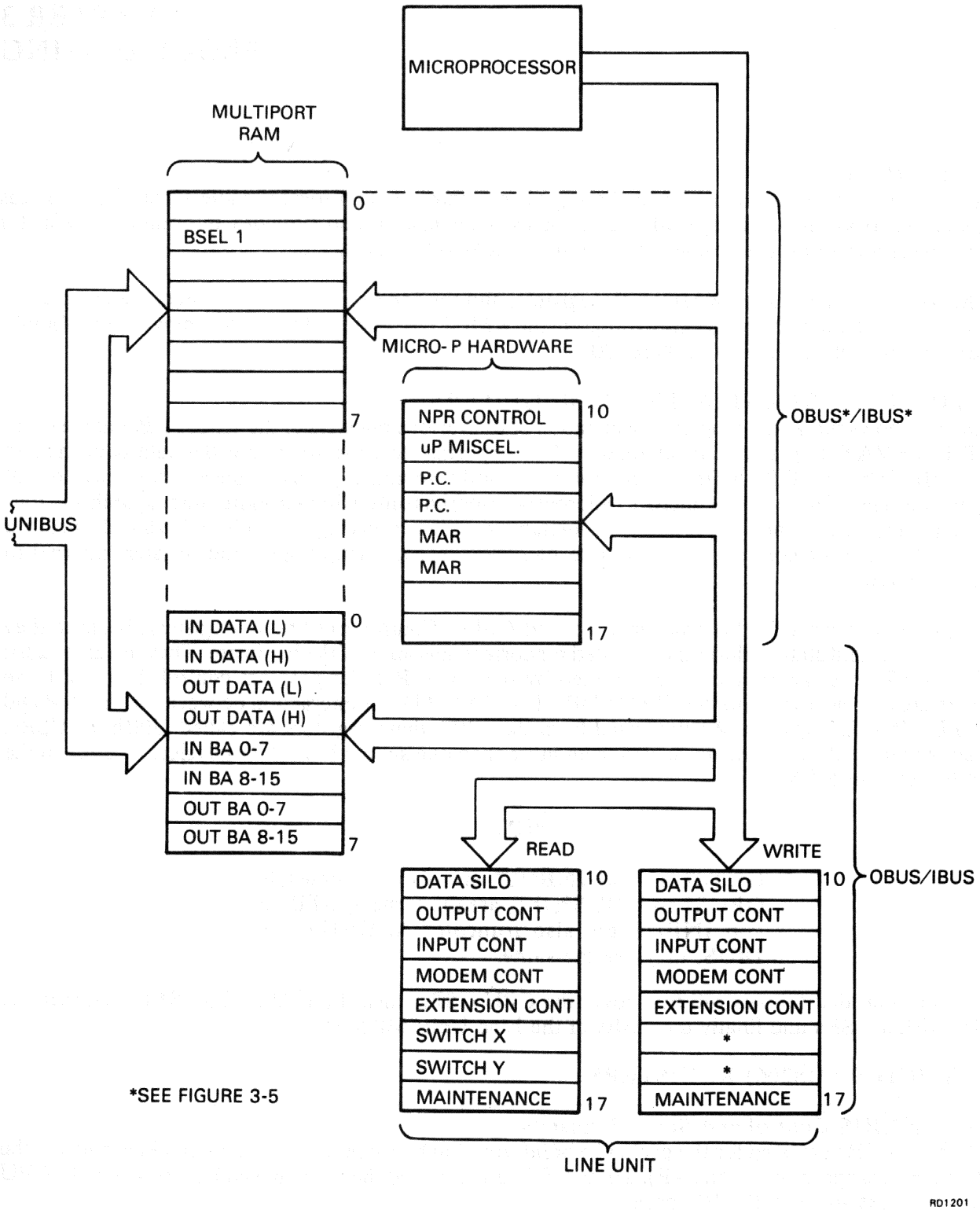


Figure 3-1 Logical Organization of Control and Status Registers

Refer to Appendix A if detailed information on floating address space is needed.

Figure 3-2 shows this set of registers. Except for BSEL 1, these registers have no hardware assignments and their function is determined by the KMC11-B firmware and the CPU software. Register BSEL 1 contains only maintenance functions, with the exception of bit 14 (MASTER CLEAR). This register is used when servicing the KMC11-B and should not be used for normal communication between the CPU and the micro-P. As may be seen from Figure 3-1, BSEL 1 register is contained in the multiport RAM. It is also implemented in the hardware, to operate with the micro-P logic in order to implement the specified functions.

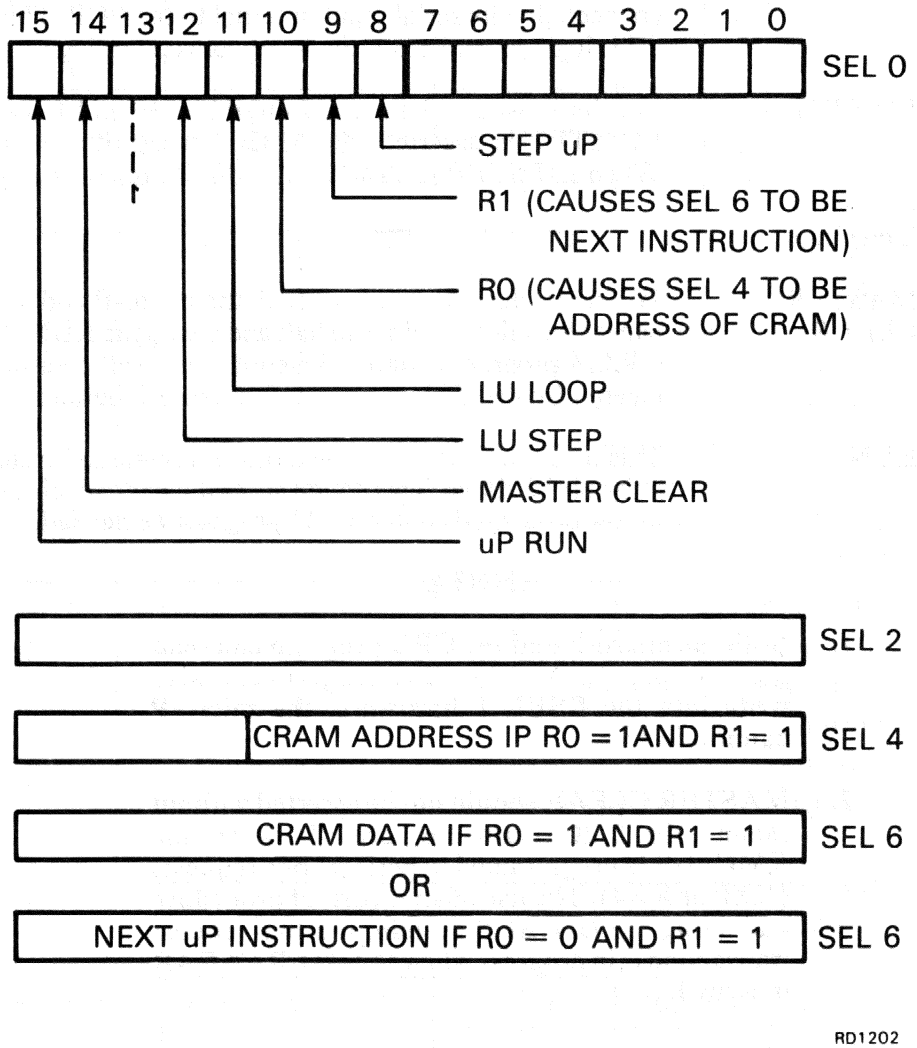


Figure 3-2 UNIBUS Control and Status Registers

The bit assignments for BSEL 1 register are described below. All bits are read/write. (See NOTE 1 at the end of the bit descriptions.)

Bit	Name	Description
8	STEP Micro-P	This bit, when set, steps the micro-P through one instruction cycle, made up of five 60-ns clock pulses. The RUN flip-flop should be cleared before executing this function.

Bit	Name	Description
9	R1	When set, causes the contents of SEL 6 to be executed as the next instruction when STEP micro-P is asserted.
10	R0	When set together with R1 (bit 9), causes the contents of SEL 4 to be an address pointer into the micro-P CRAM memory, and causes SEL 6 to be the data at that address.
11	LU LOOP	When set, causes the serial output from the M8203 Line Unit to be connected to its serial input, internal to the PCB. This is done at the TTL logic level, before the level conversion logic.
12	LU STEP	This bit is used with the LU LOOP bit. When LU LOOP is set and LU STEP is asserted, the M8203 transmitter is single stepped. When LU STEP is cleared, the M8203 receiver is single stepped.
13	Undefined	
14	MASTER CLEAR	When set, this bit initializes both the micro-P and the Line Unit. It causes the micro-P clock to halt and clears the RUN flip-flop and the CRAM program counter. This bit is not self-clearing and must be cleared by the CPU program. See Note 2 below.
15	RUN	This bit controls the micro-P clock. It is cleared by bus initialization or by bit 14 above. This action stops the micro-P clock. This bit may be set or cleared by the CPU program as needed.

NOTE

1. **Both the micro-P and the CPU program can read the multiport RAM. The CPU program can also write into the BSEL 1 hardware; the micro-P cannot do this.**

2. **MASTER CLEAR should not be asserted without raising the CPU status to level 7, when the KMC11-B is programmed to perform bus requests (XX0 or XX4). The use of an incorrect procedure may hang the UNIBUS system, if a bus request transaction is in progress when MASTER CLEAR is issued.**

3.3.2 OBUS*/IBUS* CSR Registers

Figure 3-3 shows the set of CSRs assigned to this group. The first eight bytes of this set (addresses 0 to 7), are contained in the multiport RAM, and are therefore accessible to both the micro-P and the CPU UNIBUS. In fact, these first eight bytes are the same as those described above as UNIBUS registers, but viewed from the micro-P. Therefore IBUS* 1 contains the same information as BSEL 1. Therefore, as stated above, the other seven bytes (address 0 and 2 to 7) have no hardware assignment and their function is determined by the KMC11-B firmware and by the CPU software.

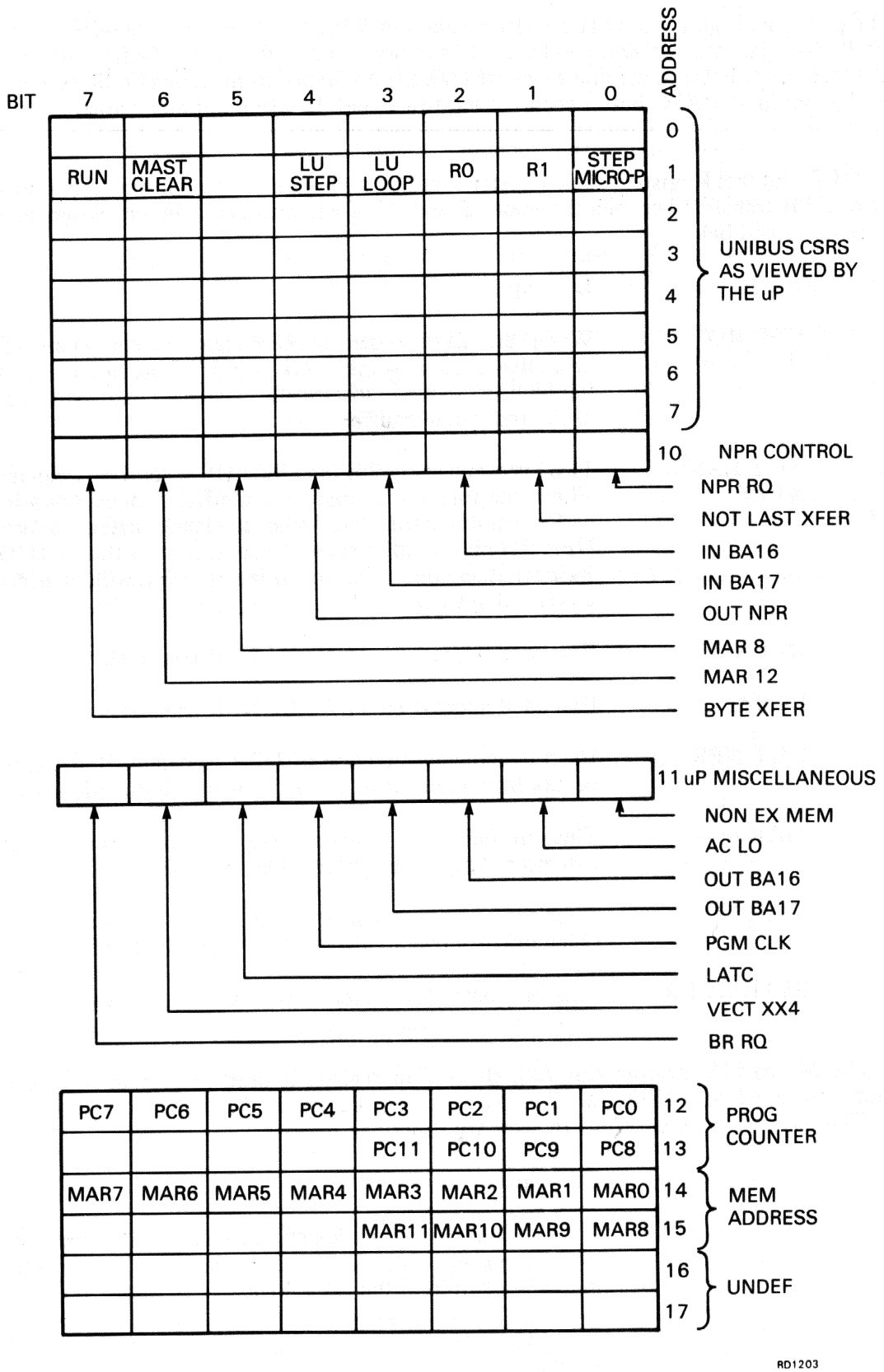


Figure 3-3 OBUS*/IBUS* CSRs

As may be seen from Figure 3-3, OBUS*/IBUS* addresses 108 to 178 contain the NPR control register, the micro-P miscellaneous register, two bytes of Memory Address Register (MAR), and two undefined registers. Note that although these addresses are logically continued from address 7, this set of eight bytes is not in the multiport RAM, but in separate hardware and therefore not accessible to the UNIBUS system.

3.3.2.1 **NPR Control Register** – This register contains control and status information used to monitor and control NPR transfers between the micro-P and the CPU memory. The bit assignments for this register are described below.

Bit	Name	Description
0	NPR RQ	When set, this bit starts the NPR logic. It requests an NPR via the UNIBUS system to the CPU memory. The micro-P cannot clear this bit because it is automatically cleared by hardware on completion of the requested transfer.
1	NOT LAST XFER	This bit, when set, holds the UNIBUS system between transfers. It allows the micro-P to maintain UNIBUS mastership in order to perform multiple transfers. When the last transfer is to be executed, NPR RQ bit should be set at the same time as this bit (NOT LAST XFER) is cleared. The following transfer will then give up the UNIBUS system.
2	IN BA16	Extended address bit 16 for IN NPR transfers.
3	IN BA17	Extended address bit 17 for IN NPR transfers.
4	OUT NPR	Used to indicate direction of NPR transfers. If set, then transfer occurs from micro-P to CPU. If clear, the direction is reversed.
5	MAR 8	This bit indicates when a page overflow occurs in the MAR (Memory Address Register). This bit is read only.
6	MAR 12	This bit indicates when a memory overflow occurs in the MAR (Memory Address Register). This bit is read only.
7	BYTE XFER	This bit controls whether word transfers or byte transfers occur. When set, byte transfers occur.

3.3.2.2 **The Micro-P Miscellaneous Register** – This register is used to contain control and status information connected with NPR transfers, but it is not directly used in the actual operation of such transfers. The bit assignments for this register are described below.

Bit	Name	Description
0	NON EX MEM	This is a flag bit which indicates that the preceding transfer was made to a non-existent location in CPU memory, and an NPR SSYN timeout occurred in the NPR logic.
1	AC LO	This bit generates an AC LO signal of half a second on the UNIBUS system.
2	OUT BA16	Extended address bit 16 for an OUT NPR transfer.

Bit	Name	Description
3	OUT BA17	Extended address bit 17 for an OUT NPR transfer.
4	PGM CLK	This bit acts as a timer for the micro-P. It can be read to determine elapsed time for timeout, flag testing, and so on.
5	LATC	Read/Write bit with no hardware assignment.
6	VECT XX4	If set, generates vector address XX4 when BR RQ is asserted. If clear, generates vector address XX0 when BR RQ is asserted.
7	BR RQ	When set, generates a bus request via the UNIBUS system at BR level 4, 5, 6 or 7. The micro-P is shipped with a BR5 priority installed. This bit is cleared only by the hardware after the BR has been completed.

3.3.2.3 Program Counter Register – This register, which is address 12 and 13 in the set, is the program counter for the KMC11-B control memory. It normally contains the address of the next instruction in CRAM, to be executed by the micro-P.

3.3.2.4 Memory Address Register – This register, which is address 14 and 15 in the set, is the memory pointer to the KMC11-B data memory.

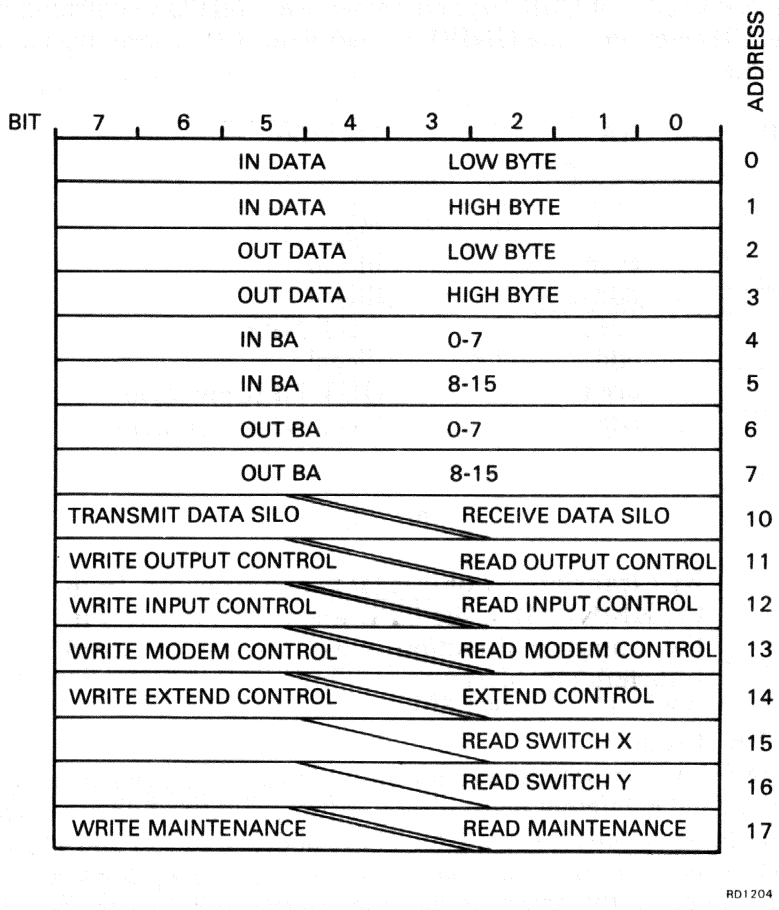


Figure 3-4 OBUS/IBUS CSRs

3.3.3 OBUS/IBUS CSR Registers

Figure 3-4 shows the set of CSRs assigned to this group. The first eight bytes of this set, (addresses 0 to 7), are contained in the multiport RAM, and are therefore accessible to both the micro-P and the CPU UNIBUS system. When viewed from the UNIBUS system, these registers supply the address and data information to the UNIBUS system during NPR transfers. The second eight addresses (108 to 178) of this set are shared by 16 registers – eight for read operations and eight for write operations – which are all contained in the M8203 Line Unit. In addition, two of the addresses connected with writing may access four different registers each, using extended addressing which is described below. The above configuration permits the mapping of 24 registers within the second eight available addresses.

3.3.3.1 Micro-P OBUS/IBUS CSR Registers – Information contained in the first eight addresses (0 to 7) of the OBUS/IBUS set of CSRs is linked with the information contained in CSR 108 of the OBUS*/IBUS* set. Therefore, when OUT NPR is cleared (bit 4 of CSR 108 is cleared), the transfer is from the CPU memory at the address specified by IN BA registers 4 and 5, with the data going into IN DATA registers 0 and 1, provided BYTE XFER (bit 7 of CSR 10) is also clear.

When OUT NPR is set (bit 4 of CSR 10 of OBUS*/IBUS* set), the transfer is from the KMC11-B data held in OUT DATA registers 2 and 3, into the CPU memory at the address specified by the OUT BA registers 6 and 7, provided BYTE XFER (bit 7 of CSR 10) is also clear. When BYTE XFER is set, byte transfers occur, and the data transferred is always from OUT DATA register 2, whether the destination is the low byte (OUT BA address even), or the high byte (OUT BA address odd). Note that when BYTE XFER is clear and word transfers occur, the address specified in OUT BA registers 6 and 7 should always be even.

Note also that OUT NPR (bit 4 of CSR 10) determines the UNIBUS control line C1, and that BYTE XFER (bit 7 of CSR 10) determines the UNIBUS control line C0. The above paragraph is expanded in the following truth table:

C1	C0	BA	Transfer
0	0	even	IN NPR
0	0	odd	Illegal
0	1	even	Illegal
0	1	odd	Illegal
1	0	even	OUT NPR
1	0	odd	Illegal
1	1	even	OUT NPR low byte
1	1	odd	OUT NPR high byte

NOTE

Byte transfers are only legal in one direction, from the KMC11-B to the CPU memory. Transfers in the opposite direction must always be word transfers (16 bits).

3.3.4 Line Unit CSR Registers

Examination of Figure 3-4 will show these as addresses 108 to 178. Each address accesses two registers, one for a read operation, and a different register for a write operation. Addresses 158 and 168, however, are read only and cannot be directly written into. These addresses (158 and 168) are also extended by means of extend bits, to provide four additional levels for read operations and three levels for write operations. When so extended, the access is into the internal registers inside the USYRT integrated circuit. Figure 3-5 shows a schematic of this configuration.

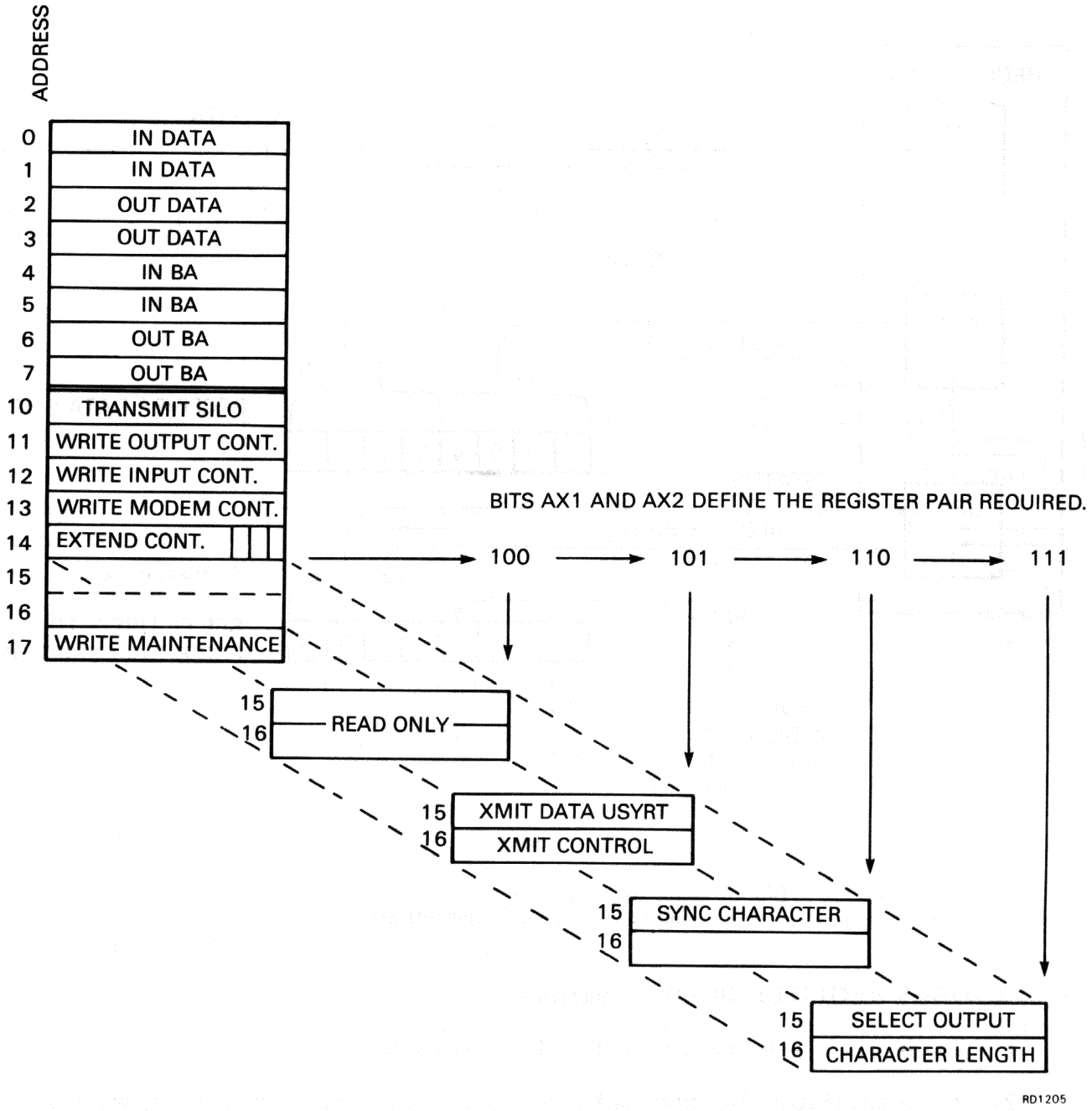


Figure 3-5 Schematic of OBUS CSRs

For easier identification, all the read registers are defined as IBUS registers (108 to 178), while all the write registers are defined as OBUS registers (108 to 148 and 178). The bit assignments for each register will be described below.

3.3.4.1 IBUS Register 10 – Read operation:

1. Reads data in and shifts the silo.
2. Status bits (register 12) are read first.
3. Register 12 status bit 4, in RDY H, must be true before any data is read from the silo.

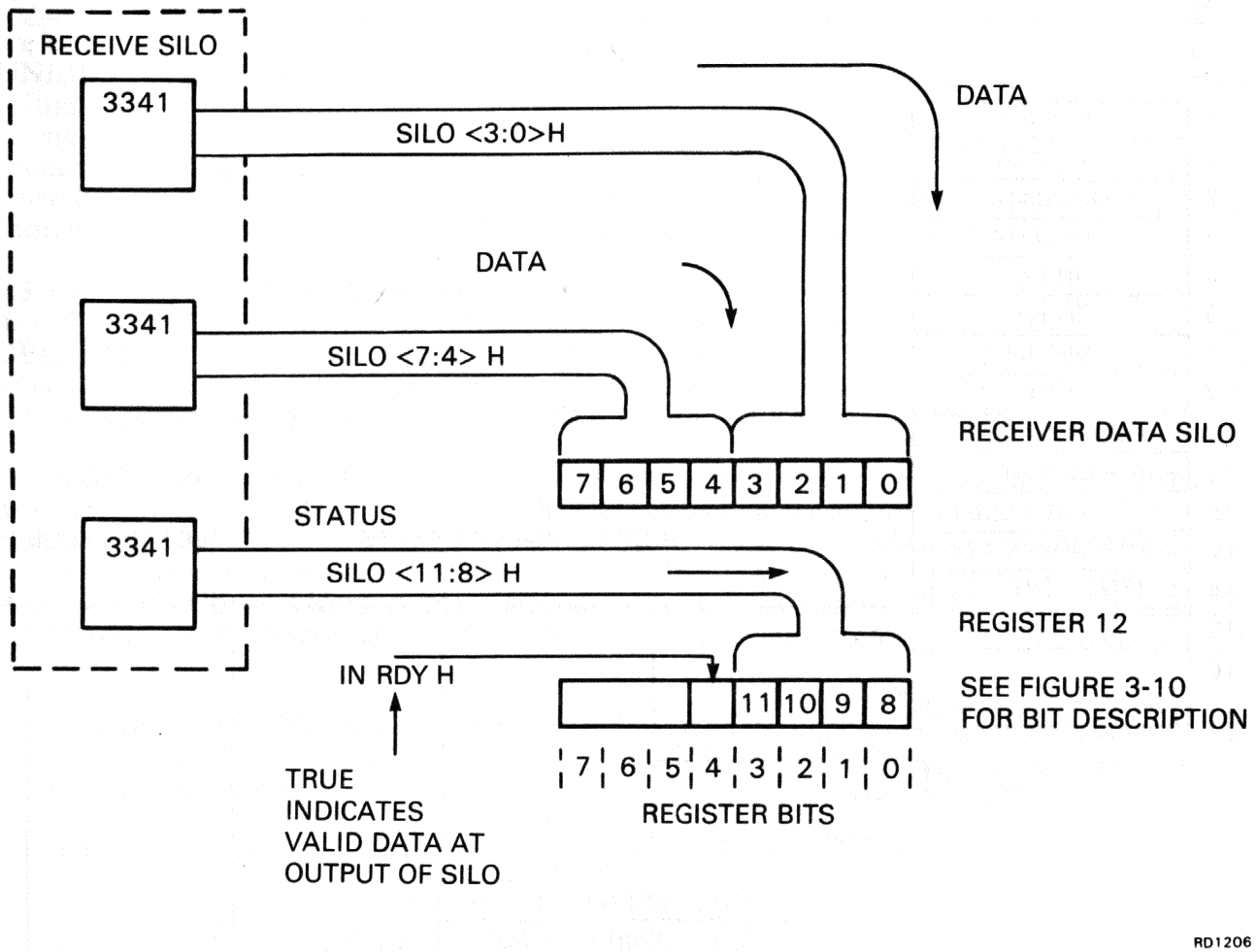


Figure 3-6 IBUS Register 10

3.3.4.2 OBUS REGISTER 10 – Write operation:

1. Loads data to be transmitted into the silo and shifts the silo.
2. Status bits (BALU 3-0) from OBUS register 11 are also loaded into the silo when OBUS register 10 loads the silo. The status bits, if they are needed, should be loaded first.
3. All bits are cleared when the silo is shifted.
4. Data should not be written into register 10 unless status bit 4 of read IBUS register 11 (Out Ready) is set.

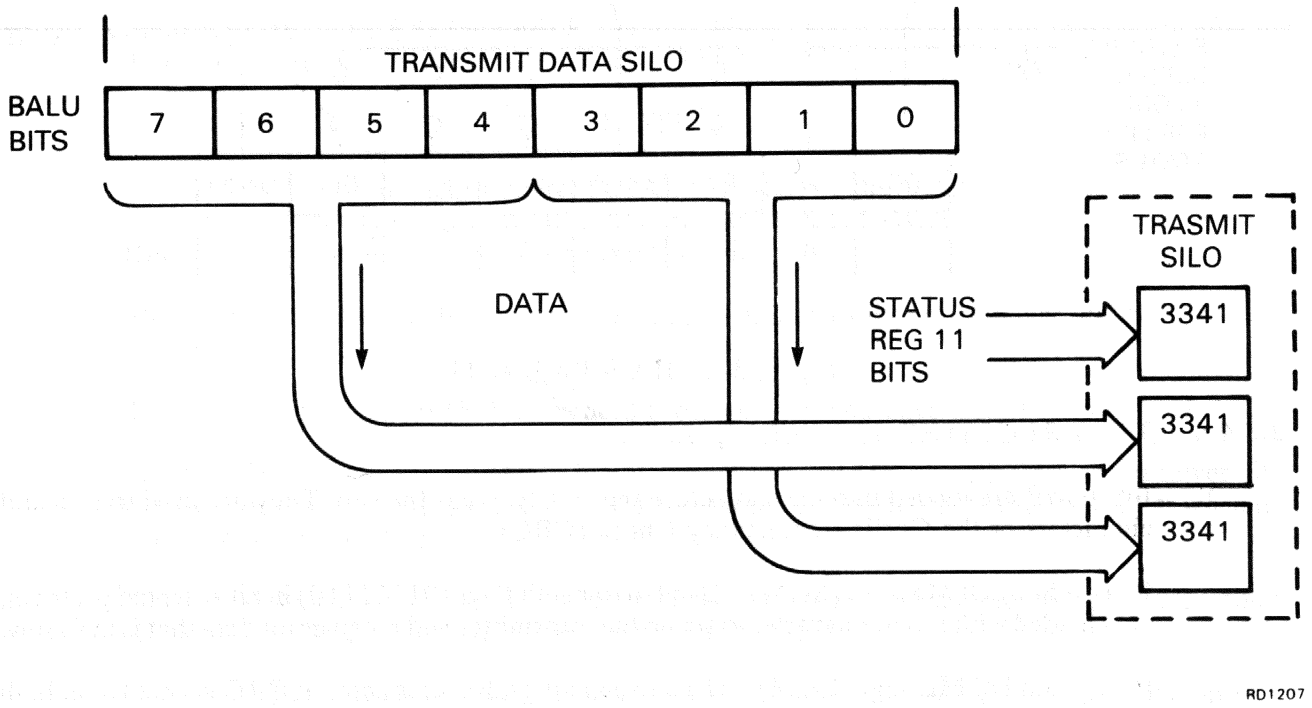


Figure 3-7 OBUS Register 10

3.3.4.3 IBUS REGISTER 11 – Read operation:

1. Bits 1 to 3 and 5 (switch) have no hardware control. They should be set up when the module is installed in the field, according to the customer link (the microcode and microprocessor used). Refer to the appropriate Options Manual.

2. Bit 0 =Transmitter Underrun – When set, it means that characters have not been provided to the transmitter fast enough, causing the USYRT to go to the IDLE state. (Can only be cleared by the next Start Of Message (SOM) or by clearing the transmitter.)

3. Bit 4 = Out Ready – The silo is ready for another character. If the silo is disabled, it indicates that the USYRT is ready for another character.

4. Bit 6 = Out Active – The USYRT is in the process of transmitting data. If Out Active is set and Request to Send is not set, no characters are processed (check Modem Ready and Clear to Send bits in IBUS register 13).

5. Bit 7 = Out Clear – The transmitter is in the process of being cleared and should not be addressed.

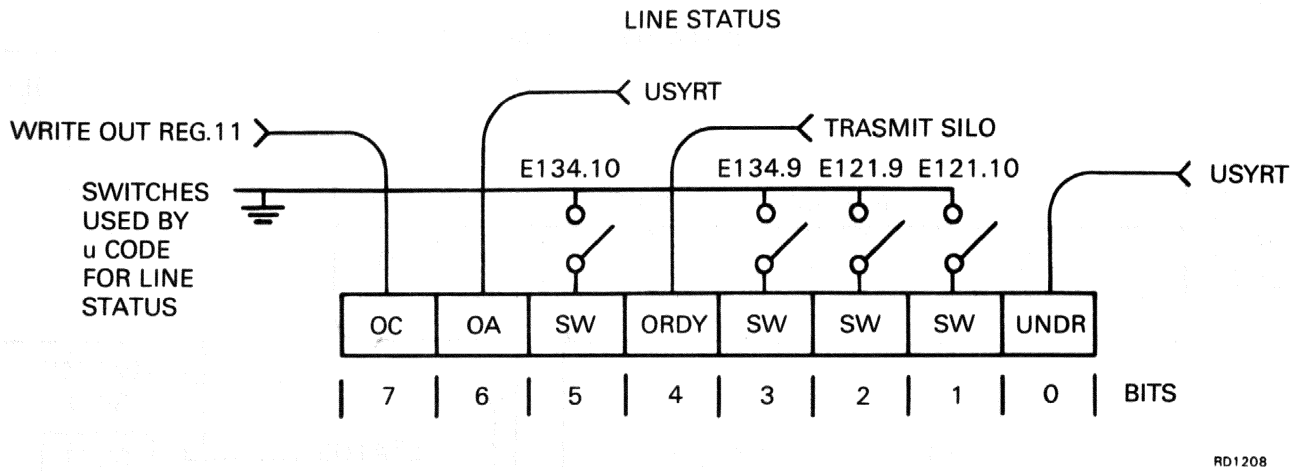


Figure 3-8 IBUS Register 11

3.3.4.4 OBUS REGISTER 11 – Write operation:

1. Bits 0 to 3 are loaded into the silo before register 10 loads the silo. They are used to transmit characters or the Cyclic Redundancy Check (CRC).

   Bit 0 = Start Of Message (SOM) – Used to transmit flags (01111110) in bit-oriented protocol, or is loaded with a sync character to set up the transmitter and receiver for data that is to follow.

   Bit 1 = End of Message (EOM) – Used to send the CRC character, if CRC is enabled in both protocols, and the trailing flag or sync character.

   NOTE

   A minimum of two SOMs must be sent at the start of a character oriented message.

   Bit 2 = Send Abort – Used in bit-oriented protocol (11111111).

   Bit 3 = Send Go-Ahead – Used in bit-oriented protocol only (01111111).

2. Bit 7 = Clear the Transmit Circuitry – Out Clear (OC) (IBUS register 11) must be 0 before loading the transmitter.

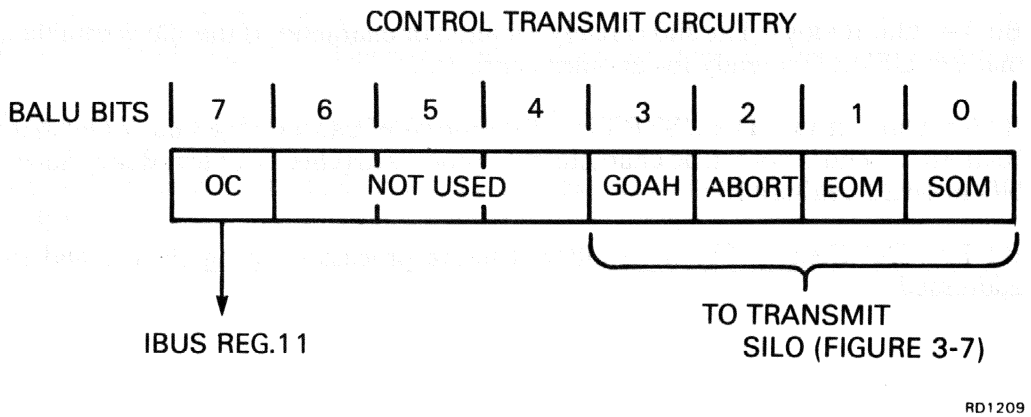


Figure 3-9 OBUS Register 11

3.3.4.5 IBUS REGISTER 12 – Read operation:

1. Bits 0 to 3 = Status of USYRT (data character in IBUS register 10) – When IBUS register 10 is read bits 0 to 3 are updated to the next character.

   Bit 0 = Block Check Character (BCC) Match – Only valid at the end of the message or after the last data character (bit-oriented protocol when EOM is set).

   NOTE

   A one means correct CRC, or match in character oriented protocol. A zero means correct CRC, or match in bit-oriented protocol.

   Bit 1 = End of Block (in bit-oriented protocol) – Indicates End of Message and BCC Match is valid.

   Bit 2 = Received Abort (in bit-oriented protocol) – Seven ones have been received.

   Bit 3 = Receiver Overrun – Data is not being removed fast enough from the receiver silo, meaning data for this message is not valid and should be discarded. OVRR will clear when the receiver is cleared (IC).

2. Bit 4 = In Ready – The next character is ready to be read from the receiver silo. If the silo is disabled, a character is ready to be read from the USYRT.

3. Bit 5 = LULP – This bit is internal to the USYRT. Do not mistake it for the line unit loop set in the microprocessor CSR 0, which is a loop back mode that is external to the USYRT. If RUN is set on the microprocessor:

   a. The USYRT is run at 24K bits/s
   b. If it is not set, the clock is generated from the Step Line Unit bit 12 of CSR0.

4. Bit 6 = Receiver Active – The receiver has started to process data. The carrier bit M in IBUS register 13 must be set or the receiver will not become active.

5. Bit 7 = In Clear – The receiver circuit of the USYRT and the silos are in the process of being cleared.

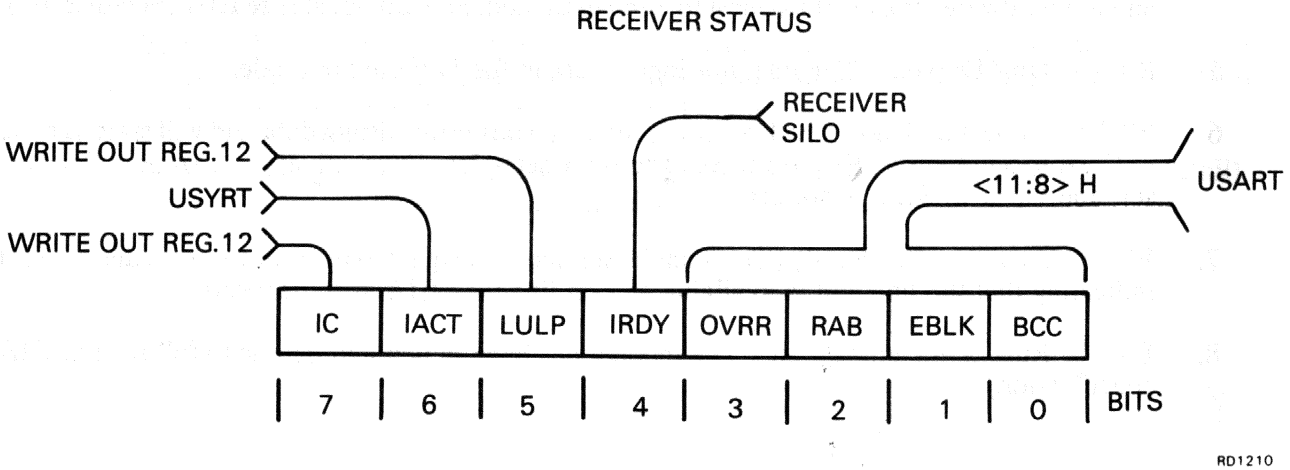


Figure 3-10 IBUS Register 12

3.3.4.6 OBUS Register 12 – Write operation:

1. Bit 5 = Line Unit Loop – Enables the maintenance mode of the USYRT, which loops the data back internally to the USYRT. Selects internal clock if RUN is set or Step Line Unit if RUN is not set.

2. Bit 7 = Clear the Receiver Circuit of the USYRT (silos also cleared) – Used to clear the receiver CRC in byte-oriented protocol.

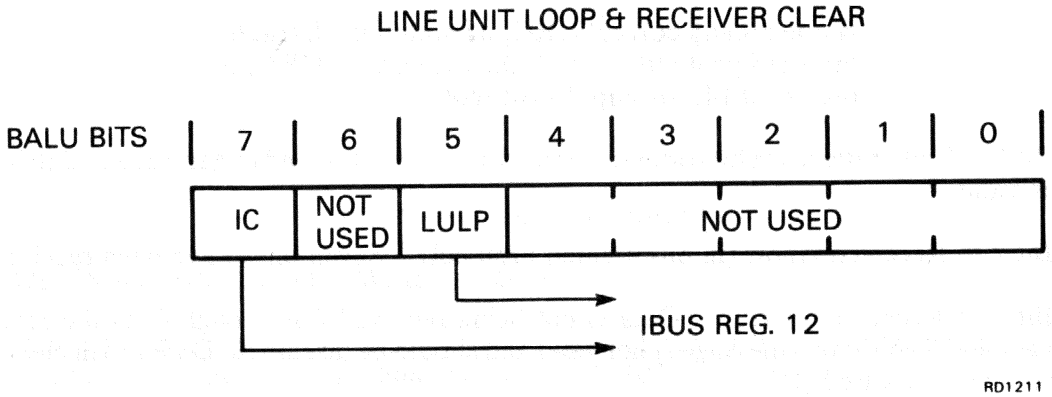


Figure 3-11 OBUS Register 12

3.3.4.7 IBUS Register 13 – Read operation:

1. Bit 0 = Carrier (Receiver Ready) – Indicates that the integral modem or modem interface is active. The carrier signal must be set before the USYRT receiver processes characters. The carrier is used by the USYRT to clear the CRC registers between messages.

2. Bit 1 = Standby – References the standby indication from the modem (see EIA specification).

3. Bit 2 = Clear to Send – A response from the modem used by hardware to start sending data. Clear to Send must be low for Request to Send to set. With the integral modem, a 100 microsecond delay occurs before Clear to Send is set.

4. Bit 3 = Modem Ready (Data Mode) – The modem is in service. Used with the modem interface and is a hardware lockout of Request to Send until modem ready is set (see EIA specification).

5. Bit 4 = Half-Duplex – The line unit logic is set in the half-duplex mode.

6. Bit 5 = Request to Send – The USYRT is ready to start transmitting data and will start as soon as Clear to Send is true. Request to Send does not set unless Out Active is set, Modem Ready is set, and Clear to Send is not set.

7. Bit 6 = Data Terminal Ready (Terminal in Service) – A signal to the modem from the line unit indicating that the line unit is available and on line (see EIA specification).

8. Bit 7 = Ring or Incoming Call – The modem has been dialed and data is to follow (see EIA specification).

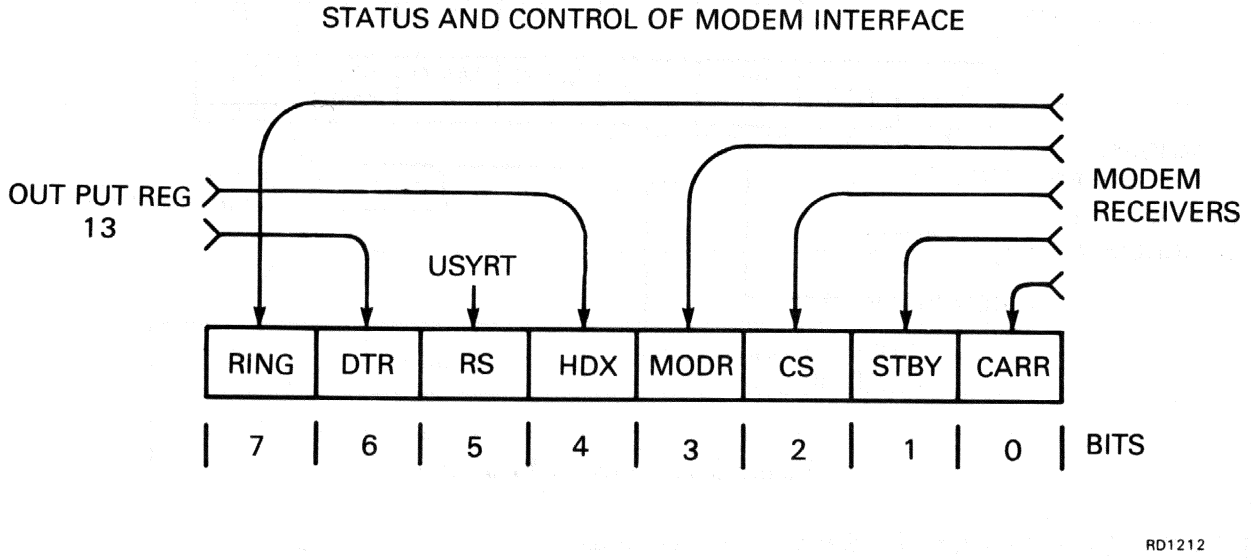


Figure 3-12 IBUS Register 13

3.3.4.8 OBUS Register 13 – Write operation:

1. Bit 1 = Select Standby – Used when a modem interface is used (see EIA specification).

2. Bit 2 = Maintenance Mode 2 – Remote loopback using the modem interface and the external modem. It is used to test the modem (see EIA specification).

3. Bit 3 = Maintenance Mode 1 – Local loop using the modem interface and the external modem. Tests the interface to the modem (see EIA specification).

4. Bit 4 = Half-Duplex – Sets the line unit in the half-duplex mode. The line unit either transmits or receives at any given time (hardware interlocked controlling the line unit).

5. Bit 5 = Select Frequency – Used on the modem interface to change modem data rates (see EIA specification).

6. Bit 6 = Data Terminal Ready (Terminal Ready) – Indicates to the modem that the line unit is ready to receive or transmit data. It must be set when the modem interface is used, otherwise the modem ignores other control signals from the line unit.

7. Bit 7 = Polling – A new function for RS-422, RS-423 and RS-449 (not defined in detail). It is planned to be used with multidrop modems.

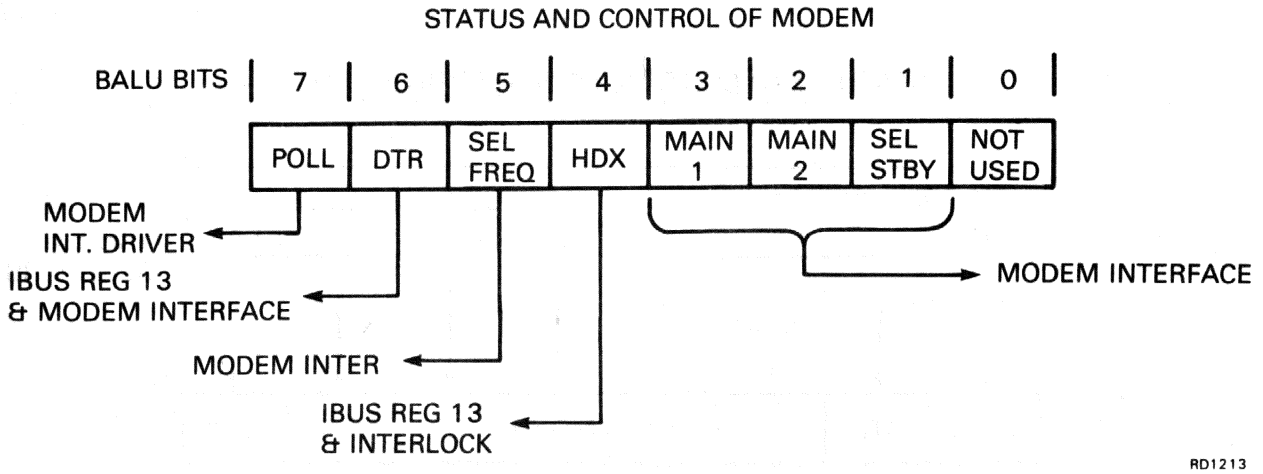


Figure 3-13 OBUS Register 13

3.3.4.9 IBUS Register 14 – Read/write operations:

NOTE

Sync character or secondary address must be loaded through the extended registers. Register 14 is used for extended register control.

1. Bit 0 = Extended Address Bit 1 – Used to select the USYRT register that is being written to or read from.
2. Bit 1 = Extended Address Bit 2
3. Bit 2 = Enables extended registers – Starts the extended operation when set.
4. Bit 3 = Select a write operation – This is done through the extended registers.
5. Bit 4 = Selects a read operation – This is done through the extended registers.
6. Bit 5 = Disable the silos — This is done so that the USYRT can be loaded and read directly.
7. Bit 6 = Transmitter Enable — Must be set before characters are loaded into the USYRT when the line unit is programmed with the silos disabled. When the silo is enabled, keep Request to Send set.
8. Bit 7 = Ready (Read only) – The operation executed through the extended registers is completed. Other bits in registers 14, 15 and 16 should not change unless the Ready bit is set.

The normal operation using extended registers:

1. Extended address must be loaded first.
2. If a write, data must be loaded in write out (OBUS) registers 15 and 16. Set WAX and the enable bit.

3. If a read, set RDAX and the enable bit.

4. The operation is complete when bit 7 becomes true.

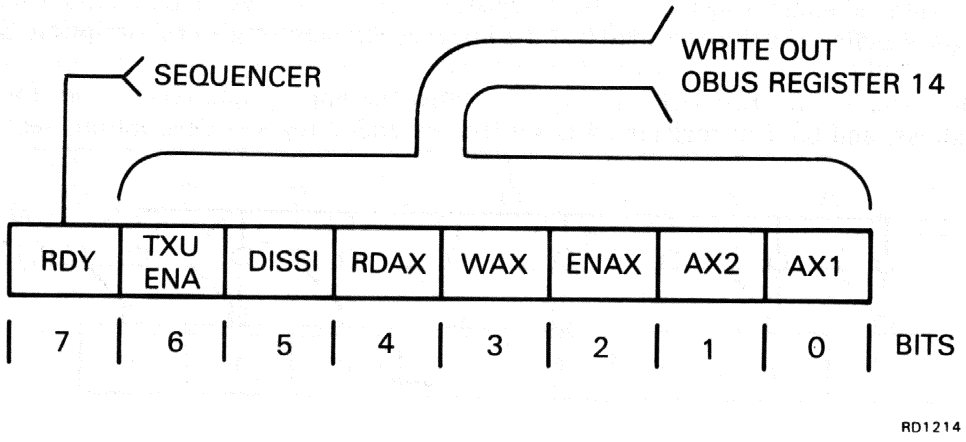


Figure 3-14 IBUS Register 14

3.3.4.10 OBUS Register 14 – Read/Write operations:

Refer to Figure 3-15 for bit definitions.

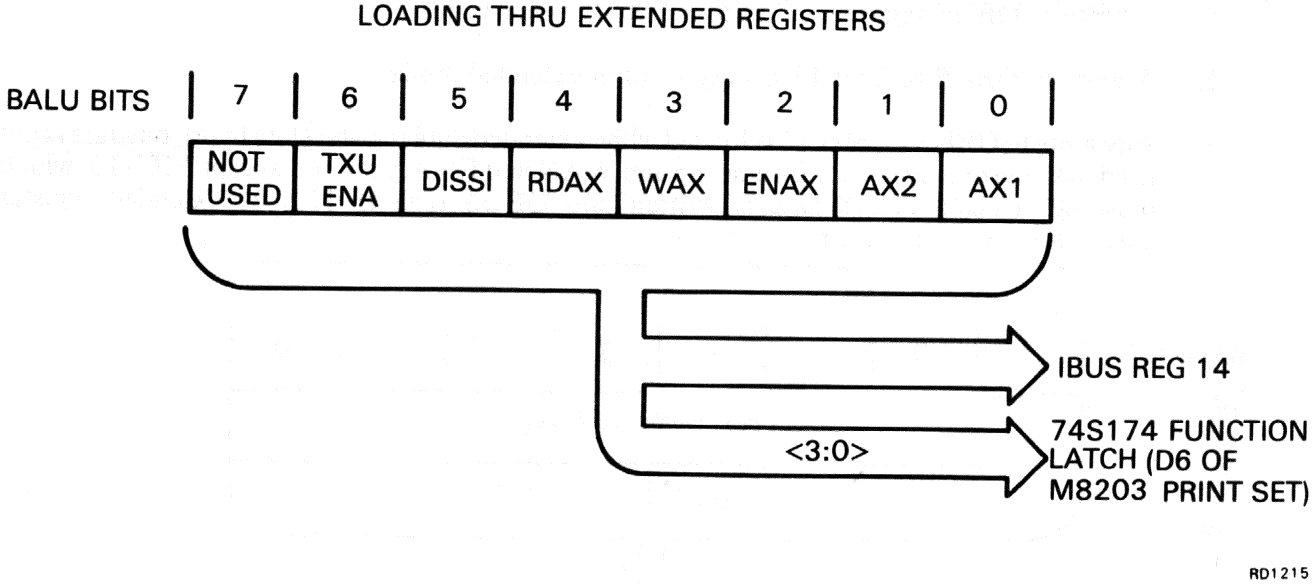


Figure 3-15 OBUS Register 14

3.3.4.11 IBUS Register 15 – Read operations:

1. A normal read from register 15 is from a switch pack defined by microcode. Refer to the appropriate option technical manual.

2. In extended addressing mode, IBUS register 15 is the low byte of data read from the extended register defined by the extended address bits (see extended register description, Section 3.3.4).

3. The extended address data is only true when the appropriate bits are set for the extended address, and bit 7 of register 14 is set (see extended register description, Section 3.3.3).

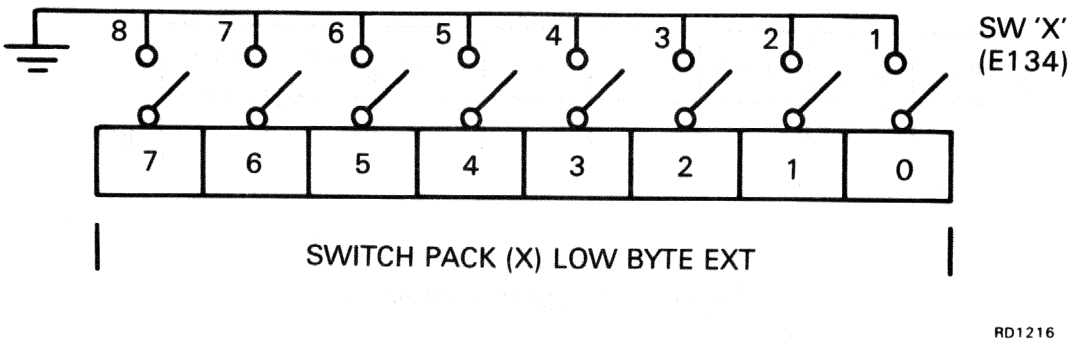


Figure 3-16 IBUS Register 15

3.3.4.12 OBUS Register 15 – Write operation:

1. A write to OBUS register 15 in normal mode is not valid.

2. A write to OBUS register 15 is only valid in extended mode.

3. Any write to OBUS register 15 is loaded in the extended data register (low byte), but data is not used until the extended address is set up and WAX and ENAX are set, except AX3-15, which must be selected before data is written into OBUS register 15 (see extended register description, Section 3.3.5).

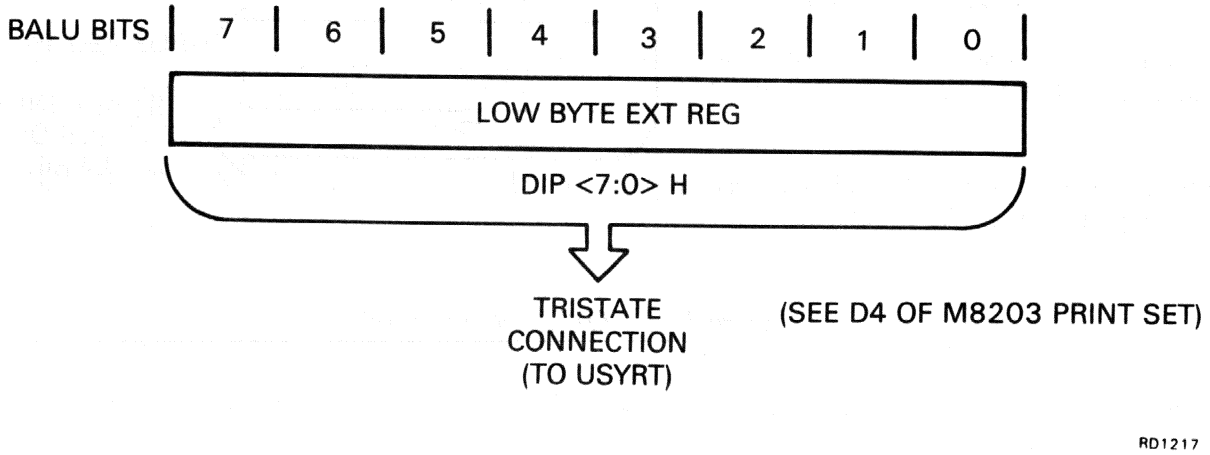


Figure 3-17 OBUS Register 15

3.3.4.13 IBUS Register 16 – Read operation:

1. Similar to register 15
2. A normal read is from the switch pack defined by microcode.
3. In extended mode, the register is the high data byte for extended addressing whose data is only valid when bit 7 of register 14 is set (refer to extended register description Section 3.3.5).

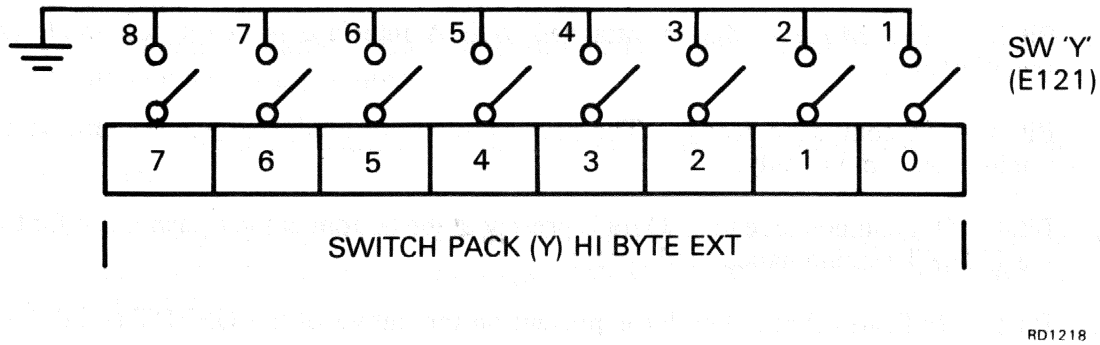


Figure 3-18 IBUS Register 16

3.3.4.14 OBUS Register 16 – Write operation:

1. A write to register 16 loads data only into the data register for the extended addressing function.
2. The data is used after the address is set up and WAX and ENAX are set (refer to extended register description, Section 3.3.5).

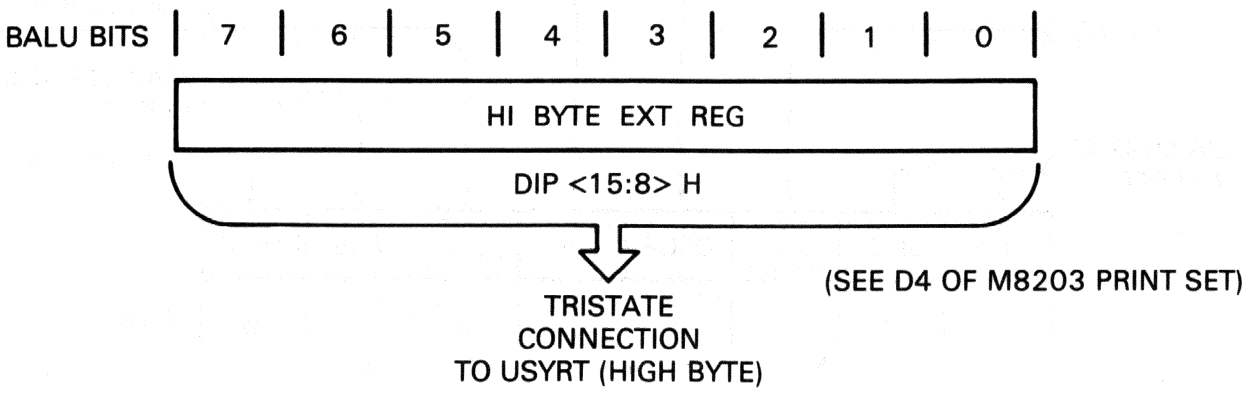


Figure 3-19 OBUS Register 16

3.3.4.15 IBUS Register 17 – Read operations:

1. Bit 0 = line unit mode

   0 = Bit-oriented protocol

   1 = Character-oriented protocol (initializes to a 1)

2. Bit 1 = Maintenance clock step line unit or 24 KHz

3. Bit 2 = Test Mode – Modem attached to EIA interface is in the test mode (see EIA specification).

4. Bit 3 = In composite ready – The receive silos are ready to receive another character (maintenance mode only).

5. Bit 4 = Out composite ready – Data is present at the bottom of the transmit silo for transfer to the USYRT (maintenance mode only).

6. Bit 5 = Indicates that a data bit is present on the output of the USYRT serial data stream (maintenance mode only).

7. Bit 6 = Signal quality indication – This comes from the EIA modem interface (see EIA specification).

8. Bit 7 = Signal rate – This comes from the EIA modem interface (see EIA specification).

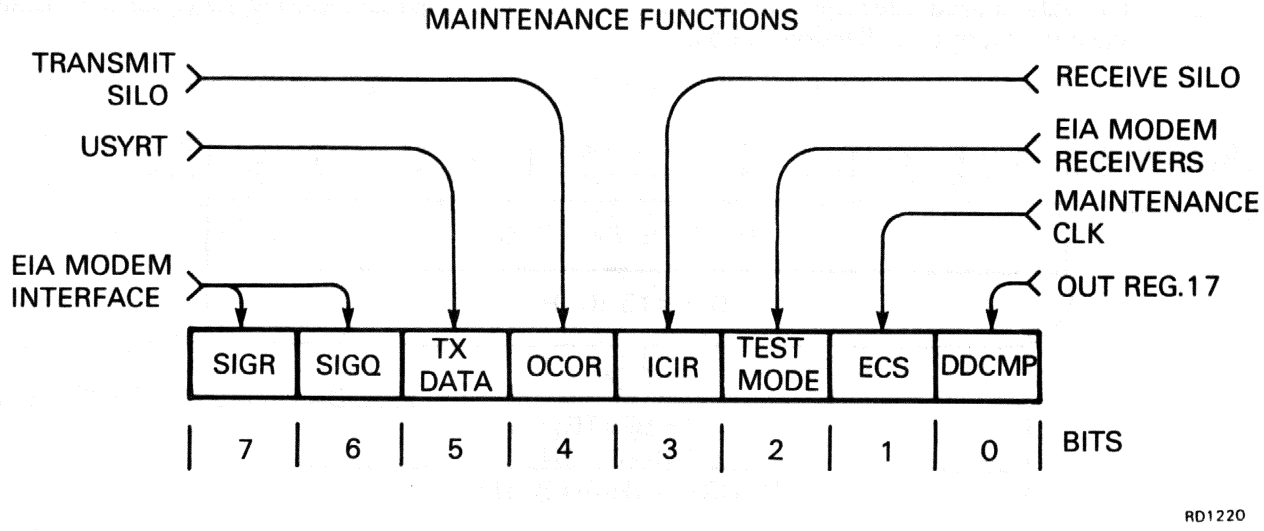


Figure 3-20 IBUS Register 17

3.3.4.16 OBUS Register 17 – Write operation:

1. Bit 0 = Mode of line unit – Initializes to a 1.

   1 = Character-oriented protocol

   0 = Bit-oriented protocol

2. Bit 1 = Insert error – Used when line unit loop is set in microprocessor CSR. All bits are shifted into the USYRT when this bit is set to 1.

3. Bit 2 = Read All Parties – Used in bit-oriented protocol, all parties address (11111111), and the normal secondary address.

4. Bit 3 = Strip sync character – Used in character-oriented protocol, after the first two characters.

5. Bit 4 = Secondary address mode for bit-oriented protocol – Enables auto detection of the secondary address, and accepts messages with its secondary address, or the all parties address if bit 3 is set.

6. Bit 5 = Idle – Uses the 23038B1 ROM, which normally sets idle in the USYRT (sync characters must be loaded by the microprocessor). With idle clear the USYRT will MARK when underrun occurs.

7. Bit 6 and 7 = Determine the type of error checking being used:

Bits	Character-oriented	Bit-oriented
7 6	Protocol	Protocol
0 0	CRC 16	CCITT 16 (Initialized to one)
0 1	Odd vertical parity	CCITT 16 (Initialized to zero)
1 0	Even vertical parity	Not used
1 1	No error checking	No error checking

Register 17 initializes to character-oriented protocol with CRC 16.

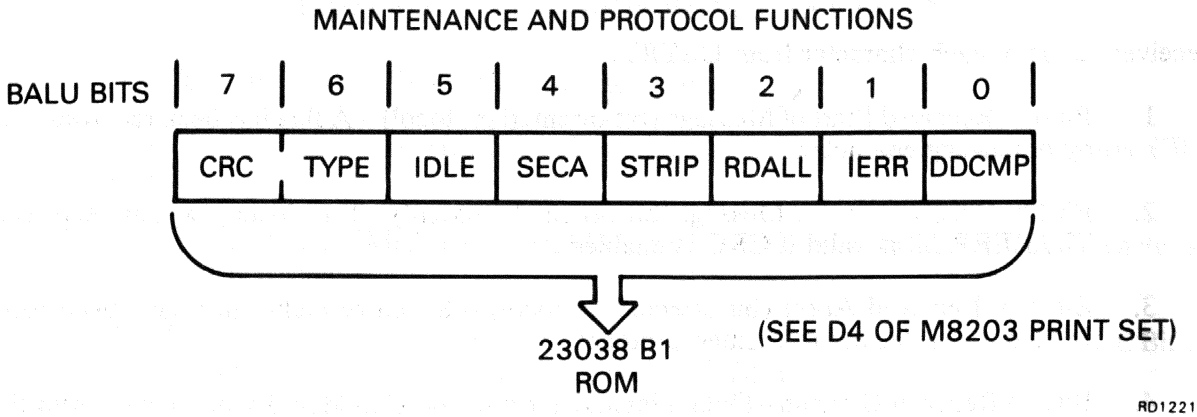


Figure 3-21 OBUS Register 17

3.3.5 Extended Registers/Indirect Addressing

Indirect addressing is used to address the USYRT directly, thereby bypassing the silos and standard hardware to run special protocols and variable word lengths. Indirect addressing is done by setting up address AX in OUT/IBUS register 14, then the data in extended registers 15 and 16. The procedure is shown in the following three steps:

1. Extended address must be loaded first.
2. For a write operation, set Enable AX and WAX. Data must be loaded in OBUS registers 15 and 16.
3. For a read operation, set Enable AX and RDAX.

When bit 7 of IBUS register 14 is set, the operation is complete. Figures 3-22 to 3-29 provide the write IBUS/OBUS register bit descriptions and qualifications for read operations.

3.3.5.1 AXO-15 Register – Read only:

1. Receiver data is directly from the USYRT.
2. The silo must be disabled (DISSI must be set).
3. Set RDAX and Enable AX.
4. IBUS register 15 is the low byte of the data read from AX0-15 as defined by the extended address bits.
5. The operation is complete when Ready bit 7 (IBUS register 14) becomes true.

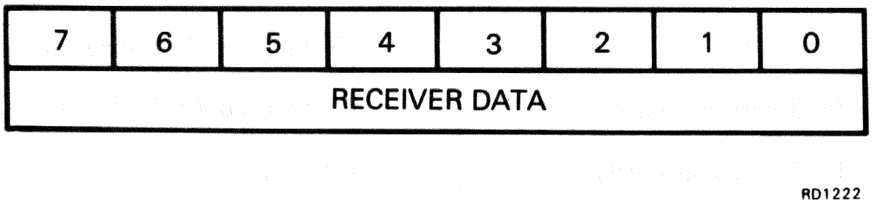


Figure 3-22 IBUS Register AX0-15

3.3.5.2 AXO-16 Register – Read only:

Receiver status of each character from USYRT.

1. Bit 0 = Received Start of Message (bit-oriented protocol) – A flag has been received followed by a non-flag character.
2. Bit 1 = Received End of Message (bit-oriented protocol) – The closing flag has been received. The RERR bit is valid if CRC is enabled.
3. Bit 2 = Received Abort (bit-oriented protocol) – Seven or eight ones have been received. Invalid character in bit-oriented protocol.
4. Bit 3 = Receiver Overrun – Data is invalid, the message should be discarded indicating that the data characters have not been removed fast enough.

5. Bits 4, 5, 6 = Number of bits assembled in the last data character – This occurred when the closing flag was received (used in variable length bit-oriented protocol).

6. Bits 7 = Receiver Error (BCC match or parity error) – Valid with the last character when CRC is enabled. A one indicates an error in bit-oriented protocol.

USYRT bits <15:8> are interpreted (seen) by the microprocessor as line unit bits <7:0>.

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8
RERR	BITS	ASSEMB		ROR	RAB	REOM	RSOM

LINE UNIT BITS

RD1223

Figure 3-23 IBUS Register AX0-16

3.3.5.3 AX1-15 Register – Read/Write:

1. Transmit data loaded into USYRT should only be used with the silos disabled (DISSI) and only read when the clock is disabled as a maintenance function.

2. With the silos disabled, OUT RDY Bit 4 (ORDY) in IBUS register 11 indicates when the next register can be loaded into AX1-15.

3. AX1-15 should not be read unless IN RDY Bit 4 of IBUS register 12 is set.

4. IBUS register 16 is the high byte of the data read from AX1-15.

7	6	5	4	3	2	1	0
TRANSMIT DATA							

RD1224

Figure 3-24 IBUS/OBUS Register AX1-15

3.3.5.4 AX1-16 Register – Read/Write (Transmitter Control):

1. Bit 0 = Transmit Start of Message - Generates sync or flag character and starts CRC computation.

2. Bit 1 = Transmit End of Message – Ends CRC generation, transmits CRC 16-bit character and flag or sync character.

3. Bit 2 = Transmit Abort (bit-oriented protocol) – Transmits an abort character if IDLE Bit 5 of OBUS register 17 is cleared, or flag character if IDLE is set.

4. Bit 3 = Transmit Go Ahead – A special bit for bit-oriented protocol (0111111).

5. Bit 7 = Transmitter Underrun (read only) = Characters have not been provided to the transmitter fast enough.

USYRT bits <15:8> = line unit bits <7:0> as seen by the microprocessor.

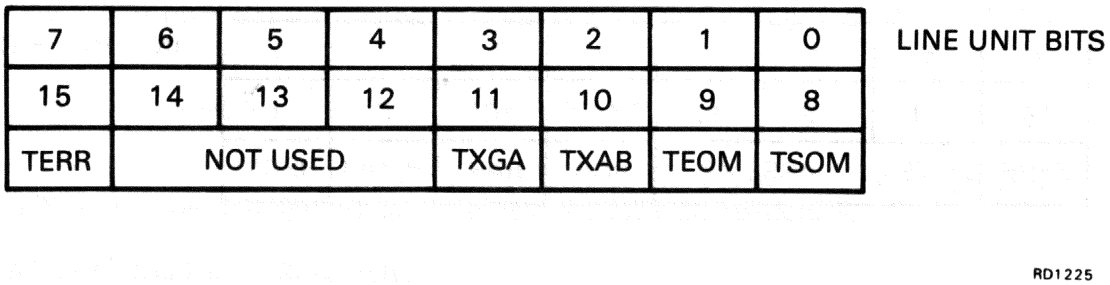


Figure 3-25 IBUS/OBUS Register AX1-16

3.3.5.5 AX2-15 Register – Read/Write: Contains the sync character in character-oriented protocol, or secondary address for bit-oriented protocol.

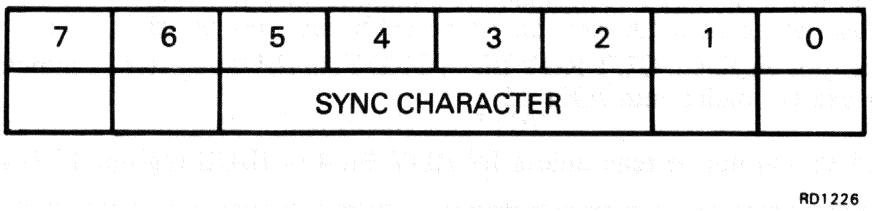


Figure 3-26 IBUS/OBUS Register AX2-15

3.3.5.6 AX2-16 Register – Read: (Functions are set via OBUS register 17.)

1. Bit 2, 1, 0 = CRC/Error Checking

Bits 2 1 0	Character-oriented Protocol	Bit-oriented Protocol
0 0 0	–	CCITT 16 initialized to a one
0 0 0	–	CCITT 16 initialized to a zero
0 1 0	Not used	Not used
0 1 1	CRC 16	–
1 0 0	Odd parity	–
1 0 1	Even parity	–
1 1 0	Not used	Not used
1 1 1	No error checking	No error checking

2. Bit 3 = Idle – Determines what will be sent when an underrun occurs or when Transmit Abort Bit 2 of AX1-16 is set (0 = marks are sent, 1 = flags or syncs are sent in transparent modes, usually run with CRC disabled).

3. Bit 4 = Secondary address enable for bit-oriented protocol

4. Bit 5 = Strip sync characters for character-oriented protocol

5. Bit 6 = 1 for character-oriented protocol = 0 for bit-oriented protocol

6. Bit 7 = Receive all parties (SEC address 377)

7	6	5	4	3	2	1	0
15	14	13	12	11	10	9	8
APA	DDCMP	STRIP	SECA	IDLE	CRC TYPE		

LINE UNIT BITS

RD1227

Figure 3-27 IBUS Register AX2-16

3.3.5.7 AX3-15 Register – Read/Write: AX3-15 is a test register for the modem interface and does not affect the USYRT. It is used to:

1. Read which interface is selected, or

2. Select the interface when test connectors are used.

   a. Bit 0 = Select Interface Bit – When in a 1 state, the modem interface is selected by another bit in the register (via 74LS157-D7 of the M8203 print set). Used when H3254 and H3255 test connectors are installed.

   b. Bit 1 = Reserved for fiber optics.

   c. Bit 2 = Enables CRC 32 chip if installed (E124).

   d. Bit 3 = Integral modem has been selected. *

   e. Bit 4 = V.35 interface selected by appropriate cable if bit 0 is not set (BC05Z cable connected to J1 connector) or if bits 0 and 4 are set (diagnostic selection).

   f. Bit 5 = Enables CRC 32 BCC match, if installed.

   g. Bit 6 = EIA single-ended (unbalanced) interface – Includes RS-232-C and RS-423 (default when bit 0 is not set, true when bits 0 and 6 are set).

   h. Bit 7 = RS-422 Differential (balanced) interface – Must be switch selected in normal mode.

NOTE

Selects the maintenance function when bit 0 is set and reads back true for the function selected.

* Bit 3 – Write when bit 0 is set, selects the integral modem. Does not select speed or filter for the integral modem. The correct cable or test connector must be used and correct data rate must be selected by switch pack number E39, switches 8, 9 and 10.

BALU

	7	6	5	4	3	2	1	0
USYRT REG	422	XYZ	BCC C32	V.35	INT	EN C32	0	TEST

MODEM INTERFACE

RD1228

Figure 3-28 IBUS/OBUS Register AX3-15

3.3.5.8 **AX3-16 Register – Read/Write:** AX3-16 is for special protocols controlled by the USYRT (directly address the USYRT). When the module is initialized, zero is loaded into the register.

1. Bits 2, 1, 0 = Receiver character length control bits – 001 through 111 are the number of bits for special protocols. 000 is for standard eight-bit character.
2. Bit 3 = Receiver character length enable
3. Bit 4 = Transmitter character length enable
4. Bit 7, 6, 5 = Transmitter character length control bits – 001 through 111 are the number of characters for special protocols 000 is for standard eight-bit character.

USYRT bits <15:8> line unit bits <7:0> as seen by the microprocessor.

7	6	5	4	3	2	1	0	LINE UNIT BITS
15	14	13	12	11	10	9	8	
TX CH LENGTH			TX CLE	RX	REC CH LENGTH			

RD1229

Figure 3-29 IBUS/OBUS Register AX3-16

CHAPTER 4
SERVICE

4.1 SCOPE

Although servicing the KMS11-P is done automatically by the diagnostic programs, this chapter details the KMC11 programming in order to give the reader a complete view of the functions implemented during maintenance operations. Also included are the maintenance philosophy, maintenance functions, preventive maintenance, and corrective maintenance. The section on corrective maintenance contains short descriptions of the diagnostics of the KMS11-P.

4.2 MAINTENANCE PHILOSOPHY

The Field Replaceable Unit (FRU) for the KMS11-P is either a defective module or cable. Training of field service personnel should be applied to functional and application troubleshooting, using diagnostics, for fault isolation to the FRU.

CAUTION

When inserting or removing the M8206 microprocessor module, make sure the priority plug is not disconnected.

4.3 MAINTENANCE FUNCTIONS/MAINTENANCE MODES

The maintenance functions are available to the KMS11-P via the maintenance control and status register (CSR)(BSEL 1). Maintenance and system tests make up the maintenance modes.

4.3.1 Maintenance Register (BSEL 1)

This register contains the high byte of address 76XXX0. A description of the CSR byte is provided in Chapter 3. The byte format and bit description are also provided in detail in this section.

BSEL 1 contains all maintenance functions, including master clear, and is not designed for normal user communications between the PDP-11 program and the microprocessor. These functions override all other control functions. All bits are read/write. The bit functions of BSEL 1 are as follows:

Bit	Name	Description
8	Step microprocessor	When set, it steps the microprocessor processor through one instruction cycle, which is usually made up of three 60 ns pulses. The Run bit should be cleared before executing this control function.
9	ROM In	When set, it applies the contents of BSEL 6 and 7 as the next microinstruction to be executed by the microprocessor, when Step microprocessor is set.
10	ROM Out	When set, it modifies the source paths for BSEL 6 and 7 to contain the contents of the addressed CRAM. If ROM Out and Step microprocessor are set, then the content of the next CROM address will be output to BSEL 6 and 7.

11	LU Loop (Line Unit Loop)	When set, it connects the serial line OUT of the line unit, back to its serial line IN. This loop back is done at the TTL level before level conversion. When the LU Loop bit is set and the Run bit (bit 15) is cleared, the Step LU clock is the only one available for shifting data in or out. When the LU Loop bit is set and the Run bit is set, data is clocked at 48K bits/s by the maintenance clock. If the LU Loop bit is cleared and the Run bit set, the loop back test connector is needed.

LU Loop	Run	Clock Source	Mode
Set	Clear	Step LU (bit 12 via program	Single-step internal maintenance
Set	Set	Maintenance clock at 48K bits/s	System test internal maintenance
Clear	Set	Maintenance clock determined by rate select SWS	External maintenance

NOTE

The KMS11-P must be set up in full-duplex mode to run in any loopback maintenance mode. For external loopback mode, cable test connectors H325, H3250 or H3251, or module test connectors H3254 or H3255 as needed.

Bit	Name	Description
12	Step LU (Step Line Receiver)	With the Run bit cleared and bit 12 set, the transmitter shifts; when bit 12 is cleared, the receiver shifts. This control function is used with the LU Loop bit 11 to simulate transmit and receiver clocks for line unit maintenance in single step maintenance mode.
13	Not Used	
14	MCLR (Master CLeaR)	When bit 14 is set, MCLR initializes both the microprocessor and the line unit.

15	Run	Run controls the microprocessor clock.

NOTE

These two bits (13 and 14) should never be set together. A restart sequence should proceed as follows:

1. **Clear the Run bit.**
2. **Set the MCLR bit.**
3. **Set the Run bit.**

This makes sure of a restart at location 0.

4.3.2 Maintenance Modes

The KMS11-P microprocessor can be tested in Maintenance mode.

The KMS11-P line unit can be tested by three basic modes:

1. Single step internal maintenance
2. System test internal maintenance
3. External maintenance

4.3.2.1 Maintenance Mode – The Maintenance Mode can be enabled using selected bits of BSEL 1. These can be used to:

1. Halt the microprocessor (clear bit 15)
2. Step the microprocessor (set bit 8)
3. Examine the current CRAM location (assert bit 10 and examine SEL 6)
4. Override the current CRAM instruction with a different instruction and execute the new instruction (load SEL 6 with the new instruction, assert bits 8 and 9, then clear bit 8).

4.3.2.2 Single Step Internal Maintenance Mode – This mode is selected by the user program setting LU Loop and clearing Run bits 11 and 15 of SEL 0. This mode allows for checking most of the line unit without disconnecting the M8203 from the modem. Line unit signal D8 LPBKL is set to keep the transmitter output active, looping the output back at TTL levels to become the receiver input. Line unit Request To Send (RTS) and Data Terminal Ready (DTR) signals are held cleared. The clocking source is the D16 Step LU signal from the microprocessor which becomes D1 Step LU at the line unit. The user program generates the clock signal which sets Step Line Unit bit 12 of SEL 0.

4.3.2.3 System Test Internal Maintenance Mode – This mode is selected by the user program setting Line Unit Loop bit 11 and bit 15 (Run) of SEL 0. This mode allows the program to perform an off-line system test by free-running the KMS11-P and checking the line unit without disconnecting the M8203 from the modem. The transmitter output is looped back at TTL level to become the receiver input. The clock source is the KMS11-P maintenance clock which is 48K bits/s.

4.3.2.4 External Maintenance Mode – External Maintenance Mode is selected by the user program placing the KMS11-P in normal running mode (bit 11 clear and bit 15 set) and terminating the cables with a test connector.

The M8203 options are configured as follows:

1. RS-232-C

   The modem must be disconnected and the H325 test connector must be attached to the BC05D-25 cable.

   Data rate switches (switches 8, 9 and 10 of E39) select the clock rate. This clock signal is looped back in the H325 to simulate modem transmit and receive clocks. The data rate for this application must not exceed 19.2K bits/s.

   Modem control signals are tested for correct level conversion and cable paths. These signals are looped back in the H325 as shown in the signal flow of Figure F-3 view A.

2. CCITT V.35/DDS

   The modem must be disconnected and the H3250 test connector must be attached to the BC17E-25 cable.

   Data rate switches (8,9 and 10 of E39) select the clock rate. This clock signal is looped back in H3250 to simulate modem transmit and receive clocks.

   Modem control signals are tested for correct level conversion and cable paths. These signals are looped in the H3250 as shown in the signal flow of Figure F-3 view B.

3. RS-422-A; RS-423-A

   The modem is disconnected and a H3251 test connector is attached to the BC55D-33 cable.

   Data rate switches (8, 9 and 10 of E39) select the clock rate. This signal is looped back through the H3251 to simulate modem transmit and receive clocks.

   Modem control signals are tested for correct level conversion and cable paths. These signals are looped in the H3251 as shown in the signal flow of Figure F-3 view C.

4.3.3 Maintenance (LED) Indicators

Six light emitting diodes (LEDs) are installed on the M8203 line unit to permit a visual check of certain conditions. Five of these apply specifically to modem conditions. The other LED (D15) shows the functional conditions of the KMS11-P. Figure 4-1 identifies the physical locations of these LEDs. Description of each indication is as follows:

LED	Name	Description
D10	Signal Quality	A signal from the modem that indicates the presence or absence of the carrier. Usually, when this signal is ON it indicates the presence of the carrier and OFF indicates an absence of the carrier.
D11	Carrier	Indicates that the carrier is present at the receiver.
D12	Receiver Data	When ON, indicates that a steady stream of '1's are being received.
D13	Transmit Data	When ON, indicates that a steady stream of '1's are being transmitted.
D14	Request to Send	When ON, indicates that the USYRT is ready to start transmitting as soon as Clear to Send is detected.
D15	Heartbeat	At master clear time, this indicator is OFF. When the KMS11-P asserts the Run bit, this indicator will go ON and stay ON.

4.4 PREVENTIVE MAINTENANCE (PM)

There is no specific KMS11-P PM schedule. A general check of voltages and connections should be done when system PM is performed. After working on the KMS11-P modules or cables, a complete checkout of the device should be done by running all diagnostics.

4.5 CORRECTIVE MAINTENANCE ON A PDP-11 PROCESSOR

All corrective diagnosis should be applied to the isolation of the failing FRU, because the FRU is either a module or cable. KMS11-P diagnostics are designed to help in the isolation process, and should be run starting with the basic microprocessor test and continuing to the interprocessor test. The correct sequence of the diagnostics is:

Diagnostic	Description
CZKMB	M8206 Static Diagnostic 1
CZKMC	M8206 Static Diagnostic 2
CZDMR	M8203 Static Diagnostic 1
CZDMS	M8203 Static Diagnostic 2
CZKMR	KMS11-P Functional Diagnostic

4.5.1 CZKMB/CZKMC

These diagnostics test the M8206 microprocessor in two parts and use the diagnostic supervisor. Through interaction with the operator, the program allows modification of device parameters, such as the UNIBUS address, vector address, and processor type.

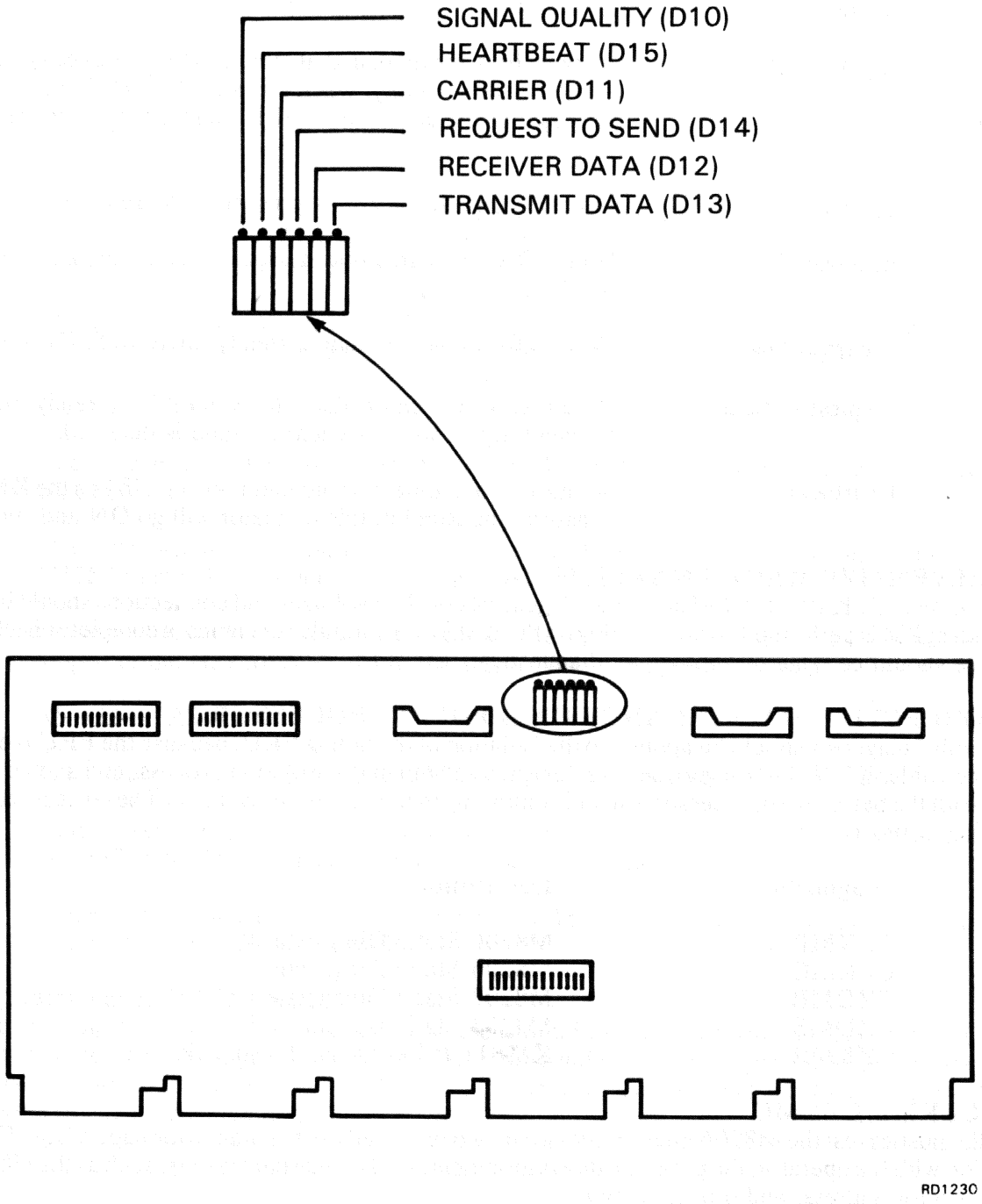


Figure 4-1 M8203 Maintenance LED Locations

These programs are compatible with the standalone version of the diagnostic supervisor. They are also compatible with ACT, APT, XXDP+, and SLIDE. They must be loaded co-resident with the diagnostic supervisor, or be previously combined with the DS and loaded as a single file. In either condition, the combined program will not exceed 16K of memory. Refer to Appendix B for details on the diagnostic supervisor.

The total time needed to run M8206 static tests is from 30 seconds to 2 minutes per pass, depending on the CPU type.

CZKMB/CZKMC are compatible with XXDP+,ACT/SLIDE and APT. XXDP+ and ACT/SLIDE may be run in dump or chain modes. APT can be run in program or script modes.

Memory management is not used in this program and, if installed, it is disabled. If parity memory is installed, memory parity traps are disabled. These diagnostics test the M8205 microprocessor in two parts and use the diagnostic supervisor. Through interaction with the operator, the programs permit modifications of device parameters such as the UNIBUS address, vector addresses and the device priority. The operator can specify specific tests to be run and a variety of looping, running, and reporting modes. Refer to Appendix B for details on the diagnostic supervisor.

An error log keeps a record of the number of errors which have occurred on each device under test, following the last start or restart command. The log may be printed by using the print command.

A summary of the tests performed are listed in Tables 4-1 and 4-2. All tests support the KMC11-B. For more detail, refer to the diagnostic listings.

Table 4-1 CZKMB Diagnostic Summary

Test Number	Description
1	Verify that referencing UNIBUS device registers does not cause a trap.
2	Verify that Run bit can be cleared
3	UNIBUS register word, dual addressing test
4-8	Control status register write/read test
9	Port 4 register write/read test
10	Port 6 register write/read test
11	UNIBUS register byte, dual addressing test
12	Maintenance instruction register test
13	Microprocessor test
14-29	Microprocessor IBUS/IBUS* register write/read tests
30-31	Microprocessor IBUS/IBUS* dual address test
32	Test the delay on pass 1 and report its value
33	Microprocessor BR register test
34	Scratchpad test
35	Scratchpad dual addressing test
36-37	Interrupt tests
38-39	Priority interrupt tests
40-42	NPR tests
43-44	Test of extended address (EA) bits 16 and 17
45-46	NPR non-existent memory test
47	NPR test
48	ALU C-bit test
49-80	ALU tests

Table 4-2 CZKMC Diagnostic Test Summary

Test Number	Description
1	Verify that referencing UNIBUS device registers does not cause a timeout.
2	BR right shift test
3,4	IOP CRAM write/read test
5	IOP CRAM dual addressing test
6,7	IOP main memory test
8	IOP main memory dual addressing test
9	IOP MAR test (4K main memory)
10	IOP (CRAM) ODT bits test
11-24	CRAM tests of Jump(i)
25	4K Main memory page dual address test
26	Jump Field, page test
27	Jump test
28	Z bit test
29	C bit test
30	Program clock bit test
31	Force Power Fail test
32	Microprocessor noise test
33	NODST instruction test
34	Extended CRAM test
35	Microcode test
36	Negative address test
37	Byte addressing test
38	PC register test
39	Branch Field H test
40	Scratchpad 0 (SP0) selection test
41	MOV INST H signal test
42	Master Clear test

4.5.2 CZDMR and CZDMS

These diagnostics perform static tests of all M8203 logic. These include:

1. Line unit register addressing
2. USYRT addressing
3. Static bit interaction and read/write logic tests
4. Basic transmitter, receiver sequencing and data buffering
5. Static operations in character and bit-stuffing modes.

In addition, data messages are sent on the line unit at TTL level, or through an external test connector with a specific modem interface selected.

Static and functional tests provide troubleshooting capabilities such as tight scope loops, switch options, and the ability to lock on intermittent errors. These programs are compatible with the standalone version of the diagnostic supervisor. They are also compatible with APT, ACT XXDP+ and SLIDE.

Through interaction with the operator, the diagnostic supervisor permits modification of device parameters such as the UNIBUS address, vector addresses and device priority. The operator can name specific tests to be run and also a variety of looping, running and reporting modes.

A summary of the tests performed are listed in Tables 4-3 and 4-4. For more detail, refer to the diagnostics listings.

Table 4-3 CZDMR Diagnostic Summary

Test Number	Description
1	Microprocessor CSR addressing test (SEL 0)
2	Inbus/Outbus register 14 initialization test
3	Inbus/Outbus register 14 read/write bit test
4	Register 14 Master Clear test
5	Register 14 UNIBUS reset (INIT) test
6	Line unit false selection test
7	Inbus register Master Clear test
8	Register 10-17 addressing test
9	Register 11 read/write bit test
10	Register 12 read/write bit test
11	Register 13 read/write bit test
12	Register 17 read/write bit test
13	Maintenance clock bit test
14	Extended register Master Clear test
15	Extended register addressing test
16	Registers 15, 16/AX2-15, AX2-16 read/write bit test
17	AX0-15, AX0-16 read/write bit test
18	AX1-15, AX1-16 read/write bit test
19	AX3-15, AX3-16 read/write bit test
20	Register 17 AX2-16 read/write, Master Clear test
21	Transmitter buffer data test
22	Transmitter buffer sequencing test
23	TX MSG timing test, character mode with CRC
24	TX MSG timing test, bit mode with CRC
25	TX MSG timing test, character mode with no CRC
26	TX UNDERRUN set and clear test, character mode
27	TX character length timing test, character mode with CRC
28	TX character length timing test, bit mode with CRC
29	TXDATA bit test, character mode with no CRC
30	USYRT RCV MSG test, character mode with CRC
31	USYRT RCV MSG test, bit mode with CRC
32	USYRT RCV MSG test, character mode with no CRC
33	USYRT RCV MSG test, bit mode with no CRC
34	Silo-disabled transmitter load test
35	Silo-disabled MSG test, bit mode with no CRC
36	RCV buffer test, character mode with CRC
37	RCV character length timing test, character mode with no CRC
38	RCV character length timing test, bit mode with no CRC
39	TX UNDERRUN error, idle marking character mode with no CRC
40	MSG termination with Go Ahead (GA) characters, bit mode with no CRC
41	Idle SYNC test, character mode
42	STRIP SYNC test

Table 4-4 CZDMS Diagnostic Summary

Test Number	Description
1	Bit stuffing test
2	RCV OVERRUN error, set and clear test
3	Abort sequence test
4	Abort and idle flags test
5	TX underrun error, idle abort characters, bit mode
6	RCV disable test
7	Assembled bit count test
8	Secondary station address bit test
9	All parties address bit (RDALL) test
10	Insert error bit (IERR) test, character mode with no CRC
11	Switch pack printout and test
12	Register AX3-15 printout
13	CRC generation test
14	CRC error detection test
15	VRC parity generation test
16	VRC error detection test
17	Integral modem interface test, character mode with CRC
18	V.35 modem interface test, character mode with CRC
19	RS-232-C and RS-423-A modem interface test, character mode with CRC
20	RS-422-A modem interface test, character mode with CRC
21	Half-duplex bit (HALF DUPX) test
22	Half-duplex RCV disabled test, with silos disabled
23	Interaction of modem control bits
24	Data test, bit mode with no error detection
25	Data test, character mode with no error detection
26	Data test, bit mode with CRC-CCITT-1 error detection
27	Data test, bit mode with CRC-CCITT-0 error detection
28	Data test, character mode with CRC-16 error detection
29	Data test, character mode with ODD VRC error detection
30	Data test, character mode with EVEN VRC error detection
31	Contiguous ones in secondary station address mode, bit mode
32	DDCMP MSG test, character mode

4.5.3 CZKMR

CZKMR diagnostic performs testing on the KMS11-P in a functional way, to verify its correct operation under microcode controlled use of the HDLC protocol. This includes the use of the microprogram loading and check command, data pattern generation, interrupt testing, and interrupt driven exercises.

Table 4-5 CZKMR Diagnostic Summary

Test Number	Description
1	Init command test
2	Receive buffer IN command test
3	Transmit buffer IN command test Buffer Transmission/Reception
4	Line transmission exercising

4.5.4 DEC/X11 KMC11-B Module

The DEC/X11 KMC11-B module is designed to exercise up to and including two KMC11-B interfaces with consecutive addresses and vectors.

It uses no line unit for receiving and transmitting data. Data buffers are transmitted and received from the PDP-11 memory to the KMC11 and in the reverse direction.

4.5.5 Examination of KMS11-P Internal Components

The following are some examples for examining KMS11-P memory and scratchpad registers assuming that there is firmware in the microprocessor.

EXAMPLE 1: Examine KMS11-P memory

	Procedures	Comments
1.	Load 0 oct. SEL 0	To clear Run bit and stop the microprocessor
2.	Load 010XXX oct. to SEL 6	Microinstruction is loaded into SEL 6, where XXX is an eight-bit memory address which is loaded into MAR HI.
3.	Load 1400 oct. to SEL 0	Set ROM In and Step microprocessor bits.
4.	Load 020xx oct. to SEL 6	Load microinstruction into SEL 6 where xxx is an eight-bit memory address, which is loaded into MAR L0.
5.	Load 1400 oct. to SEL 0	Set ROM In and Step microprocessor bits.
6.	Load 055244 oct. to SEL 6	Load microinstruction to SEL 6 to read memory content pointed to by MAR to SEL 4; MAR is incremented.
7.	Load 1400 oct. to SEL 0	Set ROM In and Step microprocessor bits.

8.	Examine BSEL 4 low byte for memory content	BSEL 4 contains content of memory location under examination.
9.	Go to Step 7 for examination of consecutive memory locations	

EXAMPLE 2: Examine KMS11-P Scratchpad Registers

	Procedures	Comments
1.	Load SEL 0 with 0 oct.	To clear Run bit
2.	Load SEL 6 with 0606XX oct.	SEL 6 is loaded with microinstruction, where XX is 0-17. Scratchpad register content of SP is loaded into the branch register.
3.	Load SEL 0 with 1400 oct.	Set ROM In and Step microprocessor bits.
4.	Load SEL 6 with 061224 oct.	Load microinstruction, where content of SPX (from BR) is loaded into BSEL 4.
5.	Load SEL 0 with 1400 oct.	Set ROM In and Step microprocessor bits.
6.	Examine BSEL 4 for content of SPX	BSEL 4 contains the contents of scratchpad X.

EXAMPLE 3: KMS11-P Base Table Dump

	Procedures	Comments
1.	Load 43 oct.	To perform an RQI for base 1 type input
2.	Examine BSEL 0 for bit 7(RDYI) set	To indicate the release of the port by the microprocessor
3.	Load 1000 oct.	Giving base address to microprocessor
4.	Load 0 to SEL 6	Clearing high order address bits and the Resume bit
5.	Load 203 oct. to BSEL 0	To give the port back to the microprocessor
6.	Load 42 oct. to BSEL 0	To force halt function with RQI
7.	Examine BSEL 0 for bit 7(RDI)set	To indicate the release of the port by the microprocessor
8.	Load 202 oct. to BSEL 0	To give the port back to the microprocessor

9. Examine 128 memory locations starting at 1000 to see base table — To see counters, buffers and other base table data

4.6 CORRECTIVE MAINTENANCE ON A VAX-11

KMS11-P diagnostics are designed to help in the fault isolation process and should be run starting with the basic microprocessor test. The correct sequence is as follows:

Diagnostic	Description
ZZ-EVDHA	M8206 Microprocessor Repair Level 3 Diagnostic
ZZ-EVDHB	M8206 Microprocessor Level 2 Diagnostic
ZZ-EVDMA	M8203 Line Unit Repair Level 3 Diagnostic
ZZ-EVDIG	M8203 Line Unit Functional Level (level 2R) Diagnostic

4.6.1 ZZ-EVDHA Microprocessor Repair Level Diagnostics

This diagnostic performs tests on the M8206 microprocessor. It includes:

1. Device initialization and RAM addressing
2. Read/Write testing
3. Interrupt generation and priority
4. NPR operation and addressing
5. ALU functions
6. Microprocessor instruction testing.

This program performs many of the tests by stepping the microprocessor through various instruction sequences. This program will be run at VAX-11 Level 3 which is a standalone repair level.

Table 4-6 ZZ-EVDHA Diagnostic Summary

Test Number	Description
1	UNIBUS device register test
2	Master clear test
3	CSR bit set/clear verification test
4	INBUS*/OUTBUS* register test
5	INBUS/OUTBUS register test
6	INBUS no dual address test
7	BRG register test
8	Scratchpad memory test
9	Microprocessor main memory test
10	Microprocessor ALU function test
11	Interrupt test
12	Non-existent memory test
13	NPR control register test
14	Power fail test

Table 4-6 ZZ-EVDHA Diagnostic Summary (Cont)

Test Number	Description
15	Program clock test
16	Microprocessor noise test
17	CRAM Read/Write test
18	CRAM no dual address test (4 mins)
19	CRAM ODT bits test
20	CRAM Jump test

4.6.2 ZZ-EVDHB Microprocessor Functional Tests

This Level 2 diagnostic checks the function of the KMC11-B in a VMS environment. Special diagnostic firmware is loaded into the KMC11-B and used to transmit, receive, and check data buffers of 512 characters. One pass is defined as 128 iterations of this sequence.

The program runs at Level 2 under the diagnostic supervisor which will support either VMS or standalone operations. When run under VMS the microprocessor driver must have been loaded before execution of the test.

4.6.3 ZZ-EVDMA Line Unit Repair Level Diagnostics

This diagnostic performs register and USYRT addressing tests, static bit interaction and read/write logic tests, basic transmitter and receiver sequencing tests, and static operation in bit-stuffing mode tests. This program performs many of the tests in internal loopback mode using the USYRT maintenance bit and the line unit loopback features. In external loopback mode it uses a turnaround connector. This program is implemented as a separate VAX-11 diagnostic, which runs at Level 3.

Table 4-7 ZZ-EVDMA Diagnostic Summary

Test Number	Description
1	Microprocessor CSR addressing (SEL 0)
2	INBUS/OUTBUS register 14 initialization test
3	INBUS/OUTBUS register 14 read/write bit test
4	Register 14 master clear test
5	Register 14 UNIBUS reset (INIT) test
6	Line unit false selection test
7	INBUS register master clear test
8	Register 10-17 addressing test
9	Register 11 read/write bit test
10	Register 12 read/write bit test
11	Register 13 read/write bit test
12	Register 17 read/write bit test
13	Maintenance clock bit test
14	Extended register master clear test
15	Extended register addressing test
16	Registers 15, 16 / AX2-15, AX2-16 read/write bit test
17	AX0-15, AX0-16 read/write bit test
18	AX1-15, AX1-16 read/write bit test
19	AX3-15, AX3-16 read/write bit test

Table 4-7 ZZ-EVDMA Diagnostic Summary (Cont)

Test Number	Description
20	Register 17 – AX2-16 read/write, master clear test
21	Transmitter buffer data test
22	Transmitter buffer sequencing test
23	TX msg. timing test, char. mode, with CRC
24	TX msg. timing test, bit mode, with CRC
25	TX msg. timing test, char. mode, with no CRC
26	TX underrun set and clear – char. mode
27	Transmit char. length timing – char. mode, CRC
28	Transmit char. length timing – bit mode, CRC
29	TX data bit – char. mode, CRC
30	USYRT receiver msg. – char. mode, CRC
31	USYRT receiver msg. – bit mode, CRC
32	USYRT receiver msg. – char. mode, no CRC
33	USYRT receiver msg. – bit mode, no CRC
34	Silo-disabled transmitter load test
35	Silo-disabled msg. – bit mode, no CRC
36	Receiver buffer – char. mode, CRC
37	Receiver char. length timing – char. mode, no CRC
38	Receiver char. length timing – bit mode, no CRC
39	Transmit underrun error, idle marking, char. mode, no CRC
40	Msg. termination with GA chars. – bit mode, no CRC
41	Idle synchs – char. mode
42	Strip synch test
43	Bit stuffing test
44	RCV overrun error set and clear test
45	Abort sequence test
46	Abort and idle flags test
47	Transmitter underrun error, idle abort chars, bit mode
48	Receiver disable test
49	Assembled bit count test
50	Secondary station address bit test
51	RDALL (all parties address) bit test
52	Insert error (IERR) bit – char. mode, no CRC
53	Switch pack printout and test
54	Register AX3-15 printout
55	CRC generation test
56	CRC error detection test
57	VRC parity generation test
58	VRC error detection test
59	Integral modem interface – char. mode, CRC
60	V.35 modem interface – char. mode, CRC
61	RS-232-C and RS-423 modem interface – char. mode, CRC
62	RS-422 modem interface – char. mode, CRC
63	Half-duplex bit (HALF DUPX) test
64	Half-duplex RCV disabled with silos disabled
65	Interaction of modem control bits
66	Data – bit mode, no ERR DET
67	Data – char. mode, no ERR DET

Table 4-7 ZZ-EVDMA Diagnostic Summary (Cont)

Test Number	Description
68	Data – bit mode, CRC-CCITT-1
69	Data – bit mode, CRC-CCITT-0
70	Data – char. mode, CRC-16
71	Data – char. mode, odd VRC
72	Data – char. mode, even VRC
73	Contiguous ones in SEC. STA. ADRS. mode, bit mode

4.6.4 ZZ-EVDIG Line Unit Functional Tests

This diagnostic is a Level 2R diagnostic. As such it checks the information path through the line unit, the microprocessor, and the microprocessor driver. This program must be run under VMS and uses a special firmware which is loaded during the program initialization phase.

The program is designed to show that the device is able to correctly transmit and receive buffers from and to the memory in DMA mode (by using the UBA registers). The interaction between firmware and application (that is, the diagnostic supervisor) is done using interrupts, as in any user application. This program performs the tests in internal loopback mode using the USYRT maintenance bit and the line unit loopback features. In external loopback mode it uses a turnaround connector.

The program runs as a level 2R diagnostic under the diagnostic supervisor and VMS. The microprocessor driver (XS DRIVER) must have been loaded using SYSGEN before the execution of the test.

The driver interface for the ZZ-EVDIG diagnostic is given in Appendix C.

Table 4-8 ZZ-EVDIG Diagnostic Summary

Test Number	Description
1	Basic transmit test
2	One buffer transmit and receive test
3	Transmit and receive buffer size test

APPENDIX A
FLOATING DEVICE ADDRESSES AND VECTORS

A.1 FLOATING DEVICE ADDRESSES

UNIBUS addresses starting at 760010 and continuing through 763776 are designed as floating device addresses (see Figure A-1). These are used as register addresses for communications (and other) devices that interface with a PDP-11 or VAX-11.

NOTE

Some devices are not supported by VAX-11, however, the same system applies; that is, gaps are provided as appropriate. The convention for assigning these addresses is shown in the following list.

Rank	Option	Decimal Size	Octal Modulus
1	DJ11	4	10
2	DH11	8	20
3	DQ11	4	10
4	DU11	4	10
5	DUP11	4	10
6	LK11A	4	10
7 *	KMS11-P	4	10
8	DZ11 and DZV11	4	10
9	KMC11	4	10
10	LPP11	4	10
11	VMV21	4	10
12	VMV31	8	20
13	DWR70	4	10
14	RL11 and RLV11	4	10 (extra only)

* Recommended Position

A gap of 10 octal must be left between the last address of one device type and the first address of the next device type. The first address of the next device type must start on a modulo 10 octal boundary. The gap of 10 octal must also be left for devices that are not installed but are skipped over in the priority ranking list. Multiple devices of the same type must be assigned contiguous addresses. Device types previously installed in the system may need to be reassigned to make room for additional ones.

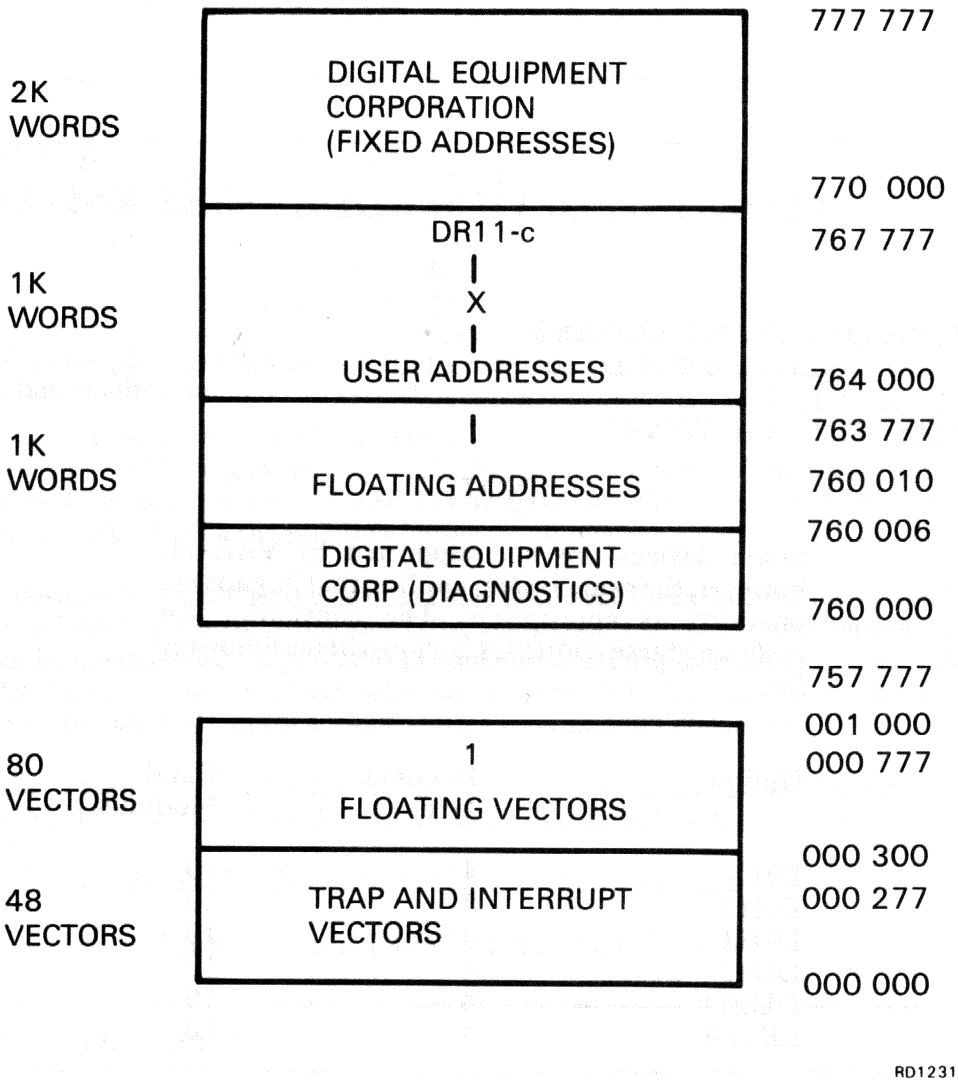


Figure A-1 UNIBUS Address Map

A.2 FLOATING VECTOR ADDRESSES

Vector addresses, starting at 300 and proceeding upward to 777, are designed as floating vectors. These are used for communications (and other) devices that interface with the PDP-11 and VAX-11.

NOTE

Some devices are not supported by VAX-11, however, the same system applies. Vector size is determined by the device type.

There are no gaps in floating vectors unless needed by physical hardware restrictions (in data communications devices, the receive vector must be on a zero boundary and the transmit vector must be on a 4 octal boundary).

Multiple devices of the same type would be assigned vectors sequentially. The following list shows the assignment sequence.

Floating interrupt vector devices are as follows:

Rank	Option	Decimal Size	Octal Modulus
1	DC11	4	10
2	KL11(extra)	4	10 **
2	DL11-A(extra)	4	10 **
2	DL11-B(extra)	4	10
3	DP11	4	10
4	DM11-A	4	10 **
5	DN11	2	4
6	DM11-BB	2	4
6	DH11 modem control	2	4
7	DR11-A	4	10 **
8	DR11-C	4	10 **
9	PA611(reader)	2	10 **
10	PA611(punch)	2	10 **
11	LPD11	4	10
12	DT11	4	10 **
13	DX11	4	10 **
14	DLC11-C	4	10 **
14	DL11-D	4	10 **
14	DL11-E	4	10 **
15	DJ11	4	10 **

** The vector for the device of this type must always be on a 10 octal boundary.

Rank	Option	Decimal Size	Octal Modulus
16	DH11	4	10 ***
17	GT40	8	10
18	LPS11	12	30 **
19	DQ11	4	10 ***
20	KW11-W	4	10
21	DU11	4	10 **
22	DUP11	4	10 **
23	DV11	4	10 **
24	DV modem control	2	4
25	LK11-A	4	10
26	DWUN	4	10
27 *	KMS11-P	4	10 **
28	DZ11	4	10 **
29	KMC11	4	10
30	LPP11	4	10
31	VMV21	4	10
32	VMV31	4	10
33	VTV01	****	****
34	DWR70	4	10 **

* Recommended Position

** The vector for the device of this type must always be on a 10 octal boundary.

*** These devices can have either an M7820 or M7821 interrupt control module. However, it should always be on a 10 octal boundary.

**** To be determined.

35	RL11/RLV11	2		4
36	RX02	2		4
37	TS11	2	(after first)	4
38	LPA11-K	4		10
39	IP11/IP300	2		4

A.3 EXAMPLES OF DEVICE AND VECTOR ADDRESS ASSIGNMENT

A.3.1 Example 1

The first device needing address assignment in this example is a DH11 (number two in the device address assignment sequence; number 16 in the vector address assignment sequence).

The devices used in this example are:

2 DH11s
2 DQ11s
1 DUP11
1 KMS11-P

Device (Option)	Device Address	Vector Address	Comment
	760010		Gap left for DJ11 (one on device address assignment sequence) which is not used
DH11	760020	300	First DH11
DH11	760040	310	Second DH11
	760060		Gap between the last DH11 used and the next device
DQ11	760070	320	First DQ11
DQ11	760100	330	Second DQ11
	760110		Gap between the last DQ11 used and the next device
	760120		Gap left for DU11s not used
DUP11	760130	340	Only one DUP11
	760140		Gap left between DUP11 and next device
	760150		Gap left for LK11-As not used
KMS11-P	760160	350	Only one KMS11-P
	760170		Gap left after the last device

A.3.2 Example 2

The devices used in this example are:

1 DJ11
1 DH11
2 DQ11s
2 DUP11s
1 KMS11-P
1 DMR11

Device (Option)	Device Address	Vector Address	Comment
DJ11	760010	300	Only one DJ11
	760020		Gap left between DJ11 and the next device
	760030		Gap – The next device, DH11, must start on an address boundary that is a multiple of 20
DH11	760040	310	Only one DH11
	760060		Gap left between DH11 and next device
DQ11	760070	320	First DQ11
DQ11	760100	330	Second DQ11
	760110		Gap left between DQ11 and next device
	760120		Gap left for DU11s not used
DUP11	760130	340	First DUP11
DUP11	760140	350	Second DUP11
	760150		Gap left between the last DUP11 and next device
	760160		Gap left for LK11-As not used
KMS11-P	760170	360	Only one KMS11-P
DMR11	760210		Gap left after the last device

APPENDIX B
PDP-11 DIAGNOSTIC SUPERVISOR SUMMARY

B.1 INTRODUCTION

The PDP-11 diagnostic supervisor is a software package which:

1. Provides run-time support for diagnostic programs running on a PDP-11 in standalone mode
2. Provides a standard operator interface to load and run a single diagnostic program or a script of programs
3. Provides a common programmer interface for diagnostic development
4. Creates a common structure on diagnostic programs
5. Guarantees compatibility with different load systems such a APT, ACT, SLIDE, XXDP+, ABS Loader
6. Performs non-diagnostic functions for programs, such as console I/O data conversion, test sequencing, program options.

B.2 VERSIONS OF THE DIAGNOSTIC SUPERVISOR

File Name	Environment
HSAA**.SYS	XXDP+
HSAB**.SYS	APT
HSAC**.SYS	ACT/SLIDE
HSAD**.SYS	Paper Tape (Absolute Loader)

In the above file names, '**' is for the REVision (REV) and patch level, such as 'A0'.

B.3 LOADING AND RUNNING A SUPERVISOR DIAGNOSTIC

A diagnostic that is compatible with the diagnostic supervisor program may be loaded and started in the normal way, using any of the supported load systems. Using XXDP+ for example, the program 'CZDMRB.BIN' is loaded and started by typing '.R CZDMRB'.

To determine if diagnostics are supervisor-compatible, use the LIST command under the SETUP utility (see Section B.5).

The diagnostic and the supervisor are automatically loaded into the memory location (as shown in Figure B-1) and the program is started. The following message is typed by the program:

```
DRS LOADED
DIAG.RUN-TIME SERVICES
CZDMR-B.O
M8203 STATIC LOGIC TESTS – PART 1 OF 2
UNIT IS M8203
DR>
```

'DR>' is the prompt for the diagnostic supervisor routine. At this point a supervisor command must be entered (the supervisor commands are listed in Section B.4).

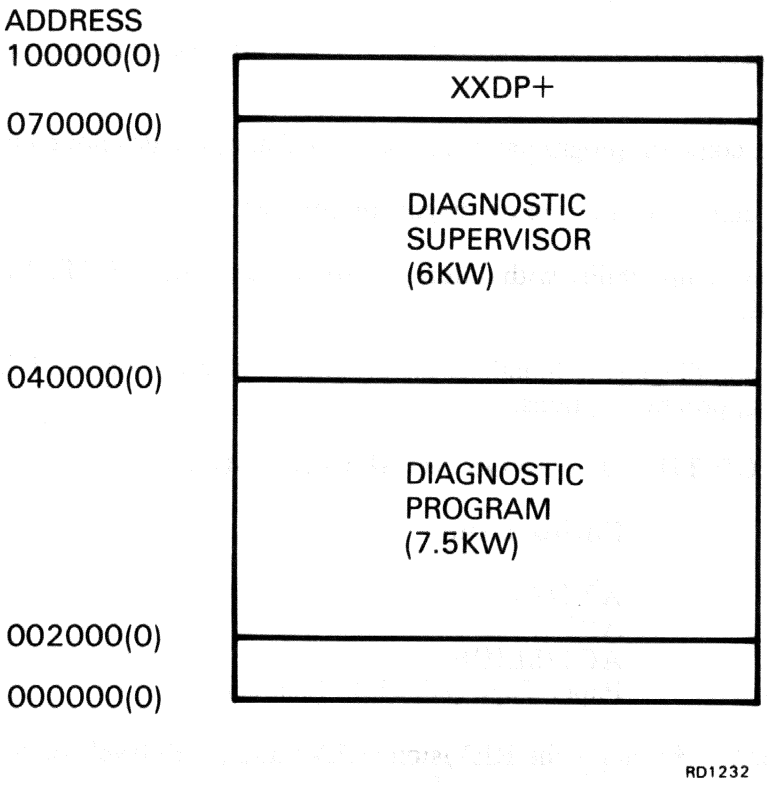


Figure B-1 XXDP+ Diagnostic Supervisor Memory Layout on a 16K word (minimum memory) System

B.3.1 Five Steps to Run a Supervisor Diagnostic

Step 1 – Enter STArt command

When the prompt 'DR>' is issued, type:

STA/PASS:1/FLAGS:HOE<CR>

The switches and flags are optional.

Step 2 – Enter number of units to be tested

The program will respond to the STArt command with:

UNITS ?

At this point the number of devices to be tested must be entered.

Step 3 – Answer hardware parameter questions

After the number of devices to be tested has been entered, the program will respond by asking a number of hardware questions. The answers to these questions are used to assemble hardware parameter tables in memory. One of these hardware P-Tables will be assembled for each device to be tested and the series of questions will be asked for each device.

Step 4 – Answer software parameter questions

When all the hardware P-Tables are assembled, the program will respond with:

CHANGE SW ?

If other than the default parameters are needed for the software, type 'Y'. If the default parameters are needed, type 'N'.

If 'Y' is typed, a series of software questions will be asked and the answers to these will be entered into the software P-Table in memory. The software questions will be asked only once, regardless of the number of units to be tested.

Step 5 – Diagnostic execution

After the software questions have been answered, the diagnostic will start to run.

What occurs next will be determined by the switch options selected with the STArt command, or errors occurring during execution of the diagnostic.

B.4 SUPERVISOR COMMANDS

The supervisor commands that may be issued in response to the 'DR>' prompt are as follows:

STArt – Used to start a diagnostic program.

REStart – When a diagnostic has stopped and control is given back to the supervisor, this command may be used to restart the program from the beginning.

CONtinue – Used to allow a diagnostic to continue running from where it was stopped.

PROceed – Causes the diagnostic to continue with the next test after the one in which it halted.

EXIt – Transfers control to the XXDP+ monitor.

DROp – Drops units specified until an ADD or STArt command is given.

ADD – Adds units specified. These units must have been previously dropped.

PRInt – Prints out statistics if available.

DISplay – Displays P-Tables.

FLAgs – Used to change flags.

ZFLags – Clears flags.

All the supervisor commands except EXIt, PRInt, FLAgs and ZFLags can be used with switch options.

B.4.1 Command Switches

Switch options may be used with most supervisor commands. The available switches and their function are as follows:

/TESTS: – Used to specify the tests to be run (the default is all tests). An example of the tests switch used with the STArt command to run tests 1 through 5, 19, and 34 through 38 would be:

```
DR>START/TESTS:1-5:19:34-38 <CR>
```

/PASS: – Used to specify the number of passes for the diagnostic to run. For example:

```
DR>START/PASS:1
```

In this example, the diagnostic would complete one pass and give control back to the supervisor.

/EOP: – Used to specify how many passes of the diagnostic will occur before the end of pass message is printed (the default is one).

/UNITS: – Used to specify the units to be run. This switch is valid only if 'N' was entered in response to 'CHANGE HW?'.

/FLAGS: – Used to check for conditions and modify program execution. The conditions checked for are:

:HOE – Halt on error (transfers control back to the supervisor).

:LOE – Loop on error.

:IER – Inhibit error reports.

:IBE – Inhibit basic error information.

:IXE – Inhibit extended error information.

:PRI – Print errors on line printer.

:PNT – Print the number of the test being executed prior to execution.

:BOE – Ring bell on error.

:UAM – Run in unattended mode, bypass manual intervention tests.

:ISR – Inhibit statistical reports.

:IOU – Inhibit dropping of units by program.

B.4.2 Control/Escape Characters Supported

The keyboard functions supported by the diagnostic supervisor are as follows:

CTRL C (C) – Used to return control to the supervisor. The 'DR>' prompt would be typed in response to CTRL C. This function can be typed at any time.

CTRL Z (Z) – Used during hardware or software interaction to terminate the interaction and select default values.

CTRL O (O) – Used to disable all printouts. This is valid only during a printout.

CTRL S (S) – Used during a printout to temporarily freeze the printout.

CTRL Q (Q) – Used to continue a printout after a CONTROL S.

In the list above 'CTRL C' is implemented by holding the CTRL (control) key pressed, followed by the letter 'C'. The diagnostic supervisor responds with ' C'.

B.5 SETUP UTILITY

SETUP is a utility program that allows the operator to create a table of parameters for a supervisor diagnostic, before execution. This is valid for either XXDP+ or ACT/SLIDE environments. SETUP asks the hardware and software questions and assembles the P-Tables.

The commands available under SETUP are:

LIST – List supervisor diagnostics
SETUP – Create P-Tables
EXIT – Return control to the supervisor

The format for the LIST command is:

```
LIST DDN:FILE NEXT
```

Its function is to type the file name and creation date of the file specified, if it is a supervisor diagnostic of revision C or later. If no file name is given, all supervisor diagnostics of revision C or later will be listed. The default for the device is the system device and wildcards ('*' and '?') are accepted. (For more information on the use of wildcards, refer to the XXDP+/Supervisor User Manual – CHQUSE0.)

The format for the SETUP command is:

```
SETUP DDN:FILE.EXT=DDN:FILE.EXT
```

It will read the input file specified and prompt the operator for information to assemble P-Tables. An output file will be created to run in the environment specified. File names for the output and input files may be the same. The output and input device may be the same. The default for the device is the system device and wildcards are not accepted.

APPENDIX C
DRIVER INTERFACE FOR EVDIG DIAGNOSTIC

C.1 GENERAL

EVDIG diagnostic is a level 2R diagnostic which runs only under VMS. It assumes the XS DRIVER has been loaded first, using SYSGEN.

The EVDIG diagnostic initially loads a diagnostic firmware which basically implements a transparent loopback mode. It works through the standard on-line interface of the XS DRIVER.

C.2 FUNCTIONS

The main functions of the XS DRIVER used are:

IO$.LOADMCODE	To load and start the firmware
IO$.INITIALIZE	To initialize the line parameters and set up the loopback feature in the firmware
IO$.CONNECT	A dummy command which tests the interrupt mode of the KMC
IO$.WRITEPBLK and IO$.READPBLK	Transmit and receive functions which are used to test transmission of different size buffers over a loopback link (internal or external loopback, which ever is selected).

APPENDIX D
COMMAND AND RESPONSE FORMAT FOR CZKMR DIAGNOSTIC

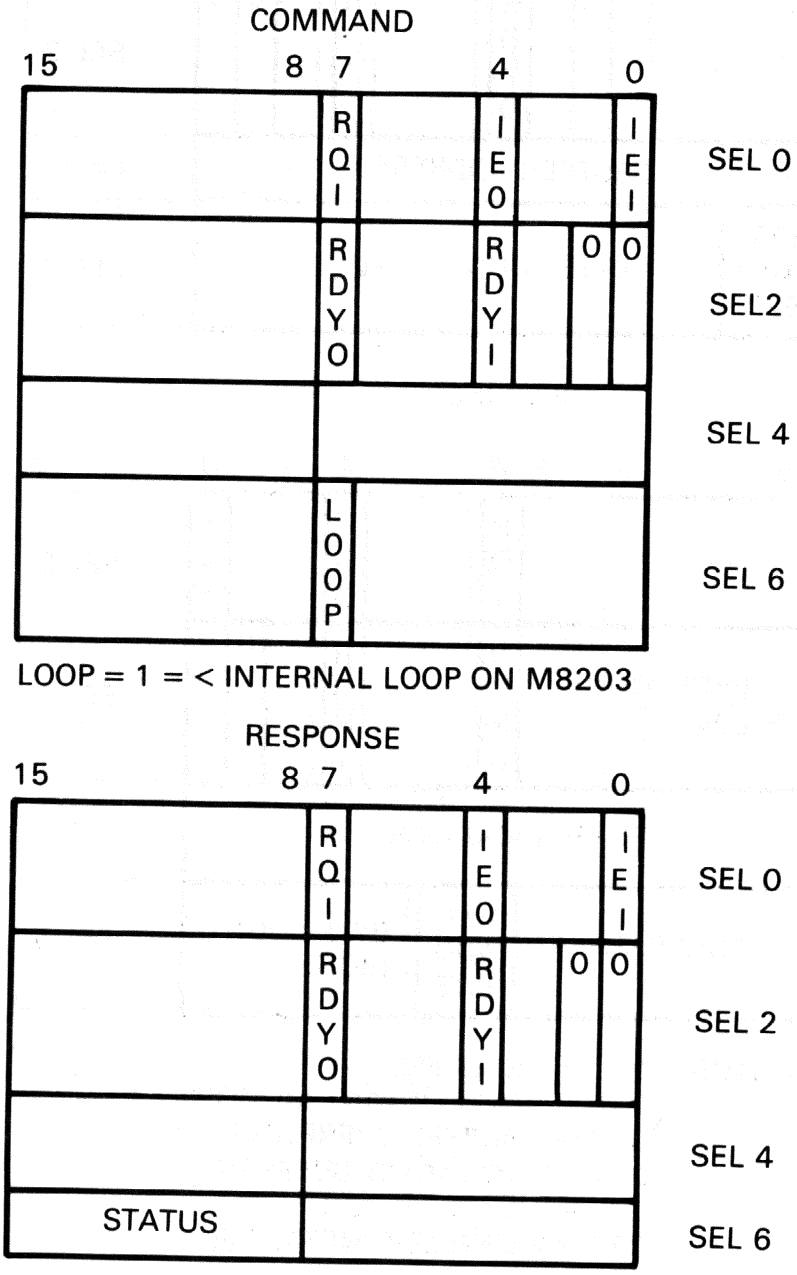
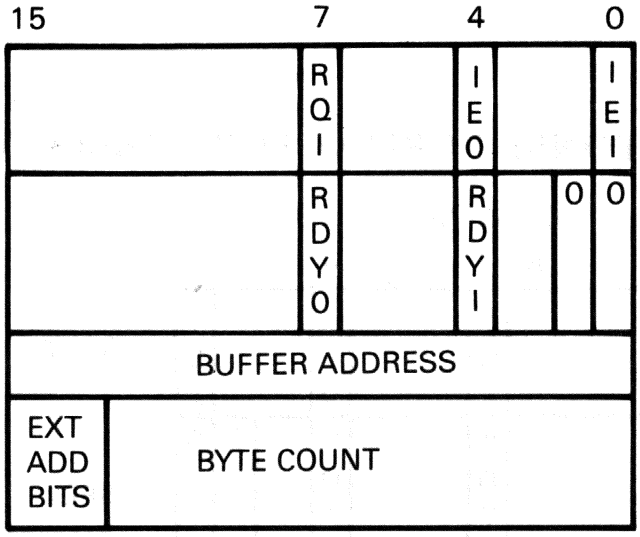
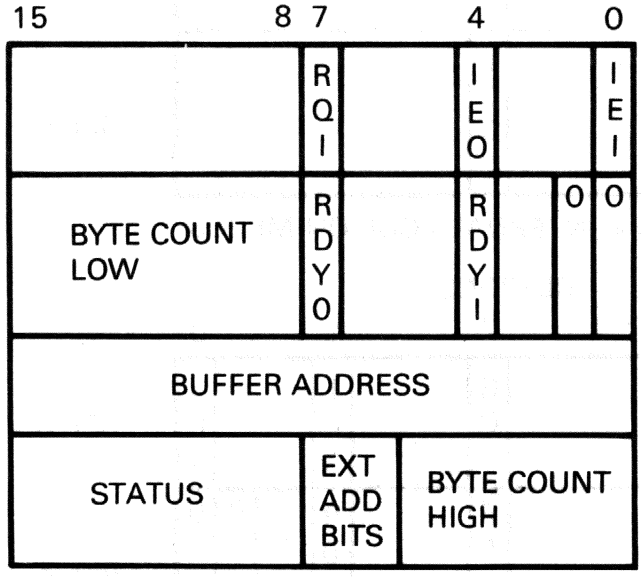


Figure D-1 Line INIT Command

COMMAND



RESPONSE

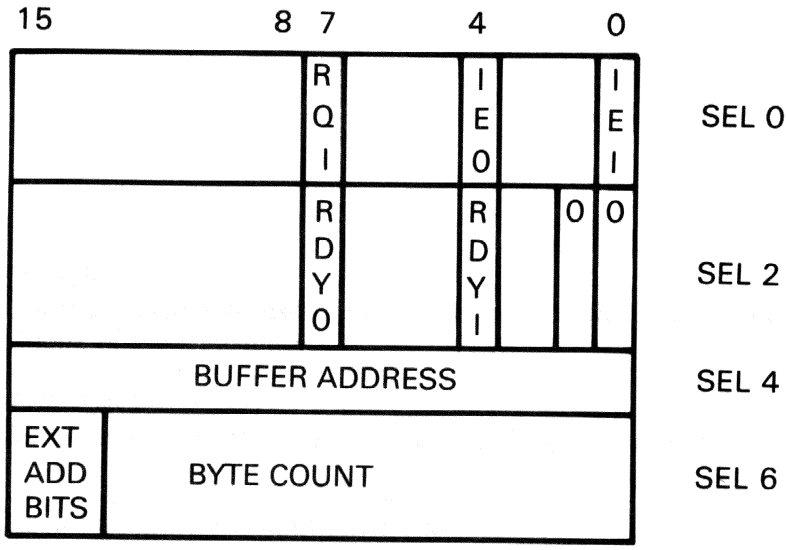


STATUS = 1 => SUCCESS
376 => NO EXISTANT MEMORY
375 => BUFFER OVERFLOW
374 => TOO MANY BUFFERS
373 => MODE ERROR
370 => LINE NOT INITIALIZED

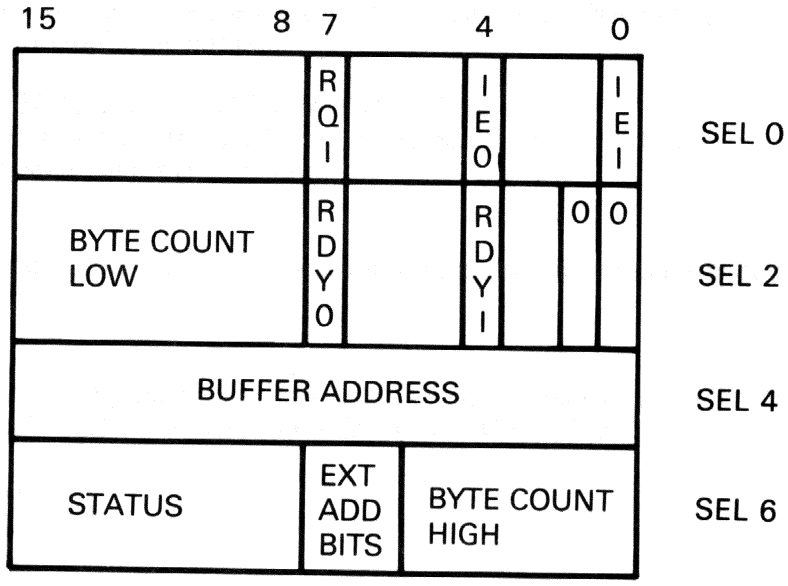
RD1234

Figure D-2 Receiver Buffer IN Command

COMMAND



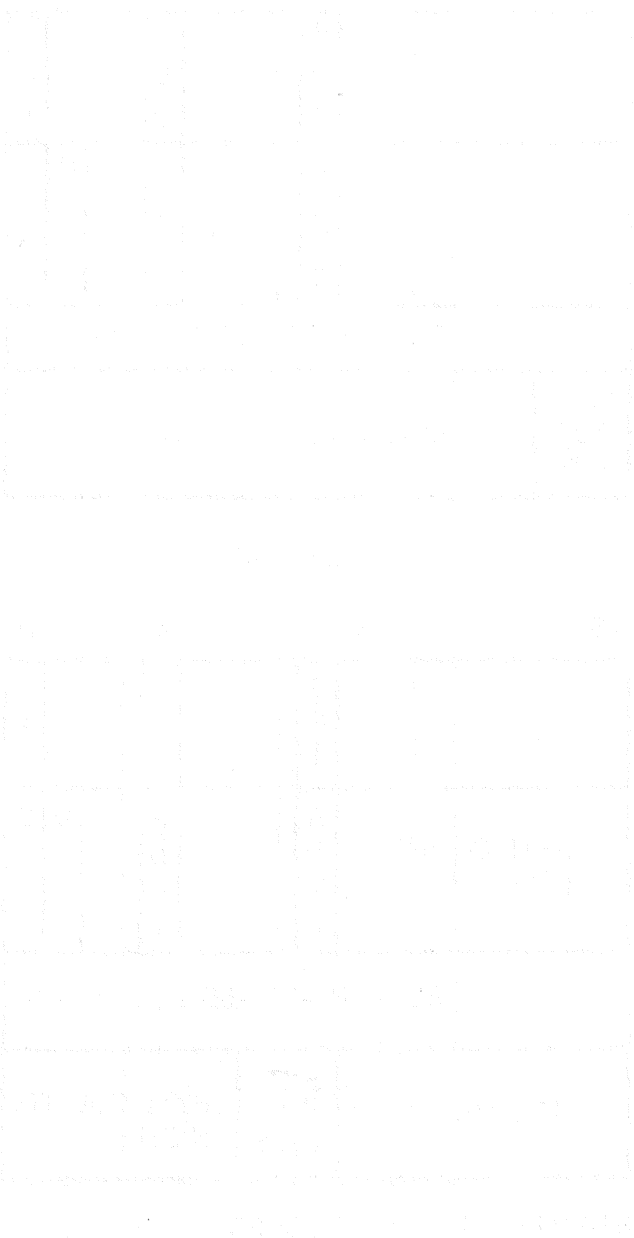
RESPONSE



STATUS = 1 => SUCCESS
367 => NO EXISTANT MEMORY
375 => BUFFER OVERFLOW
374 => TOO MANY BUFFERS
373 => MODEM ERROR
370 => LINE NOT INITIALIZED

RD1235

Figure D-3 Transmit Buffer IN Command



APPENDIX E
GLOSSARY

ACKNOWLEDGE (ACK)
This indicates that the previous transmission block was accepted by the receiver, and is ready to accept the next block of the transmission.

ARITHMETIC LOGIC UNIT (ALU)
It allows the microprocessor to perform arithmetic and logic operations.

A PORT
This is a Read/Write input to the multiport RAM.

ASYNCHRONOUS TRANSMISSION
A transmission in which the time gaps between transmitted characters may be of unequal length. Transmission is controlled by start and stop elements at the beginning and end of each character. Also called 'start-stop' transmission.

BUFFERED ARITHMETIC LOGIC UNIT (BALU)
Operations performed by the ALU are buffered by the BALU and routed to data memory, appropriate registers, and the Berg port.

BERG PORT
An 8-bit port that allows the microprocessor to communicate with other devices without using the UNIBUS system.

BIT-STUFF PROTOCOL
An insertion of zero, by the transmitter, after any five consecutive ones. This is designed for bit-oriented protocols such as Synchronous Data Link Control (SDLC).

BITS PER SECOND
This is the bit transfer rate per unit of time.

B PORT
The read address input of the multiport RAM (read only port).

BRANCH REGISTER (BRG)
A temporary storage register used for branch computation and shifting right.

BUFFER
A storage device used to allow for a difference in the rate of data flow, when transmitting data from one device to another.

CCITT
Comite Consultatif International de Telegraphie et Telephonie – An international consultative committee that sets international communication standards.

CONTROL AND STATUS REGISTERS (CSRs)
Communication of control and status information is done through these registers.

CRC (CYCLIC REDUNDANCY CHECK)
An error detection system in which the check character is generated by taking the remainder, after dividing all the serial bits in a block of data by a previously determined binary number.

CROM
A plug-in Control Read Only Memory (CROM) used as the instruction memory for the processor (see READ ONLY MEMORY).

CYCLIC REDUNDANCY CHECK (CRC)
An error detection system in which the check character is generated by taking the remainder, after dividing all the serial bits in a block of data by a previously determined binary number.

DATA LINK ESCAPE (DLE)
A control character used only to provide supplementary line control signals (control character sequences or DLE sequences). These are two-character sequences, where the first character is DLE. The second character varies according to the function needed and the code used.

DATA MULTIPLEXER (DMUX)
An 8-bit wide, 8-to-1 multiplexer used to select data for the B input of the ALU.

DATA-PHONE™ DIGITAL SERVICE (DDS)
A communications system in which data is transmitted in digital instead of analog form, therefore removing the need for modems.

DESTINATION ROM (DROM)
This controls the operand as defined by the destination of the instruction in the instruction register.

DIGITAL DATA COMMUNICATIONS PROTOCOL (DDCMP)
This is DIGITAL's standard communications protocol for character-oriented protocol.

DIRECT MEMORY ACCESS (DMA)
This permits I/O transfers directly into or out of memory, without passing through the general registers of the processor.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)
A standards organization specializing in the electrical and functional characteristics of interface equipment.

FROM
Function ROM – This controls up to 16 functions performed by the ALU.

FULL-DUPLEX (FDX)
A simultaneous independent transmission in both directions.

FIELD REPLACEABLE UNIT (FRU)
1This refers to a defective unit not to be repaired in the field. The unit is replaced with a good unit, and the defective unit is returned to a previously determined location for repair.

FIFO
A First In/First Out (FIFO) characteristic of the silo hardware buffer.

* Data-Phone is a trademark of the AT&T Company.

HALF-DUPLEX (HDX)
An alternate, one way at a time, independent transmission.

IBUS/OBUS
This makes up the microprocessor NPR control, miscellaneous registers, and CSRs.

IBUS*/OBUS*
This makes up the microprocessor NPR control, miscellaneous registers, and CSRs.

INSTRUCTION REGISTER (IR)
It contains the instruction that is being executed. The output of the register is used to control the microprocessor.

LINK MANAGEMENTS
The link management component determines the transmission and reception on links that are connected to two or more transmitters and/or receivers, in a given direction.

LU IBUS
The line unit data bus provides a path to the DMUX, using the Berg connector.

MEMORY ADDRESS REGISTER (MAR)
This controls the data memory for buffered arithmetic and logic operations to main memory.

MAIN MEMORY (MEM)
The data storage area for the microprocessor (4K X 8 RAM). It cannot be accessed directly by the CPU.

MAINTENANCE INSTRUCTION REGISTER (MIR)
This provides a destination for an instruction that can be loaded by the CPU during maintenance.

MOP
This is the Maintenance Operation Protocol (MOP).

MULTIPORT RAM
This contains all M8206 control and status registers between the microprocessor and the CPU.

NEGATIVE ACKNOWLEDGEMENT (NAK)
This indicates that the previous transmission block was in error, and that the receiver is ready to accept a retransmission of the block in which the error occurred (also a 'not ready' response to a station selection in multi-point operation).

NON-PROCESSOR REQUEST (NPR)
This refers to Direct Memory Access (DMA) type transfers, see DIRECT MEMORY ACCESS.

PROGRAM COUNTER (PC)
A 14-bit counter used to control the address of the control ROM directly. The value in the PC is controlled by branch and move instructions.

PROTOCOL
An authorized set of conventions to control the format and relative timing of message exchange between two communicating processes.

RANDOM ACCESS MEMORY (RAM)
This is usually volatile memory that can be written to and read from. The locations in the memory may be accessed in a random way.

READ ONLY MEMORY (ROM)

This is usually non-volatile memory that may contain program, data, or control information. The information can be read, but not written by the processor. This information is often placed in the ROM during its manufacture.

RS-232-C

The EIA standard single-ended interface levels and pin assignments to a modem interface.

RS-422-A

The EIA standard differential interface levels and pin assignments to a modem interface.

RS-423-A

The EIA standard single-ended interface levels and pin assignments to a modem interface.

RS-449

The EIA standard connections for RS-422-A and RS-423-A to a modem interface.

SILO

A first in, first out register – The receive silo is loaded from the USYRT, the transmit silo from the microprocessor (64 x 12).

SCRATCHPAD MEMORY (SP)

A read/write memory used for the temporary storage of data (16 x 8 bits).

SCROM

SourCe ROM – It controls the input selection for the DMUX. It also determines if a move instruction is to be executed (32 x 8 bits).

SYNCHRONOUS TRANSMISSION

A transmission in which the data characters and bits are transmitted at a fixed rate, with the transmitter and receiver synchronized.

SYSTEM CLOCK

This forms the basic timing, providing clock pulses for the microprocessor timing functions.

UNIBUS

A single high speed bus on which system components connect and communicate with each other. Addresses, data and control information is transmitted via the 56 available lines of the bus.

USYRT

Universal Synchronous Receiver/Transmitter – It handles input or output data to the modem, and the basic protocol framing and error detection.

APPENDIX F
CABINET KITS

F.1 OVERVIEW

The KMS11-P cabinet kits include I/O panels, cables and cable turnaround test connectors. When associated with the basic unit KMS1P-M, these kits allow the KMS11-P to operate within a range of speeds from 2.4K bits/s to 56K bits/s and to be adapted to from different interfaces; RS232-C, RS423-A, RS422-A and V.35.

The I/O panels are especially designed to fit with the I/O bulkhead concept, however they also fit with an adaptable bracket which can be mounted in the non-shielded cabinets.

Descriptions of the I/O panels are provided in the section F.2 and general installation procedures are given for installing the I/O panels and cabling (section F.3).

Four basic kits are available (one per interface type) and each of them can be adapted to two different types of cabinets (with or without I/O bulkhead).

Cabinet Kit

CK-KMS1P-AD EIA RS232 cabinet kit. Use with I/O bulkhead
CK-KMS1P-A1 EIA RS232 cabinet kit. Use without I/O bulkhead
CK-KMS1P-BD V.35 cabinet kit. Use with I/O bulkhead
CK-KMS1P-B1 V.35 cabinet kit. Use without I/O bulkhead
CK-KMS1P-ED RS422/449 cabinet kit. Use with I/O bulkhead
CK-KMS1P-E1 RS422/449 cabinet kit. Use without I/O bulkhead
CK-KMS1P-FD RS423/449 cabinet kit. Use with I/O bulkhead
CK-KMS1P-F1 RS423/449 cabinet kit. Use without I/O bulkhead

F.2 KIT DESCRIPTIONS

This section gives a full description of the Cabinet Kit components (descriptions and drawings).

Table F-1 Cabinet Kit Descriptions

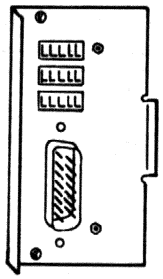
Interface	Description
CK- KMS1P-AD	**RS-232-C with an I/O Bulkhead**
• Internal Cable BC08S-10 (refer to Figure F-2 View D)	A 2m (9.84ft) ribbon cable with a 40-pin female Berg™ connector at each end. One end is plugged into J2 of the M8203 with the ribbed side facing up. The other end connects to the Berg™ connector on the I/O panel.
• I/O Panel H3001 (refer to Figure F-1 View A)	The H3001 I/O panel contains two connectors: a 40-pin male Berg™ connector on the rear, and a 25-pin male D-sub connector on the face. Three switchpacks are also included to enhance compatibility with various modems. This panel is installed in a 5.08 cm (2in) window in the I/O bulkhead, or in a 74-27292-01 adaptor bracket.

Table F-1 Cabinet Kit Descriptions (Contd)

Interface	Description
• External Cable BC22F-** (Not supplied with option) (Refer to Figure F-2 View C)	A variable length cable with a 25-pin female D-sub connector at one end and a 25-pin male D-sub connector at the other end. The female end connects to the D-sub connector on the H3001 I/O panel. The male end connects to the data communications equipment (DCE).
• Test Connector H325 (Refer to Figure F-3 View A)	A 25-pin D-sub turnaround test connector designed to test the output of either the H3001 I/O panel or the BC22F-** external cable.
CK- KMS1P-ED	**RS-422-A with an I/O Bulkhead**
• Internal Cable BC08S-10	See description under RS-232-C)
• I/O Panel H3002 (Refer to Figure F-1 View B)	The H3002I I/O panel contains two connectors: a 40-pin male Berg™ connector on the rear, and a 37-pin male D-sub connector on the face. This panel is installed in a 5.08 cm (2in) window in the I/O bulkhead, or in a 74-27292-01 adaptor bracket.
• External Cable BC55D-** (Not supplied with option) (Refer to Figure F-2 View A)	A variable length cable with a 37-pin BC55D-** female D-sub connector at one end, and a 37-pin male D-sub connector at the other end. The female end connects to the D-sub connector on the H3002 I/O panel. The male end connects to the DCE.
• Test Connector H3251 (Refer to Figure F-5 View C)	A 37-pin D-sub turnaround test connector designed to test the output of either the H3002 I/O panel or BC55D-** external cable.
CK- KMS1P-FD	**RS423-A with an I/O Bulkhead.**
• Internal Cable BC08S-10	(See description under RS-232-C)
• I/O Panel H3003 (Refer to Figure F-1 View C)	The H3003 I/O panel contains three connectors: a 40-pin male Berg connector on the rear, with a 9-pin male and a 37-pin male D-sub connector on the face (the 9-pin connector is intended for a separate application). The panel is installed in a 10.16 cm (4in) window in the I/O bulkhead, or in a 74-27292-01 adaptor bracket.

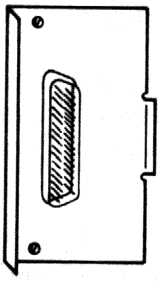
Table F-1 Cabinet Kit Descriptions (Contd)

Interface	Description
• External Cable BC55D-** (Not supplied with option)	(See description under RS-422-A/RS-449)
• Test Connector H3251	(See description under RS-422 A/RS-449)
CK- KMS1P-BD	**V.35 with an I/O Bulkhead**
• Internal Cable BC08S-10 (Refer to Figure F-2 View D)	A 3 m (9.84 ft) ribbon cable with a 40-pin female Berg™ connector at each end. One end is plugged into J1 of the M8203 with the ribbed side facing up. The other end connects to the Berg™ connector on the I/O panel.
• I/O Panel H3004 (Refer to Figure F-1 View D)	The H3004 I/O panel contains two connectors: a 40-pin male Berg™ connector on the rear, and a 37-pin male D-sub connector on the face. This panel is installed in a 5.08 cm (2in) window in the I/O bulkhead, or in a 74-27292-01 adaptor bracket.
• External Cable BC17E-25 (Refer to Figure F-2 View B)	A variable length cable with a 37-pin female D-sub connector at one end that connects to the H3004 I/O panel. A 34-pin Data Phone Digital Service (DDS) connector at the other end of the BC17E cable connects to the DCE.
• Test Connector H3250 (Refer to Figure F-3 View B)	A 34-pin female Data Phone Digital Service (DDS) turnaround test connector designed to test the output of the BC17E external cable.
CK-KMS1P-A	**Identical to CK-KMS1P-AD + ADAPTOR BRACKET**
CK-KMS1P-E1	**Identical to CK-KMS1P-ED + ADAPTOR BRACKET**
CK-KMS1P-F1	**Identical to CK-KMS1P-FD + ADAPTOR BRACKET**
CK-KMS1P-B1	**Identical to CK-KMS1P-BD + ADAPTOR BRACKET**



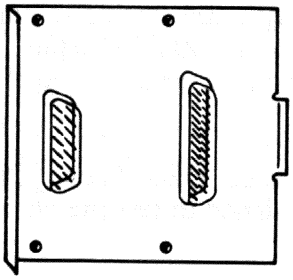
VIEW A

H3001 DISTRIBUTION PANEL



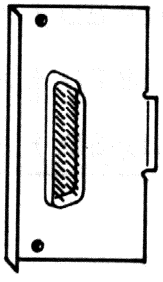
VIEW B

H3002 I/O PANEL



VIEW C

H3003 I/O PANEL

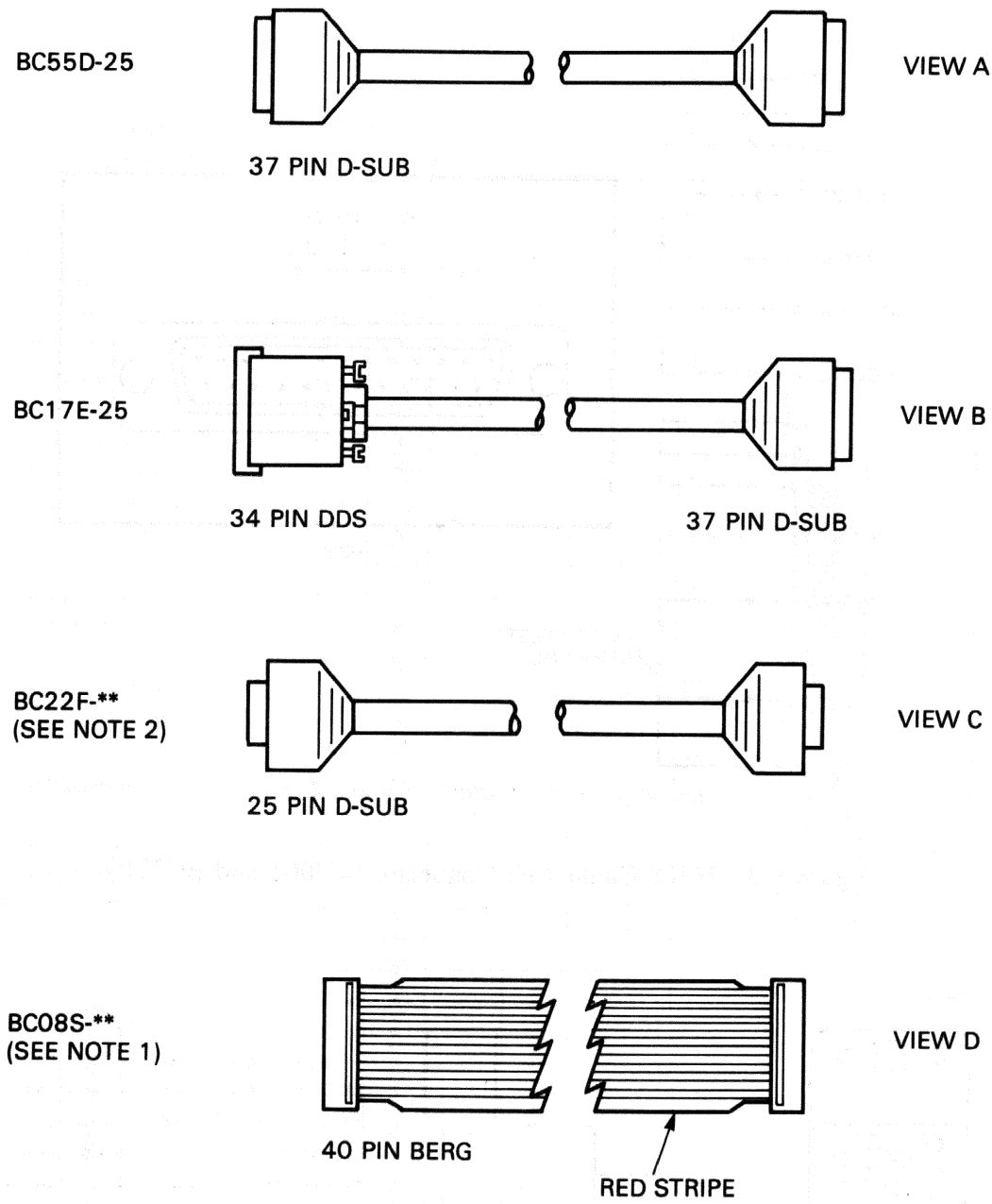


VIEW D

H3004 I/O PANEL

MK4603

Figure F-1 I/O Panel Drawings



NOTE 1
BC08S-1 INTERCONNECTS THE M8206 AND M8203 MODULES.
THE BC08S-10 CABLE CONNECTS THE M8203 LINE UNIT TO THE I/O PANEL.

NOTE 2
BC22F CABLE LENGTHS IN EXCESS OF 7.62m (25 FT) MAY EXCEED THE MAXIMUM LOAD CAPACITANCE DEFINED BY THE RS-232-C SPECIFICATION. NOTE, HOWEVER, THAT UP TO 15m (50 FT) PROVIDES SATISFACTORY PERFORMANCE LEVELS.

RD1685

Figure F-2 Cable Drawings

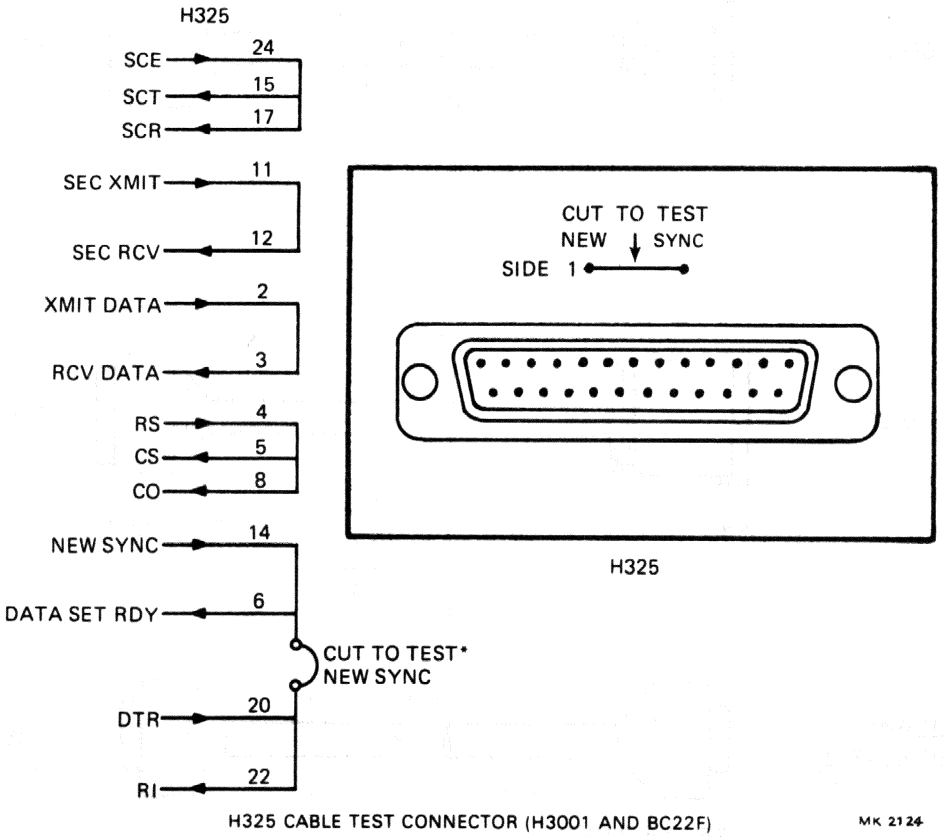


Figure F-3 H325 Cable Test Connector (H3001 and BC22F)

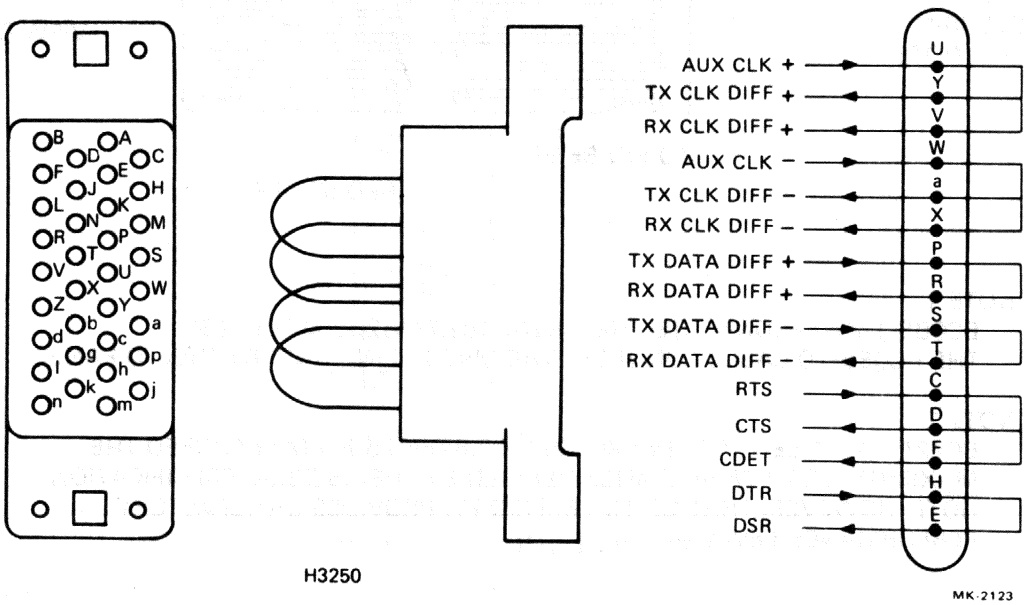


Figure F-4 H3250 Turnaround Test Connector

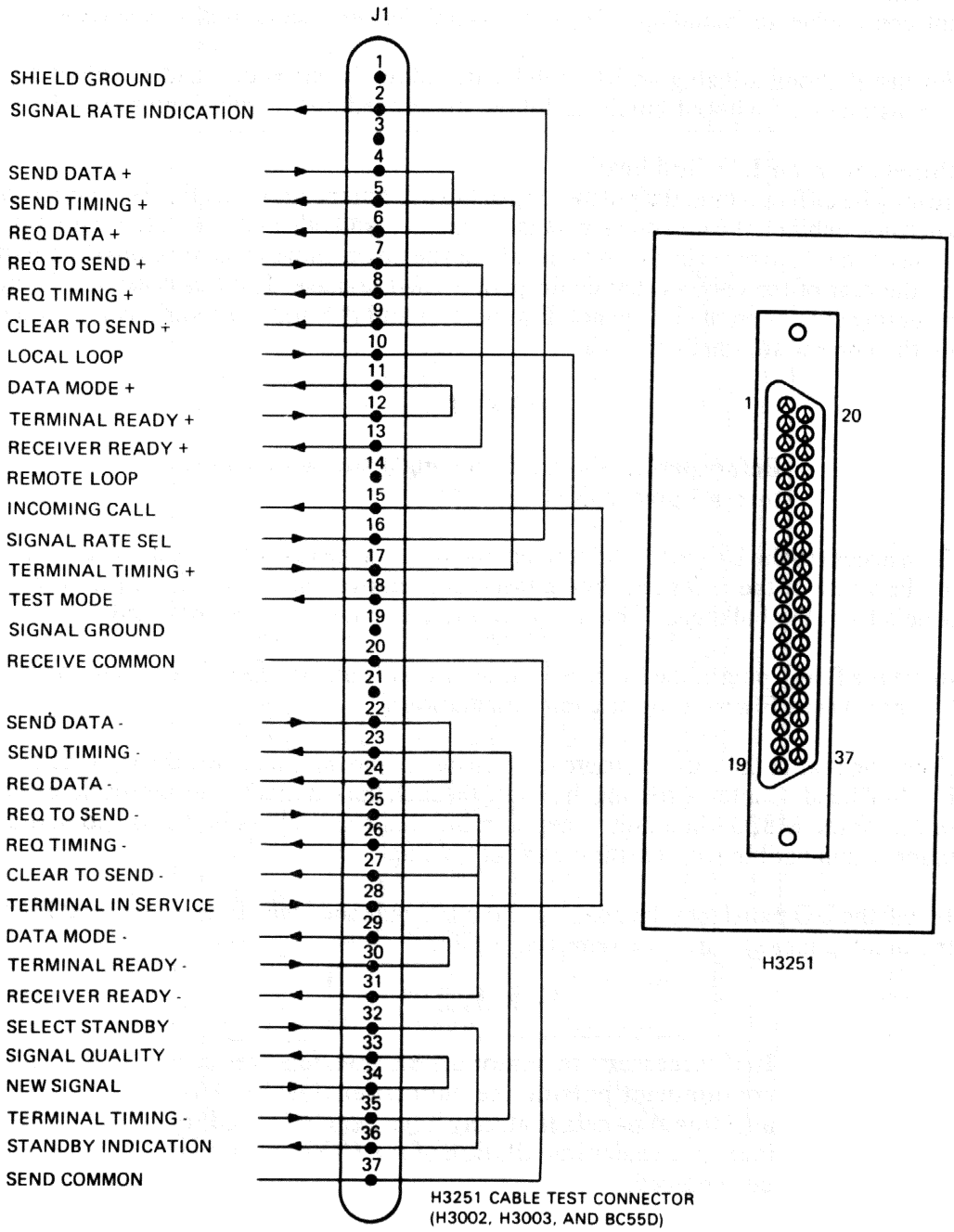


Figure F-5 H3251 Cable Test Connector (H3002. H3003 and BC55D)

F-3. INSTALLATION

Two different approaches to installing I/O panel assemblies are included in this section.

- For installations utilizing an I/O bulkhead, follow the steps outlined in sub-section F-3-1.
- For installations without bulkhead follow the procedures in sub-section F-3-2.

F.3.1. Cabinets with an I/O Bulkhead.

Though there may be differences in the positioning of the I/O bulkheads of the PDP-11 kernel cabinet, the VAX-11 expansion cabinet, the universal expansion cabinet, and other cabinets, the installation concept is the same. Once the I/O panel is installed, there should be no openings (panels omitted) remaining in the I/O frame on the rear of the cabinet that could permit EMI leakage. For this reason, it is important to tighten all mounting screws on the I/O panel. Figures F-4 and F-5 show the various I/O bulkhead types and illustrate the correct approach to each.

WARNING

Before performing the following installation steps, turn all power OFF.

1. Gain access to the I/O bulkhead through the door on the rear of the system cabinet. Depending on the width of the I/O panel being installed, remove one or two 5 cm (1.96 in) wide blank panels from the bulkhead. This is where the I/O panel is to be mounted.

2. Insert the Berg™ plug of the BC08S-10 internal cable into the Berg™ connector on the rear of the I/O panel (see Figure F-8 for cable orientation).

3. From the rear of the cabinet, route the free end of the internal cable through the opening in the I/O bulkhead. Continue routing the cable through the cabinet to the appropriate connector (J1 or J2) of the M8203 line unit. Keep in mind that the cable must be routed and dressed in a manner compatible with existing cabinet cabling.

4. Install the I/O panel into the opening of the I/O bulkhead (see Figures F-6 and F-7) in place of the blank panel(s) that were removed in Step 1.

NOTE

It is necessary to maintain an interference-free environment outside the cabinet enclosure. Any additional panels that may have been removed to facilitate easier installation of the I/O panel must be replaced.

5. Connect the external cable to the connector on the rear of the I/O panel. Refer to Figure 2-10 and 2-11 for remote cabling (EIA or CCITT). The cable should exit the cabinet with the other signal cables.

NOTE

BC22F and BC22D cable lengths in excess of 7.62m (25 ft) may exceed the maximum load capacitance as defined by the RS-232-C specification. Note, however, that up to 15.24 m (50 ft) provides satisfactory KMS11-P performance levels.

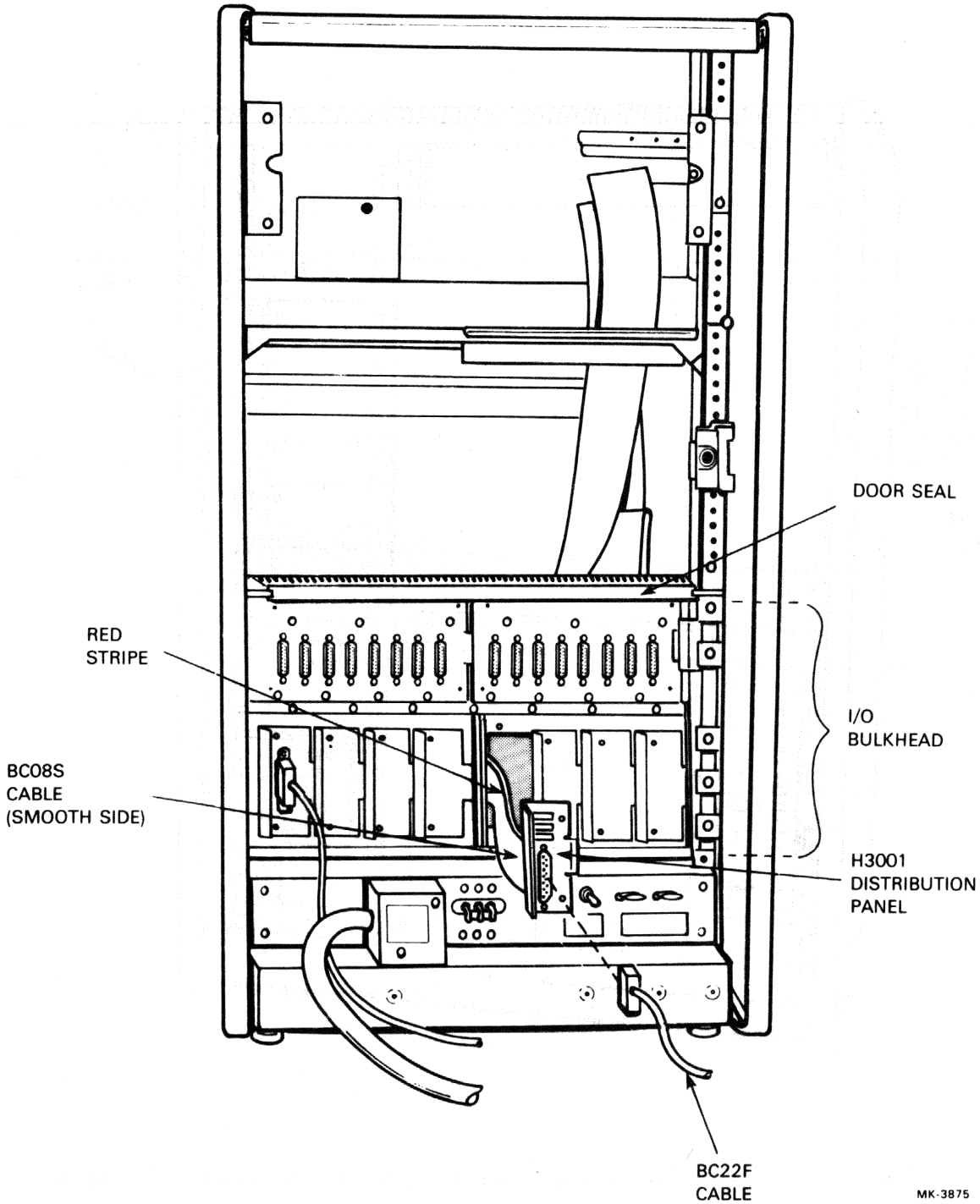


Figure F-6 Typical H3001 Installation in a Horizontally Oriented I/O Bulkhead

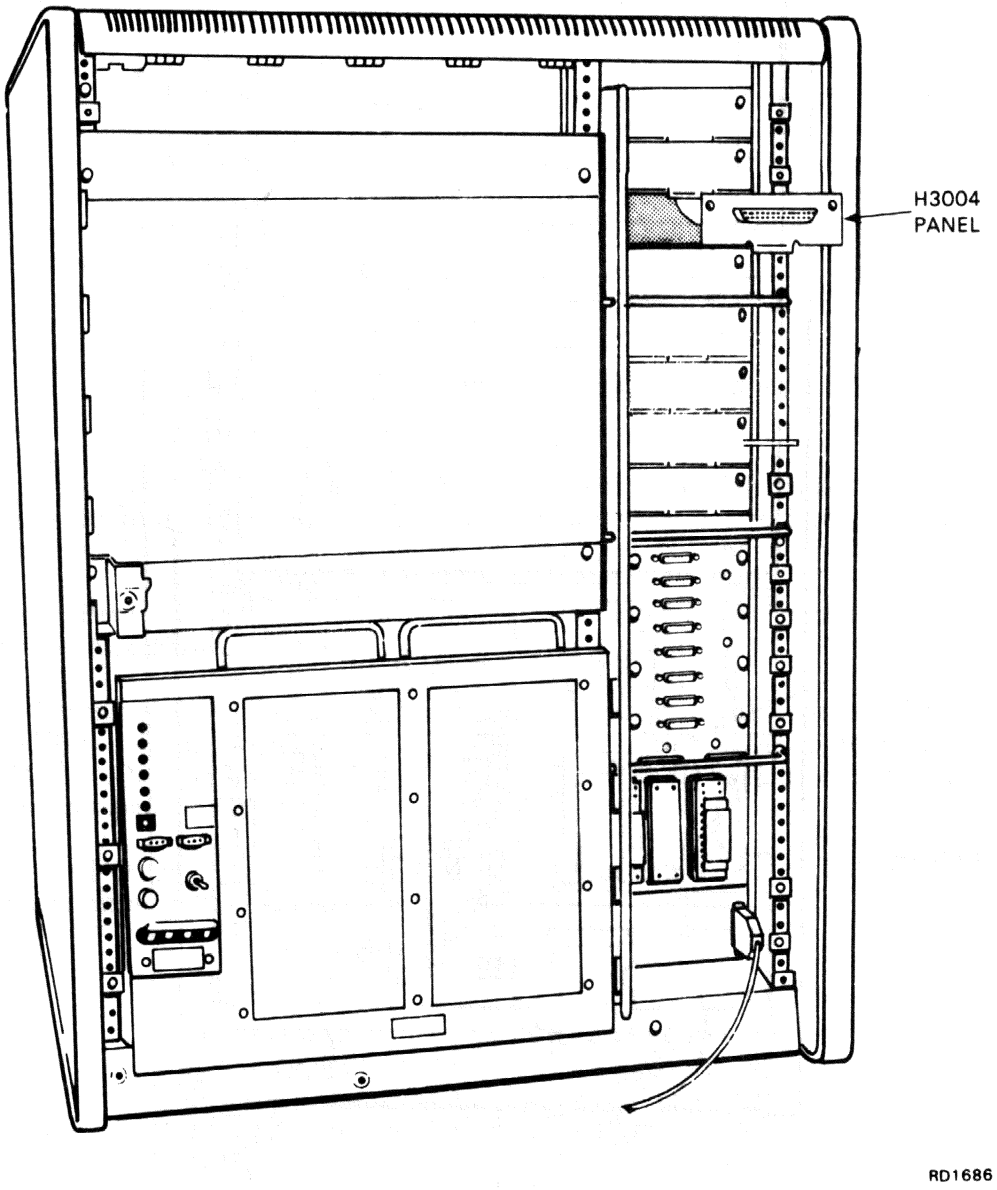


Figure F-7 Typical H3004 Installation in a Vertically Oriented I/O Bulkhead

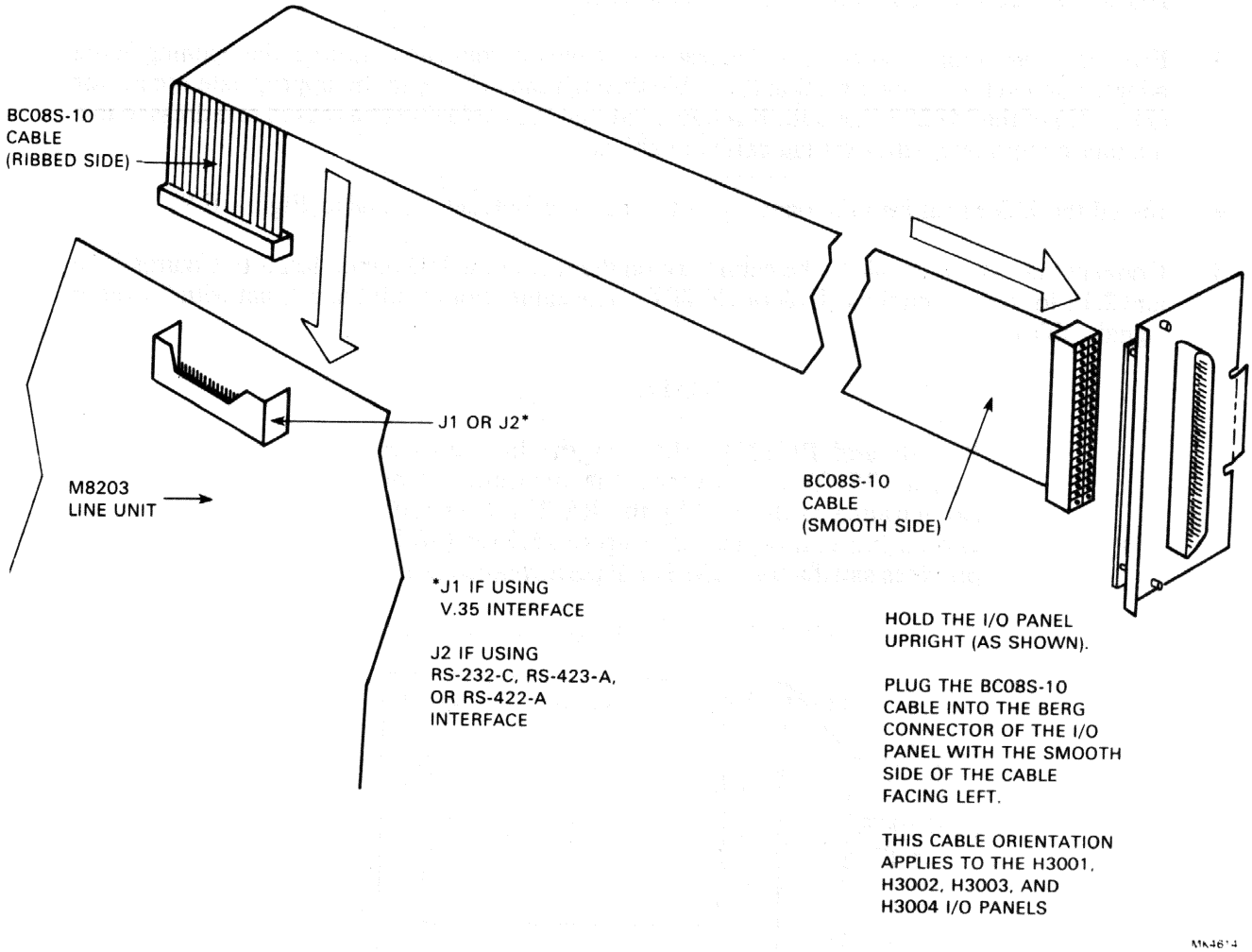


Figure F-8 BC08S-10 to I/O Panel Cable Connection

F.3.2. Cabinets without an I/O Bulkhead

WARNING

Before performing the following installation steps, turn all power OFF.

1. Gain access to the rear of the system cabinet and mount the adaptor bracket (Part Number 74-27292-01) to one of the rear vertical mounting rails. Mounting the bracket on either side of the cabinet is permissible. (Refer to Figure F-9).

NOTE

Do not install the 74-27292-01 adaptor bracket where it will physically interfere with other equipment mounted in the cabinet.

2. Insert the Berg™ plug of the BC08S-10 internal cable into the Berg™ connector on the rear of the I/O panel (see Figure F-8 for cable orientation).

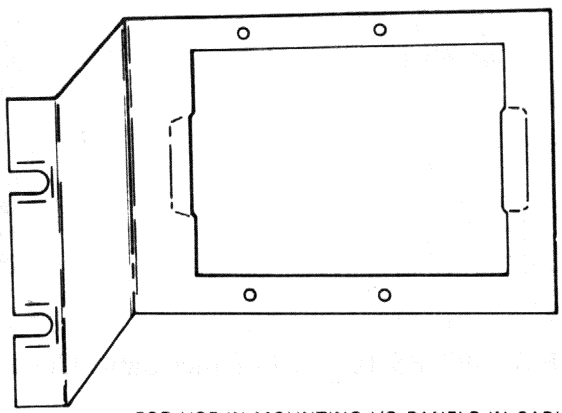
3. From the rear of the cabinet, route the free end of the internal cable through the opening in the adaptor bracket. Continue routing the cable through the cabinet to the appropriate connector (J1 or J2) of the M8203 line unit. Keep in mind that the cable must be routed and dressed in a manner compatible with existing cabinet cabling.

4. Install the I/O panel into the opening of the adaptor bracket. (Refer to Figure F-9)

5. Connect the external cable to the connector on the rear of the I/O panel. Refer to Figures 2.10 and 2.11 for remote cabling (EIA or CCITT). The cable should exit the cabinet with the other signal cables.

NOTE

BC22F and BC22D cable lengths in excess of 7.62m (25 ft) may exceed the maximum load capacitance as defined by the RS-232-C specification. Note, however, that up to 15.24m (50 ft) provides satisfactory KMS11-P performance levels.



FOR USE IN MOUNTING I/O PANELS IN CABINETS THAT DO NOT CONTAIN AN I/O BULKHEAD.

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Figure F-9 74-27292-01 Adaptor Bracket

F.3.3 DIP Switch Settings

The H3001 I/O panel includes three switchpacks which must be configured for connect operation (refer to Figure F-10 and table F.2).

The other I/O panels don't need to be configured.

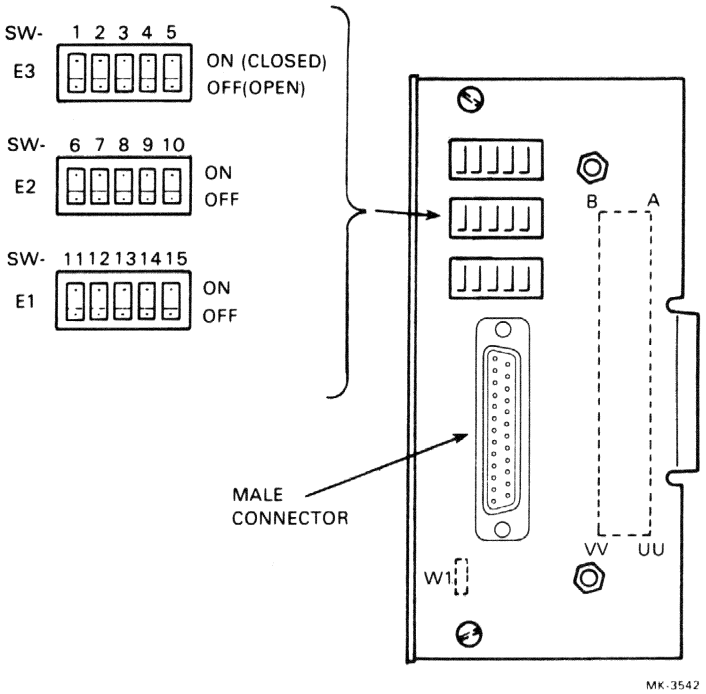

Figure F-10 H3001 Distribution Panel

Table F-2 H3001 Switch Settings

	DF03	Bell 201C™	Bell 208B™	Bell 209A™	Diagnostics & H325
S1					ON
S2					
S3					
S4					
S5					ON
S6					
S7					
S8					
S9					
S10		*			
S11					
S12					
S13					
S14					
S15					

NOTE: Switches are off unless otherwise indicated.
***On if new sync configured on M7867**
201™, 208™, and 209™ are trademarks of Western Electric.

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