EK-KMV11-UG-001

KMV11 Programmable Communications Controller User Guide

Course Prepared by Educational Services
of
Digital Equipment Corporation

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PREFACE

This user's guide describes how to use the KMV11 communications controller. It describes all the functional elements of the KMV11 communications controller and the way user-developed firmware can control those elements.

Other documents which support the KMV11 programmable communications controller are:

- KMV11 Technical Manual (EK-KMV11-TM-001)
- DCT11-AA Microprocessor User Guide (EK-DCT11-UG-001)
- NEC uPD7201 Multi-Protocol Serial Controller Technical Manual (NEC Electronics (Europe) GmbH)
- Microcomputer Processor Handbook (DIGITAL)
- Microcomputer Interface Handbook (DIGITAL)

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This chapter contains a short introduction to the operation of the KMV11. The term KMV11, as used throughout this manual, means the programmable communications controller.

In this manual the term firmware is used in relation to the KMV11, and means any set of instructions which is contained in the KMV11's memory space, and is to be interpreted and executed by the DCT11 microprocessor.

Root Firmware resides within the ROM space of the KMV11 and is a permanent component of the KMV11.

Application Firmware is to be loaded into the RAM space of the KMV11 at system startup time or after power failure.

1.2 KMV11 GENERAL DESCRIPTION

The KMV11 is designed to be used in a communication link by Q-bus-based systems. The KMV11 is microprocessor based and able to perform functions for bit-oriented synchronous protocols (like HDLC), byte-oriented synchronous protocols (like BSC), or asynchronous protocols. The application firmware defines the computer instructions that are needed to execute the protocol-related activities.

Features of the KMV11 include:

1. Direct Memory Access (DMA) across the Q-bus for medium-speed transmission and reception
2. A DCT11 microprocessor with the PDP-11 base-level instruction set
3. A 7201 PUSART (Programmable Universal Synchronous Asynchronous Receiver/ Transmitter) line controller chip
4. EPROM of 4K bytes, with root firmware and power-up self-test diagnostics
5. Customer-developed application firmware uses the PDP-11 instruction set
6. RAM space of 32K bytes, for implementation of data-link protocols.
7. Synchronous (bit-oriented or byte-oriented) as well as asynchronous capabilities for the application firmware
8. Extensive support of modem signals
9. On-board RS-422-A, RS-423-A (CCITT V.11, V.10) electrical interfaces

10. RS-232-C (CCITT V.28) compatible

11. An on-board null modem clock.

The KMV11, by using a microprocessor with a PDP-11 instruction set, makes the development of the application firmware more easy.

1.3 SYSTEM OPERATION

Communication of control and status information between the host and the KMV11 uses 8 words (16 bytes) of control and status registers (CSRs). These have addresses from 76xx00 to 76xx17. These device addresses are from here on referred to as 'byte select 0 to 17' (BSEL0 to BSEL17) for indicating individual bytes, and as 'select 0 to 16' (SEL0 to SEL16) for indicating individual words.

BSEL1 is defined by the KMV11's root firmware routines for the following functions:

1. Diagnostic firmware self-test execution
2. Application mode control
3. Special maintenance functions

In application mode, function bits are defined to load, unload, and run application firmware.

Before the KMV11 is able to execute the application firmware, this firmware must be loaded into the RAM of the KMV11.

In order to recover the contents of the RAM, an unload function is provided by the root firmware.

To start the execution of the application firmware, the host can pass to the KMV11 root firmware the start address of the application firmware.

1.4 CSR LAYOUT

Figure 1-1 shows the layout of the CSRs in the host processor I/O page.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
BSEL1								BSEL0								SEL0
BSEL3								BSEL2								SEL2
BSEL5								BSEL4								SEL4
BSEL7								BSEL6								SEL6
BSEL11								BSEL10								SEL10
BSEL13								BSEL12								SEL12
BSEL15								BSEL14								SEL14
BSEL17								BSEL16								SEL16

RD 959

Figure 1-1 CSR Definitions

1.5 BSEL1 DEFINITIONS

Figure 1-2 shows the BSEL1 layout.

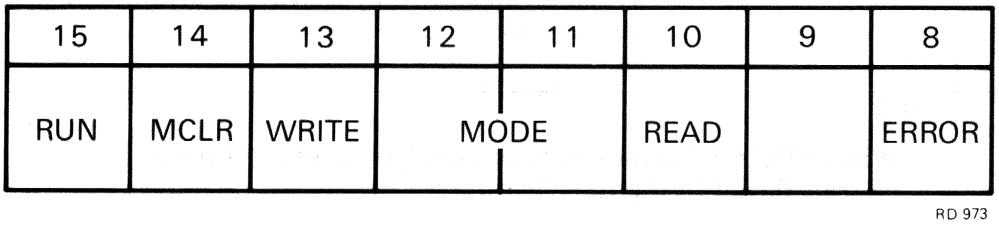


Figure 1-2 BSEL1 Definitions

Bit	Name	Function
8	Error	This bit will be set when an illegal address is specified during reading or writing in the KMV11 RAM memory. It will also be set when the address specified with the run command is illegal.
10	Read	This bit, when set, directs the root firmware to the memory read routine. The contents of SEL4 will be used as the memory address. The contents of the memory location will be returned in SEL6.
11 12	Mode	These two bits define the KMV11 mode of operation. 0 – Application mode Allows the root firmware to execute a read or a write routine, depending on the content of bits 10, 13, and 15. 1 – Reserved 2 – Maintenance mode 1 Test routines in the root firmware are executed. 3 – Maintenance mode 2 The root firmware clears master clear (MCLR) and puts itself in a continuous loop. For normal operation, these bits will always be cleared on power-up or master clear to enable the application mode.
13	Write	This bit is used in application mode. When set, it requests the loading of the contents of SEL6 into the KMV11 at the address specified in SEL4.
14	MCLR (Master Clear)	When set, this bit requests power-up initialization to clear the hardware and restart the root firmware in the mode defined by the mode bits. The bit is cleared by the KMV11 on completion of initialization.

15	Run	When this bit is set after MCLR, in the application mode, program control is transferred from root firmware to the application firmware starting at the address contained in SEL4. When set together with MCLR, the self-test is executed, before starting operation.

NOTE

When a HALT instruction is executed, program control will be transferred to the root firmware.

1.6 KMV11 — HOST INTERACTION

To define the direction of data transfer between the host and the KMV11 the terms 'IN' and 'OUT' are used throughout this manual:

'IN' applies to transfer from the host to the KMV11

'OUT' applies to transfer from the KMV11 to the host.

The terms 'TRANSMIT' and 'RECEIVE' ('TX' and 'RX') are used in conjunction with data transmitted or to be transmitted on to the communications line or received from the communications line.

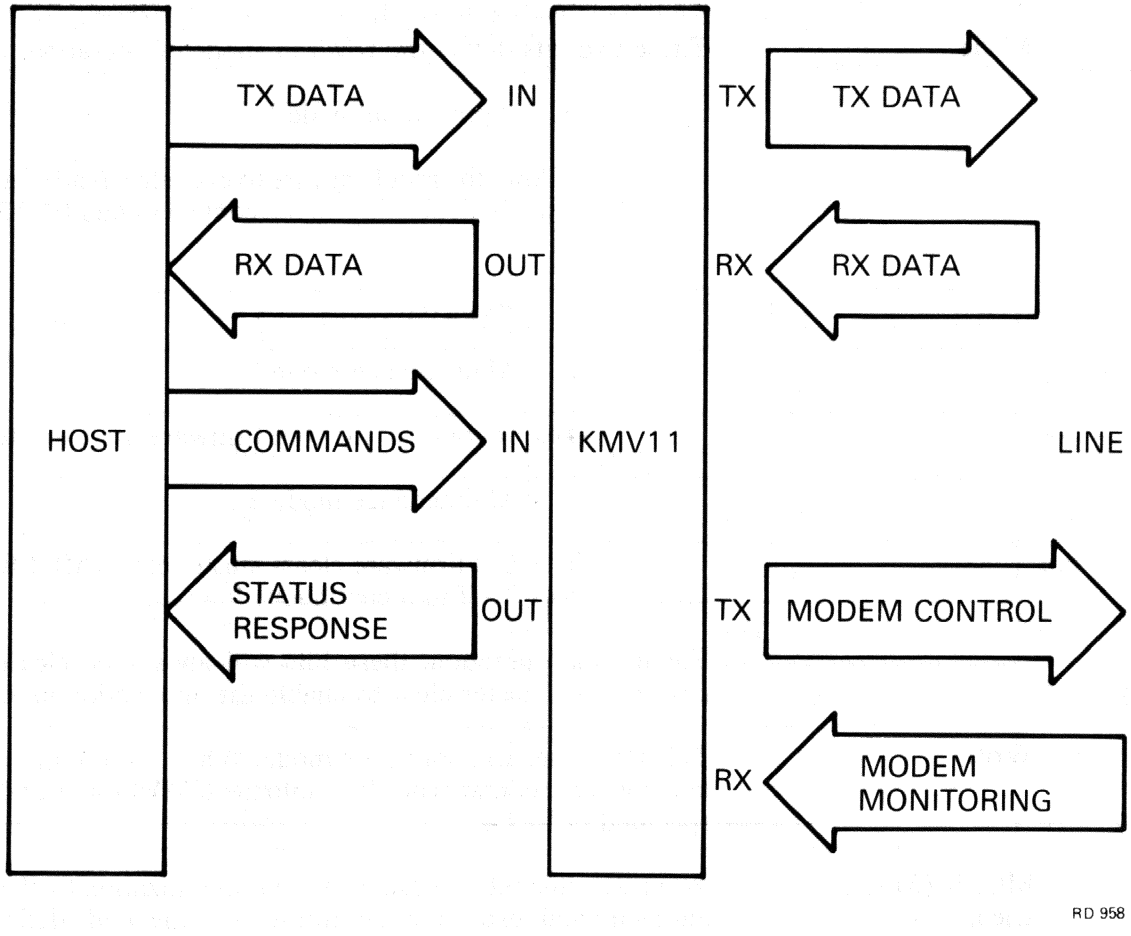


Figure 1-3 HOST — KMV11 Interaction

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter provides all the information necessary for installing and testing the KMV11. A checklist, which can be used to verify the installation process, is also included.

2.2 UNPACKING AND CHECKOUT

The KMV11 is packed according to commercial packing practices. When unpacking, remove all packing material and check the equipment against the shipping list (Table 2-1 contains a list of items shipped with each configuration). Examine all parts and carefully check the M7500 module for obvious signs of damage. Check the received components against the shipping list. Where necessary, report damages or shortages to the shipper and inform the DIGITAL representative.

Table 2-1 KMV11 Packing Lists

KMV11-A Suboption Packing List

Part Number	Description
M7500	Line unit module
H3255	Module test connector
EK-KMV11-TM-001	KMV11 Technical Manual
EK-KMV11-UG-001	KMV11 User's Guide
MP01173	Customer print set

KMV11-AA RS-232 Option Packing List

Part Number	Description
KMV11-A	Basic suboption
BC55H	RS-232 cable assembly
H325	Cable loopback connector RS-232

KMV11-AE RS-422 Option Packing List

Part Number	Description
KMV11-A	Basic suboption
BC55U	RS-422 cable assembly
H3251	Cable loopback connector RS-449

Table 2-1 KMV11 Packing Lists (Cont)

KMV11-AF RS-423 Option Packing List

Part Number	Description
KMV11-A	Basic suboption
BC55P	RS-423 cable assembly
H3251	Cable loopback connector RS-449

The diagnostics for the KMV11 are released through the Software Distribution Center (SDC). The following options can be ordered separately by self-maintenance customers:

- ZJ-360-RZ diagnostic documentation kit
- ZJ-360-FR diagnostic fiche kit
- ZJ-360-PY diagnostic RX01 kit

2.3 INSTALLATION PHASES

Installation of the KMV11 should be done in four phases:

1. Phase I – Preinstallation

   Verify KMV11 requirements with respect to power and location within the system.

2. Phase II – M7500 installation

   Configure the M7500 module for the customer application.
   Install the M7500 module and verify its operation, using the appropriate diagnostics.

3. Phase III – Modem cable assembly installation

   Install the cable, lay the cable, and verify cable and module via the appropriate diagnostics.

4. Phase IV – KMV11 system testing

   Verify the complete KMV11 subsystem operation with the functional diagnostics and system exercise programs.

2.4 PREINSTALLATION CONSIDERATIONS

The preinstallation phase checks that the host system is capable of receiving the KMV11 option.

2.4.1 Mounting Space

The KMV11 needs one quad slot with the Q-bus connected to slots A and B. The Q-bus signals may also be connected to slots C and D but will not be used there. BDMG and BIAK lines are connected through on the C and D module connector.

2.4.2 Power Requirement

+5 V @ 2.6 A
+12 V @ 0.2 A

2.4.3 Modem Cable Assembly Requirements

The BC55H, BC55U, and BC55P modem cable assemblies are designed to be mounted on the H349 bulkhead connector panel. This bulkhead panel is normally provided with PDP-11/23+ or PDP-11/23B systems.

In conditions where the H349 is not available, the BC55H, BC55U, and BC55P modem cable assemblies may be screwed onto the vertical cabinet mounting rails, normally drilled at EIA spacings.

2.5 M7500 INSTALLATION

2.5.1 Voltage Check

Before installing the M7500 module:

- Verify that the +5 V supply voltage at backplane pin AA2 is between +4.85 V and +5.15 V
- Verify that the +12 V supply voltage at backplane pin AD2 is between +11.64 V and +12.36V.

2.5.2 Switch Settings

Check that the switch settings and jumper configurations meet the system and customer requirements.

2.5.2.1 Address Switches:

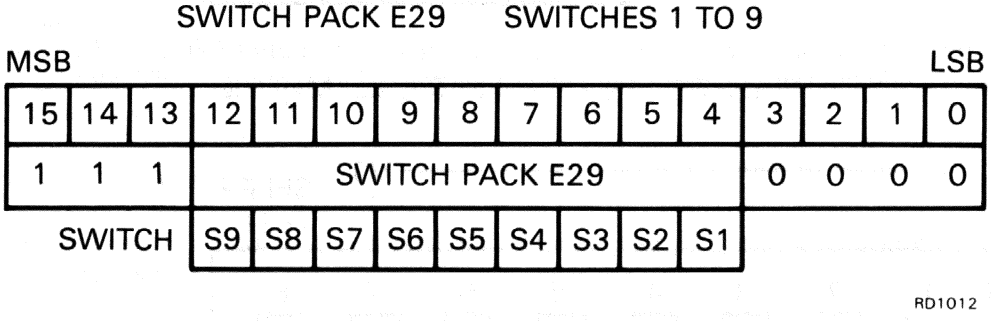


Figure 2-1 Address Switch Register Mapping

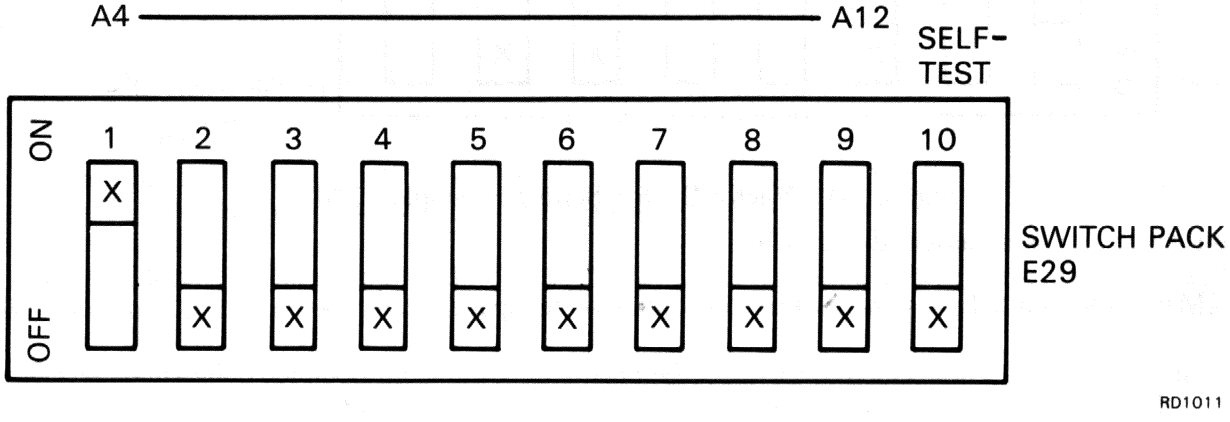


Figure 2-2 Address Switch Setting Example: 760020_8

An 'on' switch matches an asserted address bit.

The KMV11 address is to be assigned within the floating address space at rank 31. It occupies eight CSR addresses (for example, 760020_8 to 760036_8).

NOTE

The term 'rank' has no hardware significance. It denotes the position of the address in a table used by auto-configuration programs.

2.5.2.2 Vector Switches

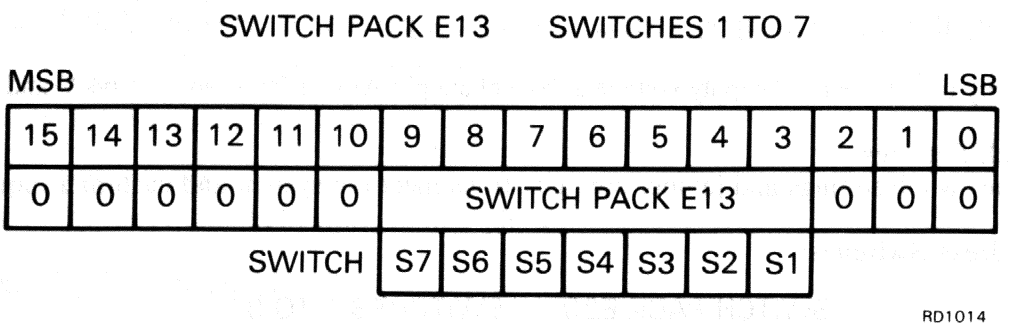


Figure 2-3 Vector Switch Register Mapping

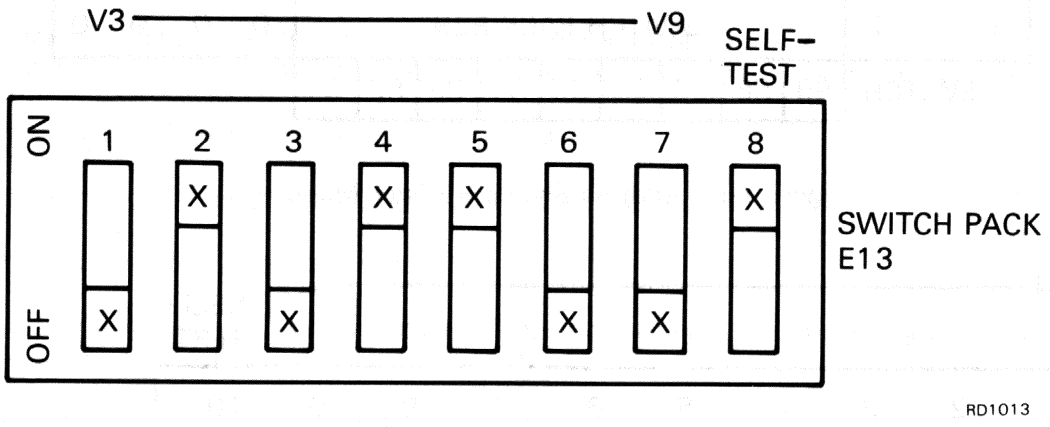


Figure 2-4 Vector Switch Setting Example: 320

An 'on' switch gives an asserted vector bit.

The KMV11 vector is to be assigned within the floating vector space at rank 54.

NOTE

The term 'rank' has no hardware significance. It denotes the position of the address in a table used by auto-configuration programs.

The other two switches on E13 and E29 affect self-test operation in the following way:

E13 SW8	E29 SW10		Self-Test Operation
ON	ON	=	Self-test disabled
ON	OFF	=	Self-test enabled (start via CSR command or at power up, for one pass)
OFF	OFF	=	Self-test manual start for continuous loop
OFF	ON	=	Extended self-test start for continuous loop

2.5.3 Jumper Configurations

1. Extended address jumpers

   Links W3, W4, and W7 to W10 are normally installed to allow extended addressing (BDAL 16 to 21). They should only be removed when the extended address lines (SPARE lines on older LSI configurations) are in contention with other signals.

2. BDMG and BIAK jumpers

   Links W11 and W13 are normally installed to provide BDMG and BIAK continuity in the C and D slots. They should only be removed when the corresponding backplane pins are used for other purposes.

3. Factory test jumpers

   Links W2 and W12 are only removed during factory module testing. They must be installed for normal KMV11 operation.

The other switches and jumpers depend on the modem interface characteristics as shown in the following notes and in Figure 2-5.

All other combinations of switches 1 to 8 are illegal.

E85 switch 9 OFF isolates pin 29 of the connector assemblies (CCITT 107). It should normally be ON, and only OFF when a modem connects a different signal to this pin.

E85 switch 10 OFF isolates pin 2 of the connector assemblies (CCITT 112). It should normally be ON, and only OFF when a modem connects a different signal to this pin.

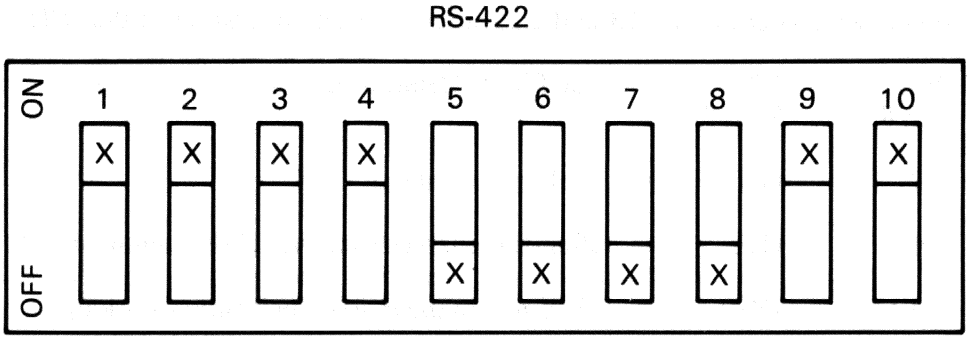
Jumper W15 forces modem signal CCITT 109 (Carrier Detect) permanently to the active (1) state . This link is normally not installed.

Jumper W14 installed connects modem signal Terminal In Service to connector assemblies pin 28. This signal is not used by most modems, but is needed for loopback testing using the H3251 loopback connector. It should therefore only be removed in situations where its presence causes a problem with the modem.

KMV11-AE, RS-422

SWITCH

1 ON
2 ON
3 ON
4 ON
5 OFF
6 OFF
7 OFF
8 OFF



KMV11-AA/AF,
RS-423, RS-232-C

SWITCH

1 OFF
2 OFF
3 OFF
4 OFF
5 ON
6 ON
7 ON
8 ON

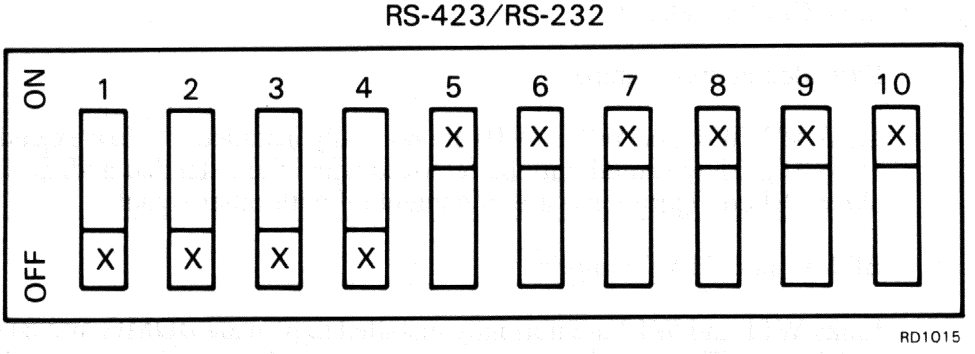


Figure 2-5 RS-422 Versus RS-423 (RS-232) on Switch Pack E85

2.5.4 Standard Switch Setting and Jumper Configuration for KMV11-A

Table 2-2 KMV11-A Switch Register and Jumper Settings

E29	Switch	1	ON	Address = 776020
		2	OFF	
		3	OFF	
		4	OFF	
		5	OFF	
		6	OFF	
		7	OFF	
		8	OFF	
		9	OFF	
E13	Switch	1	OFF	Vector = 320
		2	ON	
		3	OFF	
		4	ON	
		5	ON	
		6	OFF	
		7	OFF	
E29	Switch	10	OFF	Self-test enabled
E13	Switch	8	ON	Runs for one pass at power-up or via CSR command

Table 2-2 KMV11-A Switch Register and Jumper Settings (Cont)

W3	IN	Extended address bits 16 to 21 connected to Q-Bus
W4	IN	
W7	IN	
W8	IN	
W9	IN	
W10	IN	
W6	OUT	Not used
W11	IN	BDMG and BIAK continuity made in slots C and D
W13	IN	
W2	IN	DMA clock enabled
W12	IN	Microprocessor clock enabled

Table 2-3 KMV11-AA/AF Additional Switch and Jumper Settings

E85	Switch	1	OFF	RS-423-A/RS-232-C selected
		2	OFF	
		3	OFF	
		4	OFF	
		5	ON	
		6	ON	
		7	ON	
		8	ON	
		9	ON	CCITT 107, connected
		10	ON	CCITT 112, connected
W15	OUT			CCITT 109 (Carrier Detect) follows input
W14	IN			Terminal In Service connected.

Table 2-4 KMV11-AE Additional Switch and Jumper Settings

E85	Switch	1	ON	RS-422-A selected
		2	ON	
		3	ON	
		4	ON	
		5	OFF	
		6	OFF	
		7	OFF	
		8	OFF	
		9	ON	CCITT 107, connected
		10	ON	CCITT 112, connected
W15	OUT			CCITT 109 (Carrier Detect) follows input
W14	IN			Terminal In Service connected.

2.5.5 M7500 Insertion

When you have checked supply voltages and configured the M7500 module, you may insert the module in the selected Q-bus slot. Make sure that system power is off while inserting the module.

After insertion of the module, power up and check that the supply voltages have stayed within acceptable limits.

Perform the following quick test on the module:

1. Deposit 0 into the base address
2. Examine the base address; it should be 0
3. Deposit 44000_8 into the base address
4. Examine the base address; it should be 4000_8.

If the above test does not give the expected result, the installation must not be continued, the M7500 module must be either replaced or repaired.

2.6 MODEM CABLE ASSEMBLY INSTALLATION

At this step the connector assemblies should be installed.

2.6.1 BC55H/BC55U/BC55P Considerations

In order to install modem cable assemblies correctly, the H349 bulkhead connector panel with free slots in J12, J13, J14, or J15 should be available. Otherwise the cable assembly may be screwed directly to the vertical cabinet mounting rails, selecting a proper location where the EIA spaced holes of the mounting rail match the holes of the connector assembly.

Before installing the BC55H, BC55U, or BC55P, verify and configure the appropriate modem line jumpers.

Refer to Table 2-5 for the configuration of the BC55H, BC55U, or BC55P.

Table 2-5 BC55H, BC55U, and BC55P Jumper Settings

J2 PIN	JUMPER	RS-232-C	BELL 103J	BELL 208B	BELL 209	DATEL 200	DATEL 600	DATEL 2400	DATEL 4800	CCITT V.21	CCITT V.23	CCITT V.26B	CCITT V.27T	ISO2110-1972	ISO2110.2	ISO2110.2	EIA RS-232-C	EIA RS-449	CCITT V.24
																FUTURE D			
																X.21BIS			
																X.20BIS			
23	W1	IN				IN	IN	IN		IN	IN	IN	IN	IN		CH	SR	111
21	W2	IN		IN												CG	SQ	110
11	W3				IN				IN				IN				SF	126
23	W4															CI	SF	112
16	W5	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	SBB	SRD	119
14	W6	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	SBA	SSD	118
12	W7	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	SCF	SRR	122
21	W8								IN					IN	IN		RL	140
4	W9	IN		IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	CA	RS	105
15	W10	IN		IN	IN			IN	IN		IN	IN	IN	IN		DB	ST	114
17	W11	IN		IN	IN			IN	IN		IN	IN	IN	IN		DD	RT	115
18	W12								IN					IN	IN		LL	141
19	W13	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	SCA	SRS	121
	W14	NOT NORMALLY INSTALLED																
25	W15								IN					IN	IN		TM	142
24	W16	IN		IN	IN			IN			IN	IN		IN	IN	DA	TT	113
25	W17						IN										SB	117
24	W18						IN										SS	116
13	W19	IN				IN	IN	IN		IN	IN	IN	IN	IN	IN	SCB	SCS	121
25	W20															MAKE BUSY		
1	W21	IN	IN	IN	IN	IN	IN	IN					IN			AA		101
2																BA	SD	103
3																BB	RD	104
5																CB	CS	106
6																CC	DM	107
7																AB	SG	102
8																CF	RR	109
20																CD	TR	108
22																CE	IC	125

MK-2725

2.6.2 BC55H, BC55U, and BC55P Installation on the H349 Panel

When the connector panel is configured, it may be mounted onto the H349 bulkhead panel into any available slot from J13 to J15. Refer to Figure 2-6 for the correct panel mounting.

Connect the BC08-S flat cable between the connector panel and the M7500 module, providing a point-to-point connection. To do this, one connector end should have the ribbed side up, the other end the smooth side up. Complete the physical installation by neatly dressing and attaching the cable to the H349.

Refer to Paragraph 2.7 for the KMV11 checkout.

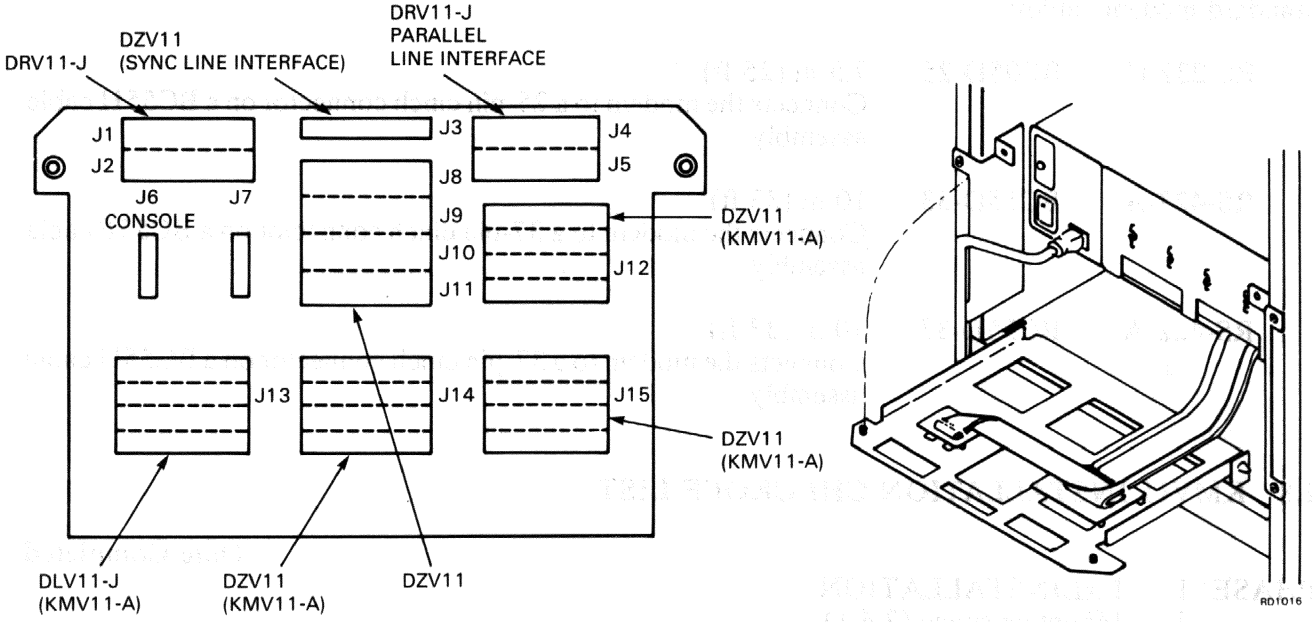


Figure 2-6 Connector Panel Installation

2.6.3 BC55H, BC55U, and BC55P Installation Without H349 Panel

When you have selected the appropriate mounting space and checked the jumper configuration, you may mount the connector panel to the cabinet frame, tightening the screws hard to provide a good shield to ground continuity.

Then connect the BC08-S flat cable between the connector panel and the M7500 module, providing a point-to-point connection.

2.7 KMV11 SYSTEM TESTING

When the physical installation of the KMV11 has been completed, it should be tested by means of the diagnostic programs.

2.7.1 Functional Diagnostic Testing.

The functional diagnostic VKMC exercises the KMV11 in a standalone mode. Make sure, before starting the diagnostic, that either the H3251 or H325 cable test connector is fitted to the cinch connector at the cable assembly panel, or the H3255 module test connector is fitted on the M7500 module.

Allow the diagnostic to run for at least five error-free passes.

If errors occur, refer to Chapter 5 to perform corrective maintenance.

2.7.2 DEC-X11 System Exerciser

The DEC-X11 system exerciser, CXKMD, will run the host, peripherals, and KMV11 in a worst-case environment similar to a user's operating system. Any error message calls for corrective maintenance to be performed. Refer to Chapter 5 for corrective maintenance.

2.7.3 Final Cable Connections

After the successful completion of diagnostic testing, remove all test connectors and install the modem or null modem cables as needed by the application.

Standard modem cables:

RS-232-C	BC05D-25	7.5 m (25 ft) Connects the modem to a 25-pin cinch connector on a BC55H cable assembly
RS-423-A	BC55D-33	10 m (33 ft) Connects the modem to a 37-pin cinch connector on a BC55P cable assembly
RS-422-A	BC55D-33	10 m (33 ft) Connects the modem to a 37-pin cinch connector on a BC55U cable assembly

2.8 KMV11 INSTALLATION CHECKOFF LIST

Date Completed

PHASE I PREINSTALLATION

1. Mounting space (2.4.1)
2. Power requirements (2.4.2)
3. Modem cable requirements (2.4.3)

PHASE II M7500 INSTALLATION

1. Unpack, check for full shipment (2.2)
2. Backplane voltages (2.5.1)
3. Switches configured (2.5.2)
   (2.5.4)
4. Jumpers configured (2.5.3)
   (2.5.4)
5. M7500 installed (2.5.5)
6. Backplane voltages (2.5.1)
7. M7500 quick check (2.5.5)

PHASE III MODEM CABLE ASSEMBLY INSTALLATION

1. H349 or mounting space on cabinet frame available for BC55H/U/P (2.6.1)
2. BC55H/U/P configured (2.6.1)
3. BC55H/U/P installed (2.6.2)
   (2.6.3)
4. BC08-S installed and connected (2.6.2)
   (2.6.3)

PHASE IV KMV11-A SYSTEM TESTING

1. Test connectors fitted (2.7.1)
2. Functional diagnostics (2.7.1)
3. DECX-11 exerciser (2.7.2)
4. Test connectors removed, modem cables installed (2.7.3)

CHAPTER 3
APPLICATION MODE

3.1 CSR DESCRIPTION

In application mode the KMV11 may use all the eight CSRs available, to provide communication between the host and the KMV11's application firmware. The CSRs have addresses from 76xx00 to 76xx16; they are also referred to as BSEL0 to BSEL17 for indicating individual bytes, and as SEL0 to SEL16 for indicating individual words.

However, only the low-order bytes of the first two CSRs will generate an interrupt in the front-end microprocessor when there are bit changes.

3.2 BSEL1 DEFINITIONS

The run bit, together with the master clear (MCLR) bit, determines whether the self-test is executed or not. If the MCLR bit is set with the run bit clear, then the application firmware is executed. If the MCLR bit is set together with the run bit, then the self-test is executed first.

The KMV11 will indicate that it is ready to accept application commands by clearing the MCLR bit. If the run bit is still set, it means that the self-test has failed.

The read, write, and run bits can then be used to load, unload, or start the application firmware. The error bit is used by the root firmware to indicate errors in the read, write, or run command parameters.

15	14	13	12	11	10	9	8
RUN	MCLR	WRITE	0	0	READ	0	ERROR

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Figure 3-1 BSEL1 Bit Layout in Application Mode

Bit	Name	Function
8	Error	This bit will be set to 1 after a read, write, or run error (odd or nonexistent address).
9		This bit must be 0 in application mode.
10	Read	This bit should be set if data is to be read from the front-end RAM memory.
11		This bit must be 0 in application mode.
12		This bit must be 0 in application mode.

Bit	Name	Function
13	Write	This bit should be set if data is to be written to the front-end RAM memory.
14	MCLR (Master Clear)	When set, this bit requests power-up initialization to clear the hardware and restart the root firmware. The bit is cleared by the KMV11 on completion of initialization.
15	Run	When this bit is set together with the MCLR bit, the self-test will be executed. If an error occurs the run bit will stay set when the MCLR drops. When it is set without the MCLR bit, transfer to the application firmware transfer address will be performed.

3.3 LOADING AND STARTING APPLICATION FIRMWARE

Load and/or compare example:

```
;+
; load and start the KMV11
;
; R0 = number of words to write
; R3 = CSR of the KMV
; R5 = RAM LOAD ADDRESS
;
; BUFF = buffer containing the instructions
; START= firmware start address
; S.LOAD = flag in STATUS to indicate load (1) or compare (0)
;
; MCLR = BSEL1 MASTER CLEAR
; RUN  = BSEL1 RUN
; READ = BSEL1 READ
; WRITE= BSEL1 WRITE
; ERROR= BSEL1 ERROR
;
; Note:
;
;    In an actual program the wait loops should be made to
;    guard against a system hang in the event of hardware
;    failure.  Self-test execution takes about 30 seconds.
;-
        CLRB    1(R3)             ;MAKE SURE MASTER CLEAR IS
                                  ;CLEARED
        MOVB    #MCLR,1(R3)       ;MASTER CLEAR KMV11
; or
        MOVB    #MCLR!RUN,1(R3)   ;MASTER CLEAR KMV11
                                  ;AND START SELF-TEST
1$:     BITB    #MCLR,1(R3)       ;KMV11 ACK
        BNE     1$                ;WAIT
                                  ;FOR POSSIBLE SELF-TEST:
        BITB    #RUN,1(R3)        ;RUN BIT CLEARED?
        BNE     25$               ;BRANCH FOR POSSIBLE ERROR
```

```
        MOV     #BUFF,R4        ;GET BUFFER ADDRESS
10$:    BIT     #S.LOAD,STATUS  ;IS IT A LOAD?
        BEQ     15$             ;BR IF COMPARE
        MOV     R5,4(R3)        ;LOAD ADDRESS IN SEL4
        MOV     (R4),6(R3)      ;LOAD DATA IN SEL6
        BISB    #WRITE,1(R3)    ;LOAD THE DATA
11$:    BITB    #WRITE,1(R3)    ;ACK?
        BNE     11$             ;WAIT
        BITB    #ERROR,1(R3)    ;ERROR?
        BNE     25$             ; QUIT

15$:    MOV     R5,4(R3)        ;LOAD ADDRESS IN SEL4
        BISB    #READ,1(R3)     ;READ THE DATA
16$:    BITB    #READ,1(R3)     ;ACK?
        BNE     16$             ;WAIT
        BITB    #ERROR,1(R3)    ;ERROR?
        BNE     25$             ; QUIT

        CMP     (R4),6(R3)      ;COMPARE DATA
        BNE     25$             ;ERROR
        ADD     #2,R4           ;NEXT BUFFER ADDRESS
        ADD     #2,R5           ;NEXT LOAD ADDRESS
        DEC     R0              ;UPDATE COUNTER
        BNE     10$             ; NEXT...

        MOV     #START,4(R3)    ;SET START ADDRESS OF FIRMWARE
        MOVB    #RUN,1(R3)      ;START IT
17$:    BITB    #RUN,1(R3)      ;ACK?
        BNE     17$             ;WAIT
        BITB    #ERROR,1(R3)    ;ERROR?
        BNE     25$             ; QUIT

        CCC                     ;SUCCESS
        BR      30$             ; DONE

25$:    SEC                     ;ERROR
30$:    RETURN
```

CHAPTER 4
APPLICATION FIRMWARE DEVELOPMENT

4.1 KMV11 I/O PROGRAMMING

Five functional elements make up the I/O section of the KMV11. These elements provide the communications path between the host and the line(s).

The line end is made up of:

- The PUSART (Programmable USART) integrated circuit
- Modem control and monitor registers
- The line clock generators used for null modem connections and maintenance purposes.

The host interface is made up of the CSR or SEL registers and DMA registers.

In addition miscellaneous logic is provided to generate Q-bus DC OK assertion, as well as a real-time clock to implement communication protocol timer functions.

The information contained in the following sections should enable the application firmware programmer to design efficient HDLC or SDLC front-end firmware.

The architecture of the KMV11 is primarily designed for dual-line operation. The basic version (KMV11-A), however, provides line transmitters and receivers for one line only. This document is valid for both single- and dual-line configurations. Differences between the two will be pointed out in the appropriate section.

4.1.1 Front-End Processor Address Space

The DC111 microprocessor address space is divided into three sections: a read-write memory section of 16K words, a read-only memory section of 4K words, and an I/O address space of 12K words.

NOTE

Addresses are given in octal notation in this chapter.

4.1.2 I/O Register Assignment

Within the I/O register space, from $100\,000_8$ to $160\,000_8$, are the locations of the device registers for the five functional components. Each component has a subaddress space of $10\,000_8$ bytes.

The functional component subaddress spaces are:

1. CSR and DMA registers (100 000 to 107 777)
2. Line controller IC (integrated circuit) (110 000 to 117 777)
3. Clock IC (120 000 to 127 777)
4. Peripheral port IC (130 000 to 137 777)
5. Q-bus control (140 000 to 147 777).

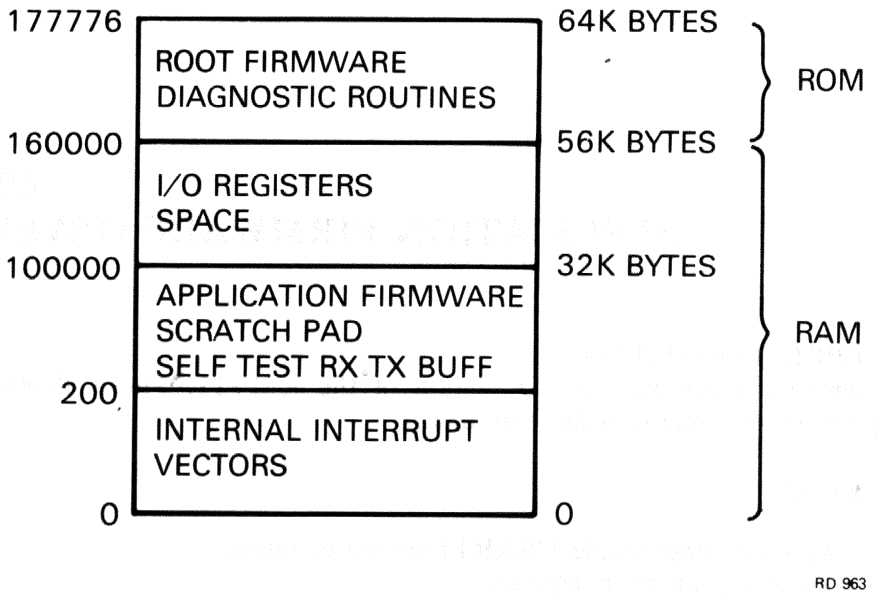


Figure 4-1 KMV11 Memory Map

Address Range	Destination	Address	Registers	
100 000 107 777	CSR RAM	100 000	CSR 0	R/W
		100 002	CSR 2	R/W
		100 004	CSR 4	R/W
		100 006	CSR 6	R/W
		100 010	CSR 10	R/W
		100 012	CSR 12	R/W
		100 014	CSR 14	R/W
		100 016	CSR 16	R/W
		100 020	DMA DATA IN	R/W
		100 022	DMA DATA OUT	R/W
		100 024	DMA ADDRESS IN	R/W
		100 026	DMA ADDRESS OUT	R/W
		100 030	ROOT FW SCRATCH	R/W
		100 032	ROOT FW SCRATCH	R/W
		100 034	EXTENDED ADDR IN	R/W
		100 036	EXTENDED ADDR OUT	R/W
110 000 117 777	7201 PUSART	110 000	CHA RX BUF	RO
		110 002	CHA TX BUF	WO
		110 004	CHA STATUS	RO
	(only low-order bytes are used)	110 006	CHA COMMAND	WO
		110 010	CHB RX BUF	RO
		110 012	CHB TX BUF	WO
		110 014	CHB STATUS	RO
		110 016	CHB COMMAND	WO

Address Range	Destination	Address	Registers	
120 000 127 777	8254 Timer	120 000	LINE CLOCK 1 RD	RO
		120 002	LINE CLOCK 1 WR	WO
		120 004	LINE CLOCK 2 RD	RO
	(only low-	120 006	LINE CLOCK 2 WR	WO
	order bytes	120 010	RT CLOCK RD	RO
	are used)	120 012	RT CLOCK WR	WO
		120 014	not used	–
		120 016	CLOCK CONTROL WR	WO
130 000 137 777	8255 I/O	130 000	A PORT READ	RO
		130 002	not used	–
		130 004	not used	–
	(only low-	130 006	C PORT WRITE	WO
	order bytes	130 010	not used	–
	are used)	130 012	B PORT WRITE	WO
		130 014	not used	–
		130 016	8255 CONTROL WR	WO
140 000 147 777	Q-bus Control	140 000	QIRQ, QDCOK	WO
150 000 157 777		RESERVED		

RO = Read-Only register
WO = Write-Only register
R/W= Read-Write register

NOTE

Only MOV or MOVB instructions may be used to operate on RO and WO registers. Instructions which first read, then perform changes in internal processor registers and write the results back like INC, BICB, BISB, ADC, and so on, may only be used with R/W registers.

4.1.3 Front-End Processor Interrupt System

The DCT11 microprocessor uses a 4-level interrupt system with eight hardwired vectors. For a detailed explanation of the leveled and vectored interrupts of the DCT11 microprocessor please refer to the DCT11 Microprocessor User's Guide, Chapters 1 to 5.

Vector assignments and priorities are as follows:

Requesting Device	Priority	Vector
RX data channel A	7	140
RX data channel B	7	150
TX data channel A	6	100
TX data channel B	6	110
PUSART special cond.	5	120
Timer	5	130
CSR 0 transaction	4	60
CSR 2 transaction	4	70

NOTE

These interrupts are not self-clearing. A request stays as long as the interrupting condition has not been taken care of.

To acknowledge the interrupts, the following actions have to be taken for each of the listed interrupt conditions:

RX DATA channel A vector 140	Read channel A receive buffer
RX DATA channel B vector 150	Read channel B receive buffer
TX DATA channel A vector 100	Load channel A transmit buffer
TX DATA channel B vector 110	Load channel B transmit buffer
PUSART special conditions vector 120	Issue a Reset External/Status Interrupts (RE/SI) command Refer to Section 4.3, Line Controller Interface
Timer vector 130	Disable RTC, enable RTC for next timer interrupt (port C, bit D0)
CSR 0 transaction vector 60	Disable CSR 0 interrupt, enable CSR 0 interrupt for next CSR 0 transaction (port C, bit D6)
CSR 2 transaction vector 70	Disable CSR 2 interrupt, enable CSR 2 interrupt for next CSR 2 transaction (port C, bit D7).

4.2 CSR AND DMA INTERFACE

4.2.1 CSR and DMA Address Register Description

Addresses 100 000 to 100 016 are implemented within the 'CSR RAM'. These eight words are referred to as CSR or SEL registers, and can be accessed by the host to implement data ports for command and response transactions. Except as stated below, bits may be assigned according to the desired host to front-end interaction.

Exception:

- BSEL1 (address 100 001) is used by the root firmware and should not be reassigned.

The use of BSEL0 and/or BSEL2 is recommended for implementation of a handshake protocol between host and front-end. This is because a write access from the host to either BSEL0 or BSEL2 may generate a vectored interrupt in the front-end processor if this feature has been enabled. (See the description in Appendix A of the KMV11 Technical Manual.)

Address 100 020 is the 'DMA data in' register. Data requested via DMA from the host's memory may be read in this register.

Address 100 022 is the 'DMA data out' register. Data to be transferred via DMA into the host memory will be written into this register.

Address 100 024 is the 'DMA address in' register. The contents of this location specify the 16 low-order bits of the host memory address used for a 'DMA in' transfer.

Address 100 026 is the 'DMA address out' register. The contents of this location specify the 16 low-order bits of the host memory address used for a 'DMA out' transfer.

Addresses 100 030 and 100 032 are reserved locations for use by the root firmware.

Address 100 034 is the 'extended address in' register. The contents of its low-order byte specify the six high-order bits of the host memory address used for a 'DMA in' transfer. The DMA itself is initiated by the action of writing to this location.

Address 100 036 is the 'extended address out' register. The contents of its low-order byte specify the six high-order bits of the host memory address used for a 'DMA out' transfer. The DMA itself is initiated by the action of writing to this location.

Register Bit Low-Order Byte	XADDR Bit
0	16
1	17
2	18
3	19
4	20
5	21

4.2.2 CSR and DMA Programming

The interface to the Q-bus host is made up of two main functional elements:

1. CSR interface
2. DMA interface.

The CSR interface is made up of eight 16-bit registers, which can be accessed by the DCT11 microprocessor, using the addresses from 100 000 to 100 016. This dual-port memory can be accessed by the host at addresses from 76xx00 to 76xx16 (xx is defined by on-board DIP switch settings). Bit 14 of SEL0, when set by the host, generates an unmaskable HALT interrupt, which restarts the root firmware.

Except for the above-stated functions, all the other register bits may be defined to set up any desired host to front-end interaction. Use of the low-order bytes of SEL0 and/or SEL2 is recommended for handshaking protocol, as a write by the host to the low-order bytes of these registers will generate an interrupt in the front-end processor at vector 60 and vector 70, in that order. To enable these interrupts, the priority of the processor must be lower than level 4, and individual CSR interrupt enable bits must be set.

1. CSR0 interrupt enable: port C bit D6 = 1
2. CSR2 interrupt enable: port C bit D7 = 1

To acknowledge these interrupts, the enable bits must be cleared, and may then again be set for a new cycle.

All CSR registers are read and write accessible.

The DMA interface is divided into two unidirectional channels:

1. The OUT DMA channel – front-end to host
2. The IN DMA channel – host to front-end.

The channels allow a 1-word transfer per transaction between the DMA registers and the host memory.

The sequences indicated below must be followed even when only 16-bit addressing is needed, as DMA hardware is only triggered by the action of a write into the extended address registers.

NOTE

Byte transfers in DMA mode are not available.

If the DMA cycle does not finish within the time defined by the Q-bus timing specifications, a timeout occurs and bit D7 in port A of the peripheral IC is set.

In order to allow the KMV11 to address other devices in the I/O page, bit D3 in port B can be set to allow access to the I/O page.

In order to allow the DMA registers to be loaded without a DMA cycle taking place, bit D5 in port B must be clear. This bit should be set when DMA cycles have to take place.

4.2.2.1 Programming Sequence for DMA OUT – First transfer:

```
        MOV    #40,@#130012      ; ENABLE DMA TRANSFER
        MOV    DATA,@#100022     ; DATA TO DMA OUT REGISTER
        MOV    ADDR,@#100026     ; LOAD ADDRESS
        MOVB   XDDR,@#100036     ; LOAD EXTENDED ADDRESS
                                 ; AND INITIATE DMA
        TSTB   @#130000          ; CHECK FOR TIMEOUT
        BMI    "TIMEOUT ERROR"
        DEC    "WORD COUNT"      ; SUBTRACT ONE FROM WORD COUNT
```

Subsequent transfers:

```
LOOP:   MOV    DATA,@#100022     ; DATA TO DMA OUT REGISTER
        ADD    #2,@#100026       ; UPDATE ADDRESS
        ADC    @#100036          ; UPDATE EXTENDED ADDRESS
                                 ; AND INITIATE DMA
        TSTB   @#130000          ; CHECK FOR TIMEOUT
        BMI    "TIMEOUT ERROR"
        DEC    "WORD COUNT"      ; SUBTRACT ONE FROM WORD COUNT
        BNE    LOOP              ; LOOP UNTIL ALL WORDS
                                 ; TRANSFERRED
```

4.2.2.2 Programming Sequence for DMA IN – First transfer:

```
        MOV    #40,@#130012      ; ENABLE DMA TRANSFER
        MOV    ADDR,@#100024     ; LOAD ADDRESS
        MOVB   XDDR,@#100034     ; LOAD EXTENDED ADDRESS
                                 ; AND INITIATE DMA
        TSTB   @#130000          ; CHECK FOR TIMEOUT
        BMI    "TIMEOUT ERROR"
        DEC    "WORD COUNT"      ; DECREMENT WORD COUNT
        MOV    @#100020,DATA     ; READ DATA

LOOP:   ADD    #2,@#100024       ; UPDATE ADDRESS
        ADC    @#100034          ; UPDATE EXTENDED ADDRESS
                                 ; AND INITIATE DMA
        TSTB   @#130000          ; CHECK FOR TIMEOUT
        BMI    "TIMEOUT ERROR"
        MOV    @#100020,DATA     ; READ DATA
        DEC    "WORD COUNT"      ; LOOP UNTIL ALL WORDS
        BNE    LOOP              ; TRANSFERRED
```

4.3 LINE CONTROLLER INTERFACE

The line controller is a 7201 PUSART, or equivalent IC.

The following protocols may be implemented:

1. Asynchronous
2. Character synchronous (monosync, bisync)
3. Bit synchronous (SDLC, HDLC).

Error-checking features:

1. Parity (odd, even)
2. CRC-16
3. CRC-CCITT
4. Break/abort detection
5. Framing error detection.

The line controller PUSART device cannot function until it is completely programmed to the required configuration. This programming is done by writing appropriate bit patterns into the PUSART device's control registers. The PUSART contains eight such control registers for each of its two channels. Initial access is to the first of these registers only: control register 0. Access to the other seven registers is through this control register 0, for each channel.

When the PUSART has been programmed, its function and operation can be checked and monitored by the examination of its status registers for each of the two channels. Access to all three of these registers is through the appropriate channel's control register 0.

Figures 4-2 to 4-10 show the summarized functions of the eight control registers; and Figures 4-11 to 4-13 show the summarized functions of the three status registers.

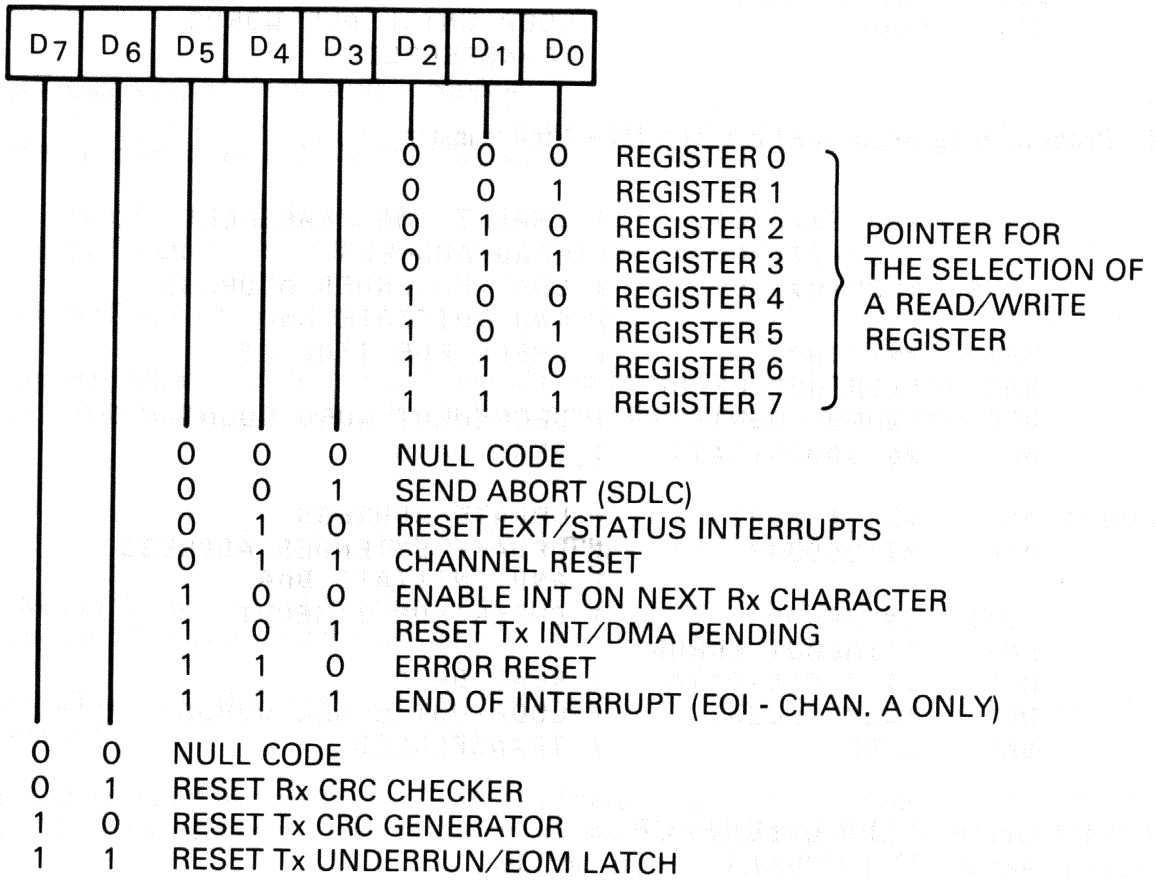


Figure 4-2 Control Register 0, Bit Functions

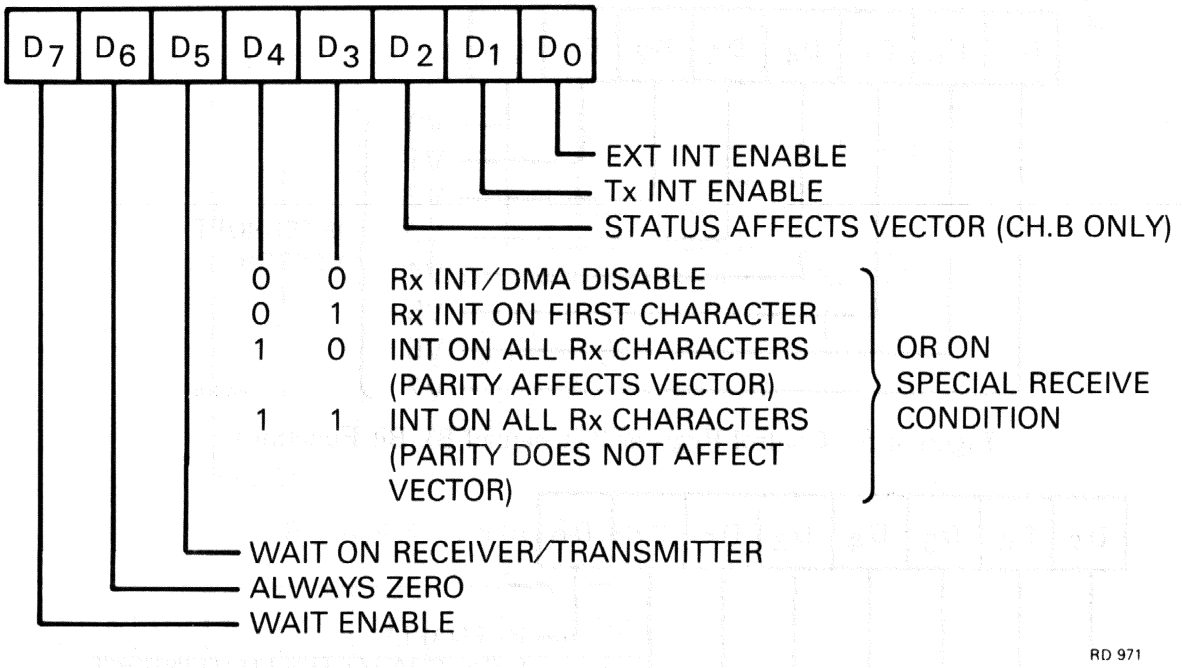


Figure 4-3 Control Register 1, Bit Functions

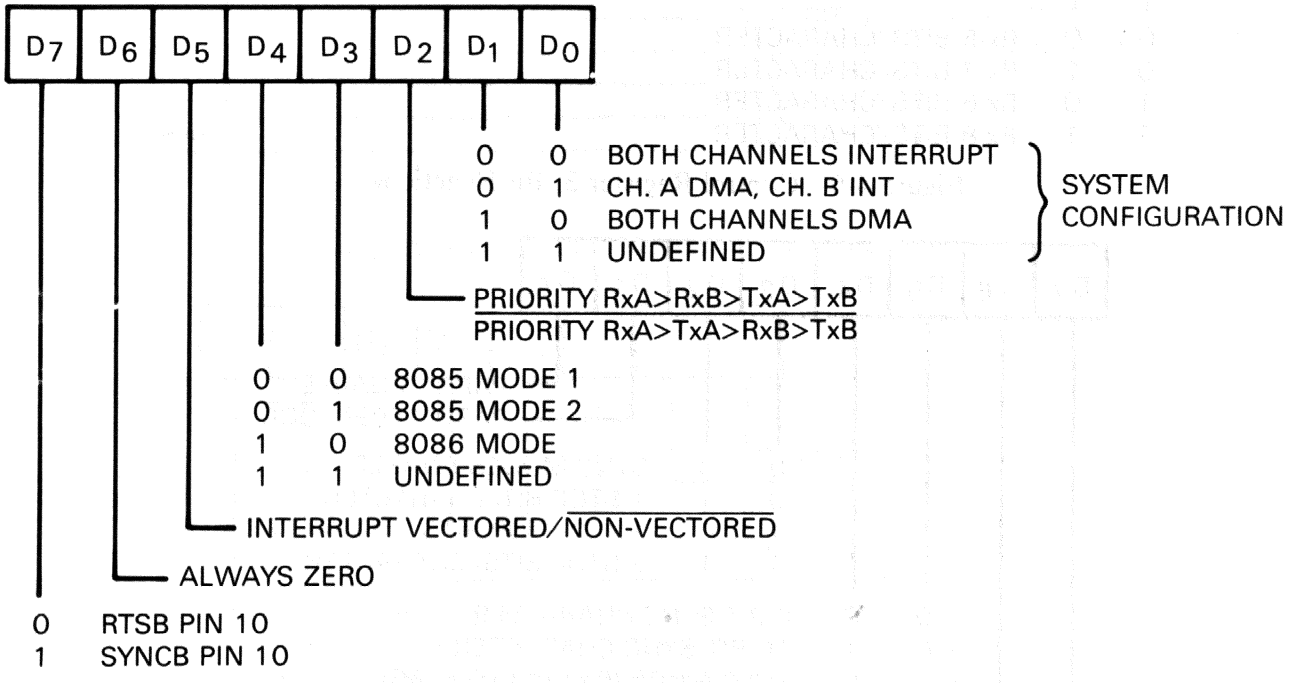


Figure 4-4 Control Register 2 (Channel A), Bit Functions

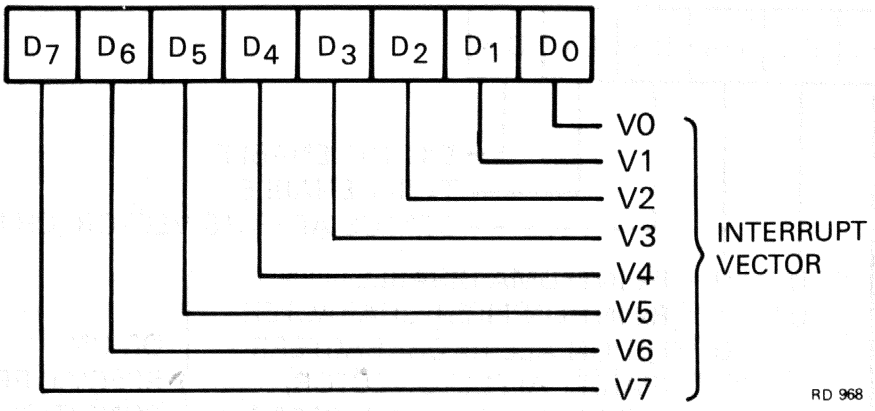


Figure 4-5 Control Register 2 (Channel B), Bit Functions

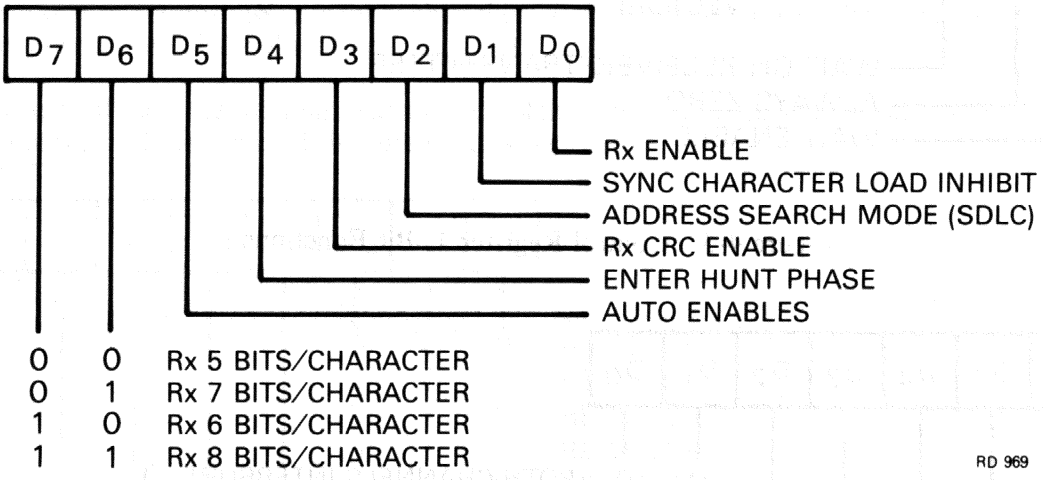


Figure 4-6 Control Register 3, Bit Functions

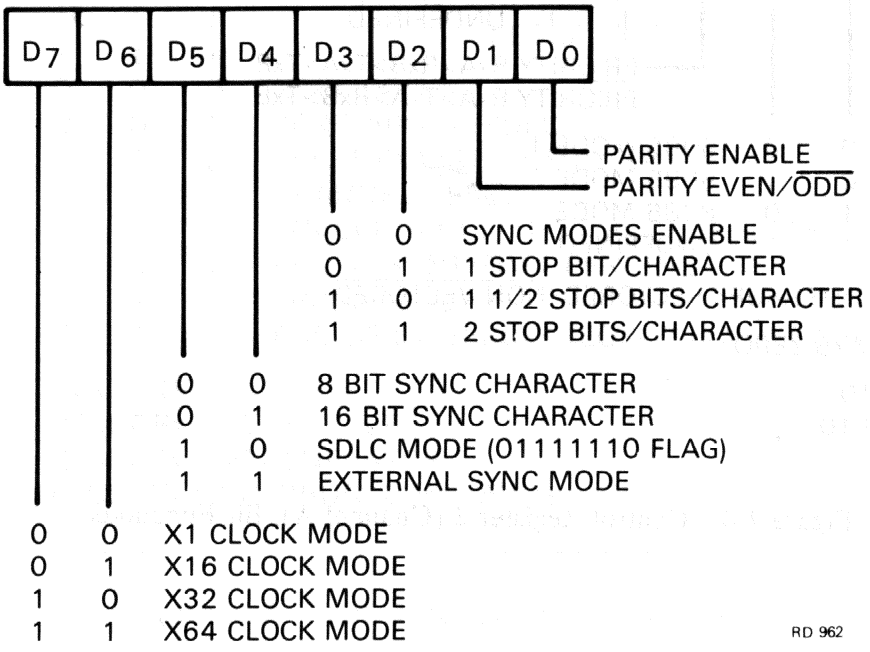


Figure 4-7 Control Register 4, Bit Functions

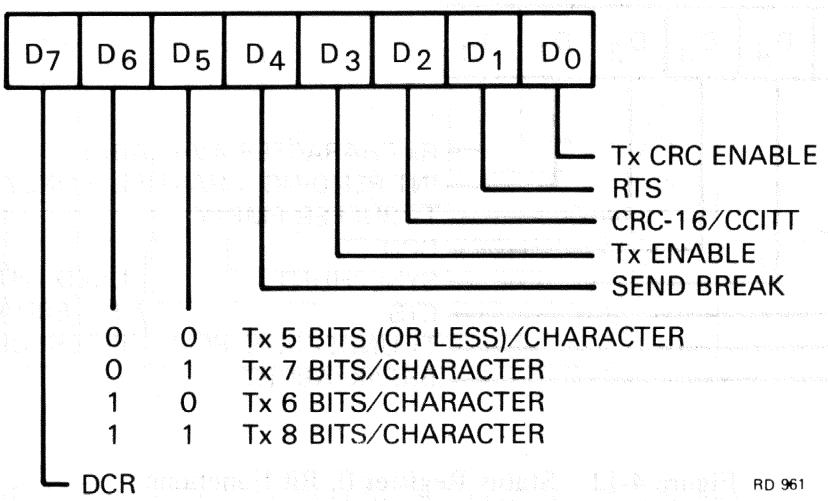


Figure 4-8 Control Register 5, Bit Functions

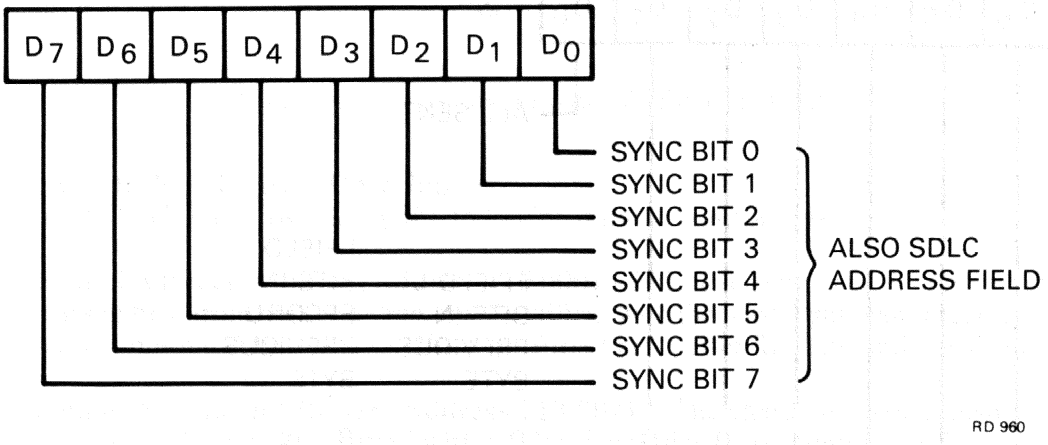
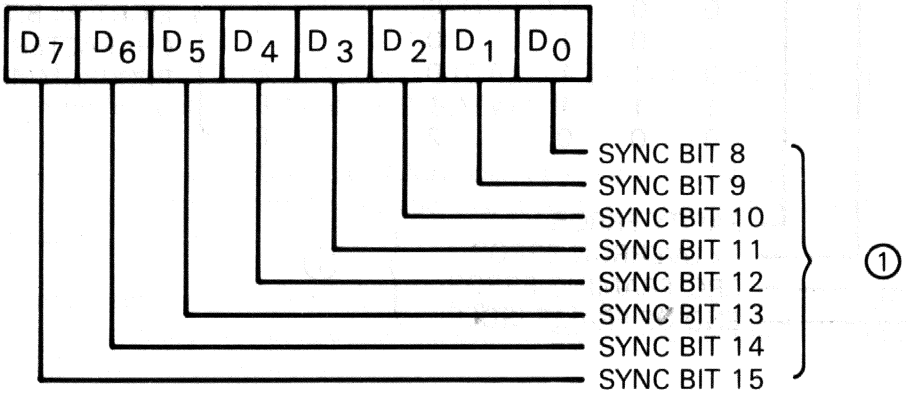


Figure 4-9 Control Register 6, Bit Functions



NOTE: ① FOR SDLC IT MUST BE PROGRAMMED TO '01111110' FOR FLAG RECOGNITION

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Figure 4-10 Control Register 7, Bit Functions

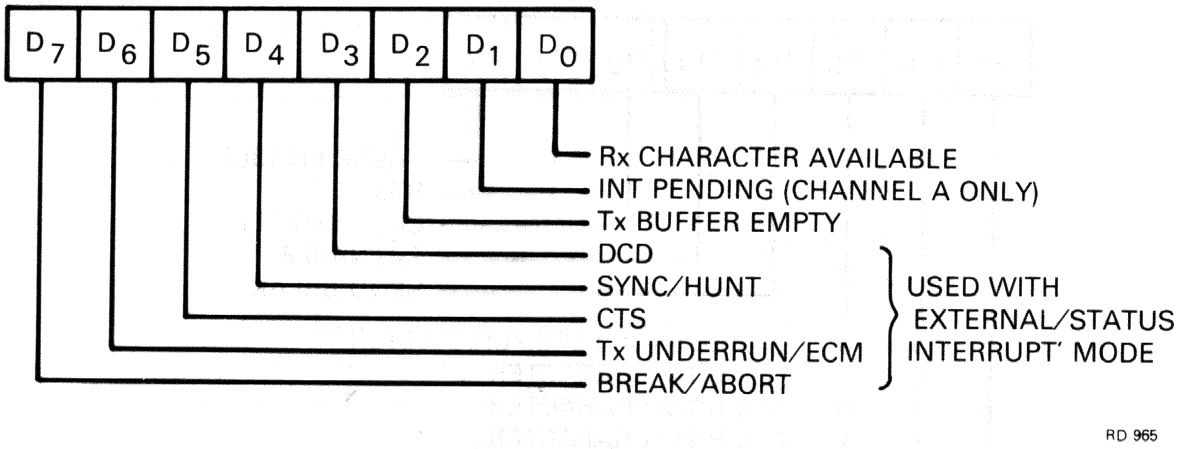


Figure 4-11 Status Register 0, Bit Functions

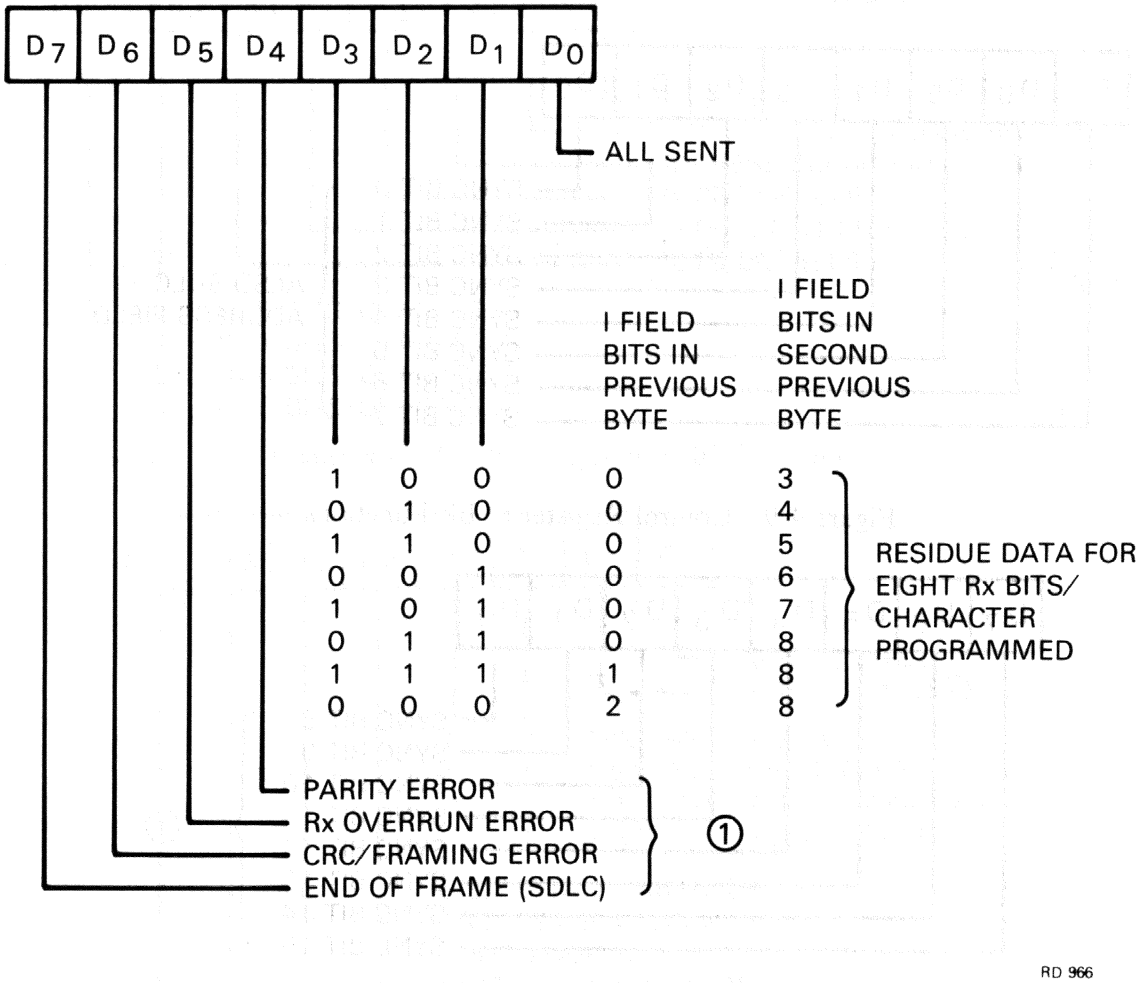
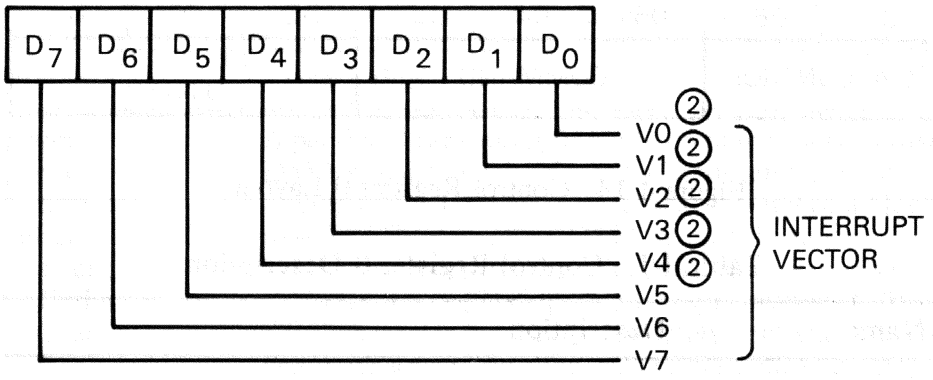


Figure 4-12 Status Register 1, Bit Functions



NOTES: ① USED WITH SPECIAL RECEIVE CONDITION MODE.
② VARIABLE IF 'STATUS AFFECTS VECTOR' IS PROGRAMMED.

RD 974

Figure 4-13 Status Register 2, Bit Functions

4.3.1 Line Controller Register Description

Access to the PUSART is provided by the following data or control bytes.

4.3.1.1 Channel A Receive Buffer (Address 110 000) – This read-only register contains the character received and assembled from the serial line, right justified, with the least significant received bit first. The PUSART has an internal 4-byte FIFO (First In, First Out) buffer for data and corresponding status.

4.3.1.2 Channel A Transmit Buffer (Address 110 002) – The character to be transmitted is loaded into this write-only register right justified with the least significant transmitted bit first.

4.3.1.3 Channel B Receive Buffer (Address 110 010) – This read-only register is the same as the channel A receive buffer, but is used only with KMV11-B.

4.3.1.4 Channel B Transmit Buffer (Address 110 012) – This write-only register is the same as the channel A transmit buffer, but is used only with KMV11-B.

4.3.1.5 Channel A Command Registers (Address 110 006) – The seven write-only command registers per channel are accessed through this address. It is also used to load the address pointer for the two read-only status registers.

All control and status registers except Control Register 2 (CR2) are separately maintained for each channel. CR2 is linked with the overall operation of the PUSART and contains different meanings when addressed through different channels.

When initializing the PUSART, CR2A (and CR2B if wanted) should be programmed first to set up the PUSART processor/bus interface mode. Each channel to be used may then be programmed separately, beginning with control register 4 to set the protocol mode for that channel. The rest of the registers may then be programmed in any order.

4.3.1.5.1 Control Register 0 – The layout of this register is shown in Figure 4-14, and the register itself is described in Table 4-1.

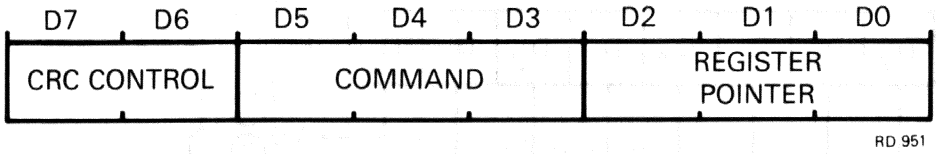


Figure 4-14 Control Register 0 Layout

Table 4-1 Control Register 0 Description

Bit	Name	Description
D 2–0	Register pointer	The register pointer specifies which register number is accessed at the next control register write or status register read. After a hardware or software reset, the register pointer is cleared to 0. Therefore, the first control byte goes to control register 0. When the register pointer is set to a value other than 0, the next control or status (C/D = 1) access is to the specified register, after which the pointer is cleared to 0. Other commands may be combined in control register 0 together with the setting of the register pointer.
D 5–3	Command	Commands normally used during the operation of the PUSART are grouped in control register 0. They are:
<000>	Null	This command has no effect and is used when it is only necessary to set the register pointer or issue a CRC command.
<001>	Send abort	When operating in HDLC mode, this command causes the PUSART to transmit the HDLC abort code, issuing from 8 to 13 consecutive 1s. Any data currently in the transmitter or the transmitter buffer is destroyed. After sending the abort, the transmitter returns to the idle phase (flags).
<010>	Reset external/ status interrupts	When the External/Status Change (E/SC) flag is set, the condition bits D3 to D7 of status register 0 are latched to allow the detection of short pulses that may occur. The Reset External/Status Interrupts (RE/SI) command clears a pending interrupt and reenables the latches so that new interrupts may be sensed.
<011>	Channel Reset	A Channel Reset (CR) command to channel A clears the internal interrupt prioritization logic. This does not occur when a CR command is issued to channel B. All control registers associated with the channel to be cleared must be initialized again.
<100>	Enable interrupt on next character	When operating the PUSART in Interrupt on First Character Only (IFCO) mode, this command may be issued at any time (normally at the end of a block or frame), to reenable the interrupt logic for the next received character.

Table 4-1 Control Register 0 Description (Cont)

Bit	Name	Description
<101>	Reset pending transmitter buffer interrupt or DMA request	A pending Transmitter Buffer Becoming Empty (TBBE) interrupt or DMA request may be cleared without sending another character, by issuing this command (normally at the end of a block or frame). A new TBBE interrupt or DMA request is not made until either (1) another character has been loaded and transferred to the transmitter shift register, or (2) if operating in synchronous or HDLC mode, the CRC character has been completely sent and the first sync or flag character loaded into the transmitter shift register.
<110>	Error reset	This command clears a Special Receive Condition (SRC) interrupt. It also reenables the Parity Error (PE) and Overrun Error (OE) latches that allow the testing for these errors at the end of a block or frame.
<111>	End of interrupt	Once an interrupt request has been issued by the PUSART, all lower priority internal and external interrupts in the daisy chain are held off. This permits the current interrupt to be serviced, while allowing higher priority interrupts to occur. At some point in the interrupt service routine (normally at the end), it will be necessary to issue the End of Interrupt (EOT) command to channel A. This enables the daisy chain, and allows any pending lower priority internal interrupt requests to occur.
D 7–6	CRC control commands	These commands control the operation of the CRC generator/ checker logic.
<00>	Null	This command has no effect and is used when issuing other commands or setting the register pointer.
<01>	Reset receiver CRC checker	This command clears the CRC checker to 0 when the channel is in synchronous mode, and sets it to all 1s when in HDLC mode.
<10>	Reset transmitter CRC checker	This command clears the CRC generator to 0 when the channel is in synchronous mode, and sets it to all 1s when in HDLC mode.
<11>	Reset IDLE/CRC Latch	This command clears the IDLE/CRC latch so that when a transmitter underrun condition occurs (that is, the transmitter has no more characters to send), the transmitter enters the CRC phase of operation and starts to send the 16-bit CRC character computed up to that point. The latch is then set so that, if the underrun condition continues, idle characters are sent following the CRC. After a hardware or software reset, the latch is in the set state.

4.3.1.5.2 **Control Register 1** – The layout of this register is shown in Figure 4-15, and the register itself is described in Table 4-2.

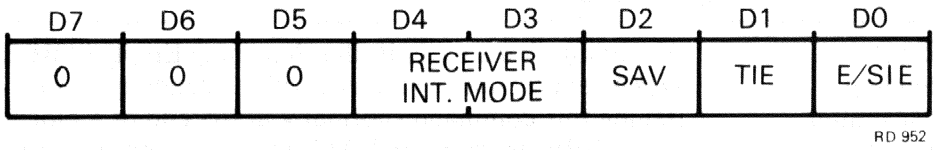


Figure 4-15 Control Register 1 Layout

Table 4-2 Control Register 1 Description

Bit	Name	Description
D 0	External/ status interrupt enable	When this bit is set to 1, the PUSART issues an interrupt when any of the following occur: 1. Transition of 109 input 2. Transition of 106 input 3. Entering or leaving synchronous hunt phase (break detection or termination in async mode) 4. HDLC abort detection or termination, IDLE/CRC latch becoming set (CRC being sent).
D 1	Transmitter interrupt enable	When this bit is set to 1, the PUSART issues an interrupt when either of the following occur: 1. The character currently in the transmitter buffer is transferred to the shift register (transmitter buffer becoming empty) 2. The transmitter enters idle phase and starts transmitting sync or flag characters.
D 2	Status affects vector	When this bit is cleared to 0, the fixed vector programmed into CR2(B) during PUSART initialization is returned in the interrupt acknowledge sequence. When this bit is set to 1, the vector is modified to indicate the condition that caused the interrupt.
D 4–3	Receiver interrupt mode	This field controls how the interrupt or DMA logic of the PUSART handles the character received condition.
<00>		Disable character mode – The PUSART does not issue an interrupt or a DMA request when a character has been received.

Table 4-2 Control Register 1 Description (Cont)

Bit	Name	Description
<01>		Interrupt on First Character Only (and issue a DMA request) (IFCO) – In this mode, the PUSART issues an interrupt only for the first character received after an Enable Interrupt on Next Character (EINC) command (CR0) has been given. If the channel is in DMA mode, a DMA request is issued for each character received, including the first. This mode is normally used with the PUSART in DMA or block transfer mode to tell the processor that the beginning of an incoming block or frame has been received. Note that there is no actual DMA hardware in the KMV11, but the facility is used to simplify the firmware and the operation.
<10>		Interrupt (and issue a DMA request) on every received character (parity error is a special receive condition) – In this mode, an interrupt (and DMA request, if DMA mode is selected) is issued when there is a character present in the receiver buffer. A parity error is considered a special receive condition. Note that there is no actual DMA hardware in the KMV11, but the facility is used to simplify the firmware and the operation.
<11>		Interrupt (and issue a DMA request) on every received character (parity error is not a special receive condition) – This mode is the same as above except that a parity error is not considered a special receive condition. The following are considered special receive conditions and, when SAV is enabled, cause an interrupt vector different from that caused by a Received Character Available (RCA) condition: • Overrun error • Asynchronous framing error • Parity error (if specified) • HDLC end of message (final flag received).

4.3.1.5.3 **Control Register 2 (Channel A)** – The layout of this register is shown in Figure 4-16, and the register itself is described in Table 3-3.

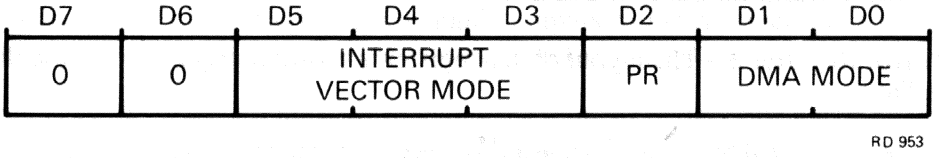


Figure 4-16 Control Register 2 (A) Layout

Table 4-3 Control Register 2 (A) Description

Bit	Name	Description
D 1–0	DMA mode select	Setting this field controls whether channels A and B are used in DMA mode (that is, data transfers are performed by a DMA controller) or in non-DMA mode where transfers are performed by the processor in either polled, interrupt, or block transfer modes. **D 1–0 Mode** <00> Channel A non-DMA, channel B non-DMA <01> Channel A DMA, channel B non-DMA (recommended for KMV11-A) <10> Channel A DMA, channel B DMA (recommended for KMV11-B) <11> Illegal
D 2	Priority	This bit allows the selection of the relative priorities of the different interrupt and DMA conditions according to the application. D2 = 0 priority 1 = channel A RxA > TxA > RxB > TxB > external D2 = 1 priority 1 = receive channel A or B RxA > RxB > TxA > TxB > external
D 5–3	Interrupt vector mode	This field determines how the PUSART will respond to an interrupt acknowledge sequence from the processor. As there is no provision for hardware vectoring, D5 should always be programmed to 0. See also Figure 4-4. The value programmed into D4 will determine which three bits will become affected when the interrupt vector is read back: 0 to 2, or 2 to 4. Refer also to Section 4.3.1.8 and to Figure 4-27. It is recommended that D3 of this field should be always programmed to 0. This bit provides a facility not supported in the KMV11. Programming both D3 and D4 to 1 is illegal.

4.3.1.5.4 Control Register 3 – The layout of this register is shown in Figure 4-17, and the register itself is described in Table 4-4.

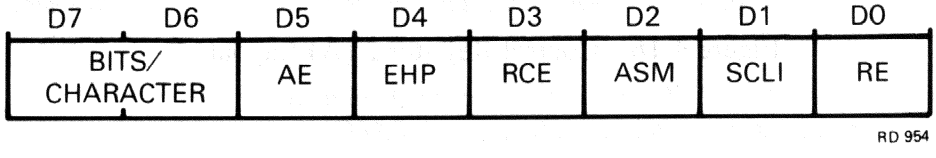


Figure 4-17 Control Register 3 Layout

Table 4-4 Control Register 3 Description

Bit	Name	Description
D 0	Receiver enable	After the channel has been completely initialized, setting this bit to 1 allows the receiver to start operation. This bit may be cleared at any time to disable the receiver.
D 1	Sync character load inhibit	In synchronous mode this bit inhibits the transfer of sync characters to the receiver buffer, so performing a 'sync stripping' operation. The load inhibit does not exclude sync characters embedded in the block or frame from the CRC computation. Therefore this feature may only be used to strip leading sync characters at the beginning of a block or frame. Synchronous protocols using other types of block checking, such as checksum or LRC, are allowed to strip embedded sync characters with this bit.
D 2	Address search mode	In HDLC mode, setting this bit places the PUSART in address search mode. Character assembly does not start until the 8-bit character (secondary address field) following the starting flag of a message matches either the address programmed into CR6 or the global address 377.
D 3	Receiver CRC enable	This bit enables or disables (1 = enable) the CRC checker, in order to control the exclusion of individual characters from the total CRC computation. The PUSART features a 1-character delay between the receiver shift register and the CRC checker. Enabling or disabling takes effect with the last character transferred from the shift register to the receiver buffer. Therefore, one full character-time is available in which to read the character and determine whether it should be included in the CRC computation.
D 4	Enter hunt phase	The PUSART receiver automatically enters sync hunt phase after a reset. Sometimes it is necessary to enter this phase again, for example, when synchronization has been lost, or, in HDLC mode, to ignore the current incoming frame. Writing a 1 into this bit at any time after initialization causes the PUSART to enter sync hunt phase again.
D 5	Auto enables	Setting this bit to 1 causes the CCITT 109* and CCITT 106* inputs to perform as enable inputs to the receiver and transmitter, in that order. This feature is not supported on the KMV11.
D 6–7	Number of received bits per character	This field specifies the number of data bits assembled to make each character. This value may be changed while a character is being assembled, and, if the change is made before the new number of bits has been reached, it affects that character. Otherwise the new specifications take effect on the next character received.

* Refer to Table 4-14 for equivalent EIA signals.

Table 4-4 Control Register 3 Description (Cont)

Bit	Name	Description
		D6 D7 Bits/Character
		<00> 5
		<01> 6
		<10> 7
		<11> 8

4.3.1.5.5 **Control Register 4** – The layout of this register is shown in Figure 4-18, and the register itself is described in Table 4-5.

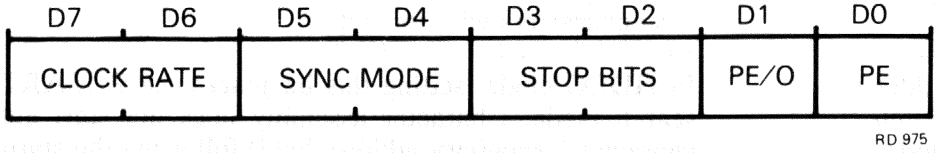


Figure 4-18 Control Register 4 Layout

Table 4-5 Control Register 4 Description

Bit	Name	Description
D 0	Parity enable	Setting this bit to 1 adds an extra data bit containing parity information to each transmitted character. Each received character is expected to contain this extra bit and the receiver parity checker is enabled.
D 1	Parity even/odd	Programming this bit to 0 when parity is enabled causes the transmitted parity bit to take on the value needed for odd parity. The received character is checked for odd parity. On the other hand, a 1 in this bit indicates even parity generation and checking.
D 4–2	Number of stop bits/ sync mode	This field specifies whether the channel is used in synchronous (or HDLC) mode or in asynchronous mode. In asynchronous mode, this field also specifies the number of bit-times used as the stop bit length by the transmitter. The receiver always checks for one stop bit.
		D3 D2 Mode
		<00> Synchronous modes
		<01> Async 1 bit-time (1 stop bit)
		<10> Async 1.5 bit-times (1.5 stop bits)
		<11> Async 2 bit-times (2 stop bits)

Table 4-5 Control Register 4 Description (Cont)

Bit	Name	Description
D 5–4	Sync mode	When the NSB/SM field is programmed for synchronous modes (D2 and D3 both clear), this field specifies the synchronous format to be used. In asynchronous mode, this field is ignored. The synchronous modes are: **D5 D4 Mode** <00> 8-bit internal sync character (monosync) <01> 16-bit internal sync character (bisync) <10> HDLC <11> Illegal
D 7–6	Clock rate	The field specifies the relationship between the transmitter and receiver clock inputs (TxC, RxC) and the actual data rate at TxD and RxD. When operating in a synchronous mode, a 1-times clock rate must be specified. In asynchronous modes, any of the rates may be specified; however, with a 1-times clock rate the receiver cannot determine the center of the start bit. In this mode, external synchronization of the sampling (rising) edge of RxC with the data is needed. **D7 D6 Clock Rate** <00> Clock rate = 1 × Data rate <01> Clock rate = 16 × Data rate <10> Clock rate = 32 × Data rate <11> Clock rate = 64 × Data rate

4.3.1.5.6 Control Register 5 – The layout of this register is shown in Figure 4-19, and it is described in Table 4-6.

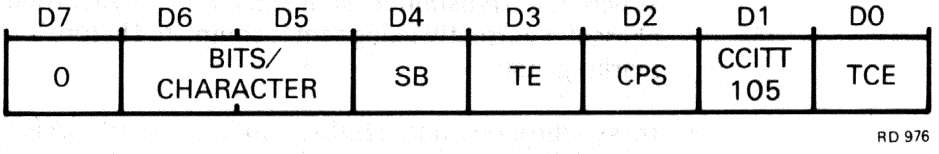


Figure 4-19 Control Register 5 Layout

Table 4-6 Control Register 5 Description

Bit	Name	Description
D 0	Transmitter CRC enable	The CRC computation is enabled when this bit is programmed to a 1, and it is disabled when the bit is programmed to 0. The enable or disable does not take effect until the next character is transferred from the transmitter buffer to the shift register. This makes it possible to include or exclude specific characters from the CRC computation. By setting or clearing this bit immediately before loading the next character, the next character and following characters are either included or excluded from the computation. If this bit is 0 when the transmitter becomes empty, the PUSART goes to the idle phase, without regard to the state of the IDLE/CRC latch.
D 1	CCITT 105	In synchronous and HDLC modes, setting this bit to 1 causes the CCITT 105* signal to go to the active (marking) state, and clearing it to 0 causes it to go inactive (spacing). In asynchronous mode, clearing this bit to 0 does not cause CCITT 105 to go inactive until the transmitter is completely empty. This feature makes it easier to program the PUSART for use with asynchronous modems.
D 2	CRC polynomial select	This bit selects the polynomial used by the transmitter and receiver for CRC generation and checking. When set, it selects the CRC-16 polynomial ($x^{16} + x^{15} + x^2 + 1$). When clear, it selects the CRC CCITT polynomial ($x^{16} + x^{12} + x^5 + 1$). In HDLC mode, it is necessary to select CRC CCITT. Either polynomial may be used in other synchronous modes.
D 3	Transmitter enable	After a reset, the transmitted data output (TxD) is held high (marking) and the transmitter is disabled until this bit is set. In asynchronous mode, TxD stays high until data is loaded for transmission. When the transmitter is disabled in asynchronous mode, any character currently being sent is completed before TxD returns to the marking state. In synchronous and HDLC modes, the PUSART automatically enters idle phase and sends the programmed sync or flag characters. If the transmitter is disabled during the data phase in synchronous mode, the current character is sent, then TxD goes high (marking). In HDLC mode, the current character is sent, but the marking line following is zero-inserted. That is, the line goes to spacing for one bit-time out of every five. The transmitter should never be disabled during the HDLC data phase unless a reset is to follow immediately. Whether a reset follows or not, any character in the buffer register is held.

* Refer to Table 4-14 for equivalent EIA signals.

Table 4-6 Control Register 5 Description (Cont)

Bit	Name	Description
		Disabling the transmitter during the CRC phase causes the rest of the CRC character to be bit-substituted with sync (or flag). The total number of bits transmitted is correct and TxD goes marking after they are sent. If the transmitter is disabled during the idle phase, the remainder of the sync (flag) character is sent, then TxD goes marking.
D 4	Send break	Setting this bit to 1 immediately forces the transmitter output (TxD) to spacing. This function overrides the normal transmitter output and destroys any data being transmitted although the transmitter stays in operation. Clearing this bit releases the transmitter output.
D 6–5	Number of transmitted bits per character	This field controls the number of data bits transmitted in each character. The number of bits per character may be changed by writing this field immediately before loading the first character to use the new specification.

D6 D5	Bits per Character
<00>	5 or less (see below)
<01>	7
<10>	6
<11>	8

Normally each character is sent to the PUSART right-justified and the bits not used are ignored. However, when sending five bits or less the data should be formatted as shown below to inform the PUSART of the correct number of bits to be sent.

D7	D6	D5	D4	D3	D2	D1	D0	Number of bits
1	1	1	1	0	0	0	D0	1
1	1	1	0	0	0	D1	D0	2
1	1	0	0	0	D2	D1	D0	3
1	0	0	0	D3	D2	D1	D0	4
0	0	0	D4	D3	D2	D1	D0	5

4.3.1.5.7 Control Register 6 – The layout of this register is shown in Figure 4-20, and the register itself is described below.

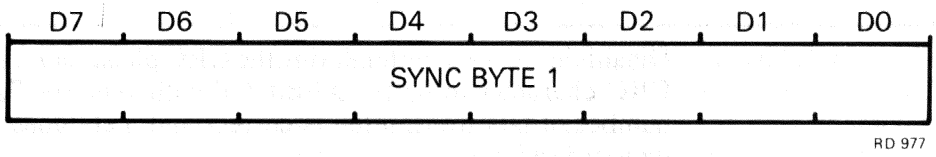


Figure 4-20 Control Register 6 Layout

Sync byte 1 is used in the following modes:

Monosync – The 8-bit sync character transmitted during the idle phase

Bisync – Least significant (first) 8 bits of the 16-bit transmit and receive sync character

HDLC – Secondary address value matched to the secondary address field of the HDLC frame when the PUSART is in address search mode.

4.3.1.5.8 Control Register 7 – The layout of this register is shown in Figure 4-21, and the register itself is described below.

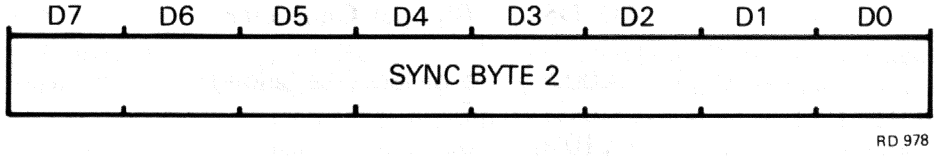


Figure 4-21 Control Register 7 Layout

Sync byte 2 is used in the following modes:

Monosync – The 8-bit sync character received

Bisync – Most significant (second) 8 bits of the 16-bit transmit and receive sync characters

HDLC – Must be programmed with the flag character, 01111110_2, in control register 7 for flag matching by the PUSART receiver.

4.3.1.6 Channel B Command Register – This write-only register has the address 110 016. The seven control register bytes of channel B are accessed through this register. It is also used for the address pointer to status registers 0, 1, and 2.

In the KMV11-B dual-line option all the control registers of channel B have the same functions as those of channel A, except for control register 2. Both channel A control register 2 and channel B control register 2, contain information which affects both channels. Both must be programmed.

In the KMV11-A single channel option, both channel A control register 2 and channel B control register 2 have the same functions as in the KMV11-B. Again both must be programmed. One additional control register is provided. It is control register 1, which is accessible through channel B addressing. Therefore its functions in the KMV11-A and in the KMV11-B are different. Access to these two channel B registers is through channel B control register 0, which has only limited functions in this option. Figure 4-22 shows the layout of control registers for both options (KMV11-A and KMV11-B).

Control registers with functions unique to channel B are shown in Figure 4-22.

4.3.1.6.1 Control Register 0 – This register is similar to that of channel A, with the following exceptions:

- Bits D6 and D7 have no meaning
- Only three commands are valid:

<000> Null (for loading the register pointer)
<010> Reset external/status interrupts
<011> Channel reset.

4.3.1.6.2 Control Register 1 – Only bits D0 and D2 are valid in this register. Their functions are the same as defined in control register 1 for channel A (see Figure 4-15). In the KMV11-A, however, the external/status signals affected by this register are only CCITT 125* and CCITT 107*. See also Section 4.3.1.8.1 for the associated status.

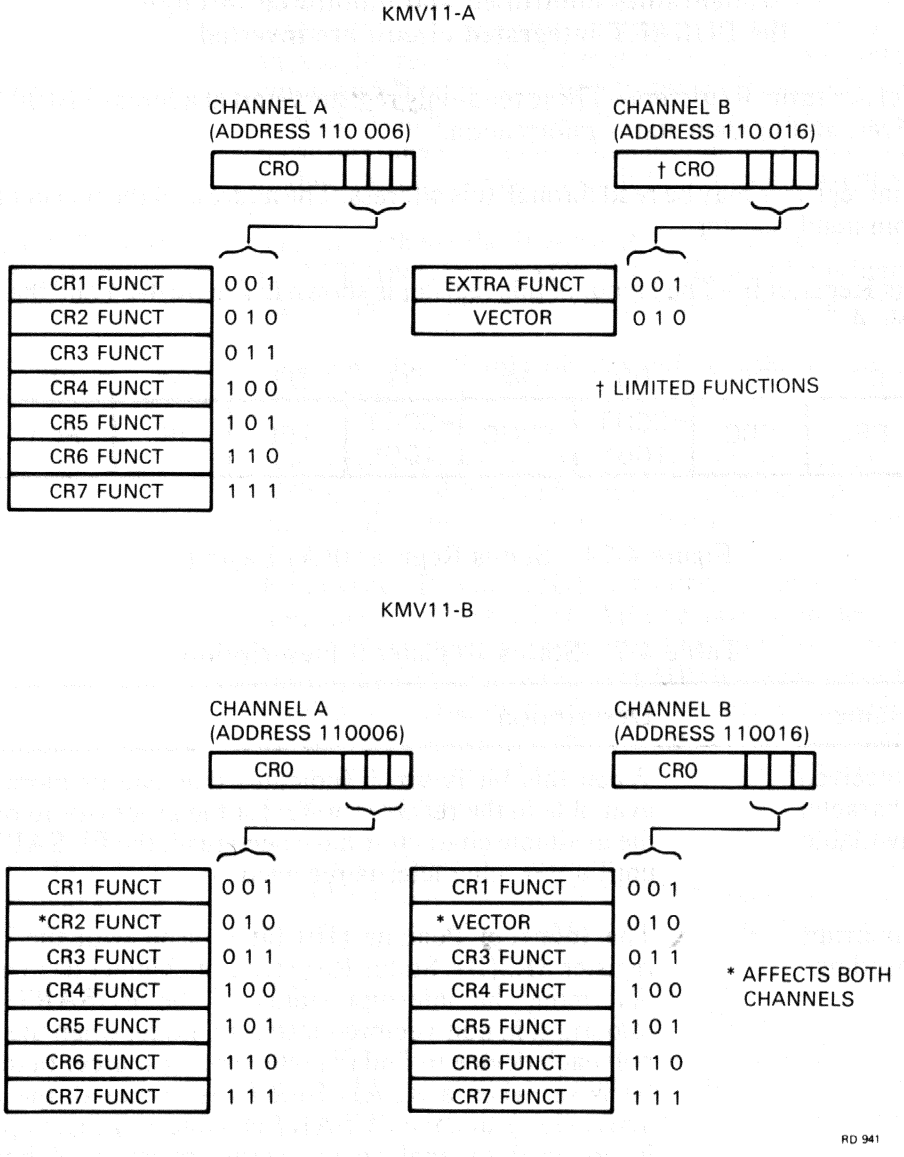


Figure 4-22 Control Registers in the KMV11-A and KMV11-B

* Refer to Table 4-14 for equivalent EIA signals.

4.3.1.6.3 Control Register 2 (Channel B) – The contents of this register are modified if the Status Affects Vector (SAV) mode is enabled. The value of CR2(B) may be read at any time. This feature is most useful in determining the cause of an interrupt when the PUSART is used in non-vectored interrupt mode.

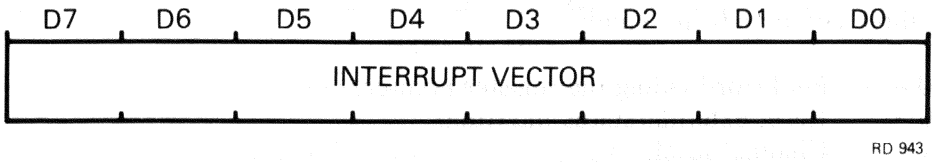


Figure 4-23 Control Register 2(B) Layout

NOTE

Modem lines controlled and monitored through the PUSART integrated circuit are inverted.

4.3.1.7 Channel A Status Registers – These read-only registers start at address 110004. They contain transmitter, receiver, and modem status information.

In fact, two internal registers may be read through this address. The address of the register is selected with the channel A command register.

4.3.1.7.1 Status Register 0 – The layout of this register is shown in Figure 4-24 and the register itself is described in Table 4-7.

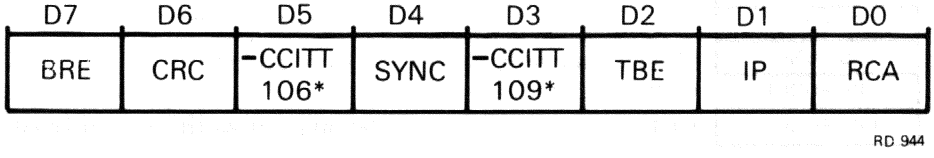


Figure 4-24 Status Register 0(A) Layout

Table 4-7 Status Register 0 Description

Bit	Name	Description
D 0	Received character available	When this bit is set, it indicates that one or more characters are available in the receiver buffer for the processor to read. Once all of the available characters have been read, the PUSART clears this bit until a new character is received.
D1 (A only)	Interrupt pending	The Interrupt Pending (IP) bit is used with the interrupt vector register SR2(B) (Status Register 2 of channel B) to make it easier to determine the interrupt status of the PUSART. This is more important in non-vectored interrupt mode, when the processor must poll each device to find the interrupting source. In this mode, the IP bit is set when a READ SR2(B) is executed, the PRI input goes active (low), and the PUSART is requesting interrupt service. There is no need to analyze the status registers of both channels to determine if an interrupt is pending. If SAV is enabled and IP is set, the vector read from SR2(B) will contain valid condition information.

Table 4-7 Status Register 0 Description (Cont)

Bit	Name	Description
D 2	Transmitter buffer empty	This bit is set when the transmitter buffer is empty, except during the transmission of CRC (the PUSART uses the buffer to make this function simpler). After a reset, the buffer is considered empty and the bit is set.
External/status flags:		The rest of the status bits indicate the state of the different conditions that could cause an interrupt if enabled. The PUSART latches all these bits after a change occurs, whether the interrupt is enabled or not. This allows the detection of transient changes on the associated lines with less timing restrictions on the software. When the PUSART is operated in interrupt-driven mode for external/status interrupts, and an interrupt occurs, status register 0 should be read, and a Reset External/Status Interrupts (RE/SI) command should be issued to reenable both the interrupt and the latches. When the PUSART is operated in non-interrupt mode, these bits may be polled by first issuing a RE/SI command in order to update the status and cause it to indicate current values.
D 3	CCITT 109* (Carrier Detect)	This bit echoes the inverse state of the CCITT 109 input. When CCITT 109 is low, the CCITT 109 status bit is high. Any transition on this bit causes an external/status interrupt request.
D 4	Sync	The meaning of this bit depends on the operating mode of the PUSART. Asynchronous mode: sync status echoes the inverse state of the SYNC input. When SYNC is low, sync status is high. Any transition on this bit causes an external/status interrupt request. Monosync, Bisync, HDLC modes: In these modes, sync status indicates whether the PUSART receiver is in the sync hunt phase or receive data phase of operation. This bit will become set as a result of setting the Enter Hunt Phase (EHP) bit or as a result of a reset. It will be clear when the PUSART is in the receive data phase of operation. As in other modes, a transition on this bit causes an external/status interrupt request. This may be cleared immediately by issuing a RE/SI command.
D 5	CCITT 106* (Clear to Send)	This bit echoes the inverse state of the CCITT 106 input. When CCITT 106 is low, the CCITT 106 status bit is high. Any transition on this bit causes an external/status interrupt request.
D 6	IDLE/CRC	This bit indicates the state of the IDLE/CRC latch used in synchronous and HDLC modes. After reset this bit is 1, indicating that when the transmitter is completely empty, the PUSART will enter idle phase and automatically transmit sync or flag characters.

* Refer to Table 4-14 for equivalent EIA signals.

Table 4-7 Status Register 0 Description (Cont)

Bit	Name	Description
		A zero indicates that the latch has been cleared by the Reset IDLE/CRC Latch (RI/CL) command. When the transmitter is completely empty, the PUSART will send the 16-bit CRC character and will set the latch again. An external/status interrupt is issued when the latch is set, indicating that CRC is being sent. No interrupt is issued when the latch is cleared.
D 7	Break/abort	In asynchronous mode, this bit indicates the detection of a break sequence (a null character plus framing error, that occurs when the RxD input is held low (spacing) for more than one character-time). The Break/Abort (B/A) bit is cleared when RxD returns to high (marking). In HDLC mode, the B/A bit indicates the detection of an abort sequence when seven or more 1s are received in sequence. It is cleared when a 0 is received. Any transition of the B/A bit causes an external/status interrupt.

4.3.1.7.2 **Status Register 1** – The layout of this register is shown in Figure 4-25 and the register itself is described in Table 4-8.

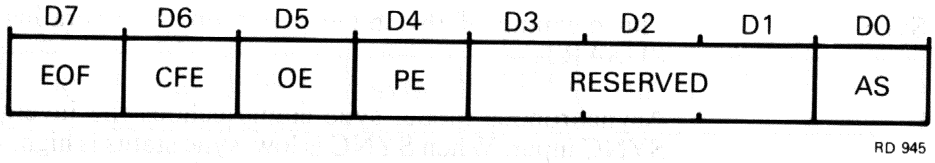


Figure 4-25 Status Register 1 Layout

Table 4-8 Status Register 1 Description

Bit	Name	Description
D 0	All sent	In asynchronous mode, this bit is set when the transmitter is empty, and cleared when a character is present in the transmitter buffer or shift register. This feature simplifies the modem-control software routines. In synchronous and HDLC modes this bit is always set to 1.
Special receive condition flags:		The rest of the status bits described below – Parity Error (PE), Overrun Error (OE), CRC/Framing Error (CFE), and End of Frame (EOF) – all represent special receive conditions. When any of these conditions occur and interrupts are enabled, the PUSART issues an interrupt request. If the Status Affects Vector (SAV) mode has been enabled, the vector generated (and the contents of SR2(B) for non-vectored interrupts) will be different from that of an RCA condition. Therefore it is not necessary to analyze SR1 with each character to determine that an error has occurred.

Table 4-8 Status Register 1 Description (Cont)

Bit	Name	Description
		As an additional facility, the PE and OE flags are latched; that is, once one of these errors occurs, the flag stays set for all subsequent characters until cleared by the ER command. With this facility, it is only necessary to read SR1 at the end of a block or frame to determine if either of these errors occurred anywhere in the block. The other flags are not latched and follow each character as it occurs in the receiver buffer.
D 4	Parity error	This bit is set and latched when parity is enabled (that is, if parity is enabled as a special receive condition) and the received parity bit does not match the sense (odd or even) computed from the data bits.
D 5	Overrun error	This error occurs and is latched when the receiver buffer already contains three characters and a fourth character is completely received, overwriting the last character in the buffer.
D 6	CRC/framing error	In asynchronous mode, a framing error is flagged (but not latched) when no stop bit is detected at the end of a character (that is, RxD is low one bit-time after the center of the last data or parity bit). When this condition occurs, the PUSART waits an additional half bit-time before sampling again, so that the framing error is not interpreted as a new start bit.
		In synchronous and HDLC modes, this bit indicates the result of the comparison between the computed CRC value and the new characters being received. It is more usually set to 1 because a correct match is seldom achieved until the complete block or frame has been received and the actual CRC is in the buffer. Note that a CRC error does not result in a special receive condition interrupt.
D 7	End of frame	This bit is used only in HDLC mode to indicate that the End of Frame (EOF) flag has been received and that the CRC error flag and residue code is valid. This flag may be cleared at any time by issuing an ER command. The PUSART also automatically clears this bit on the first character of the next message frame.

4.3.1.8 **Channel B Status Registers** – These read-only registers start at address 110 104. They are identical to the channel A status registers except for minor differences. As with control register 1, status register 0 may have a dual function. In the KMV11-A single channel option, status register 0(B) adds extra functions. Although these extra functions apply to the single channel (A) the register itself is accessed via the channel B address.

In the KMV11-B dual-line option, status register 0(B) has the same layout and functions as status register 0 for channel A.

Status register 2 of channel B operates like control register 2(B). The contents of status register 2(B) apply to channel A in the KMV11-A single channel, or to both channels in the KMV11-B dual channel option.

4.3.1.8.1 Status Register 0 KMV11-A – For the KMV11-A (single channel), this register is used to add extra functions. These functions monitor the CCITT 125 (Ring) line and the CCITT 107 (Data Set Ready) line. Figure 4-26 shows the layout of this register.

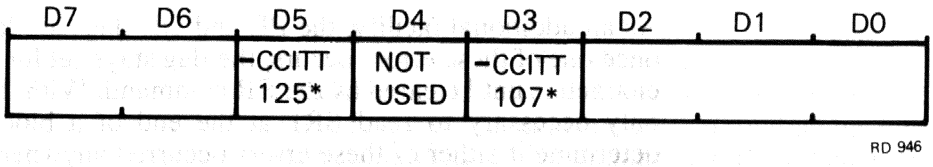


Figure 4-26 Status Register 0 (B) Layout in KMV11-A

4.3.1.8.2 Status Register 0 KMV11-B (dual line) – For the KMV11-B (dual line), this register has the same layout and functions as status register 0 for channel A, except for the IP bit (D1), which is only available in channel A, but valid for both channels.

4.3.1.8.3 Status Register 1 – Status register 1 is only useful for KMV11-B. Its layout is identical to the status register 1 channel A.

4.3.1.8.4 Status Register 2 – Status register 2, available at this address, is shared by channel A and channel B. Figure 4-27 shows the layout of this register.

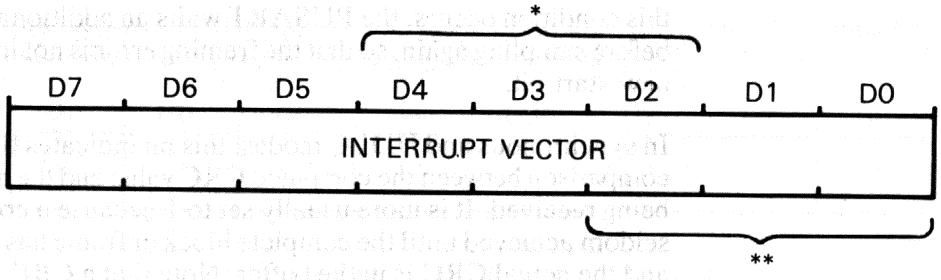


Figure 4-27 Status Register 2(B) Layout

Reading status register 2(B) returns the interrupt vector that was programmed into control register 2(B). If SAV mode is enabled, the value of the vector is modified as follows:

D4 D3 D2 or D2 D1 D0	Condition
<111>	No interrupt pending
<000>	Channel B transmitter buffer empty
<001>	Channel B external/status change
<010>	Channel B received character available
<011>	Channel B special receive condition
<100>	Channel A transmitter buffer empty
<101>	Channel A external/status change
<110>	Channel A received character available
<111>	Channel A special receive condition

As can be seen, code 111 can mean either channel A special receive condition or no interrupt pending. It is simple to separate the two by examining the IP bit (D1) of status register 0, channel A. Note that in non-vectored interrupt mode, in order for the interrupt pending to be valid, the vector register should be read first.

4.3.2 Line Controller Interrupt System and Mode Selection

The four DMA request lines (RXA DMA REQUEST, RXB DMA REQUEST, TXA DMA REQUEST, and TXB DMA REQUEST) and the PUSART interrupt request line are used to generate five different interrupt vectors according to the following:

Condition	Vector	Priority Level
Receive A	140	7
Receive B	150	7
Transmit A	100	6
Transmit B	110	6
Special condition, external/status	120	5

You are therefore recommended to initialize the PUSART with the following parameters:

- Control register 1

  1. External/status interrupt enable
  2. Transmitter interrupt (DMA) enable
  3. Status affects vector enable (channel B CR1)
  4. Receiver interrupt on first character and DMA on first and following characters

  This initialization has to be done for both channels when using the KMV11-B.

  For the KMV11-A the external/status interrupt enable (channel B) may be set if interrupts on changes of state of CCITT 125* or CCITT 107* are wanted.

  Recommended initialization parameters for control register 1 (values in octal):

KMV11-A (single line)	KMV11-B (dual line)
CHA control reg 1: 17	CHA control reg 1: 17
CHB control reg 1: 5	CHB control reg 1: 17

- Control register 2

  This control register (channel A) defines the mode of operation of the PUSART for both channels, therefore parameters are the same for the KMV11-A and the KMV11-B.

* Refer to Table 4-14 for EIA equivalent signals.

Recommended initialization parameters (in octal) for control register 2 (channel A) = 26:

1. Both channels DMA
2. Priority: RxA > RxB > TxA > TxB > special condition
3. Vector bits 0, 1, and 2 are affected on special condition interrupt or external/status interrupt.

NOTE

After power up, INIT, or channel reset, DMA interrupt requests are waiting until this register has been set up.

- Control register 2 (channel B)

  This should be loaded with 0, so that the variable vector bits would provide an offset pointer to the appropriate special condition interrupt routine or external/status interrupt routine.

NOTE

As bits 0, 1, and 2 are affected, the vector would have to be shifted one bit to the left, before being used as a word address.

The rest of the control registers would be programmed with the protocol, receiver, and transmitter parameters wanted for each channel.

The layout of these registers may be found in Section 4.3.1.

4.3.3 HDLC Operation Example

The values of bytes are given in octal notation in this section.

Mode configuration:

1. Issue a Channel Reset (CR) command [CR0(A): 30]
2. Set mode [CR2(A): 26]
3. Load dummy vector [CR2(B): 0]
4. HDLC mode [CR4(A): 40]
5. Load HDLC flag [CR7(A): 176]
6. Load HDLC address [CR6(A): xxx]

Turn on the transmitter, receiver, and modem monitor:

1. Issue a Reset External/Status Interrupts (RE/SI) command [CR0(A): 20]
2. Set interrupt/DMA enables [CR1(A): 17]

3. Set CCITT 125*, CCITT 107*, interrupt enables [CR1(B): 5]
4. Enable transmitter [CR5(A): 151]

   (the PUSART proceeds to transmit flags)

5. Enable receiver [CR3(A): 331] or enable receiver/address recognition [CR3(A): 335]
6. Issue a Reset External/Status Interrupts (RE/SI) command [CR0(A): 20]
7. Issue an Enable Interrupt on Next Character (EINC) command [CR0(A): 40]
8. Expect interrupts on modem signal changes or start of frame reception.

Frame transmissions:

1. Issue a Reset Transmitter CRC Checker (RTCC) command [CR0(A): 200]
2. Load the first character into the transmitter buffer
3. Issue a Reset IDLE/CRC Latch (RI/CL) command [CR0(A): 300]

Transmit loop:

1. On interrupts to TX vector (100) load next characters
2. Repeat above until end of block or frame
3. Ignore interrupt to TX vector, when all transmitted
4. Wait for interrupt to PUSART vector (120), indicating that CRC is being transmitted
5. Wait for interrupt to TX vector, indicating CRC is transmitted
6. If next block or frame is ready to be transmitted, go to 'Transmit loop', else:

   a. Issue a Reset External/Status Interrupts (RE/SI) command [CR0(A): 20]

   b. Issue a Reset Pending Transmitter Buffer Interrupt or DMA Request (RPTBIDR) command [CR0(A): 50]

   (The PUSART proceeds to transmit flags.)

* Refer to Table 4-14 for EIA equivalent signals.

Underrun error:

This error will be detected, at the same time as the IDLE/CRC bit (bit D6) of status register 0, when CRC transmission is started due to an empty transmitter.

1. Issue a Send Abort (SA) command [CRO(A): 10]
2. Issue a Reset External/Status Interrupts (RE/SI) command [CR0(A): 20]
3. Issue a Reset Pending Transmitter Buffer Interrupt or DMA Request (RPTBIDR) command [CR0(A): 50]

   (The PUSART proceeds to transmit flags.)

Frame reception:

1. An external/status interrupt to PUSART vector (120) will occur, indicating that a flag has been received
2. Issue a Reset External/Status Interrupts (RE/SI) command
3. The first character received will cause an interrupt to the RXA (140) and to the PUSART vector (120)
4. Read character; ignore PUSART receive interrupt.

Receive loop:

```
On interrupt to the RXA (140) vector
If status register 1 indicates no EOF
     Then read character and indicate end of interrupt
       [CR0(A): 70]
     Else
          While status register 0 indicates data available
            Read character, release latch
            [CR0(A): 60]
          Endwhile
Endif
```

(Modem line changes and abort detection are indicated by external/status interrupts.)

4.4 LINE CLOCK – REAL-TIME CLOCK INTERFACE

Two line clocks and one real-time clock are implemented within an 8254 timer/counter IC.

This IC provides three programmable down-counters.

4.4.1 Line Clock – Real-Time Clock Register Description

Address 120 000 is a 1-byte read-only register contained within the 8254 clock IC. This register may be used to read back the clock divider ratio for the channel A line clock generator.

Address 120 002 is a 1-byte write-only register contained within the 8254 clock IC. This register is used to load the clock divider ratio for the channel A line clock generator.

Addresses 120 004 and 120 006 are identical in functional description to 120 000 and 120 002, except that they apply to the channel B line clock generator.

NOTE

Channel B will not be implemented in the KMV11-A.

Addresses 120 010 and 120 012 are identical to 120 000 and 120 002, except that they apply to the real-time clock generator.

Address 120 016 is a 1-byte write-only register within the 8254 clock IC and is used to define the mode of the clock counter IC.

4.4.2 Line Clock Programming

Two counters provide local transmit/receive clocks for null modem connections or test purposes. A and B line clocks are identical, but the B line clock is only useful with the KMV11-B.

Both counters are fed with a 6912 kHz clock. The divider ratio for both counters may be programmed from 1 to $32{,}768_{10}$ in binary mode or from 1 to $10{,}000_{10}$ in BCD mode.

In order to generate a square wave with an even mark space ratio, as needed by the transmitter/receiver, the initialization parameter for the two counters should be specified as mode 3 (square wave). The use of even divider values is recommended.

By using the following formula, the synchronous bit rates may be computed.

Bit rate (kbits/s) = 6912/divider ratio

Standard bit rates:

Divider (decimal)	Bit Rate (kbits/s)	Actual Bit Rate (kbits/s)
108	64	64
124	56	55.74*
144	48	48
360	19.2	19.2
720	9.6	9.6
1440	4.8	4.8
2880	2.4	2.4
5760	1.2	1.2

* Error = 0.5%

For asynchronous bit rates, the PUSART IC needs at least a 16-times clock, and the appropriate formula is:

Bit rate (kbits/s) = 432/divider ratio

Asynchronous	Bit Rates (kbits/s)	(16-Times Clock Mode) (kbits/s)
22	19.2	19.63*
45	9.6	9.6**
90	4.8	4.8
180	2.4	2.4
360	1.2	1.2
720	0.6	0.6
1440	0.3	0.3

* Error = 2.25%

** Acceptable clock distortion of less than 1%

For maintenance or special applications the output of the A LINE CLOCK may be applied to the TRANSMIT CLOCK A, RECEIVE CLOCK A; and the output of the B LINE CLOCK to the appropriate channel B clock inputs of the PUSART IC. This is done by asserting the SCM bit (bit 5) in Port C of the 8255 IC (address 130 006).

The line clocks are always available on the CCITT 113 modem circuit, (channel A and channel B for KMV11-B), regardless of the maintenance mode referred to above.

NOTE

When PTT requirements specify that the CCITT 113 circuit is to be held in a steady OFF state, then no divider ratio should be programmed into the clock IC for the relative counter(s).

4.4.3 Real-Time Clock Programming

The third counter within the 8254 IC is available as a real-time clock.

Its output will generate an interrupt to vector 130 on priority level 5.

Two modes of operation are available:

- One-shot mode (mode 0)
- Clock mode (mode 2)

In one-shot mode the counter will interrupt after the timeout and then stop. In clock mode the counter will interrupt once for every time interval.

Time intervals for both modes may be computed according to the following formula:

Time = 18.5 microseconds × (N + 1)

where N is programmable from 1 to $32{,}768_{10}$ in binary mode, and from 1 to 10,00010 in BCD mode.

In addition to processor priority level masking, RTC bit 0 of the 8255 Port C (address 130 006) disables/enables the real-time clock interrupt.

In addition, this bit must be cleared after an RTC interrupt has taken place, to acknowledge the interrupt. It may then be set again to enable the next clock interrupt.

4.4.4 Line Clock – Real-Time Clock Parameter Setting

Before any of the three counters are to be used, the appropriate control byte has to be written into the 8254 IC. The control byte write address is 120 016.

The byte layout is shown in Figure 4-28.

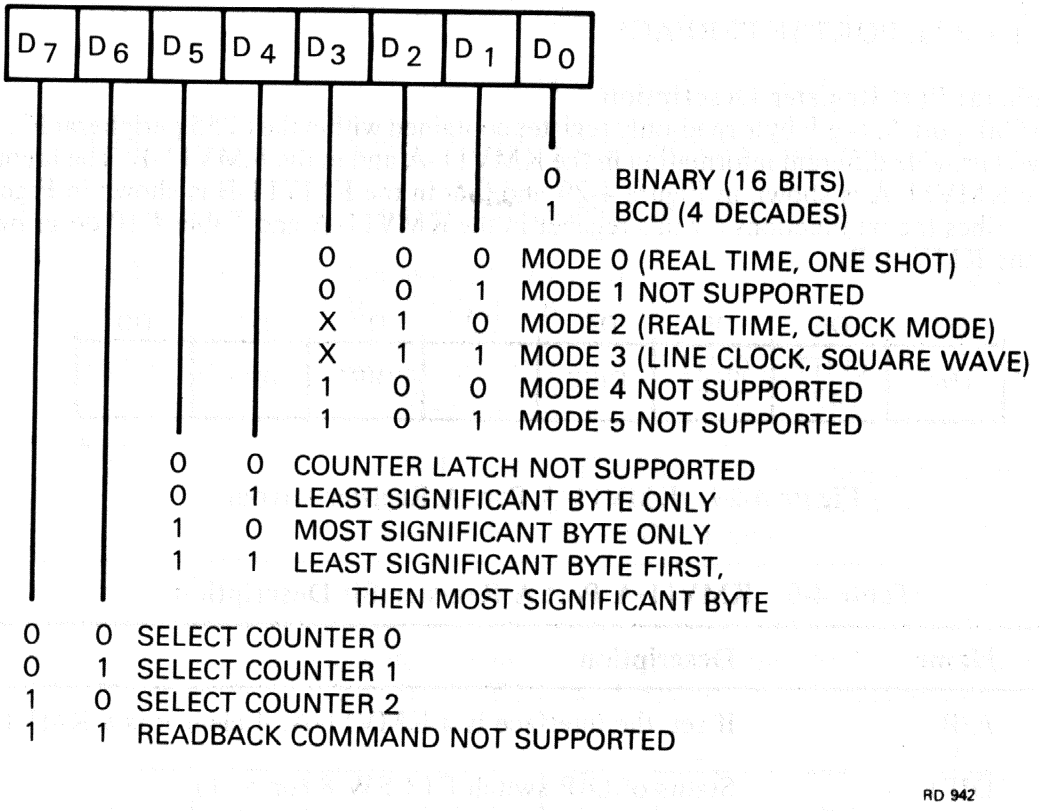


Figure 4-28 Clock Control Register Bit Functions

Typical parameter load sequences:

```
MOVB #076,@#120016  ; Control word for A-line clock
MOVB #LSB,@#120002  ; Load LSB for A-counter
MOVB #MSB,@#120002  ; Load MSB for A-counter

MOVB #136,@#120016  ; Control word for B-line clock
MOVB #LSB,@#120006  ; Load LSB for B-counter

MOVB #274,@#120016  ; Control word for RTC
MOVB #LSB,@#120012  ; Load LSB for RTC
MOVB #MSB,@#120012  ; Load MSB for RTC
```

Summary of 8254 addresses:

120 016 : IC mode line register, write only
120 000 : Line clock A counter read *
120 002 : Line clock A counter write

120 004 : Line clock B counter read *
120 006 : Line clock B counter write
120 010 : RTC counter read *
120 012 : RTC counter write

* Read operation is possible, but not supported.

4.5 PERIPHERAL PORT INTERFACE

4.5.1 Peripheral Port Register Description

Address 130 000, port A, is a 1-byte read-only register contained within the 8255 peripheral IC. Reading this register will provide different information in the KMV11-A and in the KMV11-B. The layout of this register in the KMV11-A is shown in Figure 4-29 and that in the KMV11-B is shown in Figure 4-30. Table 4-9 describes the bit functions for this register in the KMV11-A and Table 4-10 describes the bit functions in the KMV11-B.

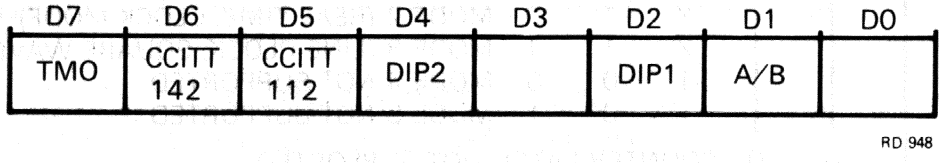


Figure 4-29 KMV11-A Port A Register Layout

Table 4-9 KMV11-A Port A Register Bit Description

Bit	Name	Description
D 1	A/B	If set, the interface is a KMV11-A, if clear it is a KMV11-B.
D 2	DIP1	Status of DIP switch E13 SW 8 (on = 1).
D 4	DIP2	Status of DIP switch E29 SW 10 (on = 1).
D 5	CCITT 112	Status of CCITT modem circuit 112 (Data Signal Rate Selector DCE), CCITT 112 on = 0.
D 6	CCITT 142	Status of CCITT modem circuit 142 (Test Indicator), CCITT 142 on = 0.
D 7	TMO	Latched timeout. This bit will be set when a timeout has occurred during a DMA IN or DMA OUT transaction. It is cleared by a following DMA IN or DMA OUT.

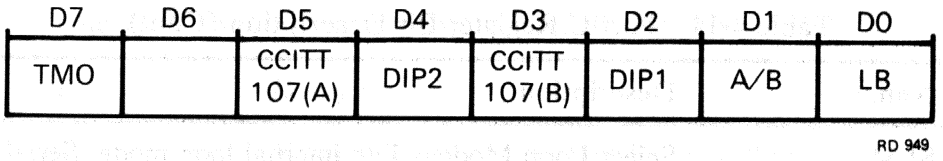


Figure 4-30 KMV11-B Port A Register Layout

Table 4-10 KMV11-B Port A Register Bit Description

Bit	Name	Description
D 0	LB	Loopback connector is in place if this bit is 0.
D 1	A/B	If set, the interface is a KMV11-A, if clear it is a KMV11-B.
D 2	DIP1	Status of DIP switch E24 SW 8 (on = 1).
D 4	DIP2	Status of DIP switch E36 SW 10 (on = 1).
D 3	CCITT 107B	Status of CCITT modem circuit 107 (Data Set Ready) for channel B, CCITT 107B on = 1.
D 5	CCITT 107A	Status of CCITT modem circuit 107 (Data Set Ready) for channel A, CCITT 107A on = 1.
D 7	TMO	Latched timeout. This bit will be set when a timeout has occurred during a DMA IN or DMA OUT transaction. It is cleared by a following DMA IN or DMA OUT.

Address 130 006, Port C, is a 1-byte write-only register contained within the 8255 peripheral IC. Figure 4-31 shows the bit layout for this register and Table 4-11 describes the bit functions.

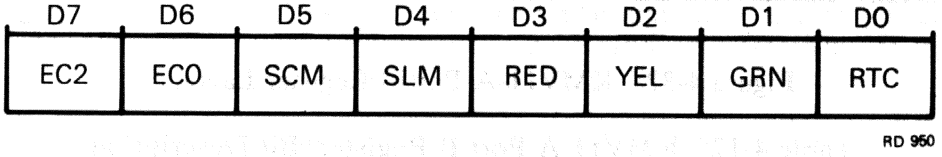


Figure 4-31 Port C Register Layout

Table 4-11 Port C Register Bit Description

Bit	Name	Description
D 0	RTC	Enable the real-time clock if this bit is set.
D 1	GRN	Green LED on if this bit is set.
D 2	YEL	Yellow LED on if this bit is set.
D 3	RED	Red LED on if this bit is set.

Table 4-11 Port C Register Bit Description (Cont)

Bit	Name	Description
D 4	SLM	Select Loop Mode – 1 = internal loop mode. Serial transmit and receive are looped internally to the PCB. The CCITT 103 (Transmit Data) lead is in the 1 (marking) state. For the KMV11-B, this mode is selected for both channels at the same time.
D 5	SCM	Select Clock Mode – 1 = internal clock mode. In internal clock mode, the DTE Transmit Signal Element Timing signals are provided by the channel A clock generator. This bit, together with bit D4, is used for maintenance purposes. For the KMV11-B, this bit selects only channel A.
D 6	EC0	Enable CSR 0 interrupt. When this bit is set, any write access from the host to BSEL0 (address 100 000) will generate an interrupt at priority level 4, via vector 60. In order to acknowledge the interrupt, the EC0 interrupt must be cleared and set again to reset the interrupt-sensing logic.
D 7	EC2	Enable CSR 2 interrupt. This bit is identical to bit D6 except that it applies to BSEL2 (address 100 002) and interrupt vector 70.

Address 130 012, port B, is a 1-byte write-only register contained within the 8255 peripheral IC. Writing into this register will program different functions in the KMV11-A and the KMV11-B. The bit layout for this register in the KMV11-A is shown in Figure 4-32 and that for the KMV11-B is shown in Figure 4-33. Table 4-12 describes the bit functions for this register in the KMV11-A, and Table 4-13 describes the bit functions in the KMV11-B.

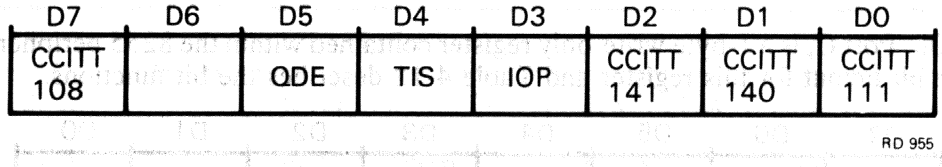


Figure 4-32 KMV11-A Port B Register Layout

Table 4-12 KMV11-A Port B Register Bit Description

Bit	Name	Description
D 0	CCITT 111	CCITT modem control line 111 (Data Signal Rate Selector DTE), 1 = CCITT 111 on.
D 1	CCITT 140	CCITT modem control line 140 (Loopback and Maintenance Test), 1 = CCITT 140 on.
D 2	CCITT 141	CCITT modem control line 141 (Local Loopback), 1 = CCITT 141 on.

Table 4-12 KMV11-A Port B Register Bit Description (Cont)

Bit	Name	Description
D 3	IOP	When this bit is set, the DMA logic will access the address indicated in the DMA registers on the I/O page. This function will allow the KMV11 to communicate with other devices on the Q-bus.
D 4	TIS	Terminal In Service – This bit is used by the diagnostic firmware to detect the presence of the loopback connector. This is called circuit IS in EIA specification RS-422-A and RS-423-A (RS-449).
D 5	QDE	This bit must be set to enable the DMA register to start a DMA cycle when the extended address bits are written.
D 7	CCITT 108	CCITT modem control line 108/2 (Data Terminal Ready), 1 = CCITT 108/2 on.

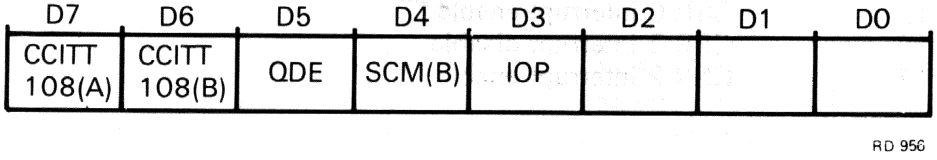


Figure 4-33 KMV11-B Port B Register Layout

Table 4-13 KMV11-B Port B Register Bit Description

Bit	Name	Description
D 3	IOP	When this bit is set the DMA logic will access the address indicated in the DMA registers on the I/O page. This function will allow the KMV11 to communicate with other devices on the Q-bus.
D 4	SCM-B	Select Clock Mode channel B. 1 = internal clock mode. In internal clock mode, the DTE Transmit Signal Element Timing signals are provided by the channel B clock generator. This bit, together with bit D4 in port C is used for maintenance purposes.
D 5	QDE	This bit must be set to enable the DMA register to start a DMA cycle when the extended address bits are written.
D 6	CCITT 108B	CCITT modem control line 108/2 for line B (Data Terminal Ready), 1 = CCITT 108/2B on.
D 7	CCITT 108A	CCITT modem control line 108/2 for line A (Data Terminal Ready), 1 = CCITT 108/2A on.

Address 130 016 is a 1-byte write-only register contained within the 8255 peripheral IC. It is loaded by the root firmware at start-up time with the correct mode for the 8255 IC (220_8).

This control register may also be used to perform bit setting and clearing of the port C register. Loading octal parameters will give the following results:

Parameter	Action
0	RTC disable
1	RTC enable
2	Green LED off
3	Green LED on
4	Yellow LED off
5	Yellow LED on
6	Red LED off
7	Red LED on
10	Internal loopback disable
11	Internal loopback enable
12	Clock source external
13	Clock source internal
14	CSR 0 interrupt disable
15	CSR 0 interrupt enable
16	CSR 2 interrupt disable
17	CSR 2 interrupt enable

4.5.2 Modem Monitoring and Control

Modem lines may be monitored or controlled in part through the PUSART line controller IC, and in part through the 8255 peripheral IC.

Modem line assignments for the single-line KMV11-A are different to those of the dual-line KMV11-B.

KMV11-A: The selection of balanced/unbalanced operation is done via DIP switches on the module. Please refer to the technical manual for location and setting.

KMV11-B: The selection of balanced/unbalanced operation is done via modem cable assembly.

Modem lines monitored through the PUSART IC:

KMV11-A: CCITT 106, CCITT 109, CCITT 107, CCITT 125

KMV11-B: CCITT 106A, CCITT 109A, CCITT 106B, CCITT 109B.

A change of state on these signals may set up an interrupt to PUSART vector 120 if the PUSART IC has been correctly set up.

See Section 4.3.1 for PUSART programming of appropriate modem lines.

Table 4-14 List of Supported Modem Signals

CCITT	RS449	RS232	DIN 66020	DEC STD 52	REMARK
101	(none)	AA	E1	PRT GND	
102	SG	AB	E2	SIG GND	
103	SD	BA	D1	TxD	D
104	RD	BB	D2	RxD	D
105	RS	CA	S2	RTS	D
106	CS	CB	M2	CTS	I,D
107	DM	CC	M1	DSR	IA,D
108/2	TR	CD	S1.2	DTR	D
109	RR	CF	ME	CD	I
111	SR	CH	S4	DSRS	A
112	SI	CI	(none)	SPDMI	A
113	TT	DA	T1	TxClock(DTE)	D
114	ST	DB	T2	TxClock(DCE)	D
115	RT	DD	T4	RxClock(DCE)	D
140	RL	(none)	PS2	Rem LPBK	A
141	LL	(none)	PS3	Local LP REQ	A
142	TM	(none)	PM1	Test Indicator	A
125	IC	CE	M3	RI	A
(none)	IS	(none)	(none)	(none)	*

SG = Signal Ground
SD = Send Data
RD = Receive Data
RS = Request to Send
CS = Clear to Send
DM = Data Mode
TR = Terminal Ready
RR = Receiver Ready
SR = Signaling Rate selector
SI = Signaling Indicator
TT = Terminal Timing
ST = Send Timing
RT = Receive Timing
RL = Remote Loopback
LL = Local Loopback
TM = Test Mode
IC = Incoming Call
IS = In Service (terminal)

COMMENTS

A = Available on KMV11-A only

D = Transmitted class 1 circuit available as either RS-422 or RS-423 signal

I = Interrupts from both KMV11-B channels

IA = Causes interrupts (KMV11-A only)

* = There is no approved CCITT equivalent circuit (it may become CCITT 135)

KMV11-A: PUSART status register 0, channel A

Bit 3 = inverse of CCITT 109
Bit 5 = inverse of CCITT 106

PUSART status register 0, channel B

Bit 3 = inverse of CCITT 107
Bit 5 = inverse of CCITT 125

KMV11-B: PUSART status register 0, channel A

Bit 3 = inverse of CCITT 109 channel A
Bit 5 = inverse of CCITT 106 channel A

PUSART status register 0, channel B

Bit 3 = inverse of CCITT 109 channel B
Bit 5 = inverse of CCITT 106 channel B

NOTE

When the PUSART is programmed for external/ status interrupt, any change in state will cause an interrupt and all the above bits will be latched. They will be unlatched via the RE/SI command.

Modem lines controlled through the PUSART integrated circuit:

CCITT 105 and CCITT 105 channel B (KMV11-B).

The Request to Send lines are controlled through PUSART control register, channel A, bit 1 and PUSART control register, channel B, bit 1 for the two channels.

With the KMV11-B, before using this bit in channel B, control register 2, channel A must have been correctly set up (bit 7 = 0).

Modem circuits monitored through the 8255 peripheral integrated circuit:

The Port A address 130 000 is used to monitor the following modem circuits in their true (non-inverse) state:

Port A	KMV11-A	KMV11-B
BIT 3	–	CCITT 107B
BIT 5	CCITT 112	CCITT 107A
BIT 6	CCITT 142	–

These signals will have to be scanned to detect a state change.

Modem circuits controlled through the 8255 peripheral IC:

The Port B address 130 013 is used to control the following modem circuits in their true (non-inverse) state.

Port B	KMV11-A	KMV11-B
BIT 0	CCITT 111	–
BIT 1	CCITT 140	–
BIT 2	CCITT 141	–
BIT 6	–	CCITT 108/2B
BIT 7	CCITT 108/2	CCITT 108/2A

Maintenance loop back:

External loop:

When loopback connections are fitted to the KMV11 module or to the modem cables(s) for test purposes, the following connections are made.

KMV11-A and KMV11-B:

103	(TxD)	to	104	(RxD)
113	(ATxCLK)	to	114	(TxCLK)
	and	to	115	(RxCLK)
105	(RTS)	to	106	(CTS)
	and	to	109	(CD)
108/2	(DTR)	to	107	(DSR)

KMV11-A only:

111	(DSRS)	to	112	(SPDMI)
141	(LL)	to	142	(Test Indicator)
	(IS)	to	125	(RI)

KMV11-B only:

103	(TxD)	to	104	(RxD)
113	(ATxCLK)	to	114	(TxCLK)
	and	to	115	(RxCLK)
105	(RTS)	to	106	(CTS)
	and	to	109	(CD)
108/2	(DTR)	to	107	(DSR)

Internal loop:

KMV11-A AND KMV11-B:

Address 130 006, bit 4 (SLM) when set, creates an internal loop.

Transmitter output (TTL) connected to receiver input.

The TxD output will be in the marking state. The RxD input is ignored. Modem lines are not affected.

For the KMV11-B, SLM creates a loop for both channels at the same time.

4.6 HOST INTERRUPT AND Q-BUS CONTROL INTERFACE

4.6.1 Host Interrupt and Q-Bus Control Register Description

Address 140 000 contains the Q-bus control register. This write-only register is implemented to allow the Q-bus control functions described in Table 4-15. The layout of this register is shown in Figure 4-34.

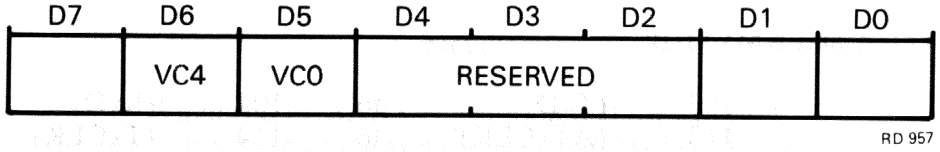


Figure 4-34 Q-Bus Control Register Layout

Table 4-15 Q-Bus Register Function Description

Bit	Name	Description
D 5	VC0	Q-IRQ0 – When this bit is set, an interrupt on the Q-bus to vector xx0 will be generated. xx is defined by the vector DIP switch configuration. As the interrupt hardware needs a leading edge, it is necessary to clear this bit before setting it. Only one interrupt will be generated per 0 to 1 transition.
D 6	VC4	Q-IRQ4 – This bit performs an identical function to bit D5, except that the interrupt vector will be xx4 instead of xx0.

4.6.2 Host Interrupt and Q-bus Control Programming

Interrupts in the host Q-bus system may be set up for two different vectors. The vectors are xx0 and xx4, where xx is defined by the setting of DIP switches. Refer to the technical manual for the correct setting.

An interrupt to vector xx0 is generated by asserting VC0, bit 5 of address 140 000.

As the interrupt logic needs a leading edge transition, the appropriate bit must be clear before setting it.

CHAPTER 5
SERVICE

5.1 SCOPE

This chapter contains information for servicing the KMV11-A. It includes the maintenance philosophy, maintenance functions, preventive maintenance, and corrective maintenance. The section on corrective maintenance contains a short description of the diagnostics for the KMV11-A.

5.2 MAINTENANCE PHILOSOPHY

The field replaceable unit (FRU) for the KMV11 is either a defective module or cable. The training of Field Service personnel concentrates on the use of diagnostics to isolate the FRU. Spare parts for module repair are not available in the field. Typical applications of the KMV11 do not permit long troubleshooting sessions. Component troubleshooting and repair needs at least a 16-channel logic analyzer.

CAUTION

When inserting or removing the KMV11 module, be sure not to move any components mounted on sockets (for example, PROMs or the microprocessor).

5.3 MAINTENANCE TOOLS AND FEATURES

The following features are provided with the KMV11 to help fault isolation and status checking:

- LED indicators
- On-board diagnostics
- Line clock and loopback connectors.

5.3.1 LED Indicators

Five small red LED indicators show the status of the following modem signals (at TTL level):

CCITT 103	Transmit Data	(inverted, MARK = LED OFF)
CCITT 104	Receive Data	(true, MARK = LED ON)
CCITT 107	Data Set Ready	(true, ON = LED ON)
CCITT 106	Clear to Send	(true, ON = LED ON)
CCITT 109	Carrier Detect	(true, ON = LED ON)

Three large colored LEDs are operated by the microcode.

The physical location of the LEDs is shown in Figure 5-1.

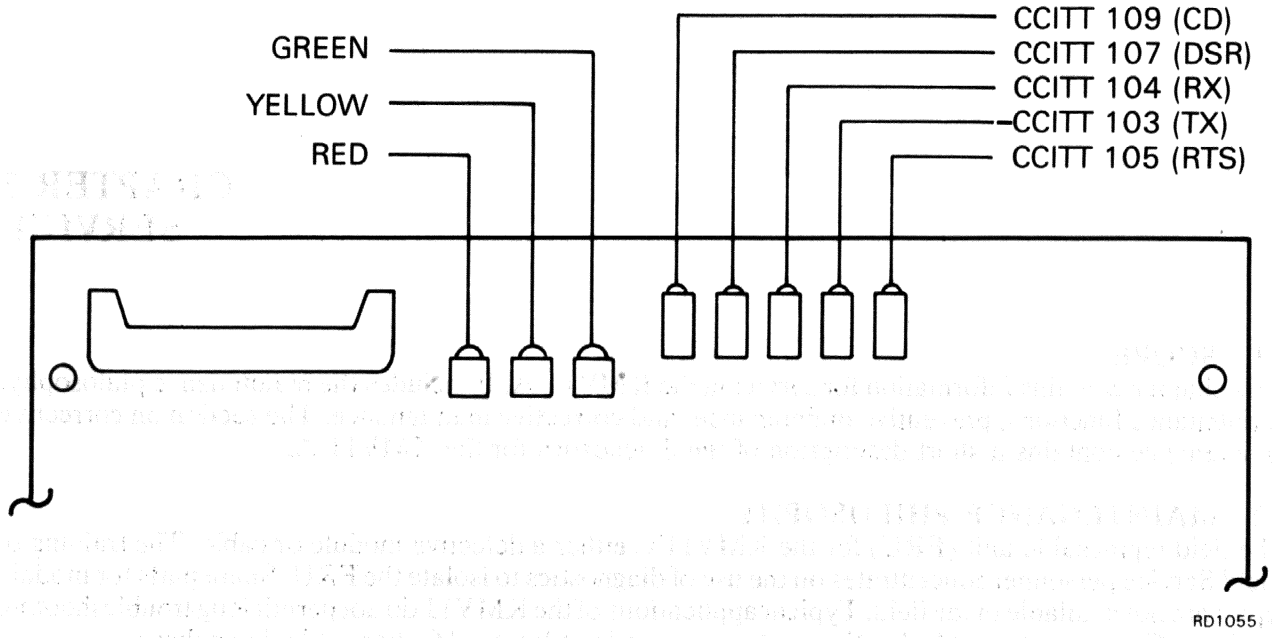


Figure 5-1 LED Indicator Location

Table 5-1 shows the meaning of the microcode-operated LED display.

NOTE

This table is only true for the PROM-resident firmware. Application firmware may drive the LEDs in other ways.

Table 5-1 LED Meaning

LED Status			State	Comment
Red	Yellow	Green		
OFF	ON	OFF	KMV power on self-test disabled self-test started	Steady state if self-test is disabled, 10 seconds, at self-test start
OFF	ON	ON	Self-test execution for 1 pass	10 seconds duration
OFF	OFF	ON	Self-test successful completion	Steady state
ON	OFF	OFF	Self-test error	Steady state on first error
OFF	ON	ON/ OFF	Normal self-test running in continuous loop	10-second period between green ON/OFF states

Table 5-1 LED Meaning (Cont)

LED Status Red	Yellow	Green	State	Comment
OFF	ON	ON/ OFF	Extended self-test running in continuous loop	½-second period between green ON/OFF states
OFF	ON	ON/ OFF	Logic or line controller diagnostic running without errors	Random periods between green ON/OFF states
OFF/ ON	ON	ON/ OFF	Logic or line controller diagnostic running with errors	Random periods between green and red ON/OFF states depending on number of errors and diagnostic

5.3.2 Self-Test

The major part of the PROM-resident firmware is for on-board diagnostic facilities. Routines may be used by the host-resident diagnostic or in a chained mode by the self-test.

The self-test will run in one of the following modes. The modes are selected by on-board dip switches:

a. Single pass on power-up or when requested by the host software's setting the run and MCLR bits together

b. Continuous loop on power-up

c. Continuous loop on power-up with extended diagnostic routines.

Refer to Table 5-2 for the switch configuration and Figure 5-2 for the self-test switch locations.

Table 5-2 Self-Test Switch Configuration

State E13–8	E29–10	Action
ON	ON	Self-test disabled
ON	OFF	Self-test runs for one pass at power-up or when run bit asserted together with MCLR bit
OFF	OFF	Self-test starts to run in endless loop at power-up: normal mode
OFF	ON	Self-test starts to run in continuous loop at power-up: extended mode

Note that the loop time for normal mode is approximately 30 seconds, while for extended mode it can be as long as 1 hour! Correct execution of the extended self-test needs either the module loopback connector (H3255) or the RS-422/RS-423 modem cable assembly with loopback connector (H3251).

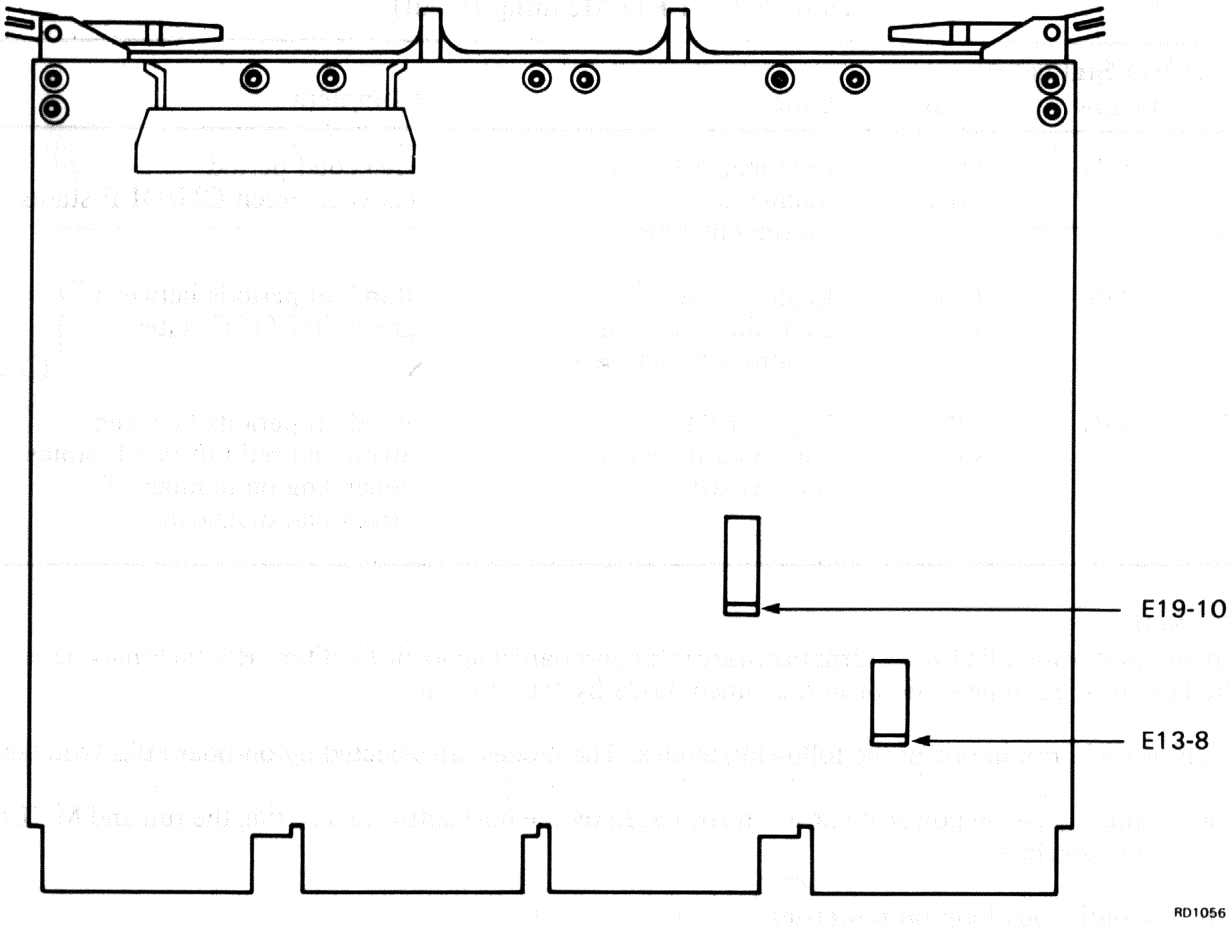


Figure 5-2 Self-Test Switch Locations

On detection of any error condition, testing will be aborted and the red LED will be ON (green and yellow OFF). In addition the low-order byte of CSR0 will contain 1xx or 2xx, where xx is the test number in error according to the test number table (Table 5-3).

Table 5-3 Self-Test List

Test	Description (Addresses and Patterns in Octal)	Comment
0	Stack push-pull test (RAM locations 77774, 77776)	S
1	CSR and DMA registers word access test (pattern 52525)	
2	CSR and DMA registers word access test (pattern 125252)	
3	CSR and DMA registers byte access test (pattern 252)	
4	CSR and DMA registers byte access test (pattern 125)	
5	Dynamic RAM data test (pattern 52525)	
6	Dynamic RAM data test (pattern 125252)	
7	Dynamic RAM address test (pattern = address)	
10	Dynamic RAM address test (pattern = address inverse)	
11	Real-time clock test (8254 clock/counter chip)	
12	Baud rate generator test, channel A (8254 clock/counter chip)	
13	Baud rate generator test, channel B (8254 clock/counter chip)	B

Table 5-3 Self-Test List (Cont)

Test	Description (Addresses and Patterns in Octal)	Comment
14	Dynamic RAM address interaction test (pattern 177777)	E
15	PROM checksum verification test	
16	KMV11-B modem signal loopback test, channel A	B,E
17	KMV11-B modem signal loopback test, channel B	B,E
20	RX-TX, channel A, internal loopback, interrupt disabled	
21	RX-TX, channel B, internal loopback, interrupt disabled	B
22	RX-TX, channel A, internal loopback, low-speed,interrupts enabled	
23	RX-TX, channel B, internal loopback, low-speed, interrupts enabled	B
24	RX-TX, channel A, internal loopback, high-speed,interrupts enabled	
25	RX-TX, channel B, internal loopback, high-speed, interrupts enabled	B
26	RX-TX, channel A, external loopback, high-speed, interrupts enabled	E
27	RX-TX, channel B, external loopback, high-speed, interrupts enabled	B,E
30	KMV11-A modem signal loopback test	A,E

COMMENTS
S: This test is always executed at power-up
A: Runs on the KMV11-A only
B: Runs on the KMV11-B only
E: Runs only in extended self-test mode

5.3.3 Line Clock and Loopback Connectors

A programmable line clock is available for transmission and reception without a modem or other external clock source.

5.3.3.1 Line Clock – Two counters provide local transmit/receive clocks for null modem connections or test purposes. The A and B line clocks are identical, but the B line clock is only useful with the KMV11-B.

Both counters are fed with a 6912 kHz clock. The divider ratio or both counters may be programmed from 1 to 32768_{10} in binary mode, or from 1 to 10000_{10} in BCD mode.

For maintenance or special applications the output of the A line clock may be applied to the TRANSMIT CLOCK A, RECEIVE CLOCK A, and the output of the B line clock to the respective channel B clock inputs of the MPSC chip.

The line clocks are always available on the CCITT 113 modem line. (Channel A and channel B for KMV11-B).

NOTE

When PTT requirements specify the CCITT 113 lines to be held in a steady OFF state, no divider ratio should be programmed into the clock chip for the counter(s) concerned.

5.3.3.2 Real-Time Clock – A third counter within the 8254 is available as a real-time clock.

Its output will generate an interrupt to vector 130 on priority level 5 (on-board DCT11 system).

Two modes of operation are available :

- One-shot mode (mode 0)
- Clock mode (mode 2)

In one-shot mode the counter will interrupt after a preset time interval and stop. In clock mode the counter will give a series of interrupts separated by the preset time interval.

Time intervals for both modes may be computed according to the following formula:

$$\text{Time} = 18.5 \text{ microseconds} \times (N + 1)$$

where N is programmable from 1 to 32768_{10} in binary mode, and from 1 to 10000_{10} in BCD mode.

In addition to processor priority level masking, RTC bit 0 of the 8255 port C (address 130 006_8) disables/enables the real-time clock interrupt.

This bit must be reset, after an RTC interrupt has occurred, to acknowledge the interrupt and may then be set again to enable the next clock interrupt.

5.3.3.3 Loopback Connectors/Tests – Three types of loopback are available for use with the KMV11-A:

1. Module – provided by H3255 for use on the M7500 module connector J1.

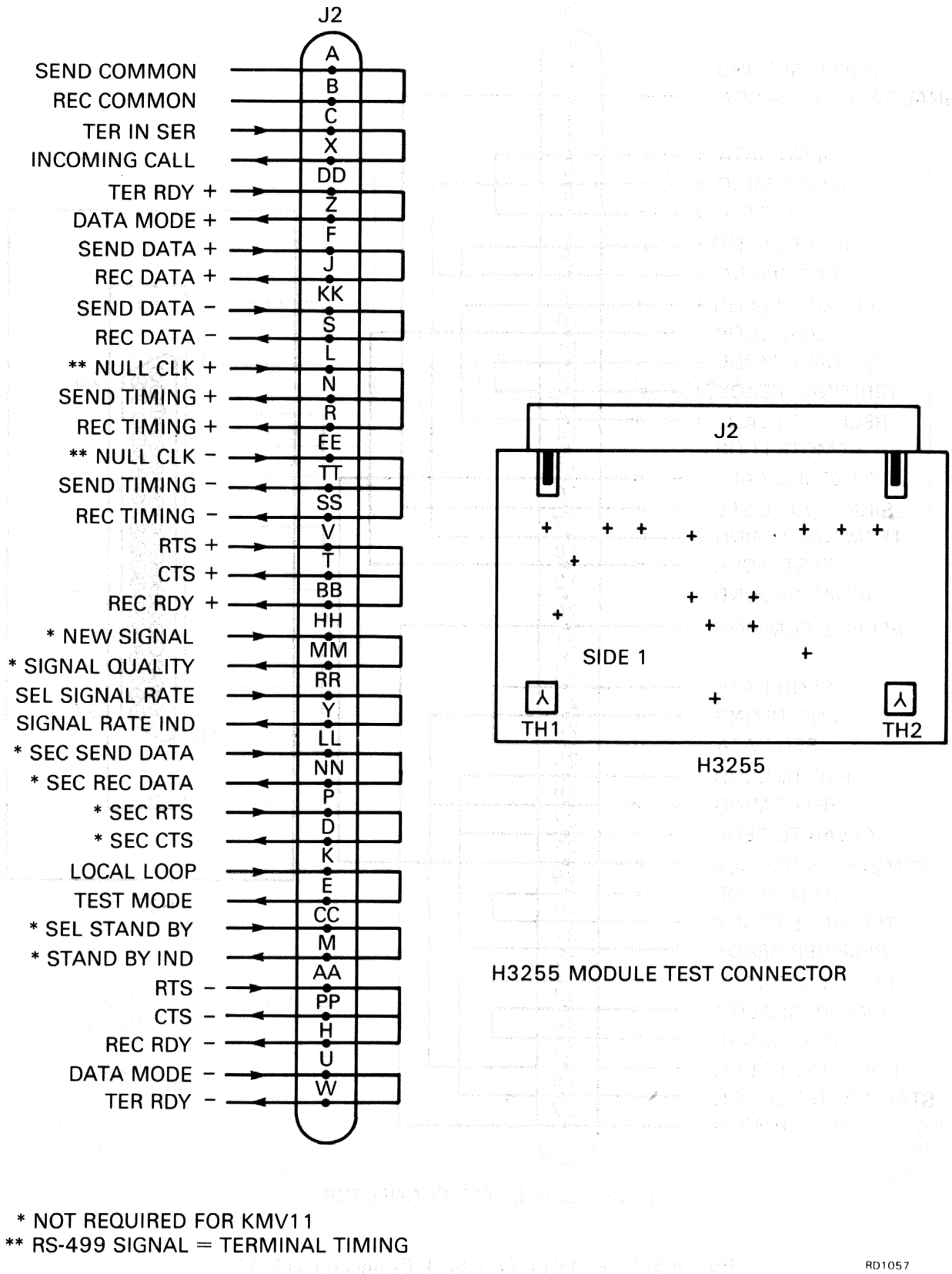
2. Cable – provided by:

   a. H3251 for 37-pin RS-449 cable connectors
   b. H325 for 25-pin RS-232 cable connectors (see note)

NOTE

The RS232 loopback (H325) connector cannot be used for modem signal loopback tests. It does not provide turnaround for all modem signals used by the KMV11.

3. Modem – some types of modem have internal loopback facilities. This feature is used by the functional diagnostic VKMC on the KMV11-A only. Both local and remote modems may provide the loopback.



H3255 MODULE TEST CONNECTOR

* NOT REQUIRED FOR KMV11
** RS-499 SIGNAL = TERMINAL TIMING

RD1057

Figure 5-3 KMV11 Loopback Connector H3255

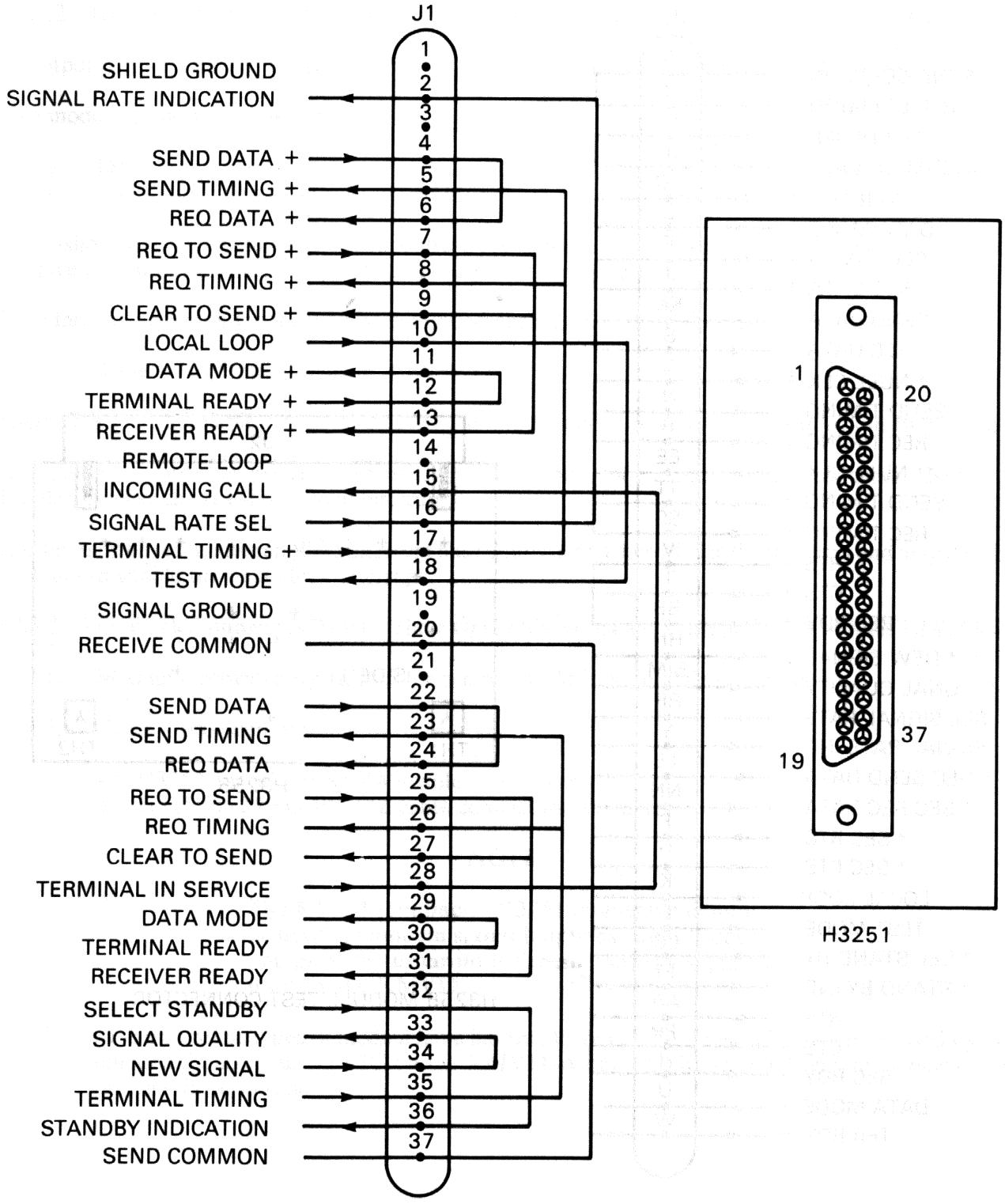


Figure 5-4 KMV11 Loopback Connector H3251

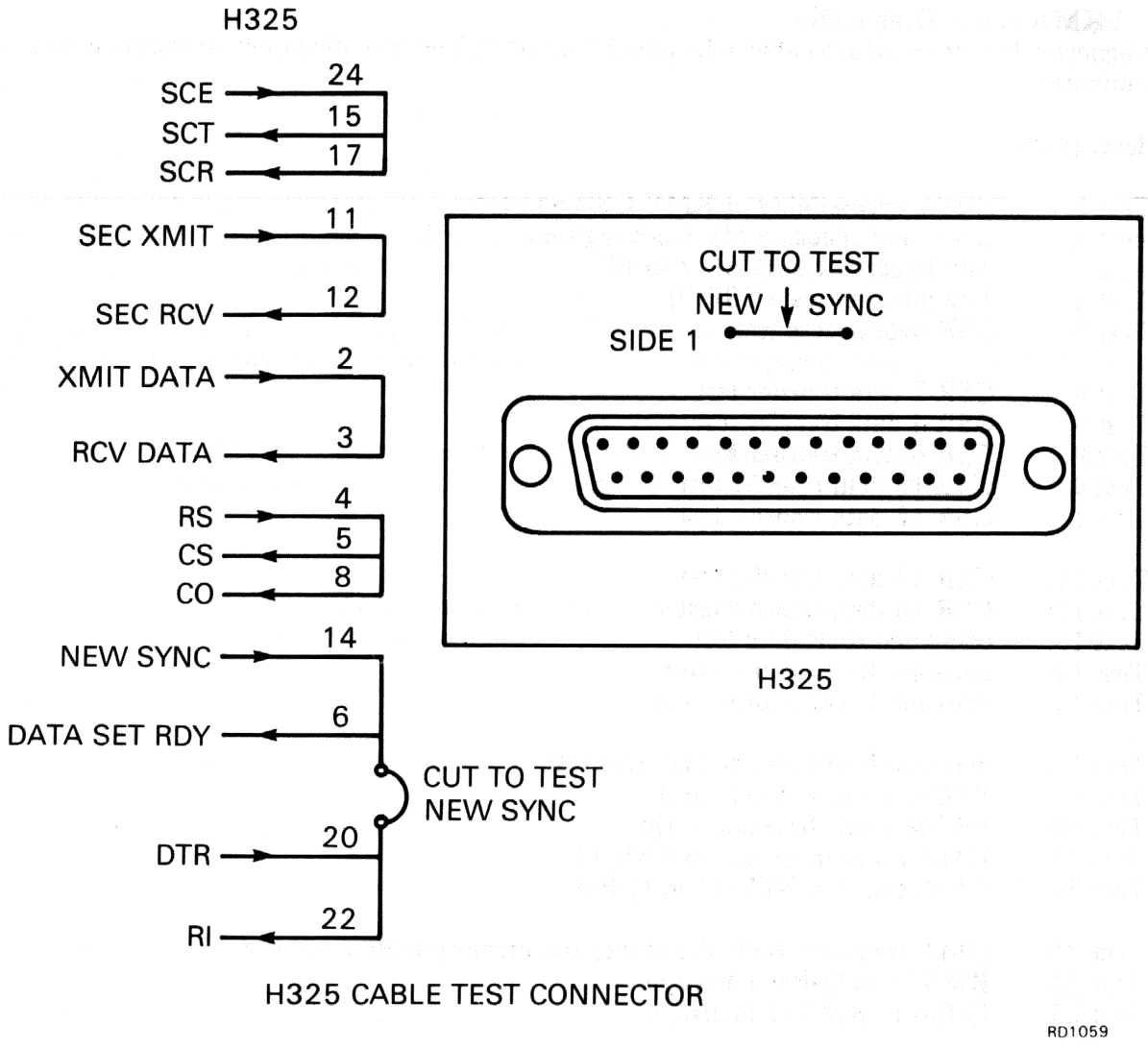


Figure 5-5 KMV11 Turnaround Connector H325

5.4 DIAGNOSTICS

As well as the on-board self-test, four diagnostic programs are provided with the KMV11-A:

1. VKMA logic diagnostic
2. VKMB line controller diagnostic
3. VKMC functional diagnostic
4. XKMD DECX-11 exerciser module

The first three programs are run under the standalone diagnostic supervisor. They must be overlaid with the diagnostic supervisor, or be previously combined with it and loaded as a single file. In both methods, the programs will not exceed 16K of memory with the exception of the VKMC functional diagnostic.

5.4.1 VKMA Logic Diagnostic

This diagnostic does not need any cable or loopback connector. The execution time for one error-free pass is five minutes.

Test description:

Test 1: checks accessibility of KMV CSR addresses
Test 2: clears and checks KMV CSR registers
Test 3: data integrity test (CSR 2 to 16)
Test 4: data integrity test (CSR 0)
Test 5: CSR byte access test

Test 6: CSR 2 data transfer test
Test 7: CSR 4 data transfer test
Test 8: CSR 6 data transfer test
Test 9: CSR 10 data transfer test
Test 10: CSR 12 data transfer test

Test 11: CSR 14 data transfer test
Test 12: CSR 16 data transfer test
Test 13: combined CSR data test
Test 14: dynamic RAM pattern test
Test 15: dynamic RAM address test

Test 16: dynamic RAM inverted address test
Test 17: PROM revision level check
Test 18: PROM read checksum verify
Test 19: DMA transfer, Q-Bus to KMV11
Test 20: DMA transfer, KMV11 to Q-Bus

Test 21: DMA transfers, both directions, and memory interaction test
Test 22: KMV11 to Q-Bus interrupts
Test 23: Q-Bus to KMV11 interrupts

5.4.2 VKMB Line Controller Diagnostic

This diagnostic may run in either internal or external loopback mode, depending on the operator's answer to the startup question on the presence of an external loopback connector.

Tests 7 and 8 will not be executed in internal mode.

Test description:

Test 1: checks accessibility of KMV CSR addresses

Test 2: PROM revision level check

Test 3: real-time clock interrupt test

Test 4: baud rate generator test

Test 5: transmit-receive various length frames in internal loop mode – no interrupts – low-speed

Test 6: transmit-receive various length frames in internal loop mode – interrupts enabled – low- to high-speed

Test 7: transmit-receive various length frames in external loop mode – interrupts enabled – high-speed

Test 8: modem leads external loopback test

5.4.3 VKMC Functional Diagnostic

This diagnostic loads firmware into the KMV11 and exercises the KMV11 as an HDLC communication controller. It provides X.25 Layer 1 (physical layer) protocol functions, and modem control. A detailed discussion appears in the appendix.

The purpose of this diagnostic is to provide troubleshooting facilities for both DIGITAL Field Service engineers and users' support staff. It is fully supported and will be updated as necessary by DIGITAL's software distribution organization.

When used on the KMV11-A this diagnostic program may be used with all types of loopback; that is module, cable, and local and remote modem (if the modems have these facilities).

NOTE

The host memory must be more than 16K words for this diagnostic

Test description:

Test 1: verifies KMV11 initialization

Test 2: runs self-test

Test 3: application firmware load, unload, and start

Test 4: CSR handshaking without interrupts

Test 5: CSR handshaking with interrupts

Test 6: QIO processing in case of resource error

Test 7: QIO processing for various command sequences

Test 8: transmit/receive buffer processing at 2.4 kbytes/s with modem control

Test 9: transmit/receive buffer processing at 2.4 kbytes/s with modem control

Test 10: transmit/receive buffer processing at 64 kbytes/s with modem control

Test 11: transmit/receive buffer processing at 64 kbytes/s without modem control

Test 12: transmit/receive buffer processing at 48 kbytes/s with modem control and address search enabled

5.4.4 XKMD DECX-11 Exerciser Module

This module is provided to allow the KMV11 to be included in the host system's DECX-11 system exerciser. Error-free operation shows that the KMV11 does not react with other system bus activity in a worst-case environment.

The module exercises the KMV11 using test routine number 14 (combined DMA data in and data out test) checking transmitted data against received data and monitoring the KMV11 status.

NOTE

No data is transmitted or received via the serial line. Only pathways and logic between the host and KMV11 are exercised.

5.5 PREVENTIVE MAINTENANCE

There is no specific KMV11 PM schedule. A general check of voltages and connections should be done when system PM is performed. After moving KMV11 modules or cables, a complete checkout of the devices, by running all diagnostics, is needed.

Special care must be exercised because some chips are installed in sockets and may be moved during removal or replacement of the KMV11 or adjacent modules.

5.6 CORRECTIVE MAINTENANCE

The FRU is either the KMV11 module or a cable. All corrective diagnostics should be applied to isolating the failing FRU. KMV11 diagnostics are designed to help in the isolation process and should be run in the following sequence:

1. VKMA logic diagnostic
2. VKMB line controller diagnostic
3. VKMC functional diagnostic
4. XKMD DECX-11 module included within the appropriate DECX-11 system exerciser.

Before considering a KMV11 module to be defective, check switch settings and the wire link configuration by referring to Chapter 2.