MicroVAX 3100 Model 85, 90, 95, 96
KA50/51/55/56 CPU
System Maintenance

Order Number: EK-M3100-SM. B01

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This manual gives maintenance information for systems that use the KA50, KA51, KA55 or KA56 CPU module.
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Contents

Preface ........................................................................................................... xi

1 KA50/51/55/56 CPU Module Description
   1.1 KA50/51/55/56 CPU Module .................................................................. 1–1
   1.1.1 Physical Description ......................................................................... 1–2
   1.1.2 Functional Description .................................................................... 1–3
   1.2 MS44 and MS44L Memory Modules ....................................................... 1–9
   1.3 MS44 or MS44L Memory Option Installation .......................................... 1–11
   1.4 Memory Tests ..................................................................................... 1–13

2 Configuration
   2.1 Memory Configurations ..................................................................... 2–1
   2.2 Mass Storage Devices ....................................................................... 2–1
   2.2.1 Internal Mass Storage Devices ......................................................... 2–2
   2.2.2 External Mass Storage Devices ......................................................... 2–2
   2.2.3 SCSI ID Numbers ........................................................................ 2–4
   2.3 Communications Options .................................................................... 2–4
   2.3.1 Asynchronous Communications Options ....................................... 2–4
   2.3.2 Synchronous Communications Options ......................................... 2–5

3 KA50/51/55/56 Firmware Commands
   3.1 Console I/O Mode Control Characters ............................................... 3–2
   3.1.1 Command Syntax .......................................................................... 3–3
   3.1.2 Address Specifiers .................................................................... 3–3
   3.1.3 Symbolic Addresses .................................................................. 3–4
   3.1.4 Console Numeric Expression Radix Specifiers .............................. 3–8
   3.1.5 Console Command Qualifiers ......................................................... 3–9
   3.1.6 Console Command Keywords ....................................................... 3–10
   3.2 Console Commands .......................................................................... 3–13
   3.2.1 BOOT ....................................................................................... 3–13
3.2.2 CONTINUE ........................................ 3-15
3.2.3 DEPOSIT .......................................... 3-15
3.2.4 EXAMINE .......................................... 3-16
3.2.5 FIND ........................................... 3-17
3.2.6 HALT ........................................... 3-18
3.2.7 HELP ........................................... 3-18
3.2.8 INITIALIZE ..................................... 3-20
3.2.9 LOGIN ........................................... 3-21
3.2.10 MOVE .......................................... 3-22
3.2.11 NEXT ........................................... 3-23
3.2.12 REPEAT ......................................... 3-24
3.2.13 SEARCH ......................................... 3-25
3.2.14 SET ............................................ 3-27
3.2.15 SHOW ........................................... 3-28
3.2.16 START .......................................... 3-31
3.2.17 TEST ........................................... 3-31
3.2.18 UNJAM ........................................... 3-35
3.2.19 X—Binary Load and Unload .................. 3-35
3.2.20! (Comment) .................................... 3-38

4 System Initialization and Acceptance Testing (Normal Operation)

4.1 Basic Initialization Flow ........................................ 4-1
4.2 Power-On Self-Tests (POST) .................................... 4-2
4.2.1 Power-Up Tests for Kernel .............................. 4-3
4.2.2 Power-Up Tests for Mass Storage Devices ............ 4-5
4.3 CPU ROM-Based Diagnostics ................................. 4-6
4.3.1 Diagnostic Tests ................................... 4-6
4.3.2 Scripts ........................................... 4-11
4.4 Basic Acceptance Test Procedure ......................... 4-13
4.5 Machine State on Power-Up ................................. 4-14
4.6 Main Memory Layout and State ......................... 4-14
4.6.1 Reserved Main Memory ................................ 4-15
4.6.1.1 PFN Bitmap .................................. 4-15
4.6.1.2 Scatter/Gather Map ............................ 4-16
4.6.1.3 Firmware "Scratch Memory" ...................... 4-16
4.6.2 Contents of Main Memory ............................... 4-16
4.6.3 Memory Controller Registers ......................... 4-17
4.6.4 On-Chip and Backup Caches ......................... 4-17
4.6.5 Translation Buffer ................................ 4-17
4.6.6 Halt-Protected Space ................................ 4-17
4.7 Operating System Bootstrap ............................... 4-17
5 System Troubleshooting and Diagnostics

5.1 Basic Troubleshooting Flow ........................................ 5-1
5.2 Product Fault Management and Symptom-Directed Diagnosis ... 5-3
  5.2.1 General Exception and Interrupt Handling ................. 5-3
  5.2.2 OpenVMS Error Handling ..................................... 5-4
  5.2.3 OpenVMS Error Logging and Event Log Entry Format ...... 5-6
  5.2.4 OpenVMS Event Record Translation ......................... 5-14
  5.2.5 Interpreting CPU Faults Using ANALYZE/ERROR .......... 5-15
  5.2.6 Interpreting Memory Faults Using ANALYZE/ERROR ...... 5-18
    5.2.6.1 Uncorrectable ECC Errors ............................ 5-18
    5.2.6.2 Correctable ECC Errors .............................. 5-22
  5.2.7 Interpreting System Bus Faults Using ANALYZE/ERROR ... 5-26
  5.2.8 Interpreting DMA <> Host Transaction Faults Using ... 5-28
    ANALYZE/ERROR ........................................ 5-28
  5.2.9 VAXsimPLUS and System-Initiated Call Logging (SICL) .. 5-32
    5.2.9.1 Converting the SICL Service Request MEL File ....... 5-37
    5.2.9.2 VAXsimPLUS Installation Tips ....................... 5-38
    5.2.9.3 VAXsimPLUS Post-installation Tips .................. 5-39
  5.2.10 Repair Data for Returning FRUs .......................... 5-41
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures ........................................ 5-41
  5.3.1 FE Utility .................................................. 5-47
  5.3.2 Overriding Halt Protection .................................. 5-48
  5.3.3 Isolating Memory Failures .................................. 5-48
5.4 Using MOP Ethernet Functions to Isolate Failures .......... 5-53
5.5 Interpreting User Environmental Test Package (UETP) OpenVMS Failures ........................................ 5-56
  5.5.1 Interpreting UETP Output .................................. 5-56
    5.5.1.1 UETP Log Files ...................................... 5-56
    5.5.1.2 Possible UETP Errors ............................... 5-57
5.6 Using Loopback Tests to Isolate Failures .................... 5-58
6 FEPROM Firmware Update

6.1 Preparing the Processor for a FEPROM Update ........................................... 6-2
6.2 Updating Firmware via Ethernet ................................................................. 6-3
6.3 Updating Firmware via Tape ........................................................................ 6-6
6.4 FEPROM Update Error Messages ................................................................. 6-7

A Address Assignments

A.1 KA50/51/55/56 General Local Address Space Map ........................................ A-1
A.2 KA50/51/55/56 Detailed Local Address Space Map ....................................... A-3
A.3 External, Internal Processor Registers ......................................................... A-8
A.4 Global Q22-bus Address Space Map ............................................................. A-9
A.5 Processor Registers .................................................................................... A-9
A.6 IPR Address Space Decoding ....................................................................... A-21

B ROM Partitioning

B.1 Firmware EPROM Layout ............................................................................ B-1
B.1.1 System Identification Registers .................................................................. B-3
B.1.1.1 PR$_SID$ (IPR 62) ................................................................................. B-3
B.1.1.2 SIE (20046004) .................................................................................. B-3
B.1.2 Call-Back Entry Points ............................................................................. B-4
B.1.2.1 CP$GETCHAR_R4 ............................................................................. B-5
B.1.2.2 CP$MSG_OUT_NOLF_R4 ................................................................. B-6
B.1.2.3 CP$READ_WTH_PRMPT_R4 ......................................................... B-6
B.1.3 Boot Information Pointers ......................................................................... B-7

C Data Structures and Memory Layout

C.1 Halt Dispatch State Machine ................................................................. C-1
C.2 Restart Parameter Block .......................................................................... C-5
C.3 VMB Argument List ................................................................................. C-9
D Configurable Machine State

E NVRAM Partitioning

E.1 SSC RAM Layout .................................................. E-1
E.1.1 Public Data Structures ....................................... E-2
E.1.1.1 Console Program MailBoX (CPMBX) .................... E-2
E.1.1.2 Terminal Status ............................................ E-3
E.1.1.3 Keyboard Status ......................................... E-3
E.1.2 Service Vectors .............................................. E-4
E.1.3 Firmware Stack ............................................. E-4
E.1.4 Diagnostic State ............................................. E-4
E.1.5 USER Area .................................................... E-4

F MOP Counters

G Error Messages

G.1 Machine Check Register Dump ................................. G-1
G.2 Halt Code Messages .......................................... G-1
G.3 VMB Error Messages .......................................... G-3
G.4 Console Error Messages ...................................... G-4

H Related Documents

Glossary

Index

Examples

1–1 Successful Running of Memory Test Script A8 ........... 1–13
1–2 Typical Failure After Running Memory Test Script A8 .... 1–14
4–1 Successful Diagnostic Countdown .......................... 4–2
4–2 Successful Power-Up to List of Bootable Devices ........ 4–5
4–3 Test 9E ......................................................... 4–8
5–1 Error Log Entry Indicating CPU Error ..................... 5–16
5–2 SHOW ERROR Display Using the OpenVMS Operating System .................................................. 5–17
5-3 Error Log Entry Indicating Uncorrectable ECC Error .......... 5-20
5-4 SHOW MEMORY Display Under the OpenVMS Operating System ................................................. 5-21
5-5 Using ANALYZE/SYSTEM to Check the Physical Address in Memory for a Replaced Page .................. 5-22
5-6 Error Log Entry Indicating Correctable ECC Error ........ 5-25
5-7 Error Log Entry Indicating Q-Bus Error ......................... 5-27
5-8 Error Log Entry Indicating Polled Error ....................... 5-29
5-9 Device Attention Entry ....................................... 5-31
5-10 SICL Service Request with Appended MEL File ........ 5-38
5-11 Sample Output with Errors .................................. 5-41
5-12 FE Utility Example ........................................... 5-48
5-13 Failure Due to a Missing SIMM (One 16 Mbyte Set) .... 5-49
5-14 Failure Due to a Missing SIMM (Two 16 Mbyte Sets) .... 5-50
5-15 Failure Due to a Bad SIMM .................................. 5-51
5-16 SIMM Wrong Size ............................................ 5-52
6-1 FEPROM Update via Ethernet .................................. 6-5
6-2 FEPROM Update via Tape ...................................... 6-7

Figures

1-1 KA50/51/55/56 CPU Module .................................. 1-2
1-2 KA50/51/55/56 CPU Module Block Diagram ................. 1-4
1-3 KA50/51/55/56 Controls, Indicators, Ports, and Connectors ....................................................... 1-6
1-4 Memory Expansion Connectors ................................ 1-10
1-5 Memory Module Installation .................................. 1-12
2-1 SZ Expansion Box Numbering System ....................... 2-3
4-1 Console Banner ................................................ 4-3
4-2 Memory Layout After Power-Up Diagnostics ................ 4-15
4-3 Memory Layout Prior to VMB Entry ......................... 4-20
4-4 Memory Layout at VMB Exit .................................. 4-22
4-5 Boot Block Format ............................................ 4-24
4-6 Locating the Restart Parameter Block ....................... 4-32
5-1 Event Log Entry Format ...................................... 5-8
5-2 Machine Check Stack Frame Subpacket .................... 5-9
5-3 Processor Register Subpacket ................................ 5-10
5–4 Memory Subpacket for ECC Memory Errors
5–5 Memory SBE Reduction Subpacket (Correctable Memory Errors)
5–6 CRD Entry Subpacket Header
5–7 Correctable Read Data (CRD) Entry
5–8 Trigger Flow for the VAXsimPLUS Monitor
5–9 Five-Level VAXsimPLUS Monitor Display
6–1 Firmware Update Utility Layout
6–2 W4 Jumper Setting for Updating Firmware
B–1 KA50/51/55/56 FEPROM Layout
B–2 SID : System Identification Register
B–3 SIE : System Identification Extension (20040004)
B–4 Boot Information Pointers
E–1 KA50/51/55/56 SSC NVRAM Layout
E–2 NVR0 (20140400) : Console Program MailBox (CPMBX)
E–3 NVR1 (20140401)
E–4 NVR2 (20140402)

Tables
1–1 Functions of Controls, Indicators, Connectors
1–2 KA50/51/55/56 CPU Module Memory Configurations
2–1 KA50/51/55/56 Internal Mass Storage Devices
2–2 Supported Asynchronous Communications Options
2–3 Supported Synchronous Communications Options
2–4 DSW42-AA Communications Support
3–1 Console Symbolic Addresses
3–2 Symbolic Addresses Used in Any Address Space
3–3 Console Radix Specifiers
3–4 Console Command Qualifiers
3–5 Command Keywords by Type
3–6 Console Command Summary
4–1 LED Codes
4–2 Scripts Available to Customer Services
4–3 Network Maintenance Operations Summary
4–4 Supported MOP Messages
4–5 MOP Multicast Addresses and Protocol Specifiers
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-1</td>
<td>OpenVMS Error Handler Entry Types</td>
<td>5-7</td>
</tr>
<tr>
<td>5-2</td>
<td>Conditions That Trigger VAXsimPLUS Notification and Updating</td>
<td>5-33</td>
</tr>
<tr>
<td>5-3</td>
<td>Five-Level VAXsimPLUS Monitor Screen Displays</td>
<td>5-35</td>
</tr>
<tr>
<td>5-4</td>
<td>KA50/51/55/56 Console Displays as Pointers to FRUs</td>
<td>5-44</td>
</tr>
<tr>
<td>5-5</td>
<td>Loopback Connectors for Common Devices</td>
<td>5-60</td>
</tr>
<tr>
<td>A-1</td>
<td>Processor Registers</td>
<td>A-9</td>
</tr>
<tr>
<td>A-2</td>
<td>IPR Address Space Decoding</td>
<td>A-21</td>
</tr>
<tr>
<td>B-1</td>
<td>System Identification Register</td>
<td>B-3</td>
</tr>
<tr>
<td>B-2</td>
<td>System Identification Extension</td>
<td>B-4</td>
</tr>
<tr>
<td>B-3</td>
<td>Call-Back Entry Points</td>
<td>B-5</td>
</tr>
<tr>
<td>C-1</td>
<td>Firmware State Transition Table</td>
<td>C-3</td>
</tr>
<tr>
<td>C-2</td>
<td>Restart Parameter Block Fields</td>
<td>C-6</td>
</tr>
<tr>
<td>C-3</td>
<td>VMB Argument List</td>
<td>C-9</td>
</tr>
<tr>
<td>E-1</td>
<td>Bit Functions for NVR0</td>
<td>E-2</td>
</tr>
<tr>
<td>E-2</td>
<td>Bit Functions for NVR1</td>
<td>E-3</td>
</tr>
<tr>
<td>E-3</td>
<td>Bit Functions for NVR2</td>
<td>E-4</td>
</tr>
<tr>
<td>F-1</td>
<td>MOP Counter Block</td>
<td>F-1</td>
</tr>
<tr>
<td>G-1</td>
<td>HALT Messages</td>
<td>G-2</td>
</tr>
<tr>
<td>G-2</td>
<td>VMB Error Messages</td>
<td>G-3</td>
</tr>
<tr>
<td>G-3</td>
<td>Console Error Messages</td>
<td>G-4</td>
</tr>
</tbody>
</table>
Preface

This manual describes the KA50 CPU module used in the MicroVAX 3100 Model 90, the KA51 CPU module used in the MicroVAX 3100 Model 95, the KA55 CPU module used in the MicroVAX 3100 Model 85, and the KA56 CPU module used in the MicroVAX 3100 Model 96 system. It provides the configuration guidelines, ROM-based diagnostic information, and troubleshooting information for systems containing the KA50/51/55/56 CPU modules.

Audience

This manual is for Digital Services personnel who provide support and maintenance for systems that use the KA50/51/55/56 CPU module. It is also for customers who have a self-maintenance agreement with Digital Equipment Corporation.

Structure of This Manual

This manual is divided into six chapters, eight appendixes, a glossary, and an index:

- Chapter 1 describes the KA50/51/55/56 CPU module.
- Chapter 2 describes the KA50/51/55/56 system configurations.
- Chapter 3 describes the console commands that you can enter at the console prompt.
- Chapter 4 describes the system initialization, testing and bootstrap process that occurs at power-up.
- Chapter 5 describes the error log interpretation of diagnostic testing, the ROM-based diagnostic testing, and troubleshooting procedures for the KA50/51/55/56 systems. Also, this chapter provides information on testing DSSI storage devices, using MOP Ethernet functions to isolate errors, and interpreting UETP failures.
- Chapter 6 describes the FEPROM firmware.
• Appendix A gives the address assignments.

• Appendix B describes ROM partitioning and subroutine entry points.

• Appendix C gives definitions of the key global data structures used by the CPU firmware.

• Appendix D gives the normal state of all configurable bits in the CPU module as they are left after the successful completion of power-up ROM diagnostics.

• Appendix E describes how the CPU firmware partitions the SCC 1 KB battery-backed-up (BBU) RAM.

• Appendix F gives MOP counters.

• Appendix G describes the error codes and messages that the system exerciser test generates.

• Appendix H gives a list of related documents.

Note

Examples in this manual may vary slightly from your particular MicroVAX 3100 system, since they are from various VAX and MicroVAX systems which share common features, options, diagnostics, and so on.
## Conventions

The following conventions are used in this manual:

<table>
<thead>
<tr>
<th>Convention</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ctrl/x</td>
<td>Ctrl/x indicates that you hold down the Ctrl key while you press another key or mouse button (indicated here by x).</td>
</tr>
<tr>
<td>x</td>
<td>A lowercase italic x indicates the generic use of a letter. For example, xxx indicates any combination of three alphabetic characters.</td>
</tr>
<tr>
<td>n</td>
<td>A lowercase italic n indicates the generic use of a number. For example, 19nn indicates a 4-digit number in which the last 2 digits are unknown.</td>
</tr>
<tr>
<td>[]</td>
<td>In format descriptions, braces indicate required elements. You must choose one of the elements.</td>
</tr>
<tr>
<td>[]</td>
<td>In format descriptions, brackets indicate optional elements. You can choose none, one, or all of the options.</td>
</tr>
<tr>
<td>( )</td>
<td>In format descriptions, parentheses delimit the parameter or argument list.</td>
</tr>
<tr>
<td>...</td>
<td>In format descriptions, horizontal ellipsis points indicate one of the following:</td>
</tr>
<tr>
<td></td>
<td>• An item that is repeated</td>
</tr>
<tr>
<td></td>
<td>• An omission such as additional optional arguments</td>
</tr>
<tr>
<td></td>
<td>• Additional parameters, values, or other information that you can enter</td>
</tr>
<tr>
<td></td>
<td>In format descriptions, a vertical bar separates similar options, one of which you can choose.</td>
</tr>
<tr>
<td>italic type</td>
<td>Italic type emphasizes important information, indicates variables, and indicates the complete titles of manuals.</td>
</tr>
<tr>
<td>boldface type</td>
<td>Boldface type in examples indicates user input. Boldface type in text indicates the first instance of terms defined either in the text, in the glossary, or both.</td>
</tr>
<tr>
<td>n nnn.nnn nnn</td>
<td>A space character separates groups of 3 digits in numerals with 5 or more digits. For example, 10 000 equals ten thousand.</td>
</tr>
<tr>
<td>n.nn</td>
<td>A period in numerals signals the decimal point indicator. For example, 1.75 equals one and three-fourths.</td>
</tr>
<tr>
<td>MONOSPACE</td>
<td>Text displayed on the screen is shown in monospace type.</td>
</tr>
<tr>
<td>Convention</td>
<td>Description</td>
</tr>
<tr>
<td>---------------</td>
<td>--------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Radix indicators</td>
<td>The radix of a number is written as a word enclosed in parentheses, for example, 23(decimal) or 34(hexadecimal).</td>
</tr>
<tr>
<td>&gt;&gt;&gt;</td>
<td>Three right angle brackets indicate the console prompt.</td>
</tr>
<tr>
<td>UPPERCASE</td>
<td>A word in uppercase indicates a command.</td>
</tr>
<tr>
<td>Note</td>
<td>A note contains information that is of special importance to the user.</td>
</tr>
<tr>
<td>Caution</td>
<td>A caution contains information to prevent damage to the equipment.</td>
</tr>
<tr>
<td>Warning</td>
<td>A warning contains information to prevent personal injury.</td>
</tr>
</tbody>
</table>
KA50/51/55/56 CPU Module Description

This chapter describes the KA50 central processing unit (CPU) module that is used in the MicroVAX 3100 Model 90, the KA51 CPU module that is used in the MicroVAX 3100 Model 95, the KA55 CPU module that is used in the MicroVAX 3100 Model 95 system, and the KA56 CPU module that is used in the MicroVAX 3100 Model 96. It gives information on the following:

- KA50/51/55/56 CPU modules
- MS44 or MS44L memory modules

The KA50, KA51, KA55 and KA56 are similar in design, and the information in this document is applicable for each of them except where noted. The differences between the KA50, KA51, KA55, and KA56 CPUs are as follows:

<table>
<thead>
<tr>
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<th>KA50</th>
<th>KA51</th>
<th>KA55</th>
<th>KA56</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>286Mhz (14ns)</td>
<td>333Mhz (12ns)</td>
<td>250Mhz (16ns)</td>
<td>400Mhz (10ns)</td>
</tr>
<tr>
<td>VIC</td>
<td>2Kb</td>
<td>2Kb</td>
<td>disabled</td>
<td>2Kb</td>
</tr>
<tr>
<td>P-cache</td>
<td>8Kb</td>
<td>8Kb</td>
<td>8Kb</td>
<td>8Kb</td>
</tr>
<tr>
<td>B-cache</td>
<td>128Kb</td>
<td>512Kb</td>
<td>128Kb</td>
<td>512Kb</td>
</tr>
</tbody>
</table>

1.1 KA50/51/55/56 CPU Module

The KA50/51/55/56 CPU module is based on the NVAX chip set. It uses MS44 or MS44L memory modules and a set of supported small computer system interface (SCSI) devices. Figure 1–1 shows the KA50 CPU module; the KA51, KA55 and KA56 modules are similar.
KA50/51/55/56 CPU Module Description
1.1 KA50/51/55/56 CPU Module

1.1.1 Physical Description

The KA50/51/55/56 CPU module is the primary component of the MicroVAX 3100 system in which it is installed. The KA50/51/55/56 CPU module contains the following components:

- The NVAX processor chip—This chip is a complementary metal oxide semiconductor (CMOS) virtual memory microprocessor. The key features of the chip are as follows:
  - Support for the MicroVAX chip subset of the VAX instruction set
  - Support for the MicroVAX chip subset of the VAX data types
  - Full VAX memory management
  - 30-bit physical memory addressing

Figure 1–1 KA50/51/55/56 CPU Module

- DC244 NVAX memory controller (NMC) memory controller chip
- DC243 NVAX CP bus adapter (NMA) and input/output (I/O) control chip
- SCSI controller and SQWF buffer chip
- Time-of-year (TOY) clock SSC chip
KA50/51/55/56 CPU Module Description
1.1 KA50/51/55/56 CPU Module

- DC541 SGEC chip Ethernet controller for standard or ThinWire Ethernet
- DC7085 (QUART) serial line controller (4 serial lines, one with modem control)
- 128K bytes (KA50/55) or 512K bytes (KA51/56) of second level write-back cache memory
- Basic system memory (16M bytes of random-access memory (RAM) consisting of four MS44L-AA memory modules or 64M bytes of RAM consisting of four MS44-CA )
- Support for up to 128M bytes of RAM
- 512K bytes of read-only memory (ROM)—This ROM contains the boot and diagnostic firmware for the system.
- 32-byte network address ROM
- Four asynchronous communications ports as follows:
  - Three DEC423 ports—These ports are modified modular jack (MMJ) connectors.
  - One modem control port—This port is a D-sub 25-way connector.
- Provision for asynchronous communications options that provide one of the following:
  - Eight or 16 additional DEC423 ports
  - Eight additional modem ports
- Provision for synchronous communications options that provide:
  - Two synchronous ports

1.1.2 Functional Description

Figure 1–2 is block diagram of the CPU module. This example shows a KA51 and KA56. The diagrams for the KA50 and KA55 are the same except that there are only 128Kb of B-cache on those modules instead of the 512Kb shown.
The KA50/51/55/56 CPU module supports the following MicroVAX data types:

- Byte, word, longword, and quadword
- Character string
- Variable-length bit field
- Absolute queues
- Self-relative queues
- f_floating-point, d_floating-point, and g_floating-point
The operating system uses software emulation to support other MicroVAX data types. The KA50/51/55/56 CPU module supports the following MicroVAX instructions:

- Integer, arithmetic and logical
- Address
- Variable-length bit field
- Control
- Procedure call
- Miscellaneous
- Queue
- Character string instructions
- MOVC3/MOVC5
- CMPC3/CMPC5
- LOCC
- SCANC
- SKPC
- SPANC
- Operating system support
- f-floating-point, d-floating-point, and g-floating-point

The NVAX processor chip provides special microcode assistance to aid the macrocode emulation of the following instruction groups:

- Character string (other than those mentioned previously)
- Decimal string
- CRC
- EDITPC

The operating system uses software emulation to support other VAX instructions. Figure 1–3 shows the controls, indicators, ports, and connectors on the KA50/51/55/56 CPU module. Table 1–1 describes the functions of the controls, indicators, ports, and connectors.
Table 1–1 Functions of Controls, Indicators, Connectors

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal SCSI connector</td>
<td>A connector that provides a connection for SCSI devices mounted inside the system enclosure.</td>
</tr>
</tbody>
</table>

(continued on next page)
Table 1–1 (Cont.)  Functions of Controls, Indicators, Connectors

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic system memory</td>
<td>Four connectors for the basic system memory modules.</td>
</tr>
<tr>
<td>connectors</td>
<td></td>
</tr>
<tr>
<td>Memory expansion</td>
<td>Four connectors for an additional memory option.</td>
</tr>
<tr>
<td>connectors</td>
<td></td>
</tr>
<tr>
<td>External SCSI connector</td>
<td>A connector that provides a connection to SCSI devices that are external to the system enclosure. (Only functional when the internal SCSI connector has a cable installed.)</td>
</tr>
<tr>
<td>Power connector</td>
<td>A connector for dc power.</td>
</tr>
<tr>
<td>ThinWire Ethernet port</td>
<td>A port that provides a connection to a ThinWire Ethernet network.</td>
</tr>
<tr>
<td>Ethernet switch</td>
<td>A two-position switch that determines the type of Ethernet that the system uses as follows:</td>
</tr>
<tr>
<td></td>
<td>• Left position—selects the standard Ethernet type</td>
</tr>
<tr>
<td></td>
<td>• Right position—selects the ThinWire Ethernet type</td>
</tr>
<tr>
<td>Standard Ethernet port</td>
<td>A port that provides a connection to a standard Ethernet network.</td>
</tr>
<tr>
<td>LED display</td>
<td>A set of six LEDs that provide power-up and self-test diagnostic code information.</td>
</tr>
<tr>
<td>Break/Enable LED</td>
<td>A LED indicator that shows the function of MMJ port 3 as follows:</td>
</tr>
<tr>
<td></td>
<td>• On—Break enable</td>
</tr>
<tr>
<td></td>
<td>• Off—Break disable on port 3</td>
</tr>
<tr>
<td>Break/Enable switch¹</td>
<td>A two-position switch that determines the function of MMJ port 3 as follows:</td>
</tr>
<tr>
<td></td>
<td>• Up position—MMJ port 3 functions as a console port; in this state, you can press the Break key on the keyboard of a terminal connected to MMJ port 3 to put the system in console mode.</td>
</tr>
<tr>
<td></td>
<td>• Down position—MMJ port 3 functions as a console port only, and the Break key is disabled.</td>
</tr>
</tbody>
</table>

¹The system recognizes the position of this switch only when the system is turned on.

(continued on next page)
### Table 1–1 (Cont.) Functions of Controls, Indicators, Connectors

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Halt button</td>
<td>A momentary-contact push button that puts the system in console mode.</td>
</tr>
<tr>
<td>Asynchronous modem control port 2</td>
<td>EIA-232 compatible asynchronous port with modem control.</td>
</tr>
<tr>
<td>MMJ port 3</td>
<td>DEC423 compatible asynchronous port. This port functions as the primary console port.</td>
</tr>
<tr>
<td>MMJ port 1</td>
<td>DEC423 compatible asynchronous port.</td>
</tr>
<tr>
<td>MMJ port 0</td>
<td>DEC423 compatible asynchronous port.</td>
</tr>
<tr>
<td>DSW42 I/O connector</td>
<td>A connector that provides a connection for the DSW42 input/output cable.</td>
</tr>
<tr>
<td>DHW42 I/O connector</td>
<td>A connector that provides a connection for the DHW42 input/output cable.</td>
</tr>
<tr>
<td>DSW42 logic board connectors</td>
<td>Two connectors that provide connections for a DSW42 logic board.</td>
</tr>
<tr>
<td>DHW42 logic board connectors</td>
<td>Two connectors that provide connections for a DHW42 logic board.</td>
</tr>
<tr>
<td>KZDDA SCSI connector option</td>
<td>Connector which provides a physical interface between the CPU module and external SCSI devices on an optional second SCSI bus (SCSI-B).</td>
</tr>
</tbody>
</table>
1.2 MS44 and MS44L Memory Modules

The MS44 and the MS44L memory modules provide memory expansion for the KA50/51/55/56 CPU module. The KA50/51/55/56 CPU module supports one variant of the MS44 memory option and one variant of the MS44L option as follows:

- The MS44L-BC (16M bytes), which contains four MS44L-AA (4M bytes) memory modules
- The MS44-DC (64M bytes), which contains four MS44-CA (16M bytes) memory modules

Note
Use only MS44 or MS44L memory modules qualified by Digital.

The rules for adding MS44 or MS44L memory options are as follows:

- You must install all four of the memory modules contained in a memory option. This means that you can expand memory in 16M byte or 64M byte increments only.

- You can install memory options only in a set of connectors that have the same numeral in the connector label. The sets are identified by the following labels:
  - 0A, 0B, 0C, 0D
  - 1E, 1F, 1G, 1H

Figure 1–4 shows the location of the basic memory (16M bytes or 64M bytes) and the memory expansion connectors. Table 1–2 lists the memory configurations.
Figure 1-4 Memory Expansion Connectors

Table 1-2 KA50/51/55/56 CPU Module Memory Configurations

<table>
<thead>
<tr>
<th>Total Memory (bytes)</th>
<th>Increment 1(^1) ((0A + 0B + 0C + 0D)^2)</th>
<th>Increment 2 ((1E + 1F + 1G + 1H)^2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16M</td>
<td>MS44L-BC</td>
<td>MS44L-BC</td>
</tr>
<tr>
<td>32M</td>
<td>MS44L-BC</td>
<td>MS44L-BC</td>
</tr>
<tr>
<td>64M</td>
<td>MS44-DC</td>
<td>MS44L-BC</td>
</tr>
<tr>
<td>80M</td>
<td>MS44-DC</td>
<td>MS44L-BC</td>
</tr>
<tr>
<td>128M</td>
<td>MS44-DC</td>
<td>MS44-DC</td>
</tr>
</tbody>
</table>

\(^1\)Basic system memory.

\(^2\)0A, 0B, 0C, 0D, 1E, 1F, 1G, and 1H are connector identifiers (see Figure 1-4).
1.3 MS44 or MS44L Memory Option Installation

The MS44 and MS44L memory options consist of four memory modules each. Install an MS44 or MS44L memory option on the KA50/51/55/56 CPU module as follows:

1. Position the KA50/51/55/56 CPU module, component side up, so that the edge connectors are facing away from you.

2. Identify the connectors on the KA50/51/55/56 CPU module into which you must install the memory option (see Figure 1–4 and Table 1–2).

3. Insert the first memory module, with the side containing the bar code facing away from you, into the connector on the KA50/51/55/56 CPU module (see Figure 1–5).

__________________________ Caution ________________________________

The connectors are keyed to ensure that you install the memory modules with the correct orientation. Do not force the modules into the connectors with an incorrect orientation.

__________________________ Caution ________________________________

Make sure that you fully install the memory module into the connector before you tilt the module toward the front of the enclosure.
4. Tilt the memory module toward the front of the enclosure until the metal locking clips on the connector lock the memory module in position.

5. Repeat the procedure in step 1 for the subsequent memory modules. Insert them into the other connectors in the set on the KA50/51/55/56 CPU module.

6. Run the MEM diagnostic test, refer to Section 1.4 after you reinstall the KA50/51/55/56 CPU module into the system enclosure to check that the memory is working correctly.

---

**Caution**

When removing memory modules, you must release the metal clips on the connectors of the CPU module.
1.4 Memory Tests

The memory tests check the system memory contained on the MS44 and/or MS44L memories. The tests run automatically as part of the power-up tests and initialization, when you turn on the system. The memory tests are a group of individual tests which can be called individually or normally as a group under a specific script number.

The recommended method to verify a new memory installation is to run the memory test script A8 which will call all of the memory tests and run them on all memory present.

Examples of successful and unsuccessful runs of memory test script A8 are shown in Example 1–1 and Example 1–2.

The individual memory tests are listed following the examples.

Example 1–1 Successful Running of Memory Test Script A8

```plaintext
>>>T A8
KA50/51/55/56 CPU Module Description

1.4 Memory Tests

Example 1–2 Typical Failure After Running Memory Test Script A8

>>>T A8
9D...31...30...4F...4E...4D...4C...4B...4A...48...48...48...48...48...48...48...48...48...48...
48...48...48...47...40...

? Test Subtest_40_06 Loop_Subtest=00 Err_Type=FF DE_Memory_count_pages.lis
Vec=0000 Prev_Errs=0004 P1=00000001 P2=00000002 P3=00000001
P4=00000000 P5=00000020 P6=00000800 P7=00000020 P8=00000000
P9=00000000 P10=00FCD4A8 r0=0FF4008 r1=00000007 r2=00000000
r3=FFFFFFFF r4=00000068 r5=00000000 r6=00000000 r7=00000002
r8=0FF4000 r9=20140758 r10=FFFFFFFF r11=FFFFFFFF
dsr=0000 csrs=00000000 intmsk=00 icar=01 pcsts=FC00 paddr=FFFFFFFF pcctl=FC13
ccttl=00000021 bctsts=0000 bcetsts=0000 cefsts=00000200 nestst=00
mncsr=01111000 mesr=00080000

Test DC - Check for No Memory Present

The only purpose of this test is to check for the specific condition of no valid memory present in the system. This occurs if no memory is present, or if memory is present and one or more SIMMs is missing or not plugged in correctly.

Test 31 - Size and Setup Memory CSRs

Find out how much memory is available and configure into consecutive memory starting at address 00000000. Verify proper configuration data in the CSRs.

Test 30 - Build a Bitmap in Memory

Set up a bitmap in RAM to be used by the memory tests. Test the area before setting up a bitmap.

This test looks for a 1 MB KB section of memory to be used for the bitmap, busmap and reserved console area and structures to run diagnostics. The test starts at the top of available memory and tests one section of memory at the top of each 4 MB section of memory until a good section is found for the maps or the bottom of memory is reached, in which case the test fails.

Test 4F - Data Pattern Tests

Verifies that each bit in the data path can be written to a one and a zero individually. This test also checks for shorts between individual paths. The test needs to be run once for each array of memory chips.

This test uses various fix patterns and also floating 1's and 0's patterns across all 572 data bits (64 data, 8 ECC). The test always checks both even and odd QWs of data so that all four SIMMs in a memory set are tested.

Test 4E - Masked Write Cycles with No Errors, BYTE, WORD

This test verifies masked write cycles to memory.
Test 4D - Address Uniqueness Test
The main purpose of the test is to verify that each set on each board can be uniquely addressed. The test writes a unique pattern to each location to be tested then verifies all locations.

Test 4C - MEMORY ECC, Verify Error Detection and Reporting
The main purpose of this test is to test ECC logic. It is not intended to test the memory RAMs explicitly.

The test verifies that single and double bit errors are reported and logged correctly in the MESR. It also verifies that single bit errors cause interrupts through vector 54 when enabled and that double bit errors cause a machine check.

In addition, the test also verifies that multiple bit errors can be detected using data patterns that generate all of the syndrome values for multiple bit errors.

Test 4B - MEMORY Verify Masked Write Cycles with Errors
The test verifies operation of masked write cycles when the location contains errors. In addition, it verifies that errors are reported and that single bit errors are corrected.

Test 4A - MEMORY ECC, Verify Ability to Correct Single Bit Errors
This test verifies the correct operation of the error correction logic (ECC). It does this by verifying that single bit errors can be detected and corrected in any of the 64 data bits and that single bit errors are detected in the eight check bits.

Test 48 - MEMORY Address/Shorts Test
This test verifies that all locations in each set can be uniquely written to and that each of the 64 data bits in each QW can be written to a one and to a zero. This test also writes all locations in memory with good ECC.

The test runs on a hexaword basis with all caches enabled to fully utilize caching to speed up the test. Two primary data patterns of AAAAAA_ AAAAAAAA and 55555555_55555555 are used by the test. The ECC checkbits for these patterns are complements of each other. By running this test, all data and ECC bits in all locations in memory will be written as a 1 and a 0. The test also detects addressing errors.

Test 47 - MEMORY Data Retention, Verify Refresh Logic
This test verifies that the refresh logic is working for all memory boards. The test loads patterns into memory, waits a specified amount of time, then verifies the patterns.
Test 40 - MEMORY Count Bad Pages Marked In Bitmap
This test is normally run last in a script of memory tests. Its only purpose is to read the bitmap when done and check to see if any pages in memory were marked bad, if so, report an error.

________________________________________________________________________

Note
________________________________________________________________________

If this test fails, do SHOW MEMORY to see which set has bad pages in it.

________________________________________________________________________
This chapter describes the KA50/51/55/56 system configurations. It gives information on the following:

- Memory configurations
- Mass storage devices
- Communications options

2.1 Memory Configurations

A KA50/51/55/56 system has a basic memory of 16M bytes or 64M bytes. This consists of four MS44L-AA memory modules or four MS44-CA memory modules. You can add memory in 16M byte or 64M byte increments, up to a maximum of 128M bytes. See Section 1.2 for information on the memory configurations.

2.2 Mass Storage Devices

A KA50/51/55/56 system supports mass storage devices in the following categories:

- Internal mass storage devices—These devices are mounted inside the system enclosure.
- External mass storage devices—These devices are self-contained units that you can connect to the system externally.
2.2 Mass Storage Devices

2.2.1 Internal Mass Storage Devices

Table 2–1 shows some of the internal mass storage devices that a KA50/51/55/56 system supports.

<table>
<thead>
<tr>
<th>Option Name</th>
<th>Description</th>
<th>Size</th>
<th>Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>RZ23L</td>
<td>Disk drive</td>
<td>3.5</td>
<td>120-MB</td>
</tr>
<tr>
<td>RZ24</td>
<td>Disk drive</td>
<td>3.5</td>
<td>209-MB</td>
</tr>
<tr>
<td>RZ24L</td>
<td>Disk drive</td>
<td>3.5</td>
<td>245-MB</td>
</tr>
<tr>
<td>RZ25</td>
<td>Disk drive</td>
<td>3.5</td>
<td>400-MB</td>
</tr>
<tr>
<td>RZ25L</td>
<td>Disk drive</td>
<td>3.5</td>
<td>535-MB</td>
</tr>
<tr>
<td>RZ25M</td>
<td>Disk drive</td>
<td>3.5</td>
<td>545-MB</td>
</tr>
<tr>
<td>RZ26</td>
<td>Disk drive</td>
<td>3.5</td>
<td>1.05-GB</td>
</tr>
<tr>
<td>RZ26L</td>
<td>Disk drive</td>
<td>3.5</td>
<td>1.05-GB</td>
</tr>
<tr>
<td>RZ28</td>
<td>Disk drive</td>
<td>3.5</td>
<td>2.10-GB</td>
</tr>
<tr>
<td>TZ30(^2)</td>
<td>Tape drive</td>
<td>5.25</td>
<td>95-MB cartridge</td>
</tr>
<tr>
<td>TZK10/TZK11(^2)</td>
<td>Tape drive</td>
<td>5.25</td>
<td>Range of cartridges</td>
</tr>
<tr>
<td>TLZ06/TLZ07(^2)</td>
<td>Tape drive</td>
<td>5.25</td>
<td>Range of cassettes</td>
</tr>
<tr>
<td>RX23/RX28(^2)</td>
<td>Diskette drive</td>
<td>3.5</td>
<td>Range of diskettes</td>
</tr>
<tr>
<td>RRD42(^2)</td>
<td>CDROM drive</td>
<td>5.25</td>
<td>600-MB CDROM</td>
</tr>
<tr>
<td>RRD43(^2)</td>
<td>CDROM drive</td>
<td>5.25</td>
<td>600-MB CDROM</td>
</tr>
</tbody>
</table>

\(^1\)Size of half-height device.
\(^2\)Removable media device.

The system enclosure determines the combinations of internal mass storage devices in a KA50/51/55/56 system. See the MicroVAX 3100 BA42B Enclosure Maintenance manual for more information.

2.2.2 External Mass Storage Devices

The external mass storage devices connect to KA50/51/55/56 systems through the SCSI connector on the back of the system enclosure. In KA50/51/55/56 systems, the SCSI bus supports a maximum of seven mass storage devices. Therefore, the number of external mass storage devices that you can connect depends on the number of mass storage devices that are mounted inside the system enclosure.
Configuration

2.2 Mass Storage Devices

The maximum number of mass storage devices in the system enclosure is five. This means that you can connect at least two external mass storage devices.

A KA50/51/55/56 system supports the SZ series of mass storage expansion boxes. The SZ number defines the contents of each expansion box. Figure 2–1 shows the numbering system for SZ expansion boxes.

Figure 2–1  SZ Expansion Box Numbering System

```
Enclosure Type
2 = BA42 Enclosure
6 = BA46 Enclosure

Power Cord Type
A = 120 V ac
B = 240 V ac

Left Compartment
A = RZ55
B = RZ56
C = RZ57
P = RZ25
R = RZ58
X = Empty

Right Compartment
A = RZ55
B = RZ56
C = RZ57
D = TLZ04
E = T2K10
F = RRD42
H = T230
L = RX33
M = RX33
P = RZ25
R = RZ58
X = Empty
```

1 The RZ25 disk drive fits in the BA42 enclosure only.
2 The TLZ04 tape drive fits in the BA46 enclosure only.

With the KZDDA SCSI option, a second SCSI connector, a KA50/51/55/56 system can support seven additional external devices on a second (external) SCSI bus.

A KA50/51/55/56 system also supports other types of external mass storage devices. See the latest Systems and Options Catalog (SOC) for a listing of supported external SCSI devices.

When you are adding mass storage devices, use these guidelines. Also, refer to documentation for your SCSI expander, if any.

- You can add a maximum of four external SCSI devices. A fully configured SZ12 enclosure contains two SCSI devices.
- You can add a maximum of two SCSI tape devices. Depending on the configuration, the system may support two TLZ04 tape drives.
Configuration

2.2 Mass Storage Devices

- The BA40 single drive expansion box contains one SCSI device.
- The RRD42 CDROM drive is a single SCSI device. You can add a maximum of three RRD42 CDROM drives.
- Terminate the SCSI bus correctly. Failure to do this can cause a system failure or corrupt data.
- Digital recommends that you connect all SCSI devices to the same ac power source.
- Do not add or remove devices that are connected to the SCSI bus while the power is on.
- Digital does not guarantee the correct operation of a SCSI bus that does not use the cables supplied by Digital or is not configured in accordance with Digital recommendations.

2.2.3 SCSI ID Numbers

Each mass storage device must have a unique SCSI ID number. SCSI ID 6 is typically used for the SCSI controller.

2.3 Communications Options

A KA50/51/55/56 system supports the following types of communications options:

- Asynchronous communications options
- Synchronous communications options

Each communications option has components that are installed in the system enclosure and components that connect to the system externally.

2.3.1 Asynchronous Communications Options

Table 2-2 lists the asynchronous communications options that KA50/51/55/56 systems support.

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DHW42-AA</td>
<td>Eight-line DEC423 asynchronous option</td>
</tr>
<tr>
<td>DHW42-BA</td>
<td>Sixteen-line DEC423 asynchronous module option</td>
</tr>
<tr>
<td>DHW42-CA</td>
<td>Eight-line EIA-232 modem asynchronous module option</td>
</tr>
<tr>
<td>DHW42-UP</td>
<td>Eight-line to 16-line DEC423 asynchronous upgrade option</td>
</tr>
</tbody>
</table>
2.3.2 Synchronous Communications Options

Table 2–3 lists the synchronous communications options that KA50/51/55/56 systems support.

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model 100</td>
<td></td>
</tr>
<tr>
<td>DSW42-AA</td>
<td>Two-line EIA-232/V.24 synchronous option with two external cables,</td>
</tr>
<tr>
<td></td>
<td>BC19D-02 (17-01110-01)</td>
</tr>
</tbody>
</table>

1This option is supplied with two external cables that support the EIA-232/V.24 interface.

The DSW42-AA option also supports the communications interfaces listed in Table 2–4, but you must order the external cables separately.

<table>
<thead>
<tr>
<th>Communications Interface</th>
<th>External Cable</th>
</tr>
</thead>
<tbody>
<tr>
<td>EIA-423/V.10</td>
<td>BC19E-021 (17-01111-01)</td>
</tr>
<tr>
<td>EIA-422/V.11</td>
<td>BC19B-021 (17-01108-01)</td>
</tr>
</tbody>
</table>

1Two required for DSW42-AA.
KA50/51/55/56 Firmware Commands

This chapter describes the console mode control characters, the command syntax, the command modifiers, and all of the console commands. You can enter these commands when the system is in console mode. Console mode is indicated when the console prompt (>>>) is displayed. If the system is running the operating system software, refer to the MicroVAX 3100 Model 85 Customer Technical Information manual, the MicroVAX 3100 Model 90 Customer Technical Information manual, the MicroVAX 3100 Model 95 Customer Technical Information manual, or the MicroVAX 3100 Model 96 Customer Technical Information manual, for information on returning the system to console mode.

If the console security feature is enabled and a security password is set, you must log in to privileged console mode before using most of these commands. Refer to the appropriate MicroVAX 3100 Customer Technical Information manual (above) for information on the console security feature.

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95, and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q–bus and DSSI, will appear on the console and/or printouts from time to time.
3.1 Console I/O Mode Control Characters

In console I/O mode, several characters have special meaning:

**RETURN**<br>Also <CR>. The carriage return ends a command line. No action is taken on a command until after it is terminated by a carriage return. A null line terminated by a carriage return is treated as a valid, null command. No action is taken, and the console prompts for input. Carriage return is echoed as carriage return, line feed (<CR><LF>).

**<DEL>**<br>When you press <DEL>, the console deletes the previously typed character. The resulting display differs, depending on whether the console is a video or a hardcopy terminal.

For hardcopy terminals, the console echoes a backslash (\), followed by the deletion of the character. If you press additional rubouts, the additional deleted characters are echoed. If you type a nonrubout character, the console echoes another backslash, followed by the character typed. The result is to echo the characters deleted, surrounding them with backslashes. For example:

EXAMINE<DEL><DEL><CR>
The console echoes: EXAMINE<E<DEL><CR>
The console sees the command line: EXAMINE<CR>

For video terminals, the previous character is erased and the cursor is restored to its previous position.

The console does not delete characters past the beginning of a command line. If you press more rubouts than there are characters on the line, the extra rubouts are ignored. A rubout entered on a blank line is ignored.

**CTRL/A** and **F14**<br>Toggle insertion/overstrike mode for command line editing. By default, the console powers up to overstrike mode.

**CTRL/B** or up arrow (or down arrow)<br>Recalls previous command(s). Command recall is only operable if sufficient memory is available. This function may then be enabled and disabled using the SET RECALL command.

**CTRL/D**<br>Move cursor left one position.

**CTRL/F**<br>Moves cursor to the end of the line.

**CTRL/R**<br>Move cursor right one position.

**CTRL/H**, backspace, and **F12**<br>Move cursor to the beginning of the line.

**CTRL/U**<br>Echoes ^U<CR> and deletes the entire line. Entered but otherwise ignored if typed on an empty line.

**CTRL/S**<br>Stops output to the console terminal until **CTRL/C** is typed. Not echoed.

**CTRL/Q**<br>Resumes output to the console terminal. Not echoed.
KA50/51/55/56 Firmware Commands

3.1 Console I/O Mode Control Characters

[CTRLR] Echoes <CR><LF>, followed by the current command line. Can be used to improve the readability of a command line that has been heavily edited.

[CTRLC] Echoes ^C<CR> and aborts processing of a command. When entered as part of a command line, deletes the line.

[CTRL/0] Ignores transmissions to the console terminal until the next [CTRL/0] is entered. Echoes ^O when disabling output, not echoed when it re-enables output. Output is re-enabled if the console prints an error message, or if it prompts for a command from the terminal. Output is also enabled by entering console I/O mode, by pressing the [BREAK] key, and by pressing [CTRLC].

3.1.1 Command Syntax

The console accepts commands up to 80 characters long. Longer commands produce error messages. The character count does not include rubouts, rubbed-out characters, or the [RETURN] at the end of the command.

You can abbreviate a command by entering only as many characters as are required to make the command unique. Most commands can be recognized from their first character. See Table 3–5.

The console treats two or more consecutive spaces and tabs as a single space. Leading and trailing spaces and tabs are ignored. You can place command qualifiers after the command keyword or after any symbol or number in the command.

All numbers (addresses, data, counts) are hexadecimal (hex), but symbolic register names contain decimal register numbers. The hex digits are 0 through 9 and A through F. You can use uppercase and lowercase letters in hex numbers (A through F) and commands.

The following symbols are qualifier and argument conventions:

|| An optional qualifier or argument

{} A required qualifier or argument

3.1.2 Address Specifiers

Several commands take one or more addresses as arguments. An address defines the address space and the offset into that space. The console supports five address spaces:

- Physical memory
- Virtual memory
- General purpose registers (GPRs)
- Internal processor registers (IPRs)
- The PSL
KA50/51/55/56 Firmware Commands

3.1 Console I/O Mode Control Characters

The address space that the console references is inherited from the previous console reference, unless you explicitly specify another address space. The initial address space is physical memory.

3.1.3 Symbolic Addresses

The console supports symbolic references to addresses. A symbolic reference defines the address space and the offset into that space. Table 3–1 lists symbolic references supported by the console, grouped according to address space. You do not have to use an address space qualifier when using a symbolic address.

<table>
<thead>
<tr>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
</tr>
</thead>
<tbody>
<tr>
<td>/G—General Purpose Registers</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R0</td>
<td>00</td>
<td>R4</td>
<td>04</td>
<td>R8</td>
<td>08</td>
<td>R12 (AP)</td>
<td>0C</td>
</tr>
<tr>
<td>R1</td>
<td>01</td>
<td>R5</td>
<td>05</td>
<td>R9</td>
<td>09</td>
<td>R13 (FP)</td>
<td>0D</td>
</tr>
<tr>
<td>R2</td>
<td>02</td>
<td>R6</td>
<td>06</td>
<td>R10</td>
<td>0A</td>
<td>R14 (SP)</td>
<td>0E</td>
</tr>
<tr>
<td>R3</td>
<td>03</td>
<td>R7</td>
<td>07</td>
<td>R11</td>
<td>0B</td>
<td>R15 (PC)</td>
<td>0F</td>
</tr>
<tr>
<td>/M—Processor Status Longword</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>/I—Internal Processor Registers</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pr$ _ksp</td>
<td>00</td>
<td>pr$ _pcbb</td>
<td>10</td>
<td>pr$ _rxcs</td>
<td>20</td>
<td>—</td>
<td>30</td>
</tr>
<tr>
<td>pr$ _esp</td>
<td>01</td>
<td>pr$ _scbb</td>
<td>11</td>
<td>pr$ _rxdb</td>
<td>21</td>
<td>—</td>
<td>31</td>
</tr>
<tr>
<td>pr$ _ssp</td>
<td>02</td>
<td>pr$ _ipl</td>
<td>12</td>
<td>pr$ _txcs</td>
<td>22</td>
<td>—</td>
<td>32</td>
</tr>
<tr>
<td>pr$ _usp</td>
<td>03</td>
<td>pr$ _astlv</td>
<td>13</td>
<td>pr$ _txdb</td>
<td>23</td>
<td>—</td>
<td>33</td>
</tr>
<tr>
<td>pr$ _isp</td>
<td>04</td>
<td>pr$ _sirr</td>
<td>14</td>
<td>—</td>
<td>24</td>
<td>—</td>
<td>34</td>
</tr>
<tr>
<td>—</td>
<td>05</td>
<td>pr$ _sisr</td>
<td>15</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>35</td>
</tr>
<tr>
<td>—</td>
<td>06</td>
<td>—</td>
<td>16</td>
<td>pr$ _mcesr</td>
<td>26</td>
<td>—</td>
<td>36</td>
</tr>
<tr>
<td>—</td>
<td>07</td>
<td>—</td>
<td>17</td>
<td>—</td>
<td>27</td>
<td>pr$ _ioreset</td>
<td></td>
</tr>
</tbody>
</table>

Note: All symbolic values in this table are in hexadecimal.

(continued on next page)
Table 3-1 (Cont.)  Console Symbolic Addresses

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<tr>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
</tr>
</thead>
<tbody>
<tr>
<td>pr$._p0br</td>
<td>08</td>
<td>pr$._icca</td>
<td>18</td>
<td>—</td>
<td>28</td>
<td>pr$._mapen</td>
<td>38</td>
</tr>
<tr>
<td>pr$._p0dr</td>
<td>09</td>
<td>pr$._nicr</td>
<td>19</td>
<td>—</td>
<td>29</td>
<td>pr$._tbia</td>
<td>39</td>
</tr>
<tr>
<td>pr$._plbr</td>
<td>0A</td>
<td>pr$._iccr</td>
<td>1A</td>
<td>pr$._savpc</td>
<td>2A</td>
<td>pr$._tbia</td>
<td>3A</td>
</tr>
<tr>
<td>pr$._pldr</td>
<td>0B</td>
<td>pr$._todr</td>
<td>1B</td>
<td>pr$._savpsl</td>
<td>2B</td>
<td>—</td>
<td>3B</td>
</tr>
<tr>
<td>pr$._shr</td>
<td>0C</td>
<td>—</td>
<td>1C</td>
<td>—</td>
<td>2C</td>
<td>—</td>
<td>3C</td>
</tr>
<tr>
<td>pr$._slr</td>
<td>0D</td>
<td>—</td>
<td>1D</td>
<td>—</td>
<td>2D</td>
<td>—</td>
<td>3D</td>
</tr>
<tr>
<td>—</td>
<td>0E</td>
<td>—</td>
<td>1E</td>
<td>—</td>
<td>2E</td>
<td>pr$._sid</td>
<td>3E</td>
</tr>
<tr>
<td>—</td>
<td>0F</td>
<td>—</td>
<td>1F</td>
<td>—</td>
<td>2F</td>
<td>pr$._tbchk</td>
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<td>pr$._ecr</td>
<td>7D</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>pr$._ctcl</td>
<td>A0</td>
<td>pr$._neoadr</td>
<td>B0</td>
<td>pr$._vmar</td>
<td>D0</td>
<td>—</td>
<td>F0</td>
</tr>
<tr>
<td>—</td>
<td>A1</td>
<td>—</td>
<td>B1</td>
<td>pr$._vtag</td>
<td>D1</td>
<td>—</td>
<td>F1</td>
</tr>
<tr>
<td>pr$._bcdedc</td>
<td>A2</td>
<td>pr$._neocmd</td>
<td>B2</td>
<td>pr$._vdata</td>
<td>D2</td>
<td>pr$._pcadr</td>
<td>F2</td>
</tr>
<tr>
<td>pr$._bcests</td>
<td>A3</td>
<td>—</td>
<td>B3</td>
<td>pr$._icsr</td>
<td>D3</td>
<td>—</td>
<td>F3</td>
</tr>
<tr>
<td>pr$._bctidx</td>
<td>A4</td>
<td>pr$._nedath</td>
<td>B4</td>
<td>—</td>
<td>D4</td>
<td>pr$._pcst</td>
<td>F4</td>
</tr>
<tr>
<td>pr$._bctag</td>
<td>A5</td>
<td>—</td>
<td>B5</td>
<td>—</td>
<td>D5</td>
<td>—</td>
<td>F5</td>
</tr>
<tr>
<td>pr$._bcststs</td>
<td>A6</td>
<td>pr$._nedatlo</td>
<td>B6</td>
<td>—</td>
<td>D6</td>
<td>—</td>
<td>F6</td>
</tr>
<tr>
<td>pr$._bcstidx</td>
<td>A7</td>
<td>—</td>
<td>B7</td>
<td>pr$._pamode</td>
<td>E7</td>
<td>—</td>
<td>F7</td>
</tr>
<tr>
<td>pr$._bcdedc</td>
<td>A8</td>
<td>pr$._neicmd</td>
<td>B8</td>
<td>—</td>
<td>E8</td>
<td>pr$._psectl</td>
<td>F8</td>
</tr>
<tr>
<td>pr$._cefadr</td>
<td>A9</td>
<td>B9</td>
<td>—</td>
<td>E9</td>
<td>—</td>
<td>F9</td>
<td></td>
</tr>
<tr>
<td>pr$._cefsst</td>
<td>AC</td>
<td>RA</td>
<td>pr$._tbadr</td>
<td>EC</td>
<td>—</td>
<td>FA</td>
<td></td>
</tr>
<tr>
<td>pr$._cests</td>
<td>AE</td>
<td>BB</td>
<td>pr$._tbsts</td>
<td>ED</td>
<td>—</td>
<td>FB</td>
<td></td>
</tr>
<tr>
<td>pr$._bctag</td>
<td>01000000 pr$._bclflush</td>
<td>01400000 pr$._pctag</td>
<td>01800000 pr$._pcdgp</td>
<td>01C00000</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(continued on next page)
### KA50/51/55/56 Firmware Commands

#### 3.1 Console I/O Mode Control Characters

Table 3-1 (Cont.) Console Symbolic Addresses

<table>
<thead>
<tr>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
</tr>
</thead>
<tbody>
<tr>
<td>qbio</td>
<td>20000000</td>
<td>qbmem</td>
<td>30000000</td>
<td>qbmbr</td>
<td>20080010</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>rom or feprom</td>
<td>20040000</td>
<td>—</td>
<td>—</td>
<td>bdr</td>
<td>20084000</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>scr</td>
<td>20080000</td>
<td>dsr</td>
<td>20080004</td>
<td>qbear</td>
<td>20080008</td>
<td>dear</td>
<td>2008000C</td>
</tr>
<tr>
<td>ipcr0</td>
<td>20001540</td>
<td>ipcr1</td>
<td>20001542</td>
<td>ipcr2</td>
<td>20001544</td>
<td>ipcr3</td>
<td>20001546</td>
</tr>
<tr>
<td>ssram/ nvr</td>
<td>20140400</td>
<td>ssocr</td>
<td>20140010</td>
<td>ctcdr</td>
<td>20140092</td>
<td>dledr</td>
<td>20140030</td>
</tr>
<tr>
<td>ad0mat</td>
<td>20140130</td>
<td>ad0msk</td>
<td>20140134</td>
<td>ad1mat</td>
<td>20140140</td>
<td>ad1msk</td>
<td>20140144</td>
</tr>
<tr>
<td>tcrl0</td>
<td>20140100</td>
<td>tirl0</td>
<td>20140104</td>
<td>tnin0</td>
<td>20140108</td>
<td>tivr0</td>
<td>2014010c</td>
</tr>
<tr>
<td>tcrl1</td>
<td>20140110</td>
<td>tirl1</td>
<td>20140114</td>
<td>tnr1</td>
<td>20140118</td>
<td>tivr1</td>
<td>2014011c</td>
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<td>nicr0</td>
<td>20008000</td>
<td>nicr1</td>
<td>20008004</td>
<td>nicr2</td>
<td>20008008</td>
<td>nicr3</td>
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<td>nicr5</td>
<td>20008014</td>
<td>nicr6</td>
<td>20008018</td>
<td>nicr7</td>
<td>2000801C</td>
</tr>
<tr>
<td>—</td>
<td>20008020</td>
<td>nicr9</td>
<td>20008024</td>
<td>nicr10</td>
<td>20008028</td>
<td>nicr11</td>
<td>2000802C</td>
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<tr>
<td>nicr12</td>
<td>20008030</td>
<td>nicr13</td>
<td>20008034</td>
<td>nicr14</td>
<td>20008038</td>
<td>nicr15</td>
<td>2000803C</td>
</tr>
<tr>
<td>sgec_setup</td>
<td>20008000</td>
<td>sgec_tpxpoll</td>
<td>20008004</td>
<td>sgec_acpoll</td>
<td>20008008</td>
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<td>20008010</td>
<td>sgec_status</td>
<td>20008014</td>
<td>sgec_mode</td>
<td>20008018</td>
<td>sgec_sbr</td>
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<td>—</td>
<td>20008020</td>
<td>sgec_wdt</td>
<td>20008024</td>
<td>sgec_mfc</td>
<td>20008028</td>
<td>sgec_ verlo</td>
<td>2000802C</td>
</tr>
<tr>
<td>sgec_verhi</td>
<td>20008030</td>
<td>sgec_proc</td>
<td>20008034</td>
<td>sgec_bpt</td>
<td>20008038</td>
<td>sgec_cmd</td>
<td>2000803C</td>
</tr>
<tr>
<td>shac_sswcr</td>
<td>20004230</td>
<td>shac_ sshma</td>
<td>20004244</td>
<td>shac_pqbbbr</td>
<td>20004248</td>
<td>shac_psr</td>
<td>2000424c</td>
</tr>
<tr>
<td>shac_pescr</td>
<td>20004250</td>
<td>shac_pfar</td>
<td>20004254</td>
<td>shac_ppr</td>
<td>20004258</td>
<td>shac_ pmscr</td>
<td>2000425C</td>
</tr>
<tr>
<td>shac_pcr</td>
<td>20004280</td>
<td>shac_ pcq1cr</td>
<td>20004284</td>
<td>shac_ pcq2cr</td>
<td>20004288</td>
<td>shac_ pcq3cr</td>
<td>2000428C</td>
</tr>
<tr>
<td>shac_pdcfer</td>
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<td>shac_ pmfcr</td>
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<td>shac_psrcr</td>
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<td>shac_pscr</td>
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<tr>
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<td>200042A0</td>
<td>shac_pircr</td>
<td>200042A4</td>
<td>shac_pmtcr</td>
<td>200042A8</td>
<td>shac_ pmtecr</td>
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</table>

(continued on next page)
Table 3–1 (Cont.)  Console Symbolic Addresses

<table>
<thead>
<tr>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
</tr>
</thead>
<tbody>
<tr>
<td>mcccwb</td>
<td>21000110</td>
<td>modr</td>
<td>21010000</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>memcon0</td>
<td>21018000</td>
<td>memcon1</td>
<td>21018004</td>
<td>memcon2</td>
<td>21018008</td>
<td>memcon3</td>
<td>2101800c</td>
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<tr>
<td>memcon4</td>
<td>21018010</td>
<td>memcon5</td>
<td>21018014</td>
<td>memcon6</td>
<td>21018018</td>
<td>memcon7</td>
<td>2101801c</td>
</tr>
<tr>
<td>memsig8</td>
<td>21018020</td>
<td>memsig9</td>
<td>21018024</td>
<td>memsig10</td>
<td>21018028</td>
<td>memsig11</td>
<td>2101802c</td>
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<td>21018030</td>
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<td>memsig14</td>
<td>21018038</td>
<td>memsig15</td>
<td>2101803c</td>
</tr>
<tr>
<td>mear</td>
<td>21018040</td>
<td>mser</td>
<td>21018044</td>
<td>nmcdar</td>
<td>21018048</td>
<td>moamr</td>
<td>2101804c</td>
</tr>
<tr>
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<td>21020000</td>
<td>cmcdar</td>
<td>21020004</td>
<td>cesar1</td>
<td>21020008</td>
<td>cesar2</td>
<td>2102000c</td>
</tr>
<tr>
<td>cioear1</td>
<td>21020010</td>
<td>cioear2</td>
<td>21020014</td>
<td>cnear</td>
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<td>21C00000</td>
<td>scddirB</td>
<td>21C00004</td>
<td>scsicr0B</td>
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<td>scsicr1B</td>
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<td>scsicr3B</td>
<td>2200008c</td>
<td>scsicr4B</td>
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<td>scsicr5B</td>
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<td>scsicr7B</td>
<td>2200009c</td>
<td>scsicr8B</td>
<td>22000A0</td>
<td>scsicr9B</td>
<td>22000A4</td>
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<td>scsicraB</td>
<td>220000A8</td>
<td>scsicrbB</td>
<td>220000Ac</td>
<td>scsicrcB</td>
<td>220000B0</td>
<td>scsicmapB</td>
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<td>intmskB</td>
<td>21C00008</td>
<td>intreqB</td>
<td>21C000c</td>
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<tr>
<td>csr</td>
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<td>lpr</td>
<td>25000004</td>
<td>tcr</td>
<td>26000008</td>
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<tr>
<td>msr</td>
<td>2500000C</td>
<td>tdr</td>
<td>2500000C</td>
<td>sar</td>
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</tr>
<tr>
<td>scdadr</td>
<td>25C00000</td>
<td>scddir</td>
<td>25C00004</td>
<td>intmsk</td>
<td>25C00008</td>
<td>intreq</td>
<td>25C0000C</td>
</tr>
<tr>
<td>scsicr0</td>
<td>26000080</td>
<td>scsicr1</td>
<td>26000084</td>
<td>scsicr2</td>
<td>26000088</td>
<td>scsicr3</td>
<td>2600008C</td>
</tr>
<tr>
<td>scsicr4</td>
<td>26000090</td>
<td>scsicr5</td>
<td>26000094</td>
<td>scsicr6</td>
<td>26c00098</td>
<td>scsicr7</td>
<td>25C0009C</td>
</tr>
<tr>
<td>scsicr8</td>
<td>260000A0</td>
<td>scsicr9</td>
<td>260000A4</td>
<td>scsicra</td>
<td>260000A8</td>
<td>scsicrb</td>
<td>260000AC</td>
</tr>
<tr>
<td>scsicrc</td>
<td>260000BU</td>
<td>scsicmap</td>
<td>27000000</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Table 3–2 lists symbolic addresses that you can use in any address space.
KA50/51/55/56 Firmware Commands
3.1 Console I/O Mode Control Characters

Table 3–2  Symbolic Addresses Used In Any Address Space

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>The location last referenced in an EXAMINE or DEPOSIT command.</td>
</tr>
<tr>
<td>+</td>
<td>The location immediately following the last location referenced in an EXAMINE or DEPOSIT command. For references to physical or virtual memory spaces, the location referenced is the last address, plus the size of the last reference (1 for byte, 2 for word, 4 for longword, 8 for quadword). For other address spaces, the address is the last address referenced plus one.</td>
</tr>
<tr>
<td>_</td>
<td>The location immediately preceding the last location referenced in an EXAMINE or DEPOSIT command. For references to physical or virtual memory spaces, the location referenced is the last address minus the size of this reference (1 for byte, 2 for word, 4 for longword, 8 for quadword). For other address spaces, the address is the last address referenced minus one.</td>
</tr>
<tr>
<td>@</td>
<td>The location addressed by the last location referenced in an EXAMINE or DEPOSIT command.</td>
</tr>
</tbody>
</table>

3.1.4 Console Numeric Expression Radix Specifiers

By default, the console treats any numeric expression used as an address or a datum as a hexadecimal integer. The user may override the default radix by using one of the specifiers listed in Table 3–3.

Table 3–3  Console Radix Specifiers

<table>
<thead>
<tr>
<th>Form 1</th>
<th>Form 2</th>
<th>Radix</th>
</tr>
</thead>
<tbody>
<tr>
<td>%b</td>
<td>^b</td>
<td>Binary</td>
</tr>
<tr>
<td>%o</td>
<td>^o</td>
<td>Octal</td>
</tr>
<tr>
<td>%d</td>
<td>^d</td>
<td>Decimal</td>
</tr>
<tr>
<td>%x</td>
<td>^x</td>
<td>Hexadecimal, default</td>
</tr>
</tbody>
</table>

For instance, the value 19 is by default hexadecimal, but it may also be represented as %b11001, %o31, %d25, and %x19 (or in the alternate form as ^b11001, ^o31, ^d25, and ^x19).
3.1.5 Console Command Qualifiers

You can enter console command qualifiers in any order on the command line after the command keyword. The three types of qualifiers are data control, address space control, and command specific. Table 3–4 lists and describes the data control and address space control qualifiers. Command specific qualifiers are listed in the descriptions of individual commands.

<table>
<thead>
<tr>
<th>Qualifier</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Control</strong></td>
<td></td>
</tr>
<tr>
<td>/B</td>
<td>The data size is byte.</td>
</tr>
<tr>
<td>/W</td>
<td>The data size is word.</td>
</tr>
<tr>
<td>/L</td>
<td>The data size is longword.</td>
</tr>
<tr>
<td>/Q</td>
<td>The data size is quadword.</td>
</tr>
<tr>
<td>/N:count</td>
<td>An unsigned hexadecimal integer that is evaluated into a longword. This qualifier determines the number of additional operations that are to take place on EXAMINE, DEPOSIT, MOVE, and SEARCH commands. An error message appears if the number overflows 32 bits.</td>
</tr>
<tr>
<td>/STEP:size</td>
<td>Step. Overrides the default increment of the console current reference. Commands that manipulate memory, such as EXAMINE, DEPOSIT, MOVE, and SEARCH, normally increment the console current reference by the size of the data being used.</td>
</tr>
<tr>
<td>/WRONG</td>
<td>Wrong. On writes, 3 is used as the value of the ECC bits, which always generates double bit errors. Ignores ECC errors on main memory reads.</td>
</tr>
</tbody>
</table>

(continued on next page)
Table 3–4 (Cont.) Console Command Qualifiers

<table>
<thead>
<tr>
<th>Qualifier</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>/G</td>
<td>General purpose register (GPR) address space, R0–R15. The data size is always longword.</td>
</tr>
<tr>
<td>/I</td>
<td>Internal processor register (IPR) address space. Accessible only by the MTPR and MFPR instructions. The data size is always longword.</td>
</tr>
<tr>
<td>/V</td>
<td>Virtual memory address space. All access and protection checking occur. If access to a program running with the current PSL is not allowed, the console issues an error message. Deposits to virtual space cause the PTE&lt;M&gt; bit to be set. If memory mapping is not enabled, virtual addresses are equal to physical addresses. Note that when you examine virtual memory, the address space and address in the response is the physical address of the virtual address.</td>
</tr>
<tr>
<td>/P</td>
<td>Physical memory address space.</td>
</tr>
<tr>
<td>/M</td>
<td>Processor status longword (PSL) address space. The data size is always longword.</td>
</tr>
<tr>
<td>/U</td>
<td>Access to console private memory is allowed. This qualifier also disables virtual address protection checks. On virtual address writes, the PTE&lt;M&gt; bit is not set if the /U qualifier is present. This qualifier is not inherited; it must be respecified on each command.</td>
</tr>
</tbody>
</table>

3.1.6 Console Command Keywords

Table 3–5 lists command keywords by type. Table 3–6 lists the parameters, qualifiers, and arguments for each console command. Parameters, used with the SET and SHOW commands only, are listed in the first column along with the command.

You should not use abbreviations in programs. Although it is possible to abbreviate by using the minimum number of characters required to uniquely identify a command or parameter, these abbreviations may become ambiguous at a later time if an updated version of the firmware contains new commands or parameters.
Table 3–5 Command Keywords by Type

<table>
<thead>
<tr>
<th>Processor Control</th>
<th>Data Transfer</th>
<th>Console Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOT</td>
<td>DEPOSIT</td>
<td>CONFIGURE</td>
</tr>
<tr>
<td>CONTINUE</td>
<td>EXAMINE</td>
<td>FIND</td>
</tr>
<tr>
<td>HALT</td>
<td>MOVE</td>
<td>REPEAT</td>
</tr>
<tr>
<td>INITIALIZE</td>
<td>SEARCH</td>
<td>SET</td>
</tr>
<tr>
<td>NEXT</td>
<td>X</td>
<td>SHOW</td>
</tr>
<tr>
<td>START</td>
<td></td>
<td>TEST</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LOGIN</td>
</tr>
<tr>
<td>UNJAM</td>
<td></td>
<td>!</td>
</tr>
</tbody>
</table>

Table 3–6 Console Command Summary

<table>
<thead>
<tr>
<th>Command</th>
<th>Qualifiers</th>
<th>Argument</th>
<th>Other(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOT</td>
<td>/R5:([boot_flags] /([boot_flags]</td>
<td>...</td>
<td>[([boot_device]),([boot_device])]</td>
</tr>
<tr>
<td>CONFIGURE</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>CONTINUE</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>DEPOSIT</td>
<td>/B /W /L /Q — /G /I /V /P /M /U /N:([count] /STEP:[size] /WRONG</td>
<td>[address] [data]</td>
<td>[data]</td>
</tr>
<tr>
<td>EXAMINE</td>
<td>/B /W /L /Q — /G /I /V /P /M /U /N:([count] /STEP:[size] /WRONG /INSTRUCTION</td>
<td>[([address])]</td>
<td>—</td>
</tr>
<tr>
<td>FIND</td>
<td>/MEM /RPB</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>HALT</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>HELP</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>INITIALIZE</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LOGIN</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

(continued on next page)
### Table 3-6 (Cont.) Console Command Summary

<table>
<thead>
<tr>
<th>Command</th>
<th>Qualifiers</th>
<th>Argument</th>
<th>Other(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOVE</td>
<td>/B /W /L /Q — N /P /U /N:[count] /STEP:[size] /WRONG</td>
<td>[src_address]</td>
<td>[dest_address]</td>
</tr>
<tr>
<td>NEXT</td>
<td>—</td>
<td>[count]</td>
<td>—</td>
</tr>
<tr>
<td>REPEAT</td>
<td>—</td>
<td>[command]</td>
<td>—</td>
</tr>
<tr>
<td>SEARCH</td>
<td>/B /W /L /Q — N /P /U /N:[count] /STEP:[size] /WRONG /NOT</td>
<td>[start_address]</td>
<td>[pattern]</td>
</tr>
<tr>
<td>SET BFLAG</td>
<td>—</td>
<td>[bitmap]</td>
<td>—</td>
</tr>
<tr>
<td>SET BOOT</td>
<td>—</td>
<td>[boot_device],[boot_device]...</td>
<td>—</td>
</tr>
<tr>
<td>SET CONTLOP</td>
<td>—</td>
<td>[0/1]</td>
<td>—</td>
</tr>
<tr>
<td>SET HALT</td>
<td>—</td>
<td>[halt_action]</td>
<td>—</td>
</tr>
<tr>
<td>SCSI_ID</td>
<td>—</td>
<td>[bus][id]</td>
<td>—</td>
</tr>
<tr>
<td>SET HOST</td>
<td>/DUP /DSSI /BUS:[0/1]</td>
<td>[node_number]</td>
<td>[task]</td>
</tr>
<tr>
<td>SET HOST</td>
<td>/DUP /UQSSP /DISK ! /TAPE</td>
<td>[controller_number]</td>
<td>[task]</td>
</tr>
<tr>
<td>SET HOST</td>
<td>/DUP /UQSSP</td>
<td>[csr_address]</td>
<td>[task]</td>
</tr>
<tr>
<td>SET HOST</td>
<td>/MAINTENANCE /UQSSP /SERVICE /MAINTENANCE /UQSSP</td>
<td>[controller_number]</td>
<td>[csr_address]</td>
</tr>
<tr>
<td>SET LANGUAGE</td>
<td>—</td>
<td>[language_type]</td>
<td>—</td>
</tr>
<tr>
<td>SET RECALL</td>
<td>—</td>
<td>[0/1]</td>
<td>—</td>
</tr>
<tr>
<td>SHOW BFLAG</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SHOW BOOT</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SHOW CONTLOP</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SHOW DSSI</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SHOW HALT</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SHOW LANGUAGE</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

1 For Open VMS version 1.3 and earlier, only one argument, the id, is used. For later versions, two arguments are accepted; the first refers to the bus, the second to the id; if only one argument is supplied, the system defaults to bus 0, and the argument is taken as the id.

(continued on next page)
3.2 Console Commands

The following sections describe all the console commands, give the command formats with their qualifiers, and describe the significance of each qualifier.

3.2.1 BOOT

The BOOT command initializes the processor and transfers execution to Virtual Memory Boot (VMB). VMB attempts to boot the operating system from the specified device or list of devices, or from the default boot device if none is specified. The console qualifies the bootstrap operation by passing a boot flags bitmap to VMB in R5.

Format:

BOOT [qualifier-list] [(boot_dev1, e), (boot_device), ...]

If you do not enter either the qualifier or the device name, the default value is used. Explicitly stating the boot flags or the boot device overrides, but does not permanently change, the corresponding default value.
KA50/51/55/56 Firmware Commands

3.2 Console Commands

When specifying a list of boot devices (up to 32 characters, with devices separated by commas and no spaces), the system checks the devices in the order specified and boots from the first one that contains bootable software.

Note

If included in a string of boot devices, the Ethernet device, EZA0, should be placed only as the last device of the string. The system will continuously attempt to boot from EZA0.

Set the default boot device and boot flags with the SET BOOT and SET BFLAG commands. If you do not set a default boot device, the processor times out after 30 seconds and attempts to boot from the Ethernet device, EZA0.

Qualifiers:

Command specific:

/R5:[boot_flags] A 32-bit hex value passed to VMB in R5. The console does not interpret this value. Use the SET BFLAG command to specify a default boot flags longword. Use the SHOW BFLAG command to display the longword.

/[boot_flags] Same as /R5:[boot_flags]

/device_name] A character string of up to 32 characters. When specifying a list of boot devices, the device names should be separated by commas and no spaces. Apart from checking the length, the console does not interpret or validate the device name. The console converts the string to uppercase, then passes VMB a string descriptor to this device name in R0. Use the SET BOOT command to specify a default boot device or list of devices. Use the SHOW BOOT command to display the default boot device. The factory default device is the Ethernet device, EZA0. Refer to the MicroVAX 3100 Customer Technical Information manuals for a list of the boot devices supported by the system.

Examples:

>>>SHOW BOOT
DKA300
>>>SHOW BFLAG
00000000
>>>B "Boot using default boot flags and device.
BOOT/R5:0 DKA300"

2.
~DKA300

3-14 KA50/51/55/56 Firmware Commands
3.2.2 CONTINUE

The CONTINUE command causes the processor to begin instruction execution at the address currently contained in the program counter (PC). This address is the address stored in the PC when the system entered console mode or an address that the user specifies using the DEPOSIT command. The CONTINUE command does not perform a processor initialization. The console enters program I/O mode.

**Format:**

**CONTINUE**

**Example:**

```plaintext
>>>CONTINUE
$ !OpenVMS DCL prompt
```

3.2.3 DEPOSIT

The DEPOSIT command deposits data into the address specified. If you do not specify an address space or data size qualifier, the console uses the last address space and data size used in a DEPOSIT, EXAMINE, MOVE, or SEARCH command. After processor initialization, the default address space is physical memory and the default data size is longword. If you specify conflicting address space or data sizes, the console ignores the command and issues an error message.

**Format:**

**DEPOSIT [qualifier-list] [address] [data] [data...]

Qualifiers:

*Data control*: /B, /N, /L, /Q, /N:[count], /STEP:[size], /WRONG

*Address space control*: /G, /I, /M, /P, /N, /U

**Arguments:**

- **[address]** A longword address that specifies the first location into which data is deposited. The address can be an actual address or a symbolic address.
- **[data]** The data to be deposited. If the specified data is larger than the deposit data size, the firmware ignores the command and issues an error response. If the specified data is smaller than the deposit data size, it is extended on the left with zeros.
- **[[data]]** Additional data to be deposited (as much as can fit on the command line).
KA50/51/55/56 Firmware Commands
3.2 Console Commands

Examples:

>>> D/P/B/N:1FF 0 0    ! Clear first 512 bytes of
        ! physical memory.

>>> D/V/L/N:3 1234 5    ! Deposit 5 into four longwords
        ! starting at virtual memory address
        ! 1234.

>>> D/N:8 R0 FFFFFFFF    ! Loads GPRs R0 through R8 with -1.

>>> D/L/P/N:10/ST:200 0 8  ! Deposit 8 in the first longword of
        ! the first 17 pages in physical
        ! memory.

>>> D/N:200 - 0    ! Starting at previous address, clear
        ! 513 longwords or 2052 bytes.

3.2.4 EXAMINE

The EXAMINE command examines the contents of the memory location or
register specified by the address. If no address is specified, + is assumed.
The display line consists of a single character address specifier, the physical
address to be examined, and the examined data.

EXAMINE uses the same qualifiers as DEPOSIT. However, the /WRONG
qualifier causes EXAMINE to ignore ECC errors on reads from physical
memory. The EXAMINE command also supports an /INSTRUCTION qualifier,
which will disassemble the instructions at the current address.

Format:

EXAMINE [qualifier-list] [address]

Qualifiers:

Data control: /B, /W, /L, /Q, /N:[count], /STEP:[size], /WRONG

Address space control: /G, /I, /M, /P, /N, /U

Command specific:

/INSTRUCTION Disassembles and displays the VAX MACRO-32 instruction at the specified
              address.

Arguments:

[[address]]       A longword address that specifies the first location to be examined. The
                  address can be an actual or a symbolic address. If no address is specified, + is
                  assumed.
Examples:

>>>EX PC
G 000000000 00000000
>>>EX SP
G 000000000 00000000
>>>EX PSL
M 000000000 041F0000
>>>E/M
M 000000000 041F0000
>>>E R4/N:5
G 000000000 00000000
G 000000000 00000000
G 000000000 00000000
G 000000000 00000000
G 000000000 00000000
G 000000000 801D9000

>>>EX PRS SCBB
i 00000011 2004A000
! Examine the SCBB, IPR 17
>>>
! (decimal).
>>>E/P 0
P 00000000 00000000

>>>EX /INS 20040000
P 20040000 11 BRB 20040019

>>>EX /INS/N:5 20040019
P 20040019 D0 MOVL I^#201400000, R#201400000
P 20040024 D2 MCOML @#20140030, R#201400502
P 2004002F D2 MCOML S^#0E, @#20140030
P 20040036 7D MOVQ R0, @#201404B2
P 2004003D D0 MOVL I^#201404B2, R1
P 20040044 DB MFPR S^#2A, B^#44(R1)

>>>E/INS
P 20040048 DB MFPR S^#2B, B^#48(R1)

>>>

3.2.5 FIND

The FIND command searches main memory, starting at address zero for a page-aligned 128-Kbyte segment of good memory, or a restart parameter block (RPB). If the command finds the segment or RPB, its address plus 512 is left in Stack Pointer (SP) R14. If it does not find the segment or RPB, the console issues an error message and preserves the contents of SP. If you do not specify a qualifier, /RPB is assumed.

Format:

FIND [qualifier-list]
**3.2 Console Commands**

**Qualifiers:**

**Command specific:**

/MEMORY

Searches memory for a page-aligned block of good memory, 128K bytes in length. The search looks only at memory that is deemed usable by the bitmap. This command leaves the contents of memory unchanged.

/RPB

Searches all physical memory for an RPB. The search does not use the bitmap to qualify which pages are looked at. The command leaves the contents of memory unchanged.

**Examples:**

```plaintext
>>>EX SP
    G 00000000 00000000
>>>FIND /MEM
    ! Look for a valid 128 Kbytes.
>>>EX SP
    G 00000000 00000200
>>>FIND /RPB
    ! Check for valid RPB.
?2C FND ERR 00C00004
    ! None to be found here.
```

**3.2.6 HALT**

The HALT command has no effect. It is included for compatibility with other VAX consoles.

**Format:**

HALT

**Example:**

```plaintext
>>>HALT    ! Pretend to halt.
```

**3.2.7 HELP**

The HELP command provides information about command syntax and usage.

**Format:**

HELP

**Example:**
>>>HELP
Following is a brief summary of all the commands supported by the console:

UPPERCASE denotes a keyword that you must type in
| denotes an OR condition
[] denotes optional parameters
<> denotes a field specifying a syntactically correct value
.. denotes one of an inclusive range of integers
... denotes that the previous item may be repeated

Valid qualifiers:
   /B /W /L /Q /INSTRUCTION
   /G /I /V /P /M
   /STEP: /N: /NOT
   /WRONG /U

Valid commands:
   BOOT [[/R5:<boot_flags>]] [[<boot_device>]]
   CONTINUE
   DEPOSIT [[<qualifiers>]] <address> <datum> [<datum>...]
   EXAMINE [[<qualifiers>'] [[<address>]]
   FIND [[/MEMORY | /RPB]
   HALT
   HELP
   INITIALIZE
   LOGIN
   MOVE [[<qualifiers>]] <address> <address>
   NEXT [[<count>]]
   REPEAT [[command>]
   SEARCH [[<qualifiers>]] <address> <pattern> [[<mask>]]
   SET BFLG <boot_flags>
   SET BOOT <boot_device>
   SET DSSI ID <bus_number> <id>
   SET HALT <0..4 | DEFAULT| RESTART| REBOOT| HALT|RESTART REBOOT>
   SET HOST/DUP/DSSI/BUS:<0..3> <node_number> [<task>]
   SET LANGUAGE <1..15>
   SET PSE <0..1 | DISABLED | ENABLED>
   SET PSWD <password>
   SET RECALL <0..1 | DISABLED | ENABLED>
   SET SCSI ID <0..7>
   SHOW BFLG
   SHOW BOOT
   SHOW CONFIG
   SHOW DEVICE
   SHOW DSSI [0..3]
   SHOW DSSI_ID
   SHOW ERRORS
   SHOW ESTAT
   SHOW ETHERNET
   SHOW HALT
   SHOW LANGUAGE
   SHOW MEMORY [[/FULL]
3.2.8 INITIALIZE

The INITIALIZE command performs a processor initialization.

**Format:**

INITIALIZE

The following registers are initialized:

<table>
<thead>
<tr>
<th>Register</th>
<th>State at Initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSL</td>
<td>041P0000</td>
</tr>
<tr>
<td>IPL</td>
<td>1F</td>
</tr>
<tr>
<td>ASTLVL</td>
<td>4</td>
</tr>
<tr>
<td>SISR</td>
<td>0</td>
</tr>
<tr>
<td>ICCS</td>
<td>Bits &lt;6&gt; and &lt;0&gt; clear; the rest are unpredictable.</td>
</tr>
<tr>
<td>RXCS</td>
<td>0</td>
</tr>
<tr>
<td>TXCS</td>
<td>80</td>
</tr>
<tr>
<td>MAPEN</td>
<td>0</td>
</tr>
<tr>
<td>Caches</td>
<td>Flushed</td>
</tr>
<tr>
<td>Instruction buffer</td>
<td>Unaffected</td>
</tr>
<tr>
<td>Console previous reference</td>
<td>Longword, physical, address 0</td>
</tr>
<tr>
<td>TODR</td>
<td>Unaffected</td>
</tr>
<tr>
<td>Main memory</td>
<td>Unaffected</td>
</tr>
<tr>
<td>General registers</td>
<td>Unaffected</td>
</tr>
<tr>
<td>Halt code</td>
<td>Unaffected</td>
</tr>
</tbody>
</table>
The firmware clears all error status bits and initializes the following:

- CDAL bus timer
- Address decode and match registers
- Programmable timer interrupt vectors
- The QUART LPR register is set to 9600 baud
- All error status bits are cleared

**Example:**

```
>>>INIT
>>> 
```

### 3.2.9 LOGIN

Allows you to put the system in privileged console mode. When the console security feature is enabled and when you put the system in secure console mode, the system operates in unprivileged console mode. You can access only a subset of the console commands. To access the full range of console commands, you must use this command. This command may only be executed in secure console mode. The format of this command is as follows:

```
LOGIN
```

When you enter the command, the system prompts you for a password as follows:

**Password:**

You must enter the current console security password. If you do not enter the correct password, the system displays the error message, INCORRECT PASSWORD. When you enter the console security password, the system operates in privileged console mode. In this mode, you can use all the console commands. The system exits from privileged console mode when you enter one of the following console commands:

- **BOOT**
- **CONTINUE**
- **HALT**
3.2 Console Commands

• START

3.2.10 MOVE

The MOVE command copies the block of memory starting at the source address to a block beginning at the destination address. Typically, this command has an /N qualifier so that more than one datum is transferred. The destination correctly reflects the contents of the source, regardless of the overlap between the source and the data.

The MOVE command actually performs byte, word, longword, and quadword reads and writes as needed in the process of moving the data. Moves are supported only for the physical and virtual address spaces.

Format:

MOVE [qualifier-list] [src_address] [dest_address]

Qualifiers:

Data control: /B, /W, /L, /Q, /N:[count], /STEP:[size], /WRONG

Address space control: /N, /U, /P

Arguments:

[src_address] A longword address that specifies the first location of the source data to be copied.

[dest_address] A longword address that specifies the destination of the first byte of data. These addresses may be an actual address or a symbolic address. If no address is specified, + is assumed.

Examples:

>>>EX/N: 4 0
P 00000000 00000000
P 00000004 00000000
P 00000008 00000000
P 0000000C 00000000
P 00000010 00000000

>>>EX/N: 4 200
P 00000200 5BDD0520
P 00000204 585E04C1
P 00000208 00FF8FBB
P 0000020C 5208A8D0
P 00000210 540C08DE

>>>MOV/N: 4 200 0
P 00000200 5BDD0520
P 00000204 585E04C1
P 00000208 00FF8FBB
P 0000020C 5208A8D0
P 00000210 540C08DE

! Observe destination.

! Observe source data.

! Move the data.
>>>EX/N: 4 0
P 00000000 58dd0520
P 00000004 585e04c1
P 00000008 00ff8fbb
P 0000000c 5208a8d0
P 00000010 540ca8de

3.2.11 NEXT

The NEXT command executes the specified number of macro instructions. If no count is specified, 1 is assumed.

After the last macro instruction is executed, the console reenters console I/O mode.

Format:

NEXT {count}

The console implements the NEXT command, using the trace trap enable and trace pending bits in the PSL and the trace pending vector in the SCB.

The console enters the "Spacebar Step Mode". In this mode, subsequent spacebar strokes initiate single steps and a carriage return forces a return to the console prompt.

The following restrictions apply:

- If memory management is enabled, the NEXT command works only if the first page in SSC RAM is mapped in S0 (system) space.
- Overhead associated with the NEXT command affects execution time of an instruction.
- The NEXT command elevates the IPL to 31 for long periods of time (milliseconds) while single-stepping over several commands.
- Unpredictable results occur if the macro instruction being stepped over modifies either the SCBB or the trace trap entry. This means that you cannot use the NEXT command in conjunction with other debuggers.

Arguments:

{count} A value representing the number of macro instructions to execute.
KA50/51/55/56 Firmware Commands
3.2 Console Commands

Examples:

>>>DEP 1000 50D650D4 ! Create a simple program.
>>>DEP 1004 125005D1
>>>DEP 1008 00FE11F9
>>>EX /INSTRUCTION /N:5 1000 ! List it.
  P 00001000 D4 CLRL R0
  P 00001002 D6 INCL R0
  P 00001004 D1 CMPL *#05,R0
  P 00001007 12 BNEQ 00001002
  P 00001009 11 BRB 00001009
  P 0000100B 00 HALT
>>>DEP PR$ SCBB 200 ! Set up a user SCBB...
>>>DEP PC I000 ! ...and the PC.

>>>>
>>>N ! Single step...
  P 00001002 D6 INCL R0 ! SPACEBAR
  P 00001004 D1 CMPL *#05,R0 ! SPACEBAR
  P 00001007 12 BNEQ 00001002 ! SPACEBAR
  P 00001002 D6 INCL R0 ! CR
>>>N 5 ! ...or multiple step the program.
  P 00001004 D1 CMPL *#05,R0
  P 00001007 12 BNEQ 00001002
  P 00001002 D6 INCL R0
  P 00001004 D1 CMPL *#05,R0
  P 00001007 12 BNEQ 00001002
>>>N 7
  P 00001002 D6 INCL R0
  P 00001004 D1 CMPL *#05,R0
  P 00001007 12 BNEQ 00001002
  P 00001002 D6 INCL R0
  P 00001004 D1 CMPL *#05,R0
  P 00001007 12 BNEQ 00001002
  P 00001009 11 BRB 00001009
>>>N
  P 00001009 11 BRB 00001009

3.2.12 REPEAT

The REPEAT command repeatedly displays and executes the specified command. Press [Ctrl/C] to stop the command. You can specify any valid console command except the REPEAT command.

Format:

REPEAT [command]
Arguments:

(command) A valid console command other than REPEAT.

Examples:

>>>REPEAT EX PR$ TCDR !Watch the clock.
I 0000001B 5AFE7BCE
I 0000001B 5AFE7BD1
I 0000001B 5AFE7BFD
I 0000001B 5AFE7900
I 0000001B 5AFE7903
I 0000001B 5AFE7907
I 0000001B 5AFE790A
I 0000001B 5AFE790D
I 0000001B 5AFE7910
I 0000001B 5AFE793C
I 0000001B 5AFE793F
I 0000001B 5AFE7942
I 0000001B 5AFE7946
I 0000001B 5AFE7949
I 0000001B 5AFE794C
I 0000001B 5AFE794F
I 0000001B 5°C

3.2.13 SEARCH

The SEARCH command finds all occurrences of a pattern and reports the addresses where the pattern was found. If the /NOT qualifier is present, the command reports all addresses in which the pattern did not match.

Format:

SEARCH [qualifier-list] [address] [pattern] [[mask]]

SEARCH accepts an optional mask that indicates bits to be ignored (don't care bits). For example, to ignore bit 0 in the comparison, specify a mask of 1. The mask, if not present, defaults to 0.

A match occurs if (pattern and not mask) = (data and not mask), where:

- Pattern is the target data.
- Mask is the optional don't care bitmask (which defaults to 0).
- Data is the data at the current address.
**SEARCH** reports the address under the following conditions:

<table>
<thead>
<tr>
<th>/NOT Qualifier</th>
<th>Match Condition</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>Absent</td>
<td>True</td>
<td>Report address</td>
</tr>
<tr>
<td>Absent</td>
<td>False</td>
<td>No report</td>
</tr>
<tr>
<td>Present</td>
<td>True</td>
<td>No report</td>
</tr>
<tr>
<td>Present</td>
<td>False</td>
<td>Report address</td>
</tr>
</tbody>
</table>

The address is advanced by the size of the pattern (byte, word, longword, or quadword), unless overridden by the /STEP qualifier.

**Qualifiers:**

- **Data control:** /B, /W, /L, /Q, /N:[count], /STEP:[size], /WRONG
- **Address space control:** /P, /N, /U

**Command specific:**

/NOT Inverts the sense of the match.

**Arguments:**

- **[start address]** A longword address that specifies the first location subject to the search. This address can be an actual address or a symbolic address. If no address is specified, + is assumed.
- **(pattern)** The target data.
- **{[mask]}** A mask of the bits desired in the comparison.

**Examples:**
3.2.14 SET

The SET command sets the parameter to the value you specify.

Format:

SET (parameter) (value)

Parameters:

BFLAG       Sets the default R5 boot flags. The value must be a hex number of up to eight digits.

BOOT        Sets the default boot device. The value must be a valid device name or list of device names as specified in the BOOT command description in Section 3.2.1.

HALT        Sets the user-defined halt action. Acceptable values are the keywords "default", "restart", "reboot", "halt", "restart_reboot", or a number in the range 0 to 4 inclusive.
KA50/51/55/56 Firmware Commands

3.2 Console Commands

HOST
Invoke the DUP or MAINTENANCE driver on the selected node. Only SET HOST/DUP accepts a value parameter. The hierarchy of the SET HOST qualifiers listed below suggests the appropriate usage. Each qualifier only supports additional qualifiers at levels below it.

LANGUAGE
Sets console language and keyboard type. If the current console terminal does not support the multinational character set (MCS), then this command has no effect and the console message appears in English. Values are 1 through 15.

PSE
Allows you to enable or disable the console security feature of the system. The SET PSE command accepts the following values:

- 0—Console security disabled
- 1—Console security enabled

When the console security feature is enabled, only a subset of the console commands is available to the user. To enable the complete set of console commands once the console security feature is enabled, you must use the LOGIN command (see Section 3.2.9).

PSWD
Allows you to set or change the console security password.

RECALL
Sets command recall state to either ENABLED (1) or DISABLED (0).

SCSI_ID
Sets the SCSI ID of the SCSI controller to a number in the range 0 to 7. The SCSI ID of the SCSI controller is set to 6 before the system is shipped. For the KZDDA option second SCSI bus, You must enter two arguments; the bus, then the id.

Qualifiers: Listed in the parameter descriptions above.

Examples:

>>>
>>>SET BFLAG 220
>>>SET BOOT DUA0
>>>SET LANGUAGE 5
>>>SET HALT RESTART
>>>
KA50/51/55/56 Firmware Commands
3.2 Console Commands

Parameters:

BFLAG Displays the default R5 boot flags.
BOOT Displays the default boot device.
CONFIG Displays the system configuration. The command displays information about the devices that the firmware has tested. It also displays the device errors that the most recent device test detected.
DEVICE Displays all devices in the system.
HALT Shows the user-defined halt action.
ESTAT Shows results from last run of the system exerciser, tests 100 to 107. Data is volatile and is destroyed by running other tests or boots, etc. SHOW ESTAT normally done immediately after running the system test.
ERRORS Shows saved data on tests which failed.
ETHERNET Displays hardware Ethernet address for all Ethernet adapters that can be found. Displays as blank if no Ethernet adapter is present.
LANGUAGE Displays console language and keyboard type. Refer to the corresponding SET LANGUAGE command for the meaning.
MEMORY Displays main memory configuration.
/FULL—Additionally, displays the normally inaccessible areas of memory, such as the PFN bitmap pages, and the console scratch memory pages. Also reports the addresses of bad pages, as defined by the bitmap.
PSE Displays the condition of the console security feature of the system.
RECALL Shows the current state of command recall, either ENABLED or DISABLED.

This information is obtained from the media type field of the MSCP command GET UNIT STATUS. The console does not display device information if a node is not running (or cannot run) an MSCP server.

SCSI Shows any SCSI devices in the system.
TRANSLATION Shows any virtual addresses that map to the specified physical address. The firmware uses the current values of page table base and length registers to perform its search; it is assumed that page tables have been properly built.
VERSION Displays the current firmware version.

Qualifiers: Listed in the parameter descriptions above.
KA50/51/55/56 Firmware Commands
3.2 Console Commands

Examples:

>>> >>>SHOW BFLAG
00000220
>>> >>>SHOW BOOT
DUA0
>>> >>>SHOW CONTROLP
>>> >>>SHOW ETHERNET
Ethernet Adapter
-EZA0 (08-00-2B-0B-29-14)
>>> >>>SHOW HALT
restart
>>> >>>SHOW LANGUAGE
English (United States/Canada)
>>> >>>show memory
16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 0400000 to 04FFFFFF, 16MB, 32768 good pages, 0 bad pages
64 MB RAM, SIMM Set (1E,1F,1G,1H) present
Memory Set 1: 00000000 to 03FFFFFF, 64MB, 131072 good pages, 0 bad pages
Total of 80MB, 163840 good pages, 0 bad pages, 136 reserved pages
>>> ;show memory / full
>>> show mem/full
16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 00000000 to 00FFFFFF, 16MB, 32768 good pages, 0 bad pages
Total of 16MB, 32768 good pages, 0 bad pages, 104 reserved pages
Memory Bitmap
-00FF3000 to 00FF3FFF, 8 pages
Console Scratch Area
-00FF4000 to 00FF7FFF, 32 pages
Scan of Bad Pages
>>>
### 3.2.16 START

The START command starts instruction execution at the address you specify. If no address is given, the current PC is used. If memory mapping is enabled, macro instructions are executed from virtual memory, and the address is treated as a virtual address. The START command is equivalent to a DEPOSIT to PC, followed by a CONTINUE. It does not perform a processor initialization.

**Format:**

```
START [[address]]
```

**Arguments:**

- **[address]**: The address at which to begin execution. This address is loaded into the user's PC.

**Example:**

```
>>>START 1000
```

### 3.2.17 TEST

The TEST command invokes a diagnostic test program specified by the test number. If you enter a test number of 0 (zero), the power-up diagnostics are executed. The console accepts an optional list of up to five additional hexadecimal arguments.

Refer to Chapter 5 for a detailed explanation of the diagnostics.

**Format:**

```
TEST [test_number] [test_arguments]
```

**Arguments:**

- **test_number**: A two-digit hex number specifying the test to be executed. No meaning to console, but meaning to tests themselves. **T 9E** lists arguments used by applicable tests.
3.2 Console Commands

(test_arguments) Up to five additional test arguments. These arguments are accepted, but they have no meaning to the console.

Example:

```plaintext
>>>TEST 0
72...71...70...69...68...67...66...65...64...63...62...61...60...59...58...57...
56...55...54...53...52...51...50...49...48...47...46...45...44...43...42...41...
40...39...38...37...36...35...34...33...32...31...30...29...28...27...26...25...
24...23...22...21...20...19...18...17...16...15...14...13...12...11...10...09...
08...07...06...05...04...03...
Tests completed.
>>>`

Example:

```plaintext
>>> ! Display the CPU registers.

>>>T 9C

savpc=20048C68 savpsl=20048C68 sbr=03FA0000 slr=00003040
p0br=80000000 p0lr=00182000 plbr=00000000 pllr=00000000
sid=13001401 sie=03020801 mapen=00000000
trcr=00000000 tir0=00000000 tnr0=00000000 tivr0=0000000078
tcr1=00000001 tir1=02AF768E tnr1=00000000F tivr1=00000007C
bdr=3FBB08F0 ssccr=00D05070 scbb=20053400
D2 csr=0020 tcr=0008 msr=07F5
scr=00000000 dser=00000000 qbear=00000000D dear=00000000
qbmbx=03FFB000 ipcr=0000
nicsr=01FF0003 3=00004030 4=00004050 5=8039PF00 6=83EF0000 7=00000000
nicsr9=04E204E2 10=00040000 11=00000000 12=00000000 13=00000000 15=00000000
NISA-0B-0B-2B-2B-2B-7A intmask=00 intreq=00 scaddr=00000000 scddir=0
SCSI_CSRs 0=00 1=00 2=00 3=00 4=00 6=05 5=05 7=00 8=16 9=5B A=5B B=00 C=04
VIC......icsr=00000001 vmr=000007E0 ecr=000000CA
PC......pcct1=000FD9F3 pccts=00FF0000 pchdr=00000000
BC_128K...cct1=00000000 bcetst=00000030 bcetidx=00FFFE00 bcetag=00FFFE00
......bcedst=00000000 bcedidx=01FFFE00 bcedec=00000000
......nest=00000000 necadr=E005F700 necmdm=00000004 necmd=000003FF
......nedath=00FF0000 nedatlo=00FF0000 cefata=00520000 cefadr=E000002C0
MEMORY...mesr=00060000 mear=04060100 Add=21018040 mxcdr=01111000
......memcon=08000000 memcon1=00000007 moamr=00000000 ssr=COCE
NCA......cesr=00000000 cmcds=00000000 cnear=00000000
......csear1=00000000 csear2=00000000 ciear1=00000000 ciear2=00000000
ci...ics=00000000 nicr=00000000 iccr=00000000
ci...icc=00000000 icc=00000000 iccr=00000000
ci...iiss=00000000 iccr=00000000 iccr=00000000
ci...iicc=00000000 iccr=00000000 iccr=00000000
ci...iic=00000000 iccr=00000000 iccr=00000000
ci...iic=00000000 iccr=00000000 iccr=00000000
>>>"
### Example:

```plaintext
>>> ! list diagnostics and scripts
>>> TEST
```

<table>
<thead>
<tr>
<th>#</th>
<th>Address</th>
<th>Name</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0052200</td>
<td>SCB</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>0055850</td>
<td>De_executive</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>006A53C</td>
<td>Memory_Init_Bitmap</td>
<td>mark_Hard_SBEs</td>
</tr>
<tr>
<td>32</td>
<td>006A834</td>
<td>Memory_Session_CSRs</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>005D148</td>
<td>NMC_registers</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>005D324</td>
<td>NMC_powerup</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>005E03D</td>
<td>SCC_ROM</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>005F939</td>
<td>B_Cache_diag_mode</td>
<td>bypass_test_mask</td>
</tr>
<tr>
<td>37</td>
<td>0061939</td>
<td>Cache_w_Memory</td>
<td>bypass_test_mask</td>
</tr>
<tr>
<td>40</td>
<td>006B5E0</td>
<td>Memory_count_pages</td>
<td>SIMM_set0 SIMM_set1 Soft_errs_allowed</td>
</tr>
<tr>
<td>41</td>
<td>0068CEC</td>
<td>Board_Reset</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>0061880</td>
<td>Chk_for_Interrupts</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>00610C4</td>
<td>P_Cache_diag_mode</td>
<td>bypass_test_mask</td>
</tr>
<tr>
<td>47</td>
<td>006AD04</td>
<td>Memory_Refresh</td>
<td>start_a end _incr_cont_on_err_time_seconds</td>
</tr>
<tr>
<td>48</td>
<td>006B02E</td>
<td>Memory_Adr_shorts</td>
<td>start_add end_add * cont_on_err pat2 pat3</td>
</tr>
<tr>
<td>4A</td>
<td>006A23C</td>
<td>Memory_ECC_BEs</td>
<td>start_add end _add _incr_cont_on_err</td>
</tr>
<tr>
<td>4B</td>
<td>006940C</td>
<td>Memory_Error_BEs</td>
<td>start_add end_add _add _incr_cont_on_err</td>
</tr>
<tr>
<td>4C</td>
<td>0069BA0</td>
<td>Memory_ECC_Logic</td>
<td>start_add end_add _add _incr_cont_on_err</td>
</tr>
<tr>
<td>4D</td>
<td>0068PE8</td>
<td>Memory_Adress</td>
<td>start_add end_add _add _incr_cont_on_err</td>
</tr>
<tr>
<td>4E</td>
<td>0069188</td>
<td>Memory_Bye</td>
<td>start_add end_add _add _incr_cont_on_err</td>
</tr>
<tr>
<td>4F</td>
<td>006B7F4</td>
<td>Memory_Data</td>
<td>start_add end_add _add _incr_cont_on_err</td>
</tr>
<tr>
<td>51</td>
<td>005B803C</td>
<td>FPA</td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>005B8530</td>
<td>SSL_Prog_TIMERS</td>
<td>which timer wait_time us</td>
</tr>
<tr>
<td>53</td>
<td>005B818</td>
<td>SSL_TOY_Clock</td>
<td>repeat_test _250ms _ea Tolerance</td>
</tr>
<tr>
<td>54</td>
<td>0057C18</td>
<td>Virtual_Mode</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>005B86C</td>
<td>Interval_Timer</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>006507C</td>
<td>SHAC LPBCK</td>
<td>From_bus To_bus passes</td>
</tr>
<tr>
<td>58</td>
<td>0065D24</td>
<td>SHAC_RESET</td>
<td>dssi_bus_port_number time_secs not pres</td>
</tr>
<tr>
<td>59</td>
<td>0062778</td>
<td>SGEC_LPBCK_ASSIST</td>
<td>time_secs</td>
</tr>
<tr>
<td>5C</td>
<td>0062D10</td>
<td>SHAC</td>
<td>SHAC_number</td>
</tr>
<tr>
<td>5F</td>
<td>00619B8</td>
<td>SGEC</td>
<td>loopback_type no ram tests</td>
</tr>
<tr>
<td>62</td>
<td>005B81C</td>
<td>console_QDSS</td>
<td>mark not_present selftest_r0 selftest_r1</td>
</tr>
<tr>
<td>63</td>
<td>005C0A4</td>
<td>QDSS_any</td>
<td>input_cfg selftest_r0 selftest_r1</td>
</tr>
<tr>
<td>80</td>
<td>00553DC</td>
<td>CQBIC_memory</td>
<td>bypass_test_mask</td>
</tr>
<tr>
<td>81</td>
<td>00569CC</td>
<td>QBUS_MSCP</td>
<td>IP csr</td>
</tr>
<tr>
<td>82</td>
<td>00598AC</td>
<td>QBUS_DELQA</td>
<td>device_num_addr</td>
</tr>
<tr>
<td>83</td>
<td>005A5BC</td>
<td>QZA Intlbckc1</td>
<td>controller_number</td>
</tr>
<tr>
<td>84</td>
<td>005BFC1</td>
<td>QZA Intlbckc2</td>
<td>controller_number</td>
</tr>
<tr>
<td>85</td>
<td>005A9AC</td>
<td>QZA_memory</td>
<td>incr test_pattern controller_number</td>
</tr>
<tr>
<td>86</td>
<td>0059F44</td>
<td>QZA_DMA</td>
<td>Controller_number main_mem_buf</td>
</tr>
<tr>
<td>90</td>
<td>0058494</td>
<td>CQBIC_registers</td>
<td></td>
</tr>
<tr>
<td>Code</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>------</td>
<td>------------------------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>91</td>
<td>CQBIC_powerup</td>
<td></td>
<td></td>
</tr>
<tr>
<td>99</td>
<td>Flush Echo Caches</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9A</td>
<td>INTERACTION</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9B</td>
<td>Init_memory</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9C</td>
<td>List_CPU_registers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9D</td>
<td>Utility</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9E</td>
<td>List_diagnostics</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9F</td>
<td>Create_A0_Script</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>SSC_RAM_Data</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>SSC_RAM_Data_Addr</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C5</td>
<td>SSC_registers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D0</td>
<td>V Cache diag_mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>O Bit diag_mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>PB Flush_Cache</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td>Speed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td>NO Memory_present</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D5</td>
<td>B Cache_Data_debug</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td>B Cache_Tag_Debug</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D7</td>
<td>O BIT_DEBUG</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D8</td>
<td>SC5I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D9</td>
<td>SC5I_Utilty</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D10</td>
<td>SC5I_MAP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D11</td>
<td>SC5I_MAP_Option</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D12</td>
<td>User defined scripts</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D13</td>
<td>Powerup tests, Functional Verify, continue on error, numeric countdown</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D14</td>
<td>Functional Verify, stop on error, test # announcements</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D15</td>
<td>Loop on A3 Functional Verify</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D16</td>
<td>Memory tests, mark only multiple bit errors</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D17</td>
<td>Memory tests</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D18</td>
<td>Memory acceptance tests, mark single and multi-bit errors, call A7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D19</td>
<td>Memory tests, stop on error</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D20</td>
<td>Extended tests plus BF, then loop</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D21</td>
<td>Extended tests, then loop</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D22</td>
<td>BF D2, SYNC, ASYNC with loopbacks</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
KA50/51/55/56 Firmware Commands
3.2 Console Commands

Load & start system exerciser
100 Customer mode, 2 passes
101 CSSE mode, 2 passes
102 CSSE mode, continuous until ^C
103 Manuf mode, continuous until ^C
104 Manuf TINA mode, continuous until ^C
105 Manuf mode, 2 passes
106 CSSE mode, select tests, continuous until ^C
107 Manuf mode, select tests, continuous until ^C

>>>>

3.2.18 UNJAM

The UNJAM command performs an I/O bus reset, by writing a 1 (one) to IPR 55 (decimal). SHAC and SGEC are explicitly reset, EDAL_INTREQ register error bits are cleared and SCSI_DMA map registers are cleared.

Format:

UNJAM

Example:

>>>UNJAM

>>>>

3.2.19 X—Binary Load and Unload

The X command is for use by automatic systems communicating with the console.

The X command loads or unloads (that is, writes to memory, or reads from memory) the specified number of data bytes through the console serial line (regardless of console type) starting at the specified address.

Format:

X [address] [count] CR [line_checksum] [data] [data_checksum]

If bit 31 of the count is clear, data is received by the console and deposited into memory. If bit 31 is set, data is read from memory and sent by the console. The remaining bits in the count are a positive number indicating the number of bytes to load or unload.

The console accepts the command upon receiving the carriage return. The next byte the console receives is the command checksum, which is not echoed. The command checksum is verified by adding all command characters, including the checksum and separating space (but not including the terminating carriage return, rubouts, or characters deleted by rubout), into an 8-bit register initially set to zero. If no errors occur, the result is zero. If the command checksum
is correct, the console responds with the input prompt and either sends
data to the requester or prepares to receive data. If the command checksum
is in error, the console responds with an error message. The intent is to
prevent inadvertent operator entry into a mode where the console is accepting
characters from the keyboard as data, with no escape mechanism possible.

If the command is a load (bit 31 of the count is clear), the console responds
with the input prompt (>>>), then accepts the specified number of bytes of data
for depositing to memory, and an additional byte of received data checksum.
The data is verified by adding all data characters and the checksum character
into an 8-bit register initially set to zero. If the final content of the register is
nonzero, the data or checksum are in error, and the console responds with an
error message.

If the command is a binary unload (bit 31 of the count is set), the console
responds with the input prompt (>>>), followed by the specified number of
bytes of binary data. As each byte is sent, it is added to a checksum register
initially set to zero. At the end of the transmission, the two's complement of
the low byte of the register is sent.

If the data checksum is incorrect on a load, or if memory or line errors occur
during the transmission of data, the entire transmission is completed, then the
console issues an error message. If an error occurs during loading, the contents
of the memory being loaded are unpredictable.

The console represses echo while it is receiving the data string and checksums.

The console terminates all flow control when it receives the carriage return at
the end of the command line in order to avoid treating flow control characters
from the terminal as valid command line checksums.

You can control the console serial line during a binary unload using control
characters (Ctrl/C, Ctrl/S, Ctrl/O, and so on). You cannot control the console
serial line during a binary load, since all received characters are valid binary
data.

The console has the following timing requirements:

* It must receive data being loaded with a binary load command at a rate of
  at least one byte every 60 seconds.
* It must receive the command checksum that precedes the data within 60
  seconds of the carriage return that terminates the command line.
* It must receive the data checksum within 60 seconds of the last data byte.

If any of these timing requirements are not met, then the console aborts the
transmission by issuing an error message and returning to the console prompt.
The entire command, including the checksum, can be sent to the console as a single burst of characters at the specified character rate of the console serial line. The console is able to receive at least 4 Kbytes of data in a single X command.
KA50/51/55/56 Firmware Commands
3.2 Console Commands

3.2.20  ! (Comment)

The comment character (an exclamation point) is used to document command sequences. It can appear anywhere on the command line. All characters following the comment character are ignored.

Format:  

Example:

>>>! The console ignores this line.
>>>
System Initialization and Acceptance Testing (Normal Operation)

This chapter describes the system initialization, testing, and bootstrap processes that occur at power-up. In addition, the acceptance test procedure to be performed when installing a system or whenever adding or replacing FRUs is described.

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95 and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q–bus and DSSI, will appear on the console and/or printouts from time to time.

4.1 Basic Initialization Flow

On power-up, the firmware identifies the console device, optionally performs a language inquiry, and runs the diagnostics.

The firmware waits for power to stabilize by monitoring SCR<15>(POK). Once power is stable, the firmware verifies that the console battery backup RAM (BBU RAM) is valid (backup battery is charged) by checking SSSCR<31>(BLO). If it is invalid or zero (battery is discharged), the BBU RAM is initialized.

After the battery check, the firmware tries to determine the type of terminal attached to the console serial line. It uses this information to determine if multinational support is appropriate.

The console uses the saved console language if the contents of the BBJ RAM are valid.
System Initialization and Acceptance Testing (Normal Operation)

4.1 Basic Initialization Flow

If the firmware detects that the contents of the BBU RAM are invalid, the firmware prompts you for the language to be used for displaying the following system messages (if the console terminal supports the multinational character set):

Loading system software.
Failure.
Restarting system software.
Performing normal system tests.
Tests completed.
Normal operation not possible.
Bootfile.
Memory configuration error.
No default boot device has been specified.
Available devices.
Device?
Retrying network bootstrap.

The position of the Break Enable/Disable switch has no effect on these conditions. The firmware will not prompt for a language if the console terminal, such as the VT100, does not support the multinational character set (MCS).

Following a successful diagnostic countdown (see Example 4–1), the console may prompt you for a default boot device.

Example 4–1 Successful Diagnostic Countdown

KA50-A VX.X, VMB 2.14
Performing normal system tests.
  12..71..70..69..68..67..66..65..64..63..62..61..60..59..58..57..
  56..55..54..53..52..51..50..49..48..47..46..45..44..43..42..41..
  40..39..38..37..36..35..34..33..32..31..30..29..28..27..26..25..
  24..23..22..21..20..19..18..17..16..15..14..13..12..11..10..09..
  08..07..06..05..04..03..
Tests completed.

4.2 Power-On Self-Tests (POST)

Power-on self-tests provide core testing of the system kernel comprised of the CPU and memory. Certain registers are flushed, and data structures are set up to initialize and set the system to a known state for the operating system.
4.2.1 Power-Up Tests for Kernel

In a nonmanufacturing environment where the intended console device is the serial line unit (SLU), the console program performs the following actions at power-up:

1. Checks for POK.
2. Establishes SLU as console device.
3. Prints banner message.
   
The banner message contains the processor name, the version of the firmware, and the version of VMB. The letter code in the firmware version indicates if the firmware is pre-field test, field test, or official release. The first digit indicates the major release number and the trailing digit indicates the minor release number (Figure 4–1).

**Figure 4–1 Console Banner**

```
KA52-A V n.n, VMB n.n
```

- minor release of VMB
- major release of VMB
- minor release of firmware
- major release of firmware
- type of release: X - engineering release
  T - field test release
  V - volume release
- processor type

4. Displays language inquiry menu on console if console supports multinational character set (MCS) and any of the following are true:
   - Battery is dead.
   - Contents of SSC RAM are invalid.

5. Calls the diagnostic executive (DE) with Test Code = 0.
   a. DE executes script A1 (Tests system module and memory).
System Initialization and Acceptance Testing (Normal Operation)
4.2 Power-On Self-Tests (POST)

While the diagnostics are running, the LEDs display a test code. A different countdown appears on the console terminal. Refer to Table 5–4 for a complete explanation of the power-up test display. Table 4–1 lists the LED codes and the associated actions performed at power-up. Example 4–2 shows a successful power-up to a list of bootable devices.

b. DE passes control back to the console program.

6. Issues end message and >>> prompt.

<table>
<thead>
<tr>
<th>LED Value</th>
<th>Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>Initial state on power-up, no code has executed</td>
</tr>
<tr>
<td>E</td>
<td>Entered ROM space, some instructions have executed</td>
</tr>
<tr>
<td>D</td>
<td>Waiting for power to stabilize (POK)</td>
</tr>
<tr>
<td>C</td>
<td>SSC RAM, SSC registers, and ROM checksum tests</td>
</tr>
<tr>
<td>B</td>
<td>O-bit memory, interval timer, and virtual mode tests</td>
</tr>
<tr>
<td>A</td>
<td>FPA tests</td>
</tr>
<tr>
<td>9</td>
<td>Backup cache tests</td>
</tr>
<tr>
<td>8</td>
<td>NMC, NCA, memory, and I/O interaction tests</td>
</tr>
<tr>
<td>7</td>
<td>CQBIC, SYNC, and ASYNC tests</td>
</tr>
<tr>
<td>6</td>
<td>Console and QUART tests</td>
</tr>
<tr>
<td>5</td>
<td>SCSI tests</td>
</tr>
<tr>
<td>4</td>
<td>SGEC Ethernet subsystem tests</td>
</tr>
<tr>
<td>3</td>
<td>&quot;Console I/O&quot; mode</td>
</tr>
<tr>
<td>2</td>
<td>Control passed to VMB</td>
</tr>
<tr>
<td>1</td>
<td>Control passed to secondary bootstrap</td>
</tr>
<tr>
<td>0</td>
<td>&quot;Program I/O&quot; mode, control passed to operating system</td>
</tr>
</tbody>
</table>
System Initialization and Acceptance Testing (Normal Operation)

4.2 Power-On Self-Tests (POST)

Example 4-2 Successful Power-Up to List of Bootable Devices

KA50-A VX.X, VMB 2.14
Performing normal system tests.
72..71..70..69..68..67..66..65..64..63..62..61..60..59..58..57..
56..55..54..53..52..51..50..49..48..47..46..45..44..43..42..41..
40..39..38..37..36..35..34..33..32..31..30..29..28..27..26..25..
24..23..22..21..20..19..18..17..16..15..14..13..12..11..10..09..
08..07..06..05..04..03..
Tests completed.
Loading system software.
No default boot device has been specified.
Available devices:
- DIAO (RF73)
- DIA1 (RF73)
- MIA5 (TF85)
- EZA0 (08-00-2B-06-10-42)
Device? [EZA0]:

4.2.2 Power-Up Tests for Mass Storage Devices

An RZ-series ISE may fail either during initial power-up or during normal operation. In both cases, the failure is indicated by the lighting of the red fault LED on the drive's front panel. The ISE also has a red fault LED, but it is not visible from the outside of the system enclosure.

If the drive is unable to execute the Power-On Self-Test (POST) successfully, the red fault LED remains lit and the ready LED does not come on, or both LEDs remain on.

POST is also used to handle two types of error conditions in the drive:

- **Controller errors** are caused by the hardware associated with the controller function of the drive module. A controller error is fatal to the operation of the drive, since the controller cannot establish a logical connection to the host. The red fault LED lights. If this occurs, replace the drive module.

- **Drive errors** are caused by the hardware associated with the drive control function of the drive module. These errors are not fatal to the drive, since the drive can establish a logical connection and report the error to the host. Both LEDs go out for about 1 second, then the red fault LED lights.
4.3 CPU ROM-Based Diagnostics

The KA50/51/55/56 ROM-based diagnostic facility is the primary diagnostic tool for troubleshooting and testing of the CPU, memory, and Ethernet. ROM-based diagnostics have significant advantages:

- Load time is virtually nonexistent.
- The boot path is more reliable.
- Diagnosis is done in a more primitive state.

The ROM-based diagnostics can detect failures in field-replaceable units (FRUs) other than the CPU module. For example, they can isolate to two memory SIMMS. (Table 5–4 lists the FRUs indicated by ROM-based diagnostic error messages.)

The diagnostics run automatically on power-up. While the diagnostics are running, the LED displays a hexadecimal number; while booting the operating system, 2 through 0 display.

The ROM-based diagnostics are a collection of individual tests with parameters that you can specify. A data structure called a script points to the tests (see Section 4.3.2). There are several field and manufacturing scripts.

A program called the diagnostic executive determines which of the available scripts to invoke. The script sequence varies if the system is in the manufacturing environment. The diagnostic executive interprets the script to determine what tests to run, the correct order to run the tests, and the correct parameters to use for each test.

The diagnostic executive also controls tests so that errors can be detected and reported. It ensures that when the tests are run, the machine is left in a consistent and well-defined state.

4.3.1 Diagnostic Tests

Example 4–3 shows a list of the ROM-based tests and utilities. To get this listing, enter T 9E at the console prompt (T is the abbreviation of TEST). The column headings have the following meanings:

<table>
<thead>
<tr>
<th>Note</th>
</tr>
</thead>
</table>

Base addresses shown in this document may not be the same as the addresses you see when you run T 9E. Run T 9E to get a list of actual addresses. See Example 4–3.
System Initialization and Acceptance Testing (Normal Operation)
4.3 CPU ROM-Based Diagnostics

- Test is the test number or utility code.
- Address is the base address of where the test or utility starts in ROM. If a test fails, entering T FE displays diagnostic state to the console. You can subtract the base address of the failing test from the last_exception_pc to find the index into the failing test's diagnostic listing.
- Name is a brief description of the test or utility.
- Parameters shows the parameters for each diagnostic test or utility. These parameters are encoded in ROM and are provided by the diagnostic executive. Tests accept up to 10 parameters. The asterisks (*) represent parameters that are used by the tests but that you cannot specify individually. These parameters are displayed in error messages, each one preceded by identifiers P1 through P10.
System Initialization and Acceptance Testing (Normal Operation)

4.3 CPU ROM-Based Diagnostics

Example 4–3  Test 9E

>>> Test 9E

<table>
<thead>
<tr>
<th>#</th>
<th>Address</th>
<th>Name</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>200531D0</td>
<td>SCB</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>20054028</td>
<td>De executive</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>200645A9</td>
<td>Memory_Init_Bitmap</td>
<td>*** mark_Hard_SBEs *****</td>
</tr>
<tr>
<td>31</td>
<td>200649C9</td>
<td>Memory_Setup_CSRs</td>
<td>*</td>
</tr>
<tr>
<td>32</td>
<td>20065288</td>
<td>NMC_registers</td>
<td>*</td>
</tr>
<tr>
<td>33</td>
<td>20065440</td>
<td>NMC_powerup</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>20050B60</td>
<td>SSC_ROM</td>
<td>*</td>
</tr>
<tr>
<td>35</td>
<td>200662F4</td>
<td>B_Cache_diag_mode</td>
<td>bypass_test_mask **</td>
</tr>
<tr>
<td>37</td>
<td>200691EC</td>
<td>Cache_w_Memory</td>
<td>bypass_test_mask **</td>
</tr>
<tr>
<td>40</td>
<td>200631F4</td>
<td>Memory_count_pages</td>
<td>*</td>
</tr>
<tr>
<td>41</td>
<td>200581F9</td>
<td>Board_Reset</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>20056E70</td>
<td>Chk_for_Interrupts</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>2006801C</td>
<td>P_Cache_diag_mode</td>
<td>bypass_test_mask **</td>
</tr>
<tr>
<td>47</td>
<td>200648B4</td>
<td>Memory_Refresh</td>
<td>start_a_end_incr_cont_on_err_time_seconds *****</td>
</tr>
<tr>
<td>48</td>
<td>200622E4</td>
<td>Memory_Addr_shorts</td>
<td>start_add_end_add * cont_on_err pat2 pat3 ***</td>
</tr>
<tr>
<td>4A</td>
<td>20062CB9</td>
<td>Memory_ECC_SBEs</td>
<td>start_add_end_add_add_incr_cont_on_err *****</td>
</tr>
<tr>
<td>4B</td>
<td>20062B24</td>
<td>Memory(Byte) Errors</td>
<td>start_add_end_add_incr_cont_on_err *****</td>
</tr>
<tr>
<td>4C</td>
<td>200630C0</td>
<td>Memory_ECC_Index</td>
<td>start_add_end_add_incr_cont_on_err *****</td>
</tr>
<tr>
<td>4D</td>
<td>20062A44</td>
<td>Memory_Address</td>
<td>start_add_end_add_incr_cont_on_err *****</td>
</tr>
<tr>
<td>4F</td>
<td>20062A0</td>
<td>Memory(Byte)</td>
<td>start_add_end_add_incr_cont_on_err *****</td>
</tr>
<tr>
<td>4F</td>
<td>200648DB</td>
<td>Memory_Data</td>
<td>start_add_end_add_incr_cont_on_err *****</td>
</tr>
<tr>
<td>51</td>
<td>2005C408</td>
<td>FPA</td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>20058C4</td>
<td>SSC_Prog timers</td>
<td>which_timer_wait_time_us ***</td>
</tr>
<tr>
<td>53</td>
<td>2005CBA</td>
<td>SSC TOY Clock</td>
<td>repeat_test_250ms_ea_Tolerance ***</td>
</tr>
<tr>
<td>54</td>
<td>2005C00</td>
<td>Virtual Mode</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>2005C07</td>
<td>Interval_Timer</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>20061060</td>
<td>SHAC_RESET</td>
<td>port_number_time_secs not_pres</td>
</tr>
<tr>
<td>59</td>
<td>20060AC</td>
<td>SHAC_LPBCK_ASSIST</td>
<td>time_secs **</td>
</tr>
<tr>
<td>5C</td>
<td>2006082C</td>
<td>SHAC</td>
<td></td>
</tr>
<tr>
<td>5F</td>
<td>2005525E</td>
<td>SSOC</td>
<td>loopback_type_no_ram_tests *****</td>
</tr>
<tr>
<td>63</td>
<td>2005D9C</td>
<td>QDSS any</td>
<td>input_csr_selftest_r0_selftest_r1 *****</td>
</tr>
<tr>
<td>80</td>
<td>20065B84</td>
<td>CBIC memory</td>
<td>bypass_test_mask *****</td>
</tr>
<tr>
<td>81</td>
<td>2005DD0</td>
<td>Qbus_MSCP</td>
<td>IP csr *****</td>
</tr>
<tr>
<td>82</td>
<td>20057AC</td>
<td>Qbus_DLOQA</td>
<td>device_num_addr ****</td>
</tr>
<tr>
<td>83</td>
<td>200597D0</td>
<td>QZA Intipback1</td>
<td>controller_number ********</td>
</tr>
<tr>
<td>84</td>
<td>2005AC74</td>
<td>QZA_intipback2</td>
<td>controller_number ********</td>
</tr>
<tr>
<td>85</td>
<td>200587C</td>
<td>QZA_memory</td>
<td>incr_test_pattern_controller_number ********</td>
</tr>
<tr>
<td>86</td>
<td>20058C74</td>
<td>QZA_TMA</td>
<td>Controller_number main_mem_buF *******</td>
</tr>
<tr>
<td>90</td>
<td>2005CB7C</td>
<td>CBIC_registers</td>
<td></td>
</tr>
<tr>
<td>91</td>
<td>2005C7AB</td>
<td>CBIC_powerup</td>
<td>**</td>
</tr>
<tr>
<td>99</td>
<td>20065A44</td>
<td>Flush_Cache</td>
<td>dis_flush_VIC dis_flush_BC dis_flush_PC</td>
</tr>
<tr>
<td>9A</td>
<td>20065CB4</td>
<td>INTERACTION</td>
<td>pass_count disable_device ****</td>
</tr>
<tr>
<td>9B</td>
<td>200654DC</td>
<td>init_memory</td>
<td></td>
</tr>
<tr>
<td>9C</td>
<td>2005D8B0</td>
<td>List_CPU_registers</td>
<td></td>
</tr>
<tr>
<td>9D</td>
<td>2005E686</td>
<td>Utility</td>
<td>Modify_CPU_type</td>
</tr>
<tr>
<td>9E</td>
<td>2005CB40</td>
<td>List_diagnostics</td>
<td>script_number</td>
</tr>
<tr>
<td>9F</td>
<td>20061610</td>
<td>Create A0_Script</td>
<td></td>
</tr>
</tbody>
</table>

(continued on next page)
System Initialization and Acceptance Testing (Normal Operation)

4.3 CPU ROM-Based Diagnostics

Example 4–3 (Cont.) Test 9E

C1 20058F88 SSC RAM Data *
C2 20058F8F SSC RAM Data Addr *
C5 20058F14 SSC registers *
C6 20058120 SSC_powerup ********
D0 2006BC8 V Cache diag mode bypass test_mask ********
D2 200660C8 O Bit diag mode bypass test_mask ********
DA 20068FFC PB Flush Cache *********
DB 200669D8 Speed print_speed ********
DC 200650C8 NO Memory present *
D0 20067118 H Cache Data debug start add end add addr incr ********
DF 20066C88 H Cache Tag Debug start add end add addr incr ********
DF 20066AFO O BIT DEBUG start add end add addr incr seq incr ******
K0 20069D8B SCSi environment reset bus time s ********
E1 20069D8B SCSi Utility environment util nbr target_ID lun ******
F2 20069F84 SCSi MAP bypass test addr incr_data last *******
E4 20069A60 DZ environment ********
E8 20069F80 SYNC environment ********
E9 200698C4 SCSi Utility environment ********
EC 20069DA8 ASYNC environment ********

Scripts
1 Description
A0 User defined scripts
A1 Powerup tests, Functional Verify, continue on error, numeric countdown
A2 Functional Verify, stop on error, test 1 announcements
A4 Loop on A3 Functional Verify
A6 Memory tests, mark only multiple bit errors
A7 Memory tests
A8 Memory acceptance tests, mark single and multi-bit errors, call A7
A9 Memory tests, stop on error
B2 Extended tests plus BP, then loop
B5 Extended tests, then loop
DF D4, SYNC, ASYNC with loopbacks

Load & start system exerciser
100 Customer mode, 2 passes
101 CSSF mode, 2 passes
102 CSSE mode, continuous until °C
103 Manuf mode, continuous until °C
104 Manuf TINA mode, continuous until °C
105 Manuf mode, 2 passes
106 CSSF mode, select tests, continuous until °C
107 Manuf mode, select tests, continuous until °C

User Determined Parameters
Parameters that you can specify are written out, as shown in the following examples:

30 2005C33C Memory_Init_Bitmap *** mark Hard_SBEs ******
54 20055181 Virtual_Mode **********
System Initialization and Acceptance Testing (Normal Operation)
4.3 CPU ROM-Based Diagnostics

For example, the virtual mode test contains several parameters, but you cannot specify any that appear in the table as asterisks. To run this test individually, enter:

>>>T 54

The MEM_bitmap test, for example, accepts 10 parameters, but you can only specify mark_hard_SBEs because the rest are asterisks. To map out solid, single-bit ECC memory errors, type:

>>>T 30 0 0 0 1

Even though you cannot change the first three parameters, you need to enter zeros (0) as placeholders. The zeros are placeholders for parameters 1 through 3, which allows the program to parse the command line correctly. The diagnostic executive then provides the proper value for the test.

You enter 1 for parameter 4 to indicate that the test should map out solid, single-bit as well as multibit ECC memory errors. You then terminate the command line by pressing [RETURN]. You do not need to specify parameters 5 through 10; placeholders are needed only for parameters that precede the user-definable parameter.

For the most part tests and scripts can be run without any special setup. If a test or script is run interactively without an intervening power up, such as after a system crash or shutdown, enter the UNJAM and INIT commands before running the tests or script. This will ensure that the CPU is in a well known state. If the commands are not entered, misleading errors may occur.

Other considerations to be aware of when running individual tests or scripts interactively:

- When using the TEST or REPEAT TEST commands, you must specify a test number, test code or script number following the TEST command before pressing [RETURN].

- The memory bitmap and Q-bus scatter-gather map are created in main memory and the memory tests are run with these data structures left intact. Therefore, the upper portion of memory should not be accessed to avoid corrupting these data structures. The location of the maps is displayed using the SHOW MEMORY/FULL command.
4.3.2 Scripts

Most of the tests shown by utility 9E are arranged into scripts. A script is a data structure that points to various tests and defines the order in which they are run. Scripts should be thought of as diagnostic tables—these tables do not contain the actual diagnostic tests themselves, instead scripts simply define what tests or scripts should be run, the order that the tests or scripts should be run, and any input parameters to be parsed by the Diagnostic Executive.

Different scripts can run the same set of tests, but these tests can be run in a different order and/or with different parameters and flags. A script also contains the following information:

- The parameters and flags that need to be passed to the test.
- The locations from which the tests can be run. For example, certain tests can be run only from the FEPROM. Other tests are program-independent code, and can be run from FEPROM or main memory to enhance execution speed.
- What is to be shown, if anything, on the console.
- What is to be shown, if anything, in the LED display.
- What action to take on errors (halt, repeat, continue).

The power-up script runs every time the system is powered on. You can also invoke the power-up script at any time by entering T0.

Additional scripts are included in the FEPROMs for use in manufacturing and engineering environments. Customer Services personnel can run these scripts and tests individually, using the T command. When doing so, note that certain tests may be dependent upon a state set up from a previous test. For this reason, use the UNJAM and INITIALIZE commands before running an individual test. You do not need these commands on system power-up because the system power-up leaves the machine in a defined state.

Customer Services Engineers (CSE) with a detailed knowledge of the system hardware and firmware can also create their own scripts by using the 9F User Script Utility. Table 4-2 lists the scripts available to Customer Services.
# System Initialization and Acceptance Testing (Normal Operation)
## 4.3 CPU ROM-Based Diagnostics

## Table 4–2 Scripts Available to Customer Services

<table>
<thead>
<tr>
<th>Script</th>
<th>Enter with TEST Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>A0</td>
<td>Runs user-defined script. Enter T 9F to create.</td>
</tr>
<tr>
<td>A1</td>
<td>A1, 0</td>
<td>Primary power-up script; builds memory bitmap; marks hard single-bit errors and multi-bit errors. Continues on error.</td>
</tr>
<tr>
<td>A3</td>
<td>A3, A4</td>
<td>Runs power-up tests, halts on first error.</td>
</tr>
<tr>
<td>A4</td>
<td>A4</td>
<td>Loops on A3. Press [Ctrl] C to exit.</td>
</tr>
<tr>
<td>A6</td>
<td>A6</td>
<td>Memory test script; initializes memory bitmap and marks only multiple bit errors.</td>
</tr>
<tr>
<td>A7</td>
<td>A7, A8</td>
<td>Memory test portion invoked by script A8. Reruns the memory tests without rebuilding and reinitializing the bitmap. Run script A8 once before running script A7 separately to allow mapping out of both single-bit and double-bit main memory ECC errors.</td>
</tr>
<tr>
<td>A8</td>
<td>A8</td>
<td>Memory acceptance. Running script A8 with script A7 tests main memory more extensively. It enables hard single-bit and multibit main memory ECC errors to be marked bad in the bitmap. Invokes script A7 when it has completed its tests.</td>
</tr>
<tr>
<td>A9</td>
<td>A9</td>
<td>Memory tests. Halts and reports the first error. Does not reset the bitmap or busmap. It is a quick way to specify which test caused a failure when a hard error is present.</td>
</tr>
<tr>
<td>AD</td>
<td>AD</td>
<td>Console program. Runs memory tests, marks bitmap, resets busmap, and resets caches. Calls script AE.</td>
</tr>
<tr>
<td>AE</td>
<td>AE, AD</td>
<td>Console program. Resets memory CSRs and resets caches. Also called by the INIT command.</td>
</tr>
<tr>
<td>AF</td>
<td>AF</td>
<td>Console program. Resets busmap and resets caches.</td>
</tr>
<tr>
<td>B2(^2)</td>
<td>B2</td>
<td>Runs extended tests, calls the BF script, then loops. Press [Ctrl] C to exit.</td>
</tr>
<tr>
<td>B5</td>
<td>B5</td>
<td>Runs extended tests, then loops. Press [Ctrl] C to exit.</td>
</tr>
<tr>
<td>BP(^2)</td>
<td>BF</td>
<td>Runs tests requiring loopback connectors for QUART, SYNC, and, ASYNC options if present. Press [Ctrl] C to exit.</td>
</tr>
</tbody>
</table>

\(^1\)Scripts AD, AE, and AF exist primarily for console program; error displays and progress messages are suppressed (not recommended for CSE use).  
\(^2\)B2 and BF require loopback connectors.
4.4 Basic Acceptance Test Procedure

Perform the acceptance testing procedure listed below, after installing a system, or whenever adding or replacing the following:

- CPU module
- MS44 memory SIMM
- SCSI device
- SYNC device
- ASYNC device

1. Run two error-free passes of the power-up scripts by entering the following command:

```plaintext
>>>T B5
```

Script B5 will halt on an error so that the error message will not scroll off the screen.

Press [CtrlC] to terminate the scripts. Refer to Chapter 5 if failures occur.

To check the memory configuration and to ensure there are no bad pages, enter the following command line:

```plaintext
>>>SHOW MEM/FULL
```

16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 00000000 to 00FFFFFF, 16MB, 32768 good pages, 0 bad pages
Total of 16MB, 32768 good pages, 0 bad pages, 104 reserved pages

Memory Bitmap
-00FF3000 to 00FF3FFF, 8 pages

Console Scratch Area
-00FF4000 to 00FF7FFF, 32 pages

Scan of Bad Pages

Q-bus Map
-01FF8000 to 01FFFFFF, 64 pages

Scan of Bad Pages

```plaintext
>>>
```

The Q22–bus map always spans the top 32 Kbytes of good memory. The memory bitmap always spans two pages (1 Kbyte) for each 4 Mbytes of memory configured. Each bit within the memory bit map represents a page of memory.

To identify registers and register bit fields, see the *KA50/51/55/56 CPU Technical Manual.*
System Initialization and Acceptance Testing (Normal Operation)

4.4 Basic Acceptance Test Procedure

Examine MEMCON 0–1 to verify the memory configuration. Each pair of MEMCONs maps one memory module as follows:

MEMCON0  Set 0; 0A, 0B, 0C, 0D
MEMCON1  Set 1; 1E, 1F, 1G, 1H

4.5 Machine State on Power-Up

This section describes the state of the kernel after a power-up halt.

The descriptions in this section assume the system has just powered-up and the power-up diagnostics have successfully completed. The state of the machine is not defined if individual diagnostics are run or for any other halts other than a power-up halt (SAVPSL<13:8>(RESTART_CODE) = 3). Refer to Appendix D for a description of the normal state of CPU configurable bits following completion of power-up tests.

4.6 Main Memory Layout and State

Main memory is tested and initialized by the firmware on power-up.
Figure 4–2 is a diagram of how main memory is partitioned after diagnostics.
4.6.1 Reserved Main Memory

In order to build the scatter/gather map and the bitmap, the firmware attempts to find a physically contiguous page-aligned 1M byte block of memory at the highest address possible.

Of the 1M byte, the upper 32 KB is dedicated to the Q22–bus scatter/gather map, as shown in Figure 4–2. Of the lower portion, up to 32K bytes at the bottom of the block is allocated to the Page Frame Number (PFN) bitmap. The size of the PFN bitmap is dependent on the extent of physical memory. Each bit in the bitmap maps one page (512 bytes) of memory. The remainder of the block between the bitmap and scatter/gather map (minimally 16 KB) is allocated for the firmware.

4.6.1.1 PFN Bitmap

The PFN bitmap is a data structure that indicates which pages in memory are deemed usable by operating systems. The bitmap is built by the diagnostics as a side effect of the memory tests on power-up. The bitmap always starts on a page boundary. The bitmap requires 1 KB for every 4 MB of main memory, hence, a 8 MB system requires 2 KB, 16 MB requires 4 KB, 32 MB requires 8 KB, and a 64 MB requires 16 KB. There may be memory above the bitmap which has both good and bad pages.
System Initialization and Acceptance Testing (Normal Operation)
4.6 Main Memory Layout and State

Each bit in the PFN bitmap corresponds to a page in main memory. There is a one to one correspondence between a page frame number (origin 0) and a bit index in the bitmap. A one in the bitmap indicates that the page is "good" and can be used. A zero indicates that the page is "bad" and should not be used.

The PFN bitmap is protected by a checksum stored in the NVRAM. The checksum is a simple byte wide, two's complement checksum. The sum of all bytes in the bitmap and the bitmap checksum should result in zero.

4.6.1.2 Scatter/Gather Map
On power-up, the scatter/gather map is initialized by the firmware to map to the first 4M bytes of main memory. Main memory pages will not be mapped if there is a corresponding page in Q22–bus memory.

On a processor halt other than power-up, the contents of the scatter/gather map is undefined, and is dependent on operating system usage.

Operating systems should not move the location of the scatter/gather map, and should access the map only on aligned longwords through the local I/O space of 20088000 to 2008FFFF, inclusive. The Q22–bus map base register (QMBR), is set up by the firmware to point to this area, and should not be changed by software.

4.6.1.3 Firmware "Scratch Memory"
This section of memory is reserved for the firmware. However, it is only used after successful execution of the memory diagnostics and initialization of the PFN bitmap and scatter/gather map. This memory is primarily used for diagnostic purposes.

4.6.2 Contents of Main Memory
The contents of main memory are undefined after the diagnostics have run. Typically, nonzero test patterns will be left in memory.

The diagnostics will "scrub" all of main memory, so that no power-up induced errors remain in the memory system. On the KA50/51/55/56 memory subsystem, the state of the ECC bits and the data bits are undefined on initial power-up. This can result in single and multiple bit errors if the locations are read before written, because the ECC bits are not in agreement with their corresponding data bits. An aligned longword write to every location (done by diagnostics) eliminates all power-up induced errors.
4.6.3 Memory Controller Registers

The SHOW MEMORY command defines the mapping of addresses to specific SIMM sets as follows:

- MEMCON0 is used with SIMM bank 0 (the 0A, 0B, 0C, and 0D memory slots)
- MEMCON1 is used with SIMM bank 1 (the 1E, 1F, 1G, and 1H memory slots)

Additional information should be captured from the NMCDSR, MOAMR, MSER, and MEAR as needed.

4.6.4 On-Chip and Backup Caches

All three caches are tested.

4.6.5 Translation Buffer

The CPU translation buffer is tested by diagnostics on power-up, but not used by the firmware because it runs in physical mode. The translation buffer can be invalidated by using PR$_{TBIA}$, IPR 57.

4.6.6 Halt-Protected Space

On the KA50/51/55/56, halt-protected space spans the first half of the 512K byte FEPROM from 20040000 to 2007FFFF. The second half of the FEPROM has data which is loaded into memory and run.

The firmware always runs in halt-protected space. When passing control to the bootstrap, the firmware exits the halt-protected space, so if halts are enabled, and the halt line is asserted, the processor will then halt before booting.

4.7 Operating System Bootstrap

Bootstrapping is the process by which an operating system loads and assumes control of the system. The KA50/51/55/56 supports bootstrap of the VAX/OpenVMS and VAXELN operating systems. Additionally, the KA50/51/55 will boot MDM diagnostics and any user application image which conforms to the boot formats described herein.

On the KA50/51/55/56 a bootstrap occurs whenever a BOOT command is issued at the console or whenever the processor halts and the conditions specified in Table G–1 for automatic bootstrap are satisfied.
4.7 Operating System Bootstrap

4.7.1 Preparing for the Bootstrap

Prior to dispatching to the primary bootstrap (VMB), the firmware initializes the system to a known state. The initialization sequence follows:

1. Check the console program mailbox "bootstrap in progress" bit (CPMBX<2>(BIP)). If it is set, bootstrap fails.

2. If this is an automatic bootstrap, display the message "Loading system software." on the console terminal.

3. Set CPMBX<2>(BIP).

4. Validate the Page Frame Number (PFN) bitmap. If PFN bitmap checksum is invalid, then:
   a. Perform an UNJAM.
   b. Perform an INIT.
   c. Retest memory and rebuild PFN bitmap.

5. Validate the boot device name. If none exists, supply a list of available devices and prompt user for a device. If no device is entered within 30 seconds, use EZA0.

6. Write a form of this BOOT request including the active boot flags and boot device on the console, for example "(BOOT/R5:0 DU0)".

7. Initialize the Q22-bus scatter/gather map.
   a. Set IPCR<8>(AUX_HLT).
   b. Clear IPCR<5>(LMEAE).
   c. Perform an UNJAM.
   d. Perform an INIT.
   e. If an arbiter, map all vacant Q22-bus pages to the corresponding page in local memory and validate each entry if that page is "good".
   f. Set IPCR<5>(LMEAE).

8. Search for a 128K byte contiguous block of good memory as defined by the PFN bitmap. If 128K bytes cannot be found, the bootstrap fails.

9. Initialize the general purpose registers as follows:
System Initialization and Acceptance Testing (Normal Operation)

4.7 Operating System Bootstrap

R0          Address of descriptor of boot device name; 0 if none specified
R2          Length of PFN bitmap in bytes
R3          Address of PFN bitmap
R4          Time-of-day of bootstrap from PR$_$TODR
R5          Boot flags
R10         Halt PC value
R11         Halt PSL value (without halt code and map enable)
AP          Halt code
SP          Base of 128-Kbyte good memory block + 512
PC          Base of 128-Kbyte good memory block + 512
R1, R6, R7, R8, R9, FP 0

10. Copy the VMB image from FEPROM to local memory beginning at the base of the 128 KB good memory block + 512.

11. Exit from the firmware to memory resident VMB.
On entry to VMB the processor is running at IPL 31 on the interrupt stack with memory management disabled. Also, local memory is partitioned as shown in Figure 4–3.
4.7.2 Primary Bootstrap Procedures (VMB)

Virtual Memory Boot (VMB) is the primary bootstrap for booting VAX processors. On the KA50/51/55/56 module, VMB is resident in the firmware and is copied into main memory before control is transferred to it. VMB then loads the secondary bootstrap image and transfers control to it.

In certain cases, such as VAXELN, VMB actually loads the operating system directly. However, for the purpose of this discussion "secondary bootstrap" refers to any VMB loadable image.
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstrap

VMB inherits a well defined environment and is responsible for further initialization. The following summarizes the operation of VMB.

1. Initialize a two-page SCB on the first-page boundary above VMB.
2. Allocate a three-page stack above the SCB.
3. Initialize the Restart Parameter Block (RPB).
4. Initialize the secondary bootstrap argument list.
5. If not a PROM boot, locate a minimum of three consecutive valid QMRs.
6. Write "2" to the diagnostic LEDs and display "2.." on the console to indicate that VMB is searching for the device.
7. Optionally, solicit from the console a "Bootfile: " name.
8. Write the name of the boot device from which VMB will attempt to boot on the console, for example, "-DIA0".
9. Copy the secondary bootstrap from the boot device into local memory above the stack. If this fails, the bootstrap fails.
10. Write "1" to the diagnostic LEDs and display "1.." on the console to indicate that VMB has found the secondary bootstrap image on the boot device and has loaded the image into local memory.
11. Clear CPMBX<2>(BIP) and CPMBX<3>(RIP).
12. Write "0" to the diagnostic LEDs and display "0.." on the console to indicate that VMB is now transferring control to the loaded image.
13. Transfer control to the loaded image with the following register usage.

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>R5</td>
<td>Transfer address in secondary bootstrap image</td>
</tr>
<tr>
<td>R10</td>
<td>Base address of secondary bootstrap memory</td>
</tr>
<tr>
<td>R11</td>
<td>Base address of RPB</td>
</tr>
<tr>
<td>AP</td>
<td>Base address of secondary boot parameter block</td>
</tr>
<tr>
<td>SP</td>
<td>Base address of secondary boot parameter block</td>
</tr>
</tbody>
</table>
In the event that an operating system has an extraordinarily large secondary bootstrap which overflows the 128 KB of "good" memory, VMB loads the remainder of the image in memory above the "good" block. However, if there are not enough contiguous "good" pages above the block to load the remainder of the image, the bootstrap fails.
4.7.3 Device Dependent Secondary Bootstrap Procedures

The following sections describe the various device dependent boot procedures.

4.7.3.1 Disk and Tape Bootstrap Procedure

The disk and tape bootstrap supports Files–11 lookup (supporting only the ODS level 2 file structure) or the boot block mechanism (used in PROM boot also). Of the standard DEC operating systems, OpenVMS and ELN use the Files–11 bootstrap procedure, and Ultrix-32 uses the boot block mechanism.

VMB first attempts a Files–11 lookup, unless the RPBUVBBLOCK boot flag is set. If VMB determines that the designated boot disk is a Files–11 volume, it searches the volume for the designated boot program, usually [SYS0.SYSEX]SYSBOOT.EXE. However, VMB can request a diagnostic image or prompt the user for an alternate file specification. If the boot image cannot be found, VMB fails.

If the volume is not a Files–11 volume or the RPBUVBBLOCK boot flag was set, the boot block mechanism proceeds as follows:

1. Read logical block 0 of the selected boot device (this is the boot block).
2. Validate that the contents of the boot block conform to the boot block format (see below).
3. Use the boot block to find and read in the secondary bootstrap.
4. Transfer control to the secondary bootstrap image, just as for a Files–11 boot.

The format of the boot block must conform to that shown in Figure 4–5.
Figure 4-5  Boot Block Format

<table>
<thead>
<tr>
<th></th>
<th>31</th>
<th>24</th>
<th>23</th>
<th>16</th>
<th>15</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BB-0:</td>
<td>1</td>
<td>n</td>
<td>any value</td>
<td>low LBN</td>
<td>high LBN</td>
<td></td>
</tr>
</tbody>
</table>

(The next segment is also used as a PROM "signature block.")

<table>
<thead>
<tr>
<th></th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BB+(2*n)+0:</td>
<td>CHK</td>
</tr>
</tbody>
</table>

any value, most likely 0

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>BB+(2*n)+8:</td>
<td>size in blocks of the image</td>
</tr>
</tbody>
</table>

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>BB+(2*n)+12:</td>
<td>load offset</td>
</tr>
</tbody>
</table>

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>BB+(2*n)+16:</td>
<td>offset into image to start</td>
</tr>
</tbody>
</table>

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>BB+(2*n)+20:</td>
<td>sum of the previous three longwords</td>
</tr>
</tbody>
</table>

Where:
1) the 18 (hex) indicates this is a VAX instruction set
2) 18 (hex) + "k" = the one's complement if "CHK"

4.7.3.2 MOP Ethernet Functions and Network Bootstrap Procedure

Whenever a network bootstrap is selected on the KA50/51/55/56, the VMB code makes continuous attempts to boot from the network. VMB uses the DNA Maintenance Operations Protocol (MOP) as the transport protocol for network bootstraps and other network operations. Once a network boot has been invoked, VMB turns on the designated network link and repeats load attempt, until either a successful boot occurs, a fatal controller error occurs, or VMB is halted from the operator console.

The KA50/51/55/56 supports the load of a standard operating system, a diagnostic image, or a user-designated program via network bootstraps. The default image is the standard operating system, however, a user may select an alternate image by setting either the RPB$V_DIAG bit or the RPB$V_SOLICIT bit in the boot flag longword R5. Note that the RPB$V_SOLICIT bit has precedence over the RPB$V_DIAG bit. Hence, if both bits are set, then the solicited file is requested.
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstrap

Note

VMB accepts a maximum 39 characters for a file specification for solicited boots. However, MOP V3 only supports a 15-character file name. If the network server is running the OpenVMS operating system, the following defaults apply to the file specification: the directory MOM$LOAD:, and the extension .SYS. Therefore, the file specification need only consist of the filename if the default directory and extension attributes are used.

The KA50/51/55/56 VMB uses the MOP program load sequence for bootstrapping the module and the MOP "dump/load" protocol type for load related message exchanges. The types of MOP message used in the exchange are listed in Table 4–3 and Table 4–4.
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstrap

Table 4-3  Network Maintenance Operations Summary

<table>
<thead>
<tr>
<th>Function</th>
<th>Role</th>
<th>Transmit</th>
<th>Receive</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MOP Ethernet and IEEE 802.3 Messages&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>Dump</td>
<td>Requester</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Server</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Load</td>
<td>Requester</td>
<td>REQ PROGRAM&lt;sup&gt;2&lt;/sup&gt;</td>
<td>VOLUNTEER</td>
</tr>
<tr>
<td></td>
<td></td>
<td>to solicit</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>REQ_MEM_LOAD</td>
<td>MEM_LOAD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>to solicit &amp; ACK</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>or</td>
<td>MEM_LOAD_w_XFER</td>
</tr>
<tr>
<td></td>
<td></td>
<td>or</td>
<td>PARAM_LOAD_w_XFER</td>
</tr>
<tr>
<td>Server</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Console</td>
<td>Requester</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Server</td>
<td>COUNTERS</td>
<td>REQ_COUNTERS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>in response to</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYSTEM_ID&lt;sup&gt;3&lt;/sup&gt;</td>
<td>REQUEST_ID</td>
</tr>
<tr>
<td></td>
<td></td>
<td>in response to</td>
<td>BOOT</td>
</tr>
<tr>
<td>Loopback</td>
<td>Requester</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Server</td>
<td>LOOPED_DATA&lt;sup&gt;4&lt;/sup&gt;</td>
<td>LOOP_DATA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>in response to</td>
<td></td>
</tr>
</tbody>
</table>

IEEE 802.3 Messages<sup>5</sup>

<table>
<thead>
<tr>
<th>Function</th>
<th>Role</th>
<th>Transmit</th>
<th>Receive</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Exchange</td>
<td>Requester</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>ID</td>
<td>Server</td>
<td>XID_RSP</td>
<td>in response to</td>
<td>XID_CMD</td>
</tr>
<tr>
<td>Test</td>
<td>Requester</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

<sup>1</sup>All unsolicited messages are sent in Ethernet (MOP V3) and IEEE 802.2 (MOP V4), until the MOP version of the server is known. All solicited messages are sent in the format used for the request.

<sup>2</sup>The initial REQ_PROGRAM message is sent to the dumpload multicast address. If an assistance VOLUNTEER message is received, then the responder's address is used as the destination to repeat the REQ_PROGRAM message and for all subsequent REQ_MEM_LOAD messages.

<sup>3</sup>SYSTEM_ID messages are sent out every 8 to 12 minutes to the remote console multicast address and, on receipt of a REQUEST_ID message, they are sent to the initiator.

<sup>4</sup>LOOPED_DATA messages are sent out in response to LOOP_DATA messages. These messages are actually in Ethernet LOOP TEST format, not in MOP format, and when sent in Ethernet frames, omit the additional length field (padding is disabled).

<sup>5</sup>IEEE 802.2 support of XID and TEST is limited to Class 1 operations.

(continued on next page)
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstrap

Table 4–3 (Cont.)  Network Maintenance Operations Summary

<table>
<thead>
<tr>
<th>Function</th>
<th>Role</th>
<th>Transmit</th>
<th>Receive</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>IEEE 802.3 Messages$^5$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Server</td>
<td>TEST_RSP in response to TEST_CMD</td>
</tr>
</tbody>
</table>

$^5$IEEE 802.2 support of XID and TEST is limited to Class 1 operations.

Table 4–4  Supported MOP Messages

<table>
<thead>
<tr>
<th>Message Type</th>
<th>Message Fields</th>
</tr>
</thead>
<tbody>
<tr>
<td>DUMP/LOAD</td>
<td></td>
</tr>
<tr>
<td>MEM_LOAD_w_ XFER</td>
<td>Code 00, Load # nn, Load addr aa-aa-aa-aa, Image data None, Xfer addr aa-aa-aa-aa</td>
</tr>
<tr>
<td>MEM_LOAD</td>
<td>Code 02, Load # nn, Load addr aa-aa-aa-aa, Image data dd-...</td>
</tr>
<tr>
<td>REQ_PROGRAM</td>
<td>Code 08, Device 25 LQA 49 SGEC, Format 01 V3 04 V4, Program 02 Sys, SW ID$^3$ C-17$^1$, Processor C-128$^2$, Info 00 Sys (see SYSTEM_ID)</td>
</tr>
<tr>
<td>REQ_MEM_LOAD</td>
<td>Code 0A, Load # nn, Error ee</td>
</tr>
</tbody>
</table>

$^1$MOP V3.0 only.
$^2$MOP v4.0 only.
$^3$Software ID field is loaded from the string stored in the 40-byte field, RPBT_FILE, of the RPB on a solicited boot.

(continued on next page)
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstrap

Table 4-4 (Cont.)  Supported MOP Messages

<table>
<thead>
<tr>
<th>Message Type</th>
<th>Message Fields</th>
<th>DUMP/LOAD</th>
</tr>
</thead>
<tbody>
<tr>
<td>PARM_LOAD_w_</td>
<td>Code 14</td>
<td>Load # nn</td>
</tr>
<tr>
<td>XFER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOLUNTEER</td>
<td>Code 03</td>
<td></td>
</tr>
<tr>
<td>REQUEST_ID</td>
<td>Code 05</td>
<td>Rsvd xx</td>
</tr>
<tr>
<td>SYSTEM_ID</td>
<td>Code 07</td>
<td>Rsvd xx</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RECV_COUNTERS</td>
<td>Code 09</td>
<td>Recpt # nn-nn</td>
</tr>
<tr>
<td>COUNTERS</td>
<td>Code 0B</td>
<td>Recpt # nn-nn</td>
</tr>
<tr>
<td>BOOT ⁴</td>
<td>Code 06</td>
<td>Verifi ca tion vv-vv</td>
</tr>
</tbody>
</table>

¹MOP V3.0 only.
²MOP x4.0 only.
³Software ID field is loaded from the string stored in the 40-byte field, RPB$T_FILE, of the RPB on a solicited boot.
⁴A BOOT message is not verified, because in this context, a boot is already in progress. However, a received BOOT message will cause the boot backoff timer to be reset to its minimum value.

(continued on next page)
Table 4-4 (Cont.) Supported MOP Messages

<table>
<thead>
<tr>
<th>Message Type</th>
<th>Message Fields</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOOPBACK</td>
<td></td>
</tr>
<tr>
<td>LOOP_DATA</td>
<td>Skpcnt</td>
</tr>
<tr>
<td></td>
<td>Skipped bytes</td>
</tr>
<tr>
<td></td>
<td>bb-...</td>
</tr>
<tr>
<td></td>
<td>nn-nn</td>
</tr>
<tr>
<td></td>
<td>Function 00-02</td>
</tr>
<tr>
<td></td>
<td>Forward addr</td>
</tr>
<tr>
<td></td>
<td>Data ee-ee-</td>
</tr>
<tr>
<td></td>
<td>ee-ee-</td>
</tr>
<tr>
<td></td>
<td>Data ee-ee</td>
</tr>
<tr>
<td>LOOPED_DATA</td>
<td>Skpcnt</td>
</tr>
<tr>
<td></td>
<td>Skipped bytes</td>
</tr>
<tr>
<td></td>
<td>bb-...</td>
</tr>
<tr>
<td></td>
<td>nn-nn</td>
</tr>
<tr>
<td></td>
<td>Function 00-01</td>
</tr>
<tr>
<td></td>
<td>Reply</td>
</tr>
<tr>
<td></td>
<td>Recpt # nn-nn</td>
</tr>
<tr>
<td></td>
<td>Data dd-...</td>
</tr>
</tbody>
</table>

IEEE 802.2

<table>
<thead>
<tr>
<th>XID_CMD/RSP</th>
<th>Form</th>
<th>Class</th>
<th>Rx window size (K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>81</td>
<td>01</td>
<td>00</td>
<td></td>
</tr>
</tbody>
</table>

| TEST_CMD/RSP   | Optional data |

VMB, the requester, starts by sending a REQ_PROGRAM message to the MOP 'dump/load' multicast address. It then waits for a response in the form of a VOLUNTEER message from another node on the network, the MOP server. If a response is received, then the destination address is changed from the multicast address to the node address of the server and the same REQ_PROGRAM message is retransmitted to the server as an Acknowledge.

Next, VMB begins sending REQ_MEM_LOAD messages to the server. The server responds with either:

- MEM_LOAD message, while there is still more to load.
- MEM_LOAD_w_XFER, if it is the end of the image.
- PARAM_LOAD_w_XFER, if it is the end of the image and operating system parameters are required.

The "load number" field in the load messages is used to synchronize the load sequence. At the beginning of the exchange, both the requester and server initialize the load number. The requester only increments the load number if a load packet has been successfully received and loaded. This forms the Acknowledge to each exchange. The server will resend a packet with a specific load number, until it sees the load number incremented. The final Acknowledge is sent by the requester and has a load number equivalent to the load number of the appropriate LOAD_w_XFER message + 1.
4.7 Operating System Bootstrap

Because the request for load assistance is a MOP "must transact" operation, the network bootstrap continues indefinitely until a volunteer is found. The REQ_PROGRAM message is sent out in bursts of eight at four second intervals, the first four in MOP Version four IEEE 802.3 format and the last four in MOP Version 3 Ethernet format. The backoff period between bursts doubles each cycle from an initial value of four seconds, to eight seconds,... up to a maximum of five minutes. However, to reduce the likelihood of many nodes posting requests in lock-step, a random "jitter" is applied to the backoff period. The actual backoff time is computed as \( (.75 + (.5 \times \text{RND}(x))) \times \text{BACKOFF} \), where \( 0 \leq x < 1 \).

4.7.3.3 Network "Listening"

While the CPU module is waiting for a load volunteer during bootstrap, it "listens" on the network for other maintenance messages directed to the node and periodically identifies itself at the end of each 8- to 12-minute interval before a bootstrap retry. In particular, this "listener" supplements the Maintenance Operation Protocol (MOP) functions of the VMB load requester typically found in bootstrap firmware and supports:

- A remote console server that generates COUNTERS messages in response to REQ_COUNTERS messages, unsolicited SYSTEM_ID messages every 8 to 12 minutes, and solicited SYSTEM_ID messages in response to REQUEST_ID messages, as well as recognition of BOOT messages.

- A loopback server that responds to Ethernet loopback messages by echoing the message to the requester.

- An IEEE 802.2 responder that replies to both XID and TEST messages.

During network bootstrap operation, the KA50/51/55/56 complies with the requirements defined in the "NI Node Architecture Specification" for a primitive node. The firmware listens only to MOP "Load/Dump", MOP "Remote Console", Ethernet "Loopback Assistance", and IEEE 802.3 XID/TEST messages (listed in Table 4–5) directed to the Ethernet physical address of the node. All other Ethernet protocols are filtered by the network device driver.

The MOP functions and message types, which are supported by the KA50/51/55/56, are summarized in Tables 4–3 and 4–5.
### 4.7 Operating System Bootstrap

#### Table 4–5  MOP Multicast Addresses and Protocol Specifiers

<table>
<thead>
<tr>
<th>Function</th>
<th>Address</th>
<th>IEEE Prefix(^1)</th>
<th>Protocol</th>
<th>Owner</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dump/Load</td>
<td>AB-00-00-01-00-00</td>
<td>08-00-2B</td>
<td>60-01</td>
<td>Digital</td>
</tr>
<tr>
<td>Remote console</td>
<td>AB-00-00-02-00-00</td>
<td>08-00-2B</td>
<td>60-02</td>
<td>Digital</td>
</tr>
<tr>
<td>Loopback assistance</td>
<td>CF-00-00-00-00-00(^2)</td>
<td>08-00-2B</td>
<td>90-00</td>
<td>Digital</td>
</tr>
</tbody>
</table>

\(^1\)MOP V4.0 only.  
\(^2\)Not used.

### 4.8 Operating System Restart

An operating system restart is the process of bringing up the operating system from a known initialization state following a processor halt. This procedure is often called restart or warmstart, and should not be confused with a processor restart which results in firmware entry.

On the KA50/51/55/56, a restart occurs if the conditions specified in Table G–1 are satisfied.

To restart a halted operating system, the firmware searches system memory for the Restart Parameter Block (RPB), a data structure constructed for this purpose by VMB. (Refer to Table C–2 in Appendix C for a detailed description of this data structure.) If a valid RPB is found, the firmware passes control to the operating system at an address specified in the RPB.

The firmware keeps a "restart in progress" (RIP) flag in CPMBX which it uses to avoid repeated attempts to restart a failing operating system. An additional "restart in progress" flag is maintained by the operating system in the RPB.

The firmware uses the following algorithm to restart the operating system:

1. Check CPMBX<3>(RIP). If it is set, restart fails.
2. Print the message "Restarting system software." on the console terminal.
3. Set CPMBX<3>(RIP).
4. Search for a valid RPB. If none is found, restart fails.
5. Check the operating system $RPB\_RSTRTFLG<0>(RIP)$ flag. If it is set, restart fails.
6. Write "0" on the diagnostic LEDs.
System Initialization and Acceptance Testing (Normal Operation)

4.8 Operating System Restart

7. Dispatch to the restart address, RPB$L_RESTART, with:

<table>
<thead>
<tr>
<th>SP</th>
<th>Physical address of the RPB plus 512</th>
</tr>
</thead>
<tbody>
<tr>
<td>AP</td>
<td>Halt code</td>
</tr>
<tr>
<td>PSL</td>
<td>041F0000</td>
</tr>
<tr>
<td>PR$_MAPEN</td>
<td>0</td>
</tr>
</tbody>
</table>

If the restart is successful, the operating system must clear CPMBX<3>(RIP).
If restart fails, the firmware prints "Restart failure." on the system console.

4.8.1 Locating the RPB

The RPB is a page-aligned control block which can be identified by the first three longwords. The format of the RPB "signature" is shown in Figure 4-6. (Refer to Table C-2 in Appendix C for a complete description of the RPB.)

Figure 4-6 Locating the Restart Parameter Block

<table>
<thead>
<tr>
<th>RPB: +00</th>
<th>physical address of the RPB</th>
</tr>
</thead>
<tbody>
<tr>
<td>+04</td>
<td>physical address of the restart routine</td>
</tr>
<tr>
<td>+08</td>
<td>checksum of first 31 longwords of restart routine</td>
</tr>
</tbody>
</table>

The firmware uses the following algorithm to find a valid RPB:

1. Search for a page of memory that contains its address in the first longword. If none is found, the search for a valid RPB has failed.

2. Read the second longword in the page (the physical address of the restart routine). If it is not a valid physical address, or if it is zero, return to step 1. The check for zero is necessary to ensure that a page of zeros does not pass the test for a valid RPB.

3. Calculate the 32 bit twos-complement sum (ignoring overflows) of the first 31 longwords of the restart routine. If the sum does not match the third longword of the RPB, return to step 1.

4. A valid RPB has been found.
5

System Troubleshooting and Diagnostics

This chapter provides troubleshooting information for the two primary diagnostic methods: online, interpreting error logs to isolate the FRU; and offline, interpreting ROM-based diagnostic messages to isolate the FRU.

In addition, the chapter provides information on using MOP Ethernet functions to isolate errors, and interpreting UETP failures.

The chapter concludes with a section on running loopback tests to test the console port and embedded Ethernet ports.

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95, and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q-bus and DSSI, may appear on the console and/or printouts from time to time.

5.1 Basic Troubleshooting Flow

Before troubleshooting any system problem, check the site maintenance log for the system's service history. Be sure to ask the system manager the following questions:

- Has the system been used before and did it work correctly?
- Have changes (changes to hardware, updates to firmware or software) been made to the system recently?
- What is the state of the system—is it on line or off line?

If the system is off line and you are not able to bring it up, use the offline diagnostic tools, such as RBDs, MDM, and LEDs.
System Troubleshooting and Diagnostics
5.1 Basic Troubleshooting Flow

If the system is on line, use the online diagnostic tools, such as error logs, crash dumps, UETP, and other log files.

Four common problems occur when you make a change to the system:

- Incorrect cabling
- Module configuration errors (incorrect CSR addresses and interrupt vectors)
- Incorrect grant continuity
- Incorrect bus node ID plugs

In addition, check the following:

- If you have received error notification using VAXsimPLUS, check the mail messages and error logs as described in Section 5.2.
- If the operating system fails to boot (or appears to fail), check the console terminal screen for an error message. If the terminal displays an error message, see Section 5.3.
- Check the LEDs on the device you suspect is bad. If no errors are indicated by the device LEDs, run the ROM-based diagnostics described in this chapter.
- If the system boots successfully, but a device seems to fail or an intermittent failure occurs, check the error log ([SYSERR]ERRLOG.SYS) as described in Section 5.2.
- For fatal errors, check that the crash dump file exists for further analysis ([SYSEX]SYSDUMP.DMP).
- Check other log files, such as OPERATOR.LOG, OPCOM.LOG, SETHOST.LOG, etc. Many of these can be found in the [SYSMGR] account. SETHOST.LOG is useful in comparing the console output with event logs and crash dumps in order to see what the system was doing at the time of the error.

Use the following command to create SETHOST.LOG files, then log into the system account.

```
$ SET HOST/LOG 0
```

After logging out this file will reside in the [SYSMGR] account.

If the system is failing in the boot or start-up phase, it may be useful to include the command SET VERIFY in the front of various start-up .COM files to obtain a trace of the start-up commands and procedures.
When troubleshooting, note the status of cables and connectors before you perform each step. Label cables before you disconnect them. This step saves you time and prevents you from introducing new problems.

Most communications modules use floating CSR addresses and interrupt vectors. If you remove a module from the system, you may have to change the addresses and vectors of other modules.

If you change the system configuration, run the CONFIGURE utility at the console I/O prompt (>>>) to determine the CSR addresses and interrupt vectors recommended by Digital.

5.2 Product Fault Management and Symptom-Directed Diagnosis

This section describes how errors are handled by the microcode and software, how the errors are logged, and how, through the Symptom-Directed Diagnosis (SDD) tool, VAXsimPLUS, errors are brought to the attention of the user. This section also provides the service theory used to interpret error logs to isolate the FRU. Interpreting error logs to isolate the FRU is the primary method of diagnosis.

5.2.1 General Exception and Interrupt Handling

This section describes the first step of error notification: the errors are first handled by the microcode and then are dispatched to the OpenVMS error handler.

The kernel uses the NVAX core chipset: NVAX CPU, NVAX Memory Controller (NMC), and NDAL to CDAL adapter (NCA).

Internal errors within the NVAX CPU result in machine check exceptions, through System Control Block (SCB) vector 004, or soft error interrupts at Interrupt Priority Level (IPL) 1A, SCB vector 054 hex.

External errors to the NVAX CPU, which are detected by the NMC or NDAL to CDAL adapter (NCA), usually result in these chips posting an error condition to the NVAX CPU. The NVAX CPU will then generate a machine check exception through SCB vector 004, hard error interrupt, IPL 1D, through SCB vector 060 (hex), or a soft error interrupt through SCB vector 054.

External errors to the NMC and NCA, which are detected by chips on the CDAL busses for transactions which originated by the NVAX CPU, are typically signaled back to the NCA adapter. The NCA adapter will post an error signal back to the NVAX CPU which generates a machine check or high level interrupt.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

In the case of Direct Memory Access (DMA) transactions where the NCA or NMC detects the error, the errors are typically signaled back to the CDAL-Bus device, but not posted to the NVAX CPU. In these cases the CDAL-Bus device typically posts a device level interrupt to the NVAX CPU via the NCA. In almost all cases, error state is latched by the NMC and NCA. Although these errors will not result in a machine check exception or high level interrupt (i.e. results in device level IPL 14–17 versus error level IPL 1A, 1D), the OpenVMS machine check handler has a polling routine that will search for this state at one-second intervals. This will result in the host logging a polled error entry.

These conditions cover all of the cases that will eventually be handled by the OpenVMS error handler. The OpenVMS error handler will generate entries that correspond to the machine check exception, hard or soft error interrupt type, or polled error.

5.2.2 OpenVMS Error Handling

Upon detection of a machine check exception, hard error interrupt, soft error interrupt or polled error, the OpenVMS operating system will perform the following actions:

- Snapshot the state of the kernel.
- In most entry points, disable the caches.
- If it is a machine check and if the machine check is recoverable, determine if instruction retry is possible.

Instruction retry is possible if one of the following conditions is true:

- If PCSTS <10>PTE_ER = 0:
  - Check that (ISTATE2 <07>VR = 1) or (PSL <27> FPD = 1)
  - Otherwise crash the system or process depending on PSL <25:24> Current Mode.

- If PCSTS <10>PTE_ER = 1:
  - Check that (ISTATE2 <07>VR = 1) and (PSL <27> FPD = 0) and (PCSTS <09>PTE_ER_WR = 0)
  - Otherwise crash the system.

ISTATE2 is a longword in the machine check stack frame at offset (SP)+24; PSL is a longword in the machine check stack frame at offset (SP)+32; VR is the VAX Restart flag; and FPD is the First Part Done flag.

- Check to see if the threshold has been exceeded for various errors (typically the threshold is exceeded if 3 errors occur within a 10 minute interval).
System Troubleshooting and Diagnostics

5.2 Product Fault Management and Symptom-Directed Diagnosis

- If the threshold has been exceeded for a particular type of cache error, mark a flag that will signify that this resource is to be disabled (the cache will be disabled in most, but not all, cases).

- Update the SYSTAT software register with results of error/fault handling.

- For memory uncorrectable Error Correction Code (ECC) errors:
  - If machine check, mark page bad and attempt to replace page.
  - Fill in MEMCON software register with memory configuration and error status for use in FRU isolation.

- For memory single-bit correctable ECC errors:
  - Fill in Corrected Read Data (CRD) entry FOOTPRINT with set, bank, and syndrome information for use in FRU isolation.
  - Update the CRD entry for time, address range, and count; fill the MEMCON software register with memory configuration information.
  - Scrub memory location for first occurrence of error within a particular footprint. If second or more occurrence within a footprint, mark page bad in hopes that page will be replaced later. Disable soft error logging for 10 minutes if threshold is exceeded.
  - Signify that CRD buffer be logged for the following events: system shutdown (operator shutdown or crash), hard single-cell address within footprint, multiple addresses within footprint, memory uncorrectable ECC error, or CRD buffer full.

- For ownership memory correctable ECC error, scrub location.

- Log error.

- Crash process or system, dependent upon PSL (Current Mode) with a fatal bugcheck for the following situations:
  - Retry is not possible.
  - Memory page could not be replaced for uncorrectable ECC memory error.
  - Uncorrectable tag store ECC errors present in writeback cache.
  - Uncorrectable data store ECC errors present in writeback cache for locations marked as OWNED.
  - Most INT60 errors.
  - Threshold is exceeded (except for cache errors).
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

- A few other errors of the sort considered nonrecoverable are present.
  - Disable cache(s) permanently if error threshold is exceeded.
  - Flush and re-enable those caches which have been marked as good.
  - Clear the error flags.
  - Perform Return from Exception or Interrupt (REI) to recover and restart or continue the instruction stream for the following situations:
    - Most INT54 errors.
    - Those INT60 and INT54 errors which result in bad ECC written to a memory location. (These errors can provide clues that the problem is not memory related.)
    - Machine check conditions where instruction retry is possible.
    - Memory uncorrectable ECC error where page replacement is possible and instruction retry is possible.
    - Threshold exceeded (for cache errors only).
    - Return from Subroutine (RSB) and return from all polled errors.

Note

The results of the OpenVMS error handler may be preserved within the operating system session (for example, disabling a cache) but not across reboots.

Although the system can recover with cache disabled, the system performance will be degraded, since access time increases as available cache decreases.

5.2.3 OpenVMS Error Logging and Event Log Entry Format

The OpenVMS error handler for the kernel can generate six different entry types, as shown in Table 5-1. All error entry types, with the exception of correctable ECC memory errors, are logged immediately.
### System Troubleshooting and Diagnostics

#### 5.2 Product Fault Management and Symptom-Directed Diagnosis

<table>
<thead>
<tr>
<th>Table 5–1</th>
<th>OpenVMS Error Handler Entry Types</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OpenVMS Entry Type</strong></td>
<td><strong>Code</strong></td>
</tr>
</tbody>
</table>
| EMB$C_MC | (002.) | Machine Check Exception  
SCB Vector 4, IPL 1F |
| EMB$C_SE | (006.) | Soft Error Interrupt  
Correctable ECC Memory Error  
SCB Vector 54, IPL 1A |
| EMB$C_INT54 | (026.) | Soft Error Interrupt  
SCB Vector 54, IPL 1A |
| EMB$C_INT60 | (027.) | Hard Error Interrupt 60  
SCB Vector 60, IPL 1D |
| EMB$C_POLLED | (044.) | Polled Errors  
No exception or interrupt generated by hardware. |
| EMB$C_BUGCHECK | | Fatal bugcheck  
Bugcheck Types:  
MACHINECHK  
ASYNCWRTER  
BADMCKCOD  
INCONSTATE  
UNIXINTEXC |

Each entry consists of an OpenVMS operating system header, a packet header, and one or more subpackets (Figure 5–1). Entries can be of variable length based on the number of subpackets within the entry. The FLAGS software register in the packet header shows which subpackets are included within a given entry.

Refer to Section 5.2.4 for actual examples of the error and event logs described throughout this section.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Figure 5–1 Event Log Entry Format

Machine check exception entries contain, at a minimum, a Machine Check Stack Frame subpacket (Figure 5–2).
**System Troubleshooting and Diagnostics**

**5.2 Product Fault Management and Symptom-Directed Diagnosis**

### Figure 5-2 Machine Check Stack Frame Subpacket

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>24 23 16 15 08 07 00</td>
</tr>
<tr>
<td>AST LVL</td>
<td>xxxxx</td>
</tr>
<tr>
<td>Machine Check Code</td>
<td>xxxxxxxx</td>
</tr>
<tr>
<td>CPU ID</td>
<td></td>
</tr>
<tr>
<td>0.</td>
<td>4. ISTATE1</td>
</tr>
<tr>
<td>8.</td>
<td>4. ISTATE1</td>
</tr>
<tr>
<td>12.</td>
<td>4. ISTATE1</td>
</tr>
<tr>
<td>16.</td>
<td>4. ISTATE1</td>
</tr>
<tr>
<td>20.</td>
<td>4. ISTATE1</td>
</tr>
<tr>
<td>24. ISTATE2</td>
<td></td>
</tr>
<tr>
<td>28.</td>
<td></td>
</tr>
<tr>
<td>32.</td>
<td></td>
</tr>
</tbody>
</table>

INT54, INT60, Polled, and some Machine Check entries contain a processor Register subpacket (Figure 5-3), which consists of some 40 plus hardware registers.
## System Troubleshooting and Diagnostics

### 5.2 Product Fault Management and Symptom-Directed Diagnosis

#### Figure 5–3 Processor Register Subpacket

<table>
<thead>
<tr>
<th>31</th>
<th>00</th>
<th>31</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>BPCR (IPR D4)</td>
<td>0.</td>
<td>MMEADR (IPR E8)</td>
<td>92.</td>
</tr>
<tr>
<td>PAMODE (IPR E7)</td>
<td>4.</td>
<td>VMAR (IPR D0)</td>
<td>96.</td>
</tr>
<tr>
<td>MMEPTE (IPR E9)</td>
<td>8.</td>
<td>TBADR (IPR EC)</td>
<td>100.</td>
</tr>
<tr>
<td>MMESTS (IPR EA)</td>
<td>12.</td>
<td>PCADR (IPR F2)</td>
<td>104.</td>
</tr>
<tr>
<td>PCSCR (IPR 7C)</td>
<td>16.</td>
<td>BCEIDIX (IPR A7)</td>
<td>108.</td>
</tr>
<tr>
<td>ICSR (IPR D3)</td>
<td>20.</td>
<td>BCEIDECC (IPR A8)</td>
<td>112.</td>
</tr>
<tr>
<td>ECR (IPR 7D)</td>
<td>24.</td>
<td>BCEIDIDX (IPR A4)</td>
<td>116.</td>
</tr>
<tr>
<td>TBSTS (IPR ED)</td>
<td>28.</td>
<td>BCETAG (IPR A5)</td>
<td>120.</td>
</tr>
<tr>
<td>PCCTL (IPR F8)</td>
<td>32.</td>
<td>MEAR (2101.8040)</td>
<td>124.</td>
</tr>
<tr>
<td>PCSTS (IPR F4)</td>
<td>36.</td>
<td>MOAMR (2101.804C)</td>
<td>128.</td>
</tr>
<tr>
<td>CCTL (IPR A0)</td>
<td>40.</td>
<td>CSEAR1 (2102.0008)</td>
<td>132.</td>
</tr>
<tr>
<td>BCEIDSTS (IPR A6)</td>
<td>44.</td>
<td>CSEAR2 (2102.000C)</td>
<td>136.</td>
</tr>
<tr>
<td>BCETSTS (IPR A3)</td>
<td>48.</td>
<td>CIOEAR1 (2102.0010)</td>
<td>140.</td>
</tr>
<tr>
<td>MESSR (2101.8044)</td>
<td>52.</td>
<td>CIOEAR2 (2102.0014)</td>
<td>144.</td>
</tr>
<tr>
<td>MMCDSR (2101.8048)</td>
<td>56.</td>
<td>CNEAR (2102.0018)</td>
<td>148.</td>
</tr>
<tr>
<td>CESR (2102.0000)</td>
<td>60.</td>
<td>CEDAR (IPR AB)</td>
<td>152.</td>
</tr>
<tr>
<td>CMCDSR (2102.0004)</td>
<td>64.</td>
<td>NEOADR (IPR B0)</td>
<td>156.</td>
</tr>
<tr>
<td>CEFSRS (IPR AC)</td>
<td>68.</td>
<td>NEDATHI (IPR B4)</td>
<td>160.</td>
</tr>
<tr>
<td>NESTS (IPR AE)</td>
<td>72.</td>
<td>NEDATLO (IPR B6)</td>
<td>164.</td>
</tr>
<tr>
<td>NEICMD (IPR B8)</td>
<td>80.</td>
<td>DEAR (2008.000C)</td>
<td>172.</td>
</tr>
<tr>
<td>DSER (2008.0004)</td>
<td>84.</td>
<td>IPCR0 (2000.1F40)</td>
<td>176.</td>
</tr>
<tr>
<td>CBTCR (2014.0020)</td>
<td>88.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note**

The byte count, although part of the stack frame, is not included in the error log entry itself.

Bugcheck entries generated by the OpenVMS kernel error handler include the first 23 registers from the processor Register subpacket along with the Time of Day Register (TODR) and other software context states.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Uncorrectable ECC memory error entries include a Memory subpacket (Figure 5–4). The memory subpacket consists of MEMCON, which is a software register containing the memory configuration and error status used for FRU isolation, and MEMCONn, the hardware register that matched the error address in MEAR.

Figure 5–4 Memory Subpacket for ECC Memory Errors

<table>
<thead>
<tr>
<th>31</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEMCON</td>
<td>0.</td>
</tr>
<tr>
<td>MEMCONn (one longword from 2101.8000 - 2101.801C)</td>
<td>4.</td>
</tr>
</tbody>
</table>

Correctable Memory Error entries have a Memory (Single-Bit Error) SBE Reduction subpacket (Figure 5–5). This subpacket, unlike all others, is of variable length. It consists solely of software registers from state maintained by the error handler, as well as hardware state transformed into a more usable format.

Figure 5–5 Memory SBE Reduction Subpacket (Correctable Memory Errors)

<table>
<thead>
<tr>
<th>31</th>
<th>Memory SBE Reduction Subpacket</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRD Entry Subpacket Header</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRD Entry #1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRD Entry #2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>CRD Entry n</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Max n = 16

The OpenVMS error handler maintains a Correctable Read Data (CRD) buffer internally within memory that is flushed asynchronously for high-level events to the error log file. The CRD buffer and resultant error log entry are maintained and organized as follows.

- Each entry has a subpacket header (Figure 5–6) consisting of LOGGING REASON, PAGE MAPOUT CNT, MEMCON, VALID ENTRY CNT, and
CURRENT ENTRY. MEMCON contains memory configuration information, but no error status as is done for the Memory subpacket.

Figure 5–6  CRD Entry Subpacket Header

- Following the subpacket header are 1 to 16 fixed-length Memory CRD Entries (Figure 5–7). The number of Memory CRD entries is shown in VALID ENTRY CNT. The entry which caused the report to be generated is in CURRENT ENTRY.
Each Memory CRD Entry represents one unique DRAM within the memory subsystem. A unique set, bank, and syndrome are stored in footprint to construct a unique ID for the DRAM.

Rather than logging an error for each occurrence of a single symbol correctable ECC memory error, the OpenVMS error handler maintains the CRD buffer—it creates a Memory CRD Entry for new footprints and updates an existing Memory CRD Entry for errors that occur within the range specified by the ID in FOOTPRINT. This reduces the amount of data logged overall without losing important information—errors are logged per unique failure mode rather than on a per error basis.

Each Memory CRD entry consists of a FOOTPRINT, STATUS, CRD CNT, PAGE MAPOUT CNT, FIRST EVENT, LAST EVENT, LOWEST ADDRESS and HIGHEST ADDRESS.

FIRST EVENT, LAST EVENT, LOWEST ADDRESS and HIGHEST ADDRESS are updated to show the range of time and addresses of errors which have occurred for a DRAM. CRD CNT is simply the total count per footprint. PAGE MAPOUT CNT is the number of pages that have been marked bad for a particular DRAM.
STATUS contains a record of the failure mode status of a particular DRAM over time. This in turn determines whether or not the CRD buffer is logged. For the first occurrence of an error within a particular DRAM, the memory location will be scrubbed (corrected read data is read, then written back to the memory location) and CRD CNT will be set to 1. Since most memory single-bit errors are transient due to alpha particles, logging of the CRD buffer will not be done immediately for the first occurrence of an error within a DRAM. The CRD buffer will, however, be logged at the time of system shutdown (operator or crash induced), or when a more severe memory subsystem error occurs.

If the FOOTPRINT/DRAM experiences another error (CRD CNT > 1), the OpenVMS operating system will set HARD SINGLE ADDRESS or MULTIPLE ADDRESSES along with SCRUBBED in STATUS. Scrubbing is no longer performed; instead, pages are marked bad. In this case, the OpenVMS operating system will log the CRD buffer immediately. The CRD Buffer will also be logged immediately if PAGE MAPOUT THRESHOLD EXCEEDED is set in SYSTAT as a result of pages being marked bad. The threshold is reached if more than one page per Mbyte of system memory is marked bad.

Note

CURRENT ENTRY will be zero in the Memory SBE Reduction subpacket header if the CRD buffer was logged, not as a result of a HARD SINGLE ADDRESS or MULTIPLE ADDRESSES error in STATUS, but as a result of a memory uncorrectable ECC error shown as RELATED ERROR, or as a result of CRD BUFFER FULL or SYSTEM SHUTDOWN, all of which are shown under LOGGING REASON.

5.2.4 OpenVMS Event Record Translation

The kernel error log entries are translated from binary to ASCII using the ANALYZE/ERROR command. To invoke the error log utility, enter the DCL command ANALYZE/ERROR_LOG.

Format:

`ANALYZE_ERROR_LOG [/qualifier(s)] [file-spec] [,...]

Example:

`$ ANALYZE/ERROR_LOG/INCLUDE=(CPU,MEMORY)/SINCE=TODAY`
System Troubleshooting and Diagnostics

5.2 Product Fault Management and Symptom-Directed Diagnosis

The error log utility translates the entry into the traditional three-column format. The first column shows the register mnemonics, the second column depicts the data in hex, and the last column shows the actual English translations.

As in the above example, the OpenVMS error handler also provides support for the /INCLUDE qualifier, such that CPU and MEMORY error entries can be selectively translated.

Since most kernel errors are bounded to either the processor module/system board or memory modules, the individual error flags and fields are not covered by the service theory. Although these flags are generally not required to diagnose a system to the FRU (Field Replaceable Unit), this information can be useful for component isolation.

ERF bit to text translation highlights all error flags that are set, and other significant state—these are displayed in capital letters in the third column. Otherwise, nothing is shown in the translation column. The translation rules also have qualifiers such that if the setting of an error flag causes other registers to be latched, the other registers will be translated as well. For example, if a memory ECC error occurs, the syndrome and error address fields will be latched as well. If such a field is valid, the translation will be shown (e.g. MEMORY ERROR ADDRESS); otherwise, no translation is provided.

5.2.5 Interpreting CPU Faults Using ANALYZE/ERROR

If the following three conditions are satisfied, the most likely FRU is the CPU module. Example 5–1 shows an abbreviated error log with numbers to highlight the key registers.

1. No memory subpacket is listed in the third column of the FLAGS register.

2. CESR register bit <09>, CP2 IO Error, is equal to zero in the KA50/51/55 /56 Register Subpacket.

3. DSER register bits <07>, Q22 Bus NXM, <05>, Q22 Bus Device Parity Error, or <02>, Q-22 Bus No Grant, are equal to zero in the KA50/51/55/56 Register Subpacket.

The FLAGS register is located in the packet header, which immediately follows the system identification header; the CESR and DSER registers are listed under the KA50/51/55/56 Register Subpacket.

CPU errors will increment an OpenVMS global counter, which can be viewed using the DCL command SHOW ERROR, as shown in Example 5–2.
To determine if any resources have been disabled, for example, if cache has been disabled for the duration of the OpenVMS session, examine the flags for the SYSTAT register in the packet header.

In Example 5–1, a translation buffer data parity error latched in the TBSTS register caused a machine check exception error.

Example 5–1 Error Log Entry Indicating CPU Error

**System Error Report**

Compiled 14-Jan-1992 18:55:52

**Error Sequence 11.**

**Logged On:** SID 13001401

**Date/Time:** 27-Sep-1991 14:40:10.85

**System Uptime:** 0 Days 00:12:12

**SCS Node:** OMEGA1

**VAX/OpenVMS V5.5-2**

**Machine Check KA50**

CPU Microcode Rev # 1. CONSOLE FW REV# 1.1

**Standard Microcode Patch**

**Patch Rev # 10.**

**Revision:** 00000000

**SYSTAT:** 00000001

**Flags:** 00000003

**Attempting Recovery**

machine check stack frame
KA50 subpacket

**Stack Frame Subpacket**

**Istate_1:** 80050000

**Machine Check Fault Code = 05(x)**

Current AST level = 4(X)

ASYNCHRONOUS HARDWARE ERROR

PSL 04140001

c-bit
executing on interrupt stack
PSL previous mode = kernel
PSL current mode = kernel
first part done set

**KA50 Register Subpacket**

(continued on next page)
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5–1 (Cont.) Error Log Entry Indicating CPU Error

<table>
<thead>
<tr>
<th>BPCR</th>
<th>ECCB0024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>TBSTS</td>
<td>800001D3</td>
</tr>
</tbody>
</table>

LOCK SET
TRANSLATION BUFFER DATA PARITY ERROR
em latch invalid
s5 command = 1D(X)
valid Ilbox specifier ref. error stored

| CESR | 00000000 |
|      |          |
|      |          |
| DSER | 00000000 |
|      |          |
| IPCR0| 00000020 |

LOCAL MEMORY EXTERNAL ACCESS ENABLED

---

**Note**

Ownership (O-bit) memory correctable or fatal errors (MESR <04> or MESR <03> of the processor Register S:abacket set equal to 1) are processor module errors, NOT memory errors.

---

Example 5–2  SHOW ERROR Display Using the OpenVMS Operating System

```
$ SHOW ERROR
Device       Error Count
CPU          1
MEMORY       1
PABO:        1
PAAO:        1
PTAO:        1
RTA2:        1
$
```
5.2.6 Interpreting Memory Faults Using ANALYZE/ERROR

If "memory subpacket" or "memory sube reduction subpacket" is listed in the third column of the FLAGS register, there is a problem with one or more of the memory modules, CPU module, or backplane.

- The "memory subpacket" message indicates an uncorrectable ECC error. Refer to Section 5.2.6.1 for instructions in isolating uncorrectable ECC error problems.

- The "memory sube reduction subpacket" message indicates correctable ECC errors. Refer to Section 5.2.6.2 for instructions in isolating correctable ECC error problems.

__________________________
Note
__________________________
The memory fault interpretation procedures work only if the memory modules have been properly installed and configured. For example, memory modules should start in backplane slot 4 (next to the processor module in slot 5) and proceed to slot 1 with no gaps.

__________________________
Note
__________________________
Although the OpenVMS error handler has built-in features to aid Services in memory repair, good judgment is needed by the Service Engineer. It is essential to understand that in many, if not most cases, correctable ECC errors are transient in nature. No amount of repair will fix them, as generally there is nothing to be fixed.

Memory modules can represent a great expense to the Corporation when they are sent back to Repair with no errors. If one disagrees with the strategy in this section or has questions or suggestions, please contact Corporate Support.

5.2.6.1 Uncorrectable ECC Errors

Refer to Example 5–3, which provides an abbreviated error log for uncorrectable ECC errors.

For uncorrectable ECC errors, a memory subpacket will be logged as indicated by "memory subpacket" listed in the third column of the FLAGS software register (●). Also, the hardware register MESR <11> (●) of the processor Register Subpacket will be set equal to 1, and MEAR will latch the error address (●).
Examine the MEMCON software register (1) under the memory subpacket. The MEMCON register provides memory configuration information.

The OpenVMS error handler will mark each page bad and attempt page replacement, indicated in SYSTAT (1). The DCL command SHOW MEMORY (Example 5–4) will also indicate the result of OpenVMS page replacement.

Uncorrectable memory errors will increment the OpenVMS global counter, which can be viewed using the DCL command SHOW ERROR.

Note

If register MESR <11> was set equal to 1, but MESR <19:12> syndrome equals 07, no memory subpacket will be logged as a result of incorrect check bits written to memory because of an NDAL bus parity error detected by the NMC. In short, this indicates a problem with the CPU module, not memory. There should be a previous entry with MESR <22>, NDAL Data Parity Error set equal to 1.

Note

One type of uncorrectable ECC error, that due to a "disown write", will result in a CRD entry like those for correctable ECC errors. The FOOTPRINT longword for this entry contains the message "Uncorrectable ECC errors due to disown write". The failing module should be replaced for this error.
Example 5-3  Error Log Entry Indicating Uncorrectable ECC Error

VA X / VM S  SYSTEM ERROR REPORT  COMPIL 6-NOV-1991 10:16:49
PAGE 25.

ERROR SEQUENCE 2.
DATE/TIME 4-OCT-1991 09:14:20:86
SYSTEM UPTIME: 0 DAYS 00:01:39
SCS NODK: OMEGA

INT54 ERROR KA50 CPU Microcode Rev # 1. CONSOLE FW REV # 1.1

ATTEMPTING RECOVERY
PAGE MARKED BAD
PAGE REPLACED .
memory subpacket .
KA50 subpacket

KA50 REGISTER SUBPACKET

ATTEMPTING RECOVERY
PAGE MARKED BAD
PAGE REPLACED .
memory subpacket .
KA50 subpacket

MEMORY SUBPACKET

MEMCON 000FFFF02 4
MEMORY CONFIGURATION:
MS44-AA SIM Memory Module 4 MB location 1E
MS44-AA SIM Memory Module 4 MB location 1F
MS44-AA SIM Memory Module 4 MB location 1G
MS44-AA SIM Memory Module 4 MB location 1H
Total memory = 16MB

(continued on next page)
5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5–3 (Cont.) Error Log Entry Indicating Uncorrectable ECC Error

MEMCON3  88000003

64 bit mode
Base address valid
RAM size = 1MB
base address = 0B(X)

Example 5–4 SHOW MEMORY Display Under the OpenVMS Operating System

$ SHOW MEMORY
System Memory Resources on 21-FEB-1992 05:58:52.28

<table>
<thead>
<tr>
<th>Physical Memory Usage (pages):</th>
<th>Total</th>
<th>Free</th>
<th>In Use</th>
<th>Modified</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Memory (128.00MB)</td>
<td>262144</td>
<td>224527</td>
<td>28759</td>
<td>8858</td>
</tr>
<tr>
<td>Bad Pages</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slot Usage (slots):</td>
<td>Total</td>
<td>Free</td>
<td>In Use</td>
<td>Static</td>
</tr>
<tr>
<td>Process Entry Slots</td>
<td>360</td>
<td>347</td>
<td>13</td>
<td>0</td>
</tr>
<tr>
<td>Balance Set Slots</td>
<td>324</td>
<td>313</td>
<td>11</td>
<td>0</td>
</tr>
<tr>
<td>Fixed-Size Pool Areas (packets):</td>
<td>Total</td>
<td>Free</td>
<td>In Use</td>
<td>Size</td>
</tr>
<tr>
<td>Small Packet (SRP) List</td>
<td>3067</td>
<td>2724</td>
<td>343</td>
<td>128</td>
</tr>
<tr>
<td>I/O Request Packet (IRP) List</td>
<td>2263</td>
<td>2070</td>
<td>193</td>
<td>176</td>
</tr>
<tr>
<td>Large Packet (LRP) List</td>
<td>87</td>
<td>61</td>
<td>26</td>
<td>1856</td>
</tr>
<tr>
<td>Dynamic Memory Usage (bytes):</td>
<td>Total</td>
<td>Free</td>
<td>In Use</td>
<td>Largest</td>
</tr>
<tr>
<td>Nonpaged Dynamic Memory</td>
<td>1037624</td>
<td>503920</td>
<td>533904</td>
<td>473184</td>
</tr>
<tr>
<td>Paged Dynamic Memory</td>
<td>1468416</td>
<td>561584</td>
<td>906832</td>
<td>560624</td>
</tr>
<tr>
<td>Paging File Usage (pages):</td>
<td></td>
<td></td>
<td></td>
<td>Total</td>
</tr>
<tr>
<td>DISK\VMS\05:SYSO.SYSEX</td>
<td>PAGEFILE.SYS</td>
<td>300000</td>
<td>266070</td>
<td>300000</td>
</tr>
</tbody>
</table>

Of the physical pages in use, 24120 pages are permanently allocated to OpenVMS.

Using the OpenVMS command ANALYZE/SYSTEM, you can associate a page that had been replaced (Bad Pages in SHOW MEMORY display) with the physical address in memory.

In Example 5–5, 5ff8 (under the Page Frame Number (PFN) column) is identified as the single page that has been replaced. The command EVAL 5ff8 * 200 converts the PFN to a physical page address. The result is 0bff7000, which is the MEAR address translated in Example 5–3. (Bits <8:0> of the addresses may differ since the page address from EVAL always shows bits <8:0> as 0.)
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5–5  **Using ANALYZE/SYSTEM to Check the Physical Address in Memory for a Replaced Page**

```bash
$ ANALYZE/SYSTEM
VAX/OpenVMS System analyzer
SDA> SHOW PFN /BAD
Bad page list
----------
Count:        1
Lolimit:      -1
High limit:   1073741824

PFN    PTE ADDRESS    BAK    REFCNT    FLINK    BLINK    TYPE    STATE
----------    ----------    -----    ------    ------    ------    -------    ------
0005FFB8  00000000  00000000  0  00000000  00000000  20 PROCESS  02 BADLIST

SDA> EVAL 5ffb8 * 200
Hex = 0BFF7000  Decmal = 201289728
SDA> EXIT
```

5.2.6.2 **Correctable ECC Errors**

Refer to Example 5–6, which provides an error log showing correctable ECC errors.

For correctable ECC errors, a Single-Bit Error (SBE) Memory Subpacket will be logged as indicated by "memory sbe reduction subpacket" listed in the third column of the FLAGS software register (○).

The Memory SBE Reduction Subpacket header contains a CURRENT ENTRY register (○) that displays the number of the Memory CRD Entry that caused the error notification. If CURRENT ENTRY > 0, examine which bits are set in the STATUS register (○) for this entry—GENERATE REPORT should be set.

**Note**

If CURRENT ENTRY = 0, then the entry was logged for something other than a single-bit memory correctable error Footprint. You will need to examine all of the Memory CRD Entries and Footprints to try to determine the likely FRU.

Check for the following:

- **SCRUBBED (○)**—If SCRUBBED is the only bit set in the STATUS register, memory modules should NOT generally be replaced.
5.2 Product Fault Management and Symptom-Directed Diagnosis

The kernel performs memory scrubbing of DRAM memory cells that may flip due to transient alpha particles. Scrubbing simply reads the corrected data and writes it back to the memory location. Returning memory modules that only have SCRUBBED set in STATUS will cost the corporation money, since the repair centers will generally not find a problem.

Unlike uncorrectable ECC errors, the error handling code cannot indicate if the page has been replaced. To get some idea, use DCL command, SHOW MEMORY. If the page mapout threshold has not been reached ("PAGE MAPOUT THRESHOLD EXCEEDED" is not set in SYSTAT packet header register (5)), the system should be restarted at a convenient time to allow the power-up self-test and ROM-based diagnostics to map out these pages. This can be done by entering TEST 0 at the console prompt, running an extended script TEST A9, or by powering down then powering up the system. In all cases, the diagnostic code will mark the page bad for hard single address errors, as well as any uncorrectable ECC error by default.

If there are many locations affected by hard single-cell errors, on the order of one or more pages per MB of system memory, the memory module should be replaced. The console command SHOW MEMORY will indicate the number of bad pages per module. For example, if the system contains 64 MB of main memory and there are 64 or more bad pages, the affected memory should be replaced.

Note

Under the OpenVMS operating system, the page mapout threshold is calculated automatically. If "PAGE MAPOUT THRESHOLD EXCEEDED" is set in SYSTAT (6), the failing memory module should be replaced.

In cases of a new memory module used for repair or as part of system installation, one may elect to replace the module rather than having diagnostics map them out, even if the threshold has not been reached for hard single-address errors.

- MULTIPLE ADDRESSES (6)—If the second occurrence of an error within a footprint is at a different address (LOWEST ADDRESS not equal to HIGHEST ADDRESS (6), MULTIPLE ADDRESSES will be set in STATUS along with SCRUBBED. Scrubbing will not be attempted for this situation. In most cases, the failing memory module should be replaced regardless of the page mapout threshold.

System Troubleshooting and Diagnostics  5–23
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

If CRD BUFFER FULL is set in LOGGING REASON (1) (located in the subpacket header) or PAGE MAPOUT THRESHOLD EXCEEDED is set in SYSTAT (2), the failing memory module should be replaced regardless of any thresholds.

For all cases (except when SCRUBBED is the only flag set in STATUS) isolate the offending memory by examining the translation in FOOTPRINT called MEMORY ERROR STATUS (1): The memory module is identified by its backplane position. In Example 5–6, SIMM memory modules in locations 0A and 0B are identified as failing.

The Memory SBE Reduction Subpacket header translates the MEMCON register (3) for memory subsystem configuration information.

Unlike uncorrectable memory and CPU errors, the OpenVMS global counter, as shown by the DCL command SHOW ERROR, is not incremented for correctable ECC errors unless it results in an error log entry for reasons other than system shutdown.

________________________________________ Note _______________________________________

If footprints are being generated for more than one memory module, especially if they all have the same bit in error, the processor module, backplane, or other component may be the cause.

________________________________________ Note _______________________________________

One type of uncorrectable ECC error, that due to a “disown write”, will result in a CRD entry like those for correctable ECC errors. The FOOTPRINT longword for this entry contains the message “Uncorrectable ECC errors due to disown write”. The failing module should be replaced for this error.

________________________________________
Example 5–6  Error Log Entry Indicating Correctable ECC Error

PAGE 1.

ERROR SEQUENCE 7.
SYSTEM UPTIME: 0 DAYS 00:05:06
SCS NODE: OMEGA1

CORRECTABLE MEMORY ERROR KA50 CPU Microcode Rev # 1. CONSOLE FW REV# 1.1

REVISION  00000000
SYSTAT  00000040  ☐
FLAGS  00000008

memory sbe reduction subpacket

MEMORY SBE REDUCTION SUBPACKET
LOGGING REASON  00000004  ☐

PAGE MAPOUT CNT  00000000
MEMCON  000FD01  ☐

MEMORY CONFIGURATION:
MS44-AA SIM Memory Module (4MB) Loc QA
MS44-AA SIM Memory Module (4MB) Loc QB
MS44-AA SIM Memory Module (4MB) Loc QC
MS44-AA SIM Memory Module (4MB) Loc QD
Total memory = 16MB
sets enabled = 000000001

MEMORY ERROR STATUS:
SIMM MEMORY MODULES: LOCATIONS QA & QB
Set = 0(X)
Bank = A

VALID ENTRY CNT  00000001
CURRENT ENTRY  00000000

MEMORY CRD ENTRY 1.

FOOTPRINT  00000073

(continued on next page)
Example 5-6 (Cont.) Error Log Entry Indicating Correctable ECC Error

MEMORY ERROR STATUS:
SIMM MEMORY MODULE: LOCATION 0A
set = 0
bank = 0.
ECC SYNDROME = 73(X)
CORRECTED DATA BIT = 0.

STATUS 1 00000010
CRD CNT 00000001
PAGE MAPOUT CNT 00000000
FIRST EVENT 16B0F640
009622CB
16-OCT-1992 11:03:36.10
LAST EVENT 16B0F640
009622CB
16-OCT-1992 11:03:36.10
LOWEST ADDRESS 0BFF4000
HIGHEST ADDRESS 0BFF4000

Note

Ownership (O-bit) memory correctable or fatal errors (MESR <04> or MESR <03> of the processor Register Subpacket set equal to 1) are processor module errors, NOT memory errors.

5.2.7 Interpreting System Bus Faults Using ANALYZE/ERROR

If hardware register CESR <09> (●) and/or CQBIC hardware register DSER <07>, <05>, or <02> (●) is set equal to 1, there may be a problem with the Q–bus or Q–bus option.

When CESR <09> is set equal to 1, examine the hardware register CIOEAR2 (●) to determine the address of the offending option.

Example 5–7 provides an error log showing a faulty Q–bus option. The CIOEAR2 error register indicates the first UQSSP controller as the offending address.
System Troubleshooting and Diagnostics

5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5-7  Error Log Entry Indicating Q-Bus Error

PAGE 1.

****************************************************************** ENTRY 75. ******************************************************************
ERROR SEQUENCE 1052.
SYSTEM UPTIME: 12 DAYS 20:04:19
SCS NODE: VAX/OpenVMS V5.5-2

MACHINE CHECK KA50  CPU Microcode Rev #1. CONSOLE FW REV# 1.1

REVISION 00000000
SYSTAT 00000001
FLAGS 00000003

ATTEMPTING RECOVERY
machine check stack frame
KA50 subpacket

STACK FRAME SUBPACKET
ISTATE 1  80060000

PSL 03C00000
PSL previous mode = user
PSL current mode = user
First part done set

KA50 REGISTER SUBPACKET

(continued on next page)
Example 5–7 (Cont.) Error Log Entry Indicating Q-Bus Error

BPCR     ECC80024

CESR     80000200  CP2 IO ERROR
ERROR SUMMARY

DSER     00000080  Q-22 BUS NXM

CIOEAR2   00001468  cp2 IO error address = 20001468
NDAL commander id (cp2 transac) = 0(X)

IPCR0     00000020  LOCAL MEMORY EXTERNAL ACCESS ENABLED

5.2.8 Interpreting DMA ↔ Host Transaction Faults Using ANALYZE/ERROR

Some kernel errors may result in two or more entries being logged. If the SGEC Ethernet controller or other CDAL device (residing on the processor module) encounter host main memory uncorrectable ECC errors, main memory NXMs or CDAL parity errors or timeouts, more than one entry results. Usually there will be one Polled Error entry logged by the host, and one or more Device Attention and other assorted entries logged by the device drivers.

In these cases the processor module or one of the four memory modules are the most likely cause of the errors. Therefore, it is essential to analyze Polled Error entries, since a polled entry usually represents the source of the error versus other entries, which are simply aftereffects of the original error.

Example 5–8 provides an abbreviated error log for a polled error. Example 5–9 provides an example of a device attention entry.
Example 5-8 Error Log Entry Indicating Polled Error

VAX/VMS SYSTEM ERROR REPORT

PAGE 1.

ERROR SEQUENCE 15.
DATE/TIME 17-FEB-1992 05:22:00.90
SYSTEM UPTIME: 0 DAYS 00:27:48

LOGGED ON: SID 13001401
SYS_TYPE 00310A01

VAX/OPENVMS V5.5-2

POLLED ERROR KA50 CPU Microcode Rev 4.1. CONSOLE FW REV# 1.1

REVISION 00000000
SYSTAT 00000001

FLAGS 00000006

ATTEMPTING RECOVERY

memory subpacket

KA50 subpacket

KA50 REGISTER SUBPACKET

APCR ECC80024
.
.
MESR 8001B000

UNCORRECTABLE MEMORY ECC ERROR
ERROR SUMMARY
MEMORY ERROR SYNDROME = 1B(X)
.
.
MEAR 50000410

main memory error address = 00001040
ndal commander ld = 05(X)
.
.
IPCRO 0000020

LOCAL MEMORY EXTERNAL ACCESS ENABLED

MEMORY SUBPACKET

MEMCON 00000020

MEMORY CONFIGURATION:
MS44-AA SIM Memory Module 4 MB location 1E
MS44-AA SIM Memory Module 4 MB location 1F
MS44-AA SIM Memory Module 4 MB location 1G
MS44-AA SIM Memory Module 4 MB location 1H
_total memory = 16MB

(continued on next page)
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5–8 (Cont.) Error Log Entry Indicating Polled Error

MEMCON0  80000003

64 bit mode
Base address valid
RAM size = 1MB
base address = 00(X)

ANAL/ERR/OUT-TBI TBI.ZPD
Example 5–9 Device Attention Entry

V A X / V M S  SYSTEM ERROR REPORT  COMPiled 17-FEB-1992 05:32:21
PAGE 1.

ERROR SEQUENCE 15.
DATE/TIME 17-FEB-1992 05:22:00.90
SYSTEM UPTIME: 0 DAYS 00:27:48
SCS NODE:

DEVICE ATTENTION KA50  CPU Microcode Rev $ 1.  CONSOLE FW REV@ 1.1

OSSI SUB-SYSTEM, PABO: - PORT WILL BE RE-STARTED

PORT TIMEOUT, DRIVER RESETING PORT

CNF  03060022

PMCSR  00000000
PSR   80010000
PFAR  40001044
PESR  00010000
PPR   00000000

UCBSB_ERTCNT  2C
UCBSB_ERTMAX  32
UCB5L_CHAR  0C450000

UCBSW_STS  0010
UCBSW_ERRCNT  0007

ANAL/ERR/ENTRY (ST:2,END:3)/OUT=POLL SHM
5.2.9 VAXsimPLUS and System-Initiated Call Logging (SICL) Support

Symptom-Directed Diagnostic (SDD) toolkit support for KA50/51/55/56 kernels is provided in version 2.0 of the toolkit. If version 2.0 is not available, you should install the previous version, as it provides support for many existing options.

MicroVAX 3100 systems use Symptom-Directed Diagnosis tools primarily for notification. The VAX System Integrity Monitor Plus (VAXsimPLUS) interactive reporting tool triggers notification for high-level events recorded in SYSTAT and LOGGING REASON.

The VAXsimPLUS monitor simply parses for a handful of SYSTAT flags and LOGGING reason codes. The VAXsimPLUS monitor display is updated and triggering occurs if the threshold has been reached. Some flags have a threshold of one; for example, SYSTAT <08> ERROR THRESHOLD EXCEEDED will trigger VAXsimPLUS upon the first occurrence, since at least three errors would have already occurred and been handled by the OpenVMS operating system.

All lower level errors will ultimately set one of the conditions shown in Table 5–2. VAXsimPLUS will examine the conditions within a 24-hour period—thresholds are typically one or two flags or logging reason codes within that period.

Table 5–2 lists the conditions that will trigger VAXsimPLUS notification and updating. Figure 5–8 shows the flow for the VAXsimPLUS monitor trigger (for decision blocks with only one branch, the alternative is treated as an ignore condition). The entries ultimately are classified as either hard or soft. Errors that require corrective maintenance are classified as hard; while errors potentially requiring corrective maintenance are classified as soft.
### System Troubleshooting and Diagnostics

#### 5.2 Product Fault Management and Symptom-Directed Diagnosis

<table>
<thead>
<tr>
<th>Condition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYSTAT &lt;00&gt; = 1</td>
<td>&quot;Attempting recovery&quot;</td>
</tr>
<tr>
<td>SYSTAT &lt;00&gt; = 0</td>
<td>&quot;Full recovery or retry not possible&quot;</td>
</tr>
<tr>
<td>SYSTAT &lt;08&gt; = 1</td>
<td>&quot;Error threshold exceeded&quot;</td>
</tr>
<tr>
<td>SYSTAT &lt;09&gt; = 1</td>
<td>&quot;Page marked bad for uncorrectable ECC error in main memory&quot;</td>
</tr>
<tr>
<td>SYSTAT &lt;11&gt; = 1</td>
<td>&quot;Page mapout threshold for single bit ECC errors in main memory exceeded&quot;</td>
</tr>
<tr>
<td>LOGGING REASON &lt;3:0&gt; = 1</td>
<td>&quot;Memory CRD buffer full&quot;</td>
</tr>
<tr>
<td>LOGGING REASON &lt;3:0&gt; = 2</td>
<td>&quot;Generate report as a result of hard single address or multiple address DRAM memory fault&quot;</td>
</tr>
<tr>
<td>LOGGING REASON &lt;3:0&gt; = 0, 3, 5–F</td>
<td>&quot;Illegal LOGGING REASON&quot;</td>
</tr>
</tbody>
</table>
VAXsimPLUS triggering notifies the customer and Services using three message types: HARD, SOFT, and SICL Service Request. Each message contains the single STARS article theory number, as well as the SYSTAT or LOGGING REASON state. In addition, the SICL Service Request will have a Merged Error Log (MEL) datafile appended. Both hard and soft triggers will generate SICL Service Request messages.
5.2 Product Fault Management and Symptom-Directed Diagnosis

Figure 5–9 shows the five VAXsimPLUS monitor screen displays. Table 5–3 provides a brief explanation of the five levels of screen displays.

Table 5–3 Five-Level VAXsimPLUS Monitor Screen Displays

<table>
<thead>
<tr>
<th>Level</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. System</td>
<td>The system level screen provides one box for each system being analyzed (in Figure 5–9 a single system is being analyzed). As with each screen level, the number of reported errors is displayed in the box. The boxes blink when the hard error thresholds are reached; the boxes are highlighted when the soft error thresholds are reached.</td>
</tr>
<tr>
<td>2. Subsystem</td>
<td>The subsystem level screen provides separate boxes for the kernel and node information. Other boxes that may be displayed are bus, disk, tape, etc.</td>
</tr>
<tr>
<td>3. Unit</td>
<td>The unit level screen provides a box for the kernel. If the subsystem has more than one unit or device with errors, those will be displayed as well.</td>
</tr>
<tr>
<td>4. Error Class</td>
<td>The error class level screen provides a box for both hard and soft errors.</td>
</tr>
<tr>
<td>5. Error Detail</td>
<td>Two error detail level screens (hard and soft) provide the number of reported errors along with a brief error description.</td>
</tr>
</tbody>
</table>
Once notification occurs, the service engineer should examine the error log file (after using the ANALYZE/ERROR command) or read the appended Merged Error Log (MEL) file in the SICL service request message. (The MEL file is encrypted, refer to Section 5.2.9.1 for instructions in converting these files.)
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Using the theory of interpretation provided in the previous sections, you can manually interpret the error logs.

Note

The interpretation theory provided in this manual is also a STARS article and can be accessed via the Decoder Kit. (Theory 30B01.xxx reproduces in full, Section 5.2 of this manual).

In summary, a service engineer should use VAXsimPLUS notification as follows:

1. Make sure all four message types are sent to the Field and System accounts.
2. Log into the Field or System account.
3. Read mail (look for the SICL service request message with its appended MEL file).
4. Convert the encrypted MEL file and use the theory provided in this manual to interpret the error log file.

5.2.9.1 Converting the SICL Service Request MEL File

Use the following procedure to convert the encrypted MEL file that is appended to the SICL service request message (MEL files can be converted on site or at a support center). Example 5–10 shows a sample SICL service request message and appended MEL file.

1. Extract the SICL mail message from mail.
2. Edit the extracted file to obtain the appended MEL file. The MEL file is the encrypted code that appears between the rows of asterisks and includes the words “SICL” and “end.”
3. Convert the encrypted code to a binary file using the VAXsimPLUS decode command file as follows:
   
   $ MCR SDD$EXE:FMGR$SICL_DECODE [MEL filename] [binary filename]

4. Use the ANALYZE/ERROR command to produce an error log entry.
Example 5-10  SICL Service Request with Appended MEL File

To: SYSTEM
CC:
Subj: SDD T2.0 Service Request - Analysis:[30801.200]

VAXsimPLUS Notification Message

VAXsimPLUS has detected that the following device needs attention:

DEVICE: ABIXSKERNEL (NVAX4000)
NODE: ABIX
SYSTEM SERIAL NUMBER: KA136H1520
SYSTEM TYPE: VAX 4000-600

VAXsimPLUS Diagnosis Information

Attn: Field Service
Device: ABIXSKERNEL (NVAX4000)
Count: 1.
Theory: [30801.200]
Evidence: Urgent action required - ABIXSKERNEL Hard error(s):

SYSTAT <9> = 1 - Page Marked Bad For Uncorrectable ECC Error In Main Memory

******************************************************************************
%% SDDSPLFIE is defined to be NONE, no Customer Profile included in message %%
******************************************************************************

SICL

134
M @ S O O=O  A$24U)3S\('  % @ G!:G*Y*5
M @ 034N=2-=7 60@ @ I P' W @ 0 "<<
M !F|F| " I  %/%SP @ RO R P \%3103 !P @ !
M !H G 0* /S $X \A ! F 6 /CA*0 (P0
M@AP( % T 0 ' "S , ' ' % "
M @ S+1P 12 P P \[ 2Y#P% " !/ D 04 ( end

5.2.9.2 VAXsimPLUS Installation Tips

When installing VAXsimPLUS, the system will prompt you for information. You will need to know the serial number and system model number for the system on which you are installing VAXsimPLUS. The serial number is located on the front of the chassis at the bottom and to the left (the front door must be open). The system model number is attached to the outside of the door.

5-38 System Troubleshooting and Diagnostics
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Also, if the system does not have dialout capability, you should answer no when asked if you want to enable SICL—if you enter yes, the system will attempt to send mail via DSNLink resulting in error messages. After VAXsimPLUS is installed you can activate SICL and customize the VAXsimPLUS mailing lists so that SICL messages are sent to an appropriate destination(s) on site. This way, SICL messages are received onsite without incurring error messages regarding remote link failures.

5.2.9.3 VAXsimPLUS Post-Installation Tips

Once VAXsimPLUS is installed, you can set up mailing lists to direct VAXsimPLUS messages to the appropriate destinations. If the system has no dialout capability, SICL messages should be directed to the System and/or Field account—this is good practice for systems with dialout and service center support as well.

In the example that follows, the four types of mailing lists are displayed and System and Field accounts are added to all four mailing lists using VAXSIM /FAULT_MANAGER commands.

_________________________  Note  ____________________________

The commands can be abbreviated.

DSN%SICL appears under the SICL mailing list if you enabled SICL during installation.

_________________________
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

$ VAXSIM/FAULT SHOW MAIL
  -- FSE mailing list --
    FIELD
    -- CUSTOMER mailing list --
    SYSTEM
    -- MONITOR mailing list is empty --
    -- SICL mailing list --
    DSN%SICL

$ VAXSIM/FAULT ADD SYSTEM ALL
$ VAXSIM/FAULT ADD FIELD ALL
$ VAXSIM/FAULT SHOW MAIL
  -- FSE mailing list --
    FIELD
    SYSTEM
    -- CUSTOMER mailing list --
    FIELD
    SYSTEM
    -- MONITOR mailing list --
    FIELD
    SYSTEM
    -- SICL mailing list --
    DSN%SICL
    FIELD
    SYSTEM

To activate SICL after installation, use the following command:

$ VAXSIM/FAULT SET SICL ON

VAXsimPLUS customer notification messages should display a phone number for the customer to call in the event the system needs service. Use the following commands to examine and set the phone number parameter:

$ VAXSIM/FAULT SHOW PARAMETER

(SET parameter) (Parameter settings)
PHONE_NUMBER Customer Service Phone Number is unknown
COPY Automatic copying is OFF
SICL System Initiated Call Logging is ON
SYSTEM_INFO System info for AB1X
  Serial number KA136H1520
  System type VAX 4000-600
$ VAXSIM/FAULT SET PHONE 1-800-DIGITAL

Finally, the VAXSIMPLUS/MERGE command is useful in examining how a device is functioning in a cluster. The merge command collects the messages that are being sent to the other CPUs in the cluster.

5.2.10 Repair Data for Returning FRUs

When sending back an FRU for repair, include as much of the error log information as possible. If one or more error flags are set in a particular entry, record the mnemonic(s) of the register(s), the hex data, and error flag translation(s) on the repair tag. If an error address is valid, include the mnemonic, hex data, and translation on the repair tag as well. For memory and cache errors, include the syndrome and corrected-bit/bit-in-error information, along with the register mnemonic and hex data. Other registers which should be recorded for any entry type are SYSTAT, MEMCON and FOOTPRINT.

5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

If any of the tests fail, the test code displays on the console LED and, if specified in the firmware script, a diagnostic console printout displays in the format shown in Example 5–11.

Example 5–11 Sample Output with Errors

```
? Test_Subtest_40 06 Loop_Subtest=00 Err_Type=FF D_E_Memory_count_pages_1.m

Vec=0000 Prev_Errs=0004 P1=00000001 P2=00000002 P3=00000001 P4=00000000
P5=00000020 P6=00000000 P7=00000020 P8=00000000 P9=00000000 P10=000FCD4B
r0=00FF4008 rl=00000007 r2=00000000 r3=FFFFFFFE r4=00000008 r5=00000000
r6=00000000 r7=00000002 r8=00FF4000 r9=20140758 r10=FFFFFFFE r11=FFFFFFF

dser=0000 cesr=00000000 intmsk=00 icmsk=01 pcists=FC00 pcaddr=FFFFFFFB pcctl=FC13
ccnt=00000021 bcnts=0000 bcedsts=0000 cefsts=00000200 nest=s 0
mmncsr=01110000 merr=00000000

>>> 
```

Several lines are printed in the error display. The first line has eight column headings:

1 Test identifies the diagnostic test, test ?40 in Example 5–11. Using
   Table 5–4, you can use the test number to point to possible problems in
   field replaceable units (FRUs).
System Troubleshooting and Diagnostics
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

2 Subtest log is two hex digits identifying, usually within 10 instructions, where in the diagnostic the error occurred.

3 Loop_subtest_log is an additional log generated out of the current test specified by the current test number and subtestlog. Usually these logs occur in common subroutines called from a diagnostic test.

4 Error_type (diagnostic executive error) signals the diagnostic's state and any illegal behavior. This field indicates a condition that the diagnostic expects on detecting a failure. FE or EF in this field means that an unexpected exception or interrupt was detected. FF indicates an error as a result of normal testing, such as a miscompare. The possible codes are:

<table>
<thead>
<tr>
<th>Error Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF</td>
<td>Normal error exit from diagnostic</td>
</tr>
<tr>
<td>FE</td>
<td>Unanticipated interrupt</td>
</tr>
<tr>
<td>FD</td>
<td>Interrupt in cleanup routine</td>
</tr>
<tr>
<td>FC</td>
<td>Interrupt in interrupt handler</td>
</tr>
<tr>
<td>FB</td>
<td>Script requirements not met</td>
</tr>
<tr>
<td>FA</td>
<td>No such diagnostic</td>
</tr>
<tr>
<td>EF</td>
<td>Unanticipated exception in executive</td>
</tr>
</tbody>
</table>

5 ASCII messages Shows the name of the listing file that contains the failed diagnostic.

6 Vec identifies the SCB vector through which the unexpected exception or interrupt trapped, when the de_error field detects an unexpected exception or interrupt (FE or EF).

7 Prev_errs is four hex digits showing the number of previous errors that have occurred (four in Example 5–11).

Lines 2 and 3 of the error printout are parameters 1 through 10. When the diagnostics are running normally, these parameters are the same parameters listed in Example 4–3.

When returning a module for repair, always record the the test number, subtest, and Err_type from line 1 of the printout. Also record the Vec from line 2. If possible, record additional information. If the error can be saved onto a printer, then enclose the full printout with the failing module.
System Troubleshooting and Diagnostics

5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

---

**Note**

Do not confuse the countdown pattern of powerup tests with the test number. In the following the last countdown was 58; this number should not be reported! The test number was 31.

---

The countdown pattern is used to indicate progress in the power-up tests. The actual true test number associated with a countdown value can change from one release of the ROM code to another. For example:

```plaintext
KA50-A T1.2-156, VMB 2.14
Performing normal system tests.
72...71...70...69...68...67...66...65...64...63...62...61...60...59...58...
```

```plaintext
? Test Subtest_31_06 Loop_Subtest=05 Err_Type=FF DE Memory_Setup_CSRs.lis
Vecc=0000 Prev_Errs=0000 F1=C94AC94A F2=01000000 F3=00000002 F4=00000000
```

Minimum recording for this error is:

```plaintext
Test = 31
Subtest = 6
Loop_subtest = 5
Err_type = FF
Vec = 0.
```

Table 5-4 lists the hex LED display, the default action on errors, and the most likely unit that needs replacing reading from left to right. Example, 1,4 indicates 1 is most likely, then 4. The Default on Error column refers to the action taken by the diagnostic executive when the test fails in the script.

Memory tests are usually treated differently; when an error occurs, the memory tests usually try to continue and mark the bitmap. Test 40 reports failing pages in the bitmap.

When any memory test fails, always do a SHOW MEMORY to help identify the FRU. SHOW MEMORY will identify the FRU to a SET of SIMMs or to an individual SIMM if possible.

If a single set of SIMMs is present, and replacing a suspected bad SIMM or set does not fix the problem, assume that the system board is bad. Always check the seating of SIMMs before replacing. If nonvolatile data is lost after powerup or you always get a request to select a language at powerup, the battery may be bad.

Table 5-4 shows the various LED values and console terminal displays as they point to problems in field-replaceable units (FRUs).
### System Troubleshooting and Diagnostics

#### 5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

<table>
<thead>
<tr>
<th>On Error Hex LED</th>
<th>Normal Console Display</th>
<th>Default Action on Error</th>
<th>Falling Test Number</th>
<th>Test Description</th>
<th>FRU</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power-Up Tests (Script A1)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>None</td>
<td>Loop</td>
<td>None</td>
<td>Power up</td>
<td>1, 4</td>
</tr>
<tr>
<td>E</td>
<td>None</td>
<td>None</td>
<td>ROM code execution begun</td>
<td>1, 4</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>None</td>
<td>Loop</td>
<td>None</td>
<td>Wait for power</td>
<td>1, 4</td>
</tr>
<tr>
<td>B</td>
<td>72</td>
<td>Cont</td>
<td>9D</td>
<td>Utility</td>
<td>1, 4</td>
</tr>
<tr>
<td>B</td>
<td>71</td>
<td>Cont</td>
<td>42</td>
<td>Chk_for_interrupts</td>
<td>1, 3</td>
</tr>
<tr>
<td>9</td>
<td>70</td>
<td>Cont</td>
<td>35</td>
<td>B_Cache_diag_mode</td>
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<tr>
<td>B</td>
<td>69</td>
<td>Cont</td>
<td>33</td>
<td>NMC_powerup</td>
<td>1</td>
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<td>B</td>
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<td>Cont</td>
<td>D0</td>
<td>V_Cache_diag_mode</td>
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<td>B</td>
<td>66</td>
<td>Cont</td>
<td>D2</td>
<td>O_bit_Diag_mode</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>65</td>
<td>Cont</td>
<td>DF</td>
<td>O_bit_debug</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>64</td>
<td>Cont</td>
<td>46</td>
<td>P_cache_diag_mode</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>63</td>
<td>Cont</td>
<td>35</td>
<td>B_cache_diag_mode</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>62</td>
<td>Cont</td>
<td>DE</td>
<td>B_Cache_tag_debug</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>61</td>
<td>Cont</td>
<td>DD</td>
<td>B_Cache_data_debug</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>60</td>
<td>Cont</td>
<td>DA</td>
<td>PB_Flush_cache</td>
<td>1</td>
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<td>8</td>
<td>59</td>
<td>Halt</td>
<td>DC</td>
<td>NO_Memory_present</td>
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<td>8</td>
<td>58</td>
<td>Cont</td>
<td>31</td>
<td>Memory_Setup_CSRs</td>
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<td>8</td>
<td>57</td>
<td>Halt</td>
<td>30</td>
<td>Memory_Init_Bitmap</td>
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<td>7</td>
<td>56</td>
<td>Cont</td>
<td>91</td>
<td>CQBCI_powerup</td>
<td>1, 3</td>
</tr>
</tbody>
</table>

1Field-replaceable unit key:

1 = KA50
2 = MS44
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(continued on next page)
System Troubleshooting and Diagnostics
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Table 5-4 (Cont.)  KA50/51/55/56 Console Displays as Pointers to FRUs

<table>
<thead>
<tr>
<th>On Error Hex LED</th>
<th>Normal Console Display</th>
<th>Default Action on Error</th>
<th>Falling Test Number</th>
<th>Test Description</th>
<th>FRU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-Up Tests (Script A1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>7</td>
<td>55</td>
<td>Cont</td>
<td>90</td>
<td>CQBIC_registers</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>54</td>
<td>Cont</td>
<td>C6</td>
<td>SSC_powerup</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>53</td>
<td>Cont</td>
<td>52</td>
<td>SSC_Prog_timers</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>52</td>
<td>Cont</td>
<td>52</td>
<td>SSC_Prog_timers</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>51</td>
<td>Cont</td>
<td>53</td>
<td>SSC_TOY_Clock</td>
<td>1</td>
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<tr>
<td>C</td>
<td>50</td>
<td>Cont</td>
<td>C1</td>
<td>SSC_RAM_Data</td>
<td>1</td>
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<tr>
<td>C</td>
<td>49</td>
<td>Cont</td>
<td>34</td>
<td>SSC_ROM</td>
<td>1</td>
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<tr>
<td>C</td>
<td>48</td>
<td>Cont</td>
<td>C5</td>
<td>SSC_registers</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>47</td>
<td>Cont</td>
<td>55</td>
<td>Interval_Timer</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>46</td>
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<td>4F</td>
<td>Memory_Data</td>
<td>2, 1</td>
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<td>8</td>
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<td>Cont</td>
<td>4E</td>
<td>Memory_Byte</td>
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<td>8</td>
<td>44</td>
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<td>4B</td>
<td>Memory_Byte_Errors</td>
<td>2, 1</td>
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<tr>
<td>8</td>
<td>43</td>
<td>Cont</td>
<td>4A</td>
<td>Memory_ECC_SBEs</td>
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<td>8</td>
<td>42</td>
<td>Cont</td>
<td>4C</td>
<td>Memory_ECC_Logic</td>
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<td>41</td>
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<td>Memory_Addr_shorts</td>
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<td>Memory_addr_shorts</td>
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<td>Cont</td>
<td>48</td>
<td>Memory_addr_shorts</td>
<td>2, 1</td>
</tr>
</tbody>
</table>

1 Field-replaceable unit key:

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(continued on next page)
### System Troubleshooting and Diagnostics

#### 5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

<table>
<thead>
<tr>
<th>Error</th>
<th>Normal Console Display</th>
<th>Default Action on Error</th>
<th>Failing Test Number</th>
<th>Test Description</th>
<th>FRU¹</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>Power-Up Tests (Script A1)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
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<td>48</td>
<td>Memory_addr_shorts</td>
<td>2, 1</td>
</tr>
<tr>
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<td>34</td>
<td>Cont</td>
<td>48</td>
<td>Memory_addr_shorts</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>33</td>
<td>Cont</td>
<td>4D</td>
<td>Memory_address</td>
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<td>8</td>
<td>32</td>
<td>Cont</td>
<td>47</td>
<td>Memory_Refresh</td>
<td>2, 1</td>
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<td>31</td>
<td>Halt</td>
<td>40</td>
<td>Memory_count_pages</td>
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<td>Memory_count_pages</td>
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<td>29</td>
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<td>E4</td>
<td>DZ</td>
<td>1</td>
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<td>28</td>
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<td>54</td>
<td>Virtual_Mode</td>
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<td>27</td>
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<td>37</td>
<td>Cache_w_memory</td>
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<td>C</td>
<td>26</td>
<td>Cont</td>
<td>C2</td>
<td>SSC_RAM_Data_Addr</td>
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<td>25</td>
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<td>80</td>
<td>CQBIC_memory</td>
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<td>9</td>
<td>24</td>
<td>Cont</td>
<td>37</td>
<td>Cache_w_memory</td>
<td>1, 2</td>
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<tr>
<td>A</td>
<td>23</td>
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<td>51</td>
<td>FPA</td>
<td>1</td>
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<td>5</td>
<td>22</td>
<td>Cont</td>
<td>E2</td>
<td>SCSI_MAP</td>
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<td>20</td>
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<td>5F</td>
<td>SGEC</td>
<td>1</td>
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<td>19</td>
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<td>5C</td>
<td>SHAC</td>
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<td>B</td>
<td>18</td>
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<td>9A</td>
<td>INTERACTION</td>
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<td>7</td>
<td>17</td>
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<td>83</td>
<td>QZA_Intlpbck1</td>
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<td>7</td>
<td>16</td>
<td>Cont</td>
<td>84</td>
<td>QZA_Intlpbck2</td>
<td>3</td>
</tr>
</tbody>
</table>

¹Field-replaceable unit key:

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(continued on next page)
### System Troubleshooting and Diagnostics

#### 5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Table 5-4 (Cont.) KA50/51/55/56 Console Displays as Pointers to FRUs

<table>
<thead>
<tr>
<th>On Error Hex LED</th>
<th>Normal Console Display</th>
<th>Default Action on Error</th>
<th>Failing Test Number</th>
<th>Test Description</th>
<th>FRU$^1$</th>
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<tbody>
<tr>
<td>Power-Up Tests (Script A1)</td>
<td></td>
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<td>Cont</td>
<td>85</td>
<td>QZA_memory</td>
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<td>7</td>
<td>14</td>
<td>Cont</td>
<td>86</td>
<td>QZA_DMA</td>
<td>3</td>
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<td>7</td>
<td>13</td>
<td>Cont</td>
<td>63</td>
<td>QDSS_any</td>
<td>3</td>
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<tr>
<td>7</td>
<td>12</td>
<td>Cont</td>
<td>63</td>
<td>QDSS_any</td>
<td>3</td>
</tr>
<tr>
<td>B</td>
<td>11</td>
<td>Cont</td>
<td>DB</td>
<td>Speed</td>
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<td>10</td>
<td>Cont</td>
<td>EC</td>
<td>ASYNC</td>
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<td>09</td>
<td>Cont</td>
<td>E8</td>
<td>SYNC</td>
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<td>C</td>
<td>08</td>
<td>Cont</td>
<td>52</td>
<td>SSC_Prog_timers</td>
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<td>C</td>
<td>07</td>
<td>Cont</td>
<td>52</td>
<td>SSC_Prog_timers</td>
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</tr>
<tr>
<td>C</td>
<td>06</td>
<td>Cont</td>
<td>53</td>
<td>SSC_TOY_Clock</td>
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<td>C</td>
<td>05</td>
<td>Cont</td>
<td>C1</td>
<td>SSC_RAM_Data</td>
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<tr>
<td>B</td>
<td>04</td>
<td>Cont</td>
<td>55</td>
<td>Interval_Timer</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>03</td>
<td>Cont</td>
<td>41</td>
<td>Board_Reset</td>
<td>1, 3</td>
</tr>
</tbody>
</table>

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#### 5.3.1 FE Utility

In addition to the diagnostic console display and the LED code, the FE utility dumps the diagnostic state to the console (Example 5–12). This state indicates the major and minor test code of the test that failed, the 10 parameters associated with the test, and additional diagnostic state information.
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Example 5–12  FE Utility Example

```
>>> FF

Bitmap=00FF3000, Length=00001000, Checksum=807F, Busmap=00FF8000
Test_number=00, Subtest=00, Loop Subtest=00, Error_type=00
Error_vector=0060, Severity=02, Last_exception_PC=20057C37
Total_error_count=0004, Led display=08, Console display=81, save mchk code=00
parameter 1=00000002  2=00000000  3=2000116A  4=00000000  5=20057420
parameter 6=00000001  7=00000000  8=00000000  9=00000000  10=00000000
previous errors, Test Subtest Loop Subtest Error_type
Test 81 02 00 FE Test 40 06 00 FF Test E8 03 00 FF Test E4 02 00 FF
Flags=FFFF FFFCF 0408443E BCache Disable=06 KA50 128KB BC 14.0 ns
Return_stack=201406CC, Subtest_pc=2005D7FF, Timeout=000007D0

```
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Example 5–13  Failure Due to a Missing SIMM (One 16 Mbyte Set)

KA50-A V1.2, VMB 2.14
Performing normal system tests.
72...71...70...69...68...67...66...65...64...63...62...61...60...59...

? Test Subtest_DC_38  Loop_Subtest=05  Err_Type=FF  DE NO Memory present.xls

Vec=0000  Prev_Errs=0000  P1=C90AC90A  P2=00000000  P3=00000000  P4=00001006
P5=00000000  P6=7FF7FF33  P7=00000000  P8=00000000  P9=FFFF0000  P10=200636E4
r0=00000000  r1=21018000  r2=C90AC90A  r3=00000000  r4=00000000  r5=00000000
r6=00000000  r7=00000000  r8=00000000  r9=20140758  r10=FFFFF8  r11=FFFFF8F

dse=0000  cesr=00000000  intmsk=00  icsr=01  pcnts=FA00  paddr=FFFFF8  pcct1=FE13
ccct=00000000  bcetsts=03E0  bceodsts=0F00  cefsts=0001EC20  nesets=00

Error:  SIMM Set 1 (1E,1F,1G,1H), SSR = C90A
SIMM_1E = 16MB    SIMM_1F = 00MB ??    SIMM_1G = 16MB    SIMM_1H = 16MB

Total of 0MB, 0 good pages, 0 bad pages, 0 reserved pages
Normal operation not possible.

Note
The value listed by each SIMM is either 16 MB or 64 MB which indicates the full size of the set of SIMMs if all are present.

ACTION:

• If SIMM 1F is missing, install a SIMM.
• If SIMM 1F is present in socket, reseat the SIMM.
• If reseating SIMM 1F does not fix the problem, replace the SIMM with a new SIMM.
• At this point the system board is probably bad. If no new system board is available, try moving the SIMMs to the other set of sockets.

Example 5–14 shows a memory failure due to a missing SIMM. In this case two 16-MB sets (4 SIMMs of 4 MB each) are present with one SIMM missing in Set 1. Since one of memory is fully usable, all testing is completed. At the end SHOW MEMORY is automatically executed as before. SIMM 1H is missing or not installed correctly. The system is usable but with only 16 MB of memory instead of 32 MB.
Example 5–14  Failure Due to a Missing SIMM (Two 16 Mbyte Sets)

KA50-A T1.2-156, VMB 2.14
Performing normal system tests.
72..71..70..69..68..67..66..65..64..63..62..61..60..59..58..

? Test Subtest 31.06 Loop Subtest=05 Err Type=FF DE Memory Setup CSRs.lis
Vec=0000 Prev Errs=0000 P1=C94AC94A P2=01000000 P3=00000002 P4=00000000
P5=25800000 P6=FFFFFFFF P7=00000000 P8=00000000 P9=0000C94A P10=C94AC14A
r0=00000000 r1=21018000 r2=C94AC94A r3=81000000 r4=01000000 r5=04000000
r6=00000002 r7=21018048 r8=00000000 r9=20140758 r10=FFFFFFFF r11=FFFFFFFF

dser=0000 cesr=00000000 intmsk=00 icsr=00 pcsta=FA00 pcadr=FFFFF08 pctl=F013
cctl=00000006 bcetst=00360 bcetst=00 F00 cefst=002065E20 nest=0

57..56..55..54..53..52..51..50..49..48..47..46..45..44..43..42..
41..40..39..38..37..36..35..34..33..32..31..30..29..28..27..26..
25..24..23..22..21..20..19..18..17..16..15..14..13..12..11..10..
09..08..07..06..05..04..03..

16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 00000000 to 00FFFFFF, 16MB, 32768 good pages, 0 bad pages

Error: SIMM Set 1 (1E,1F,1G,1H), SSR = C94A

SIMM_1E = 16MB  SIMM_1F = 16MB  SIMM_1G = 16MB  SIMM_1H = 00MB ??

Total of 16MB, 32768 good pages, 0 bad pages, 104 reserved pages

Normal operation not possible.

ACTION:

- If SIMM 1H is missing, install a SIMM.
- If SIMM 1H is present in socket, reseat the SIMM.
- If reseating SIMM 1H does not fix the problem then replace the SIMM with a new SIMM.
- At this point the system board is probably bad.

Example 5–15 shows a memory failure due to a bad SIMM. In this case two 16-MB sets (4 SIMMs of 4 MB each) are present with one bad SIMM. SIMM 1H is marked as being bad.
Example 5–15  Failure Due to a Bad SIMM

KA50-A V1.2, VMEB 2.14
Performing normal system tests.
72..71..70..69..68..67..66..65..64..63..62..61..60..59..58..57..
56..55..54..53..52..51..50..49..48..47..46..45..44..43..42..41..
40..39..38..37..36..35..34..33..32..31..30..

? Test_Subtest_40_06  Loop_Subtest=00  Err_Type=FF  DE_Memory_count_pages.ls
29..28..27..26..25..24..23..22..21..20..19..18..17..16..15..14..
13..12..11..10..09..08..07..06..05..04..03..

16 MB RAM, SIMM Set (OA,OB,OC,OD) present
Memory Set 0: 000000000 to 00FFFFFF, 16MB, 32768 good pages, 0 bad pages

Error: SIMM Set 1 (1E,1F,1G,1H), SSR = C14A
      SIMM 1E = 16MB  SIMM 1F = 16MB  SIMM 1G = 16MB  SIMM 1H = 16MB ??
Memory Set 1: 010000000 to 01FFFFFE, 16MB, 0 good pages, 32768 bad pages
Total of 32MB, 32768 good pages, 32768 bad pages, 112 reserved pages

>>> ACTION

• Reseat the SIMM 1H.

• If reseating SIMM 1H does not fix the problem then replace the SIMM with a new SIMM.

• At this point the system board is probably bad.

Example 5–16 indicates that a large SIMM is mixed in with a set of small SIMMs. If a full set of SIMMs is present and one or more is the incorrect size then the diagnostic code will configure the set as a small set and run the tests. In this example, SIMM 1G is the wrong size SIMM. Because the set is configured as a small set, it is usable as a 16-MB set.
System Troubleshooting and Diagnostics
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Example 5–16 SIMM Wrong Size

Error: SIMM Set 1 (1E,1F,1G,1H), SSR = C14A
SIMM 1E = 16MB    SIMM 1F = 16MB    SIMM 1G = 64MB ??    SIMM 1H = 16MB
Memory Set 1: 01000000 to 01FFFFFF, 16MB, 32768 good pages, 0 bad pages

ACTION:

Replace SIMM 1G with one of the correct size.

The diagnostics cannot always determine which SIMM caused a failure. If this occurs and more than one set is present, usually the failing set can be identified by using the SHOW MEMORY command.

>>>SHOW MEMORY
16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 00000000 to 00FFFFFF, 16MB, 32768 good pages, 0 bad pages
16 MB RAM, SIMM Set (1E,1F,1G,1H) present
Memory Set 1: 01000000 to 01FFFFFF, 16MB, 32768 good pages, 32768 bad pages
Total of 32MB, 32768 good pages, 32768 bad pages, 112 reserved pages

ACTION:

Replace SIMM set 1 (1E,1F,1G,1H).

After installing a new set of SIMMs and successfully running power-up tests, run memory test script A8.

>>>T A8

Note

Script A9 is another memory test script. This script will stop on the first occurrence of any error. It will also stop on a soft error. If a failure occurs in A9 and if A9 then runs successfully 10 times and script A8 runs without error the problem is a soft error and does not require action.

Note

If a memory failure is marked in the bitmap, it will not be erased until either the system is powered up or the bitmap placing test is run with
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

parameter P4 set to 0 to rebuild the bitmap.

To force rebuilding the bitmap to all good memory, enter the following commands:

\[ \text{T 30 0 0 0 0} \quad \text{; T 30 will not work by itself.} \]
\[ \text{T 0} \quad \text{; rerun powerup script} \]

5.4 Using MOP Ethernet Functions to Isolate Failures

The console requester can receive LOOPED_DATA messages from the server by sending out a LOOP_DATA message using NCP to set this up. An example follows.

Identify the Ethernet adapter address for the system under test (system 1) and attempt to boot over the network.

```plaintext
*** system 1 (system under test) ***
>>>SHOW ETHERNET
Ethernet Adapter
-EZAO (08-00-2B-28-18-2C)
>>>BOOT EZAO
(RBOOT/R5:2 EZAO)
  2.
  -EZAO
Retrying network bootstrap.

Unless the system is able to boot, the "Retrying network bootstrap" message will display every 8–12 minutes.

Identify the system's Ethernet circuit and circuit state, enter the SHOW KNOWN CIRCUITS command from the system conducting the test (system 2).

*** system 2 (system conducting test) ***

5 MCR NCP
NCP>SHOW KNOWN CIRCUITS

Known Circuit Volatile Summary as of 14-NOV-1991 16:01:53

<table>
<thead>
<tr>
<th>Circuit</th>
<th>State</th>
<th>Loopback Name</th>
<th>Adjacent Routing Node</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISA-0</td>
<td>on</td>
<td></td>
<td>25.1023 (LAR25)</td>
</tr>
</tbody>
</table>
```
System Troubleshooting and Diagnostics
5.4 Using MOP Ethernet Functions to Isolate Failures

NCP> SET CIRCUIT ISA-0 STATE OFF
NCP> SET CIRCUIT ISA-0 SERVICE ENABLED
NCP> SET CIRCUIT ISA-0 STATE ON
NCP> LOOP CIRCUIT ISA-0 PHYSICAL ADDRESS 08-00-2B-28-18-2C
WITH ERRORS
NCP> EXIT

If the loopback message was received successfully, the NCP prompt will reappear with no messages.

The following two examples show how to perform the Loopback Assist Function using another node on the network as an assistant (system 3) and the system under test as the destination. Both the assistant and the system under test are attempting to boot from the network. We will also need the physical address of the assistant node.

***system #3 (loopback assistant)***

>>> SHOW ETHERNET
Ethernet Adapter
-EZAO (08-00-2B-1E-76-9E)
>>> b ezao
(BOOT/R5:2 EZAO)
...
-EZAO
Retrying network bootstrap.

***system #2***

NCP> LOOP CIRCUIT ISA-0 PHYSICAL ADDRESS 08-00-2B-28-18-2C ASSISTANT PHYSICAL
ADDRESS 08-00-2B-1E-76-9E WITH MIXED COUNT 20 LENGTH 200 HELP FULL
NCP>

Instead of using the physical address, you could use the assistant node's area address. When using the area address, system 3 is running the OpenVMS operating system.

***system #3***

SMC R NCP
NCP> SHOW NODE KIATCH
Executor node = 25.900 (KIATCH)
State = on
Identification = DECnet-VAX V5.4-1, OpenVMS V5.4-2
Active links = 2

NCP> SHOW KNOWN LINES CHARACTERISTICS
Known Line Volatile Characteristics as of 27-FEB-1992 11:20:50
Line = ISA-0
System Troubleshooting and Diagnostics

5.4 Using MOP Ethernet Functions to Isolate Failures

Receive buffers = 6
Controller = normal
Protocol = Ethernet
Service timer = 4000
Hardware address = 08-00-28-18-76-9E
Device buffer size = 1498

NCP>SET CIRCUIT ISA-0 STATE OFF
NCP>SET CIRCUIT ISA-0 SERVICE ENABLED
NCP>SET CIRCUIT ISA-0 STATE ON
NCP>EXIT
$

***system 2***
5 MCR NCP
NCP>LOOP CIRCUIT ISA-0 PHYSICAL ADDRESS 08-00-28-28-18-2C ASSISTANT NODE 25.900
WITH MIXED COUNT 20 LENGTH 200 HELP FULL
NCP>EXIT
$

Note

The kernel's Ethernet buffer is 1024 bytes deep for the LOOP functions and will not support the maximum 1500-byte transfer length.

In order to verify that the address is reaching this node, a remote node can examine the status of the periodic SYSTEM_IDs sent by the KA50/51/55/56 Ethernet server. The SYSTEM_ID is sent every 8–12 minutes using NCP as in the following example:

***system 2***
5 MCR NCP
NCP>SET MODULE CONFIGURATOR CIRCUIT ISA-0 SURVEILLANCE ENABLED
NCP>SHOW MODULE CONFIGURATOR KNOWN CIRCUITS STATUS TO ETHER.LIS
NCP>EXIT
5 TYPE ETHER.LIS

Circuit name = ISA-0
Surveillance flag = enabled
Elapsed time = 00:09:37
Physical address = 08-00-28-28-18-2C
Time of last report = 27-Feb 11:50:34
Maintenance version = V4.0.0
Function list = Loop, Multi-block loader, Boot, Data link counters
Hardware address = 08-00-28-28-18-7C
Device type = ISA

Depending on your network, the file used to receive the output from the SHOW MODULE CONFIGURATOR command may contain many entries, most of which do not apply to the system you are testing. It is helpful to use an editor to search the file for the Ethernet hardware address of the system under test.
5.4 Using MOP Ethernet Functions to Isolate Failures

Existence of the hardware address verifies that you are able to receive the address from the system under test.

5.5 Interpreting User Environmental Test Package (UETP) OpenVMS Failures

When UETP encounters an error, it reacts like a user program. It either returns an error message and continues, or it reports a fatal error and terminates the image or phase. In either case, UETP assumes the hardware is operating properly and it does not attempt to diagnose the error.

If the cause of an error is not readily apparent, use the following methods to diagnose the error:

- **OpenVMS Error Log Utility**—Run the Error Log Utility to obtain a detailed report of hardware and system errors. Error log reports provide information about the state of the hardware device and I/O request at the time of each error. For information about running the Error Log Utility, refer to the *OpenVMS Error Log Utility Manual* and Section 5.2 of this manual.

- **Diagnostic facilities**—Use the diagnostic facilities to test exhaustively a device or medium to isolate the source of the error.

5.5.1 Interpreting UETP Output

You can monitor the progress of UETP tests at the terminal from which they were started. This terminal always displays status information, such as messages that announce the beginning and end of each phase and messages that signal an error.

The tests send other types of output to various log files, depending on how you started the tests. The log files contain output generated by the test procedures. Even if UETP completes successfully, with no errors displayed at the terminal, it is good practice to check these log files for errors. Furthermore, when errors are displayed at the terminal, check the log files for more information about their origin and nature.

5.5.1.1 UETP Log Files

UETP stores all information generated by all UETP tests and phases from its current run in one or more UETP.LOG files, and it stores the information from the previous run in one or more OLDUETP.LOG files. If a run of UETP involves multiple passes, there will be one UETP.LOG or one OLDUETP.LOG file for each pass.
System Troubleshooting and Diagnostics

5.5 Interpreting User Environmental Test Package (UETP) OpenVMS Failures

At the beginning of a run, UETP deletes all OLDEUTP.LOG files, and renames any UETP.LOG files to OLDEUTP.LOG. Then UETP creates a new UETP.LOG file and stores the information from the current pass in the new file. Subsequent passes of UETP create higher versions of UETP.LOG. Thus, at the end of a run of UETP that involves multiple passes, there is one UETP.LOG file for each pass. In producing the files UETP.LOG and OLDEUTP.LOG, UETP provides the output from the two most recent runs.

If the run involves multiple passes, UETP.LOG contains information from all the passes. However, only information from the latest run is stored in this file. Information from the previous run is stored in a file named OLDEUTP.LOG. Using these two files, UETP provides the output from its tests and phases from the two most recent runs.

The cluster test creates a NETSERVER.LOG file in SYS$TEST for each pass on each system included in the run. If the test is unable to report errors (for example, if the connection to another node is lost), the NETSERVER.LOG file on that node contains the result of the test run on that node. UETP does not purge or delete NETSERVER.LOG files; therefore, you must delete them occasionally to recover disk space.

If a UETP run does not complete normally, SYS$TEST might contain other log files. Ordinarily these log files are concatenated and placed within UETP.LOG. You can use any log files that appear on the system disk for error checking, but you must delete these log files before you run any new tests. You may delete these log files yourself or rerun the entire UETP, which checks for old UETP.LOG files and deletes them.

5.5.1.2 Possible UETP Errors
This section is intended to help you identify problems you might encounter running UETP.

The following are the most common failures encountered while running UETP:

- Wrong quotas, privileges, or account
- UETINIT01 failure
- Ethernet device allocated or in use by another application
- Insufficient disk space
- Incorrect VAXcluster setup
- Problems during the load test
- DECnet–VAX error
- Lack of default access for the FAL object
System Troubleshooting and Diagnostics
5.5 Interpreting User Environmental Test Package (UETP) OpenVMS Failures

- Errors logged but not displayed
- No PCB or swap slots
- Hangs
- Bug checks and machine checks

For more information refer to the VAX 3520, 3540 OpenVMS Installation and Operations (ZKS166) manual.

5.6 Using Loopback Tests to Isolate Failures

You can use external loopback tests to isolate problems with the console port, and Ethernet controller (SGEC chip).

5.6.1 Testing the Console Port

To test the console port at power-up, set the Power-Up Mode switch on the console module to the Loop Back Test Mode position (bottom) and install an H3103 loopback connector into the MMJ. The H3103 connects the console port transmit and receive lines. At power-up, the SLU_EXT_LOOPBACK test then runs a continuous loopback test.

While the test is running, the LED display on the console module should alternate between 6 and 3. A value of 6 latched in the display indicates a test failure. If the test fails, one of the following parts is faulty: the KA50/51/55/56 or the cabling.

To test out to the end of the console terminal cable:

1. Plug the MMJ end of the console terminal cable into the back BA42B.
2. Disconnect the other end of the cable from the terminal.
3. Place an H8572 adapter into the disconnected end of the cable.
4. Connect the H3103 to the H8572.
5. Cycle power and observe the LED.

5.6.2 Embedded Ethernet Loopback Testing

Note

Before running Ethernet loopback tests, check that the problem is not due to a missing terminator on a ThinWire T-connector.
System Troubleshooting and Diagnostics
5.6 Using Loopback Tests to Isolate Failures

Test 5F is the internal loopback test for SGEC (Ethernet controller).

>>>T 5F

For an external SGEC loopback, enter "1".

>>>T 5F 1

Before running test 5F on the ThinWire Ethernet port, connect an H8223 T-connector with two H8225 terminators.

Before running test 5F on the standard Ethernet port, you must have a 12–22196–02 loopback connector installed.

______________________ Note _______________________

Make sure the Ethernet Connector Switch is set for the correct Ethernet port.

______________________

T 59 polls other nodes on Ethernet to verify SGEC functionality. The Ethernet cable must be connected to a functioning Ethernet. A series of MOP messages are generated; look for response messages from other nodes.

>>>T 59

Reply received from node: AA-00-04-00-FC-64
Total responses: 1
Reply received from node: AA-00-04-00-47-16
Total responses: 2
Reply received from node: 08-00-2B-15-48-70
Total responses: 3
...

Reply received from node: AA-00-04-00-17-14
Total responses: 25
>>>
### Table 5–5 Loopback Connectors for Common Devices

<table>
<thead>
<tr>
<th>Device</th>
<th>Module Loopback</th>
<th>Cable Loopback</th>
</tr>
</thead>
<tbody>
<tr>
<td>CXA16/CXB16</td>
<td>H3103 + H8572(^1)</td>
<td>-</td>
</tr>
<tr>
<td>CXY08</td>
<td>H3046 (50-pin)</td>
<td>H3197 (25-pin)</td>
</tr>
<tr>
<td>DIV32</td>
<td>H3072</td>
<td>-</td>
</tr>
<tr>
<td>DPV11</td>
<td>12–15336–10 or H325</td>
<td>H329 (12–27351–01)</td>
</tr>
<tr>
<td>DRQB3</td>
<td>-</td>
<td>17–01481–01 (from port 1 to port 2)</td>
</tr>
<tr>
<td>DRV1W</td>
<td>70–24767–01</td>
<td>-</td>
</tr>
<tr>
<td>DZQ11</td>
<td>12–15336–10 or H325</td>
<td>H329 (12–27351–01)</td>
</tr>
<tr>
<td>Ethernet(^2)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IBQ01</td>
<td>IBQ01–TA</td>
<td>-</td>
</tr>
<tr>
<td>IEQ11</td>
<td>17–01988–01</td>
<td>-</td>
</tr>
<tr>
<td>KMV1A</td>
<td>H3255</td>
<td>H3251</td>
</tr>
<tr>
<td>KZQSA</td>
<td>12–30552–01</td>
<td>-</td>
</tr>
<tr>
<td>LPV11</td>
<td>12–15336–11</td>
<td>-</td>
</tr>
</tbody>
</table>

\(^1\)Use the appropriate cable to connect transmit-to-receive lines. \(^2\)H3101 and H3103 are double-ended cable connectors.

For ThinWire, use H8223–00 plus two H8225–00 terminators. For standard Ethernet, use 12–22196–02.
FEPROM Firmware Update

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95, and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q-bus and DSSI, will appear on the console and/or printouts from time to time.

KA50/51/55/56 firmware is located on four chips, each 128 K by 8 bits of FLASH programmable EPROMs, for a total of 512 Kbytes of ROM. (A FLASH EPROM (FEPROM) is a programmable read-only memory that uses electrical (bulk) erasure rather than ultraviolet erasure.)

FEPROMs provide nonvolatile storage of the CPU power-up diagnostics, console interface, and operating system primary bootstrap (VMB). An advantage of this technology is that the entire image in the FEPROMs may be erased, reprogrammed, and verified in place without removing the CPU module or replacing components.

A slight disadvantage to the FEPROM technology is that the entire part must be erased before reprogramming. Hence, there is a small "window of vulnerability" when the CPU has inoperable firmware. Normally, this window is less than 30 seconds. Nonetheless, an update should be allowed to execute undisturbed.

Firmware updates are provided through a package called the Firmware Update Utility. A Firmware Update Utility contains a bootable image, which can be booted from tape or Ethernet, that performs the FEPROM update. Firmware update packages, like software, are distributed through Digital's SSB. Service engineers are notified of updates through a service blitz or Engineering Change Order (ECO)/Field Change Order (FCO) notification.
**Note**

The NVAX CPU chip has an area called the Patchable Control Store (PCS), which can be used to update the microcode for the CPU chip. Updates to the PCS require a new version of the firmware.

A Firmware Update Utility image consists of two parts, the update program and the new firmware, as shown in Figure 6–1. The update program uniformly programs, erases, reprograms, and verifies the entire FEPROM.

**Figure 6–1 Firmware Update Utility Layout**

```
Update Program

New Firmware Image
```

Once the update has completed successfully, normal operation of the system may continue. The operator may then either halt or reset the system and reboot the operating system.

### 6.1 Preparing the Processor for a FEPROM Update

Complete the following steps to prepare the processor for a FEPROM update:

1. The system manager should perform operating system shutdown.

2. Enter console mode by pressing the Halt button once to halt the system. If the Break Enable/Disable switch on the console module is set to enable (indicated by 1), you can halt the system by pressing the Break key on the console terminal.
6.2 Updating Firmware via Ethernet

To update firmware via the Ethernet, the “client” system (the target system to be updated) and the “server” system (the system that serves boot requests) must be on the same Ethernet segment. The Maintenance Operation Protocol (MOP) is the transport used to copy the network image.

Use the following procedure to update firmware via the Ethernet:

1. Enable the server system’s NCP circuit using the following OpenVMS commands:

   $ MCR NCP
   NCP>SET CIRCUIT <circuit> STATE OFF
   NCP>SET" CIRCUIT <circuit> SERVICE ENABLED
   NCP>SET CIRCUIT <circuit> STATE ON
6.2 Updating Firmware via Ethernet

Where <circuit> is the system Ethernet circuit. Use the SHOW KNOWN CIRCUITS command to find the name of the circuit.

Note

The SET CIRCUIT STATE OFF command will bring down the system's network.

Note

2. Copy the file containing the updated code to the MOM$LOAD area on the server (this procedure may require system privileges). Refer to the Firmware Update Utility Release Notes for the Ethernet bootable filename. Use the following command to copy the file:

$ COPY <filename>.SYS MOM$LOAD:*.*

Where <filename> is the Ethernet bootable filename provided in the release notes.

3. On the client system, enter the command BOOT/100 EZ at the console prompt (>>>).

The system then prompts you for the name of the file.

Note

Do NOT type the "SYS" suffix when entering the Ethernet bootfile name. The MOP load protocol only supports 15 character filenames.

Note

4. After the FEPROM upgrade program is loaded, simply type "Y" at the prompt to start the FEPROM blast. Example 6–1 provides a console display of the FEPROM update program.

Caution

Once you enter the bootfile name, do not interrupt the FEPROM blasting program, as this can damage the CPU module. The program takes several minutes to complete.
Example 6-1  FEPROM Update via Ethernet

***** On Server System *****

$ MCR NCP
NCP>SET CIRCUIT ISA-0 STATE OFF
NCP>SET CIRCUIT ISA-0 SERVICE ENABLED
NCP>SET CIRCUIT ISA-0 STATE ON
NCP>EXIT
$
$ COPY KA50_V41_E1.SYS MEM$LOAD:*.*
$

***** On Client System *****

>>>b/100 eza0
(BOOT/R5:100 EZA0)
2..
Bootfile: ka50_v12
-EZA0
 1:0..

FEPROM update program

---CAUTION---

--- Executing this program will change your current FEPROM ---
Do you want to continue [Y/N] ? : y
Blasting in V1.2-41. The program will take at most several minutes.

DO NOT ATTEMPT TO INTERRUPT PROGRAM EXECUTION
Doing so may result in loss of operable state !!!

10...9...8...7...6...5...4...3...2...1...0
FEPROM Programming successful

?06 HLT INST
   PC = 00008E24

Note

If the update does not work, check to be sure the "write enable" on-board jumper is installed (see Figure 6-2).

5. Recycle power or enter "T 0" at the console prompt (>>>).
6. If the customer requires, return the jumper on the module to the "write disable mode" setting.
6.3 Updating Firmware via Tape

To update firmware via tape, the system must have a TZ30, TF85, TK70, TK50 or TLZ04 tape drive.

If you need to make a bootable tape, copy the bootable image file to a tape as shown in the following example. Refer to the release notes for the name of the file.

$ INIT MKA500:"VOLUME_NAME"
$ MOUNT/BLOCK_SIZE = 512 MKA500:"VOLUME_NAME"
$ COPY/CONTIG<file_name> MKA500:<file_name>
$ DISMOUNT MKA500
$

Use the following procedure to update firmware via tape:

1. Be sure the on board jumper is in the correct ("write enable mode") position (Section 6.1).

2. At the console prompt (>>>), enter the BOOT/100 command for the tape device, for example: BOOT/100 MKA500.

   Use the SHOW DEVICE command if you are not sure of the device name for the tape drive.

   The system prompts you for the name of the file. Enter the bootfile name.

3. After the FEPROM upgrade program is loaded, simply type "Y" at the prompt to start the FEPROM blast. Example 6–2 provides a console display of the FEPROM update program.

   ____________________________________________________________________________
   Caution
   ____________________________________________________________________________

   Once you enter the bootfile name, do not interrupt the FEPROM blasting program, as this can damage the CPU module. The program takes several minutes to complete.

   ____________________________________________________________________________

4. Press the Restart button on the SCP or enter "T 0" at the console prompt (>>>).

5. If the customer requires, return the jumper on the CPU module to the "write disable mode" setting.
Example 6-2  FEPROM Update via Tape

>>> BOOT/100 MKA500
   (BOOT/R5:100 MKA500)

  2..
Boot file: MKA50_V41_RZ
-MKA500

  1.0..
FEPROM update program

---CAUTION---
--- Executing this program will change your current FEPROM ---

Do you want to continue [Y/N]? : y

Blasting in V1.2-41. The program will take at most several minutes.

DO NOT ATTEMPT TO INTERRUPT PROGRAM EXECUTION
Doing so may result in loss of operable state !!!

+----------------------------------------+
| 10...9...8...7...6...5...4...3...2...1...0 |
+----------------------------------------+

FEPROM Programming successful

206 HL TinS
   PC = 00008E24

>>>  

6.4 FEPROM Update Error Messages

The following is a list of error messages generated by the FEPROM update program and actions to take if the errors occur.

MESSAGE:
?? ERROR update enable jumper is disconnected
  unable to blast ROMs...
ACTION:
Reposition update enable jumper (Section 6.1).

MESSAGE:
?? ERROR, FEPROM programming failed
ACTION:
Turn off the system, then turn it on. If you see the banner message as
expected, reenter console mode and try booting the update program again.
If you do not see the usual banner message, replace the CPU module.
Patchable Control Store (PCS) Loading Error Messages

The following is a list of error messages that may appear if there is a problem with the PCS. The PCS is loaded as part of the power-up stream (before ROM-based diagnostics are executed).

**MESSAGE:**
CPU is not an NVAX

**COMMENT:**
CPU_TYPE as read in NVAX SID is not = 19 (decimal), as is should be for an NVAX processor.

**MESSAGE:**
Microcode patch/CPU rev mismatch

**COMMENT:**
Header in microcode patch does not match MICROCODE_REV as read in NVAX SID.

**MESSAGE:**
Pcs Diagnostic failed

**COMMENT:**
Something is wrong with the PCS. Replace the NVAX chip (or CPU module).
Address Assignments

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95 and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q-bus and DSSI, will appear on the console and/or printouts from time to time.

A.1 KA50/51/55/56 General Local Address Space Map
Address Assignments
A.1 KA50/51/55/56 General Local Address Space Map

**VAX Memory Space**

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 0000 - 1FFFF FFFF</td>
<td>Local Memory Space (512MB)</td>
</tr>
</tbody>
</table>

**VAX I/O Space**

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 0000 - 2000 1FFFF</td>
<td>Local Q22-Bus I/O Space (8KB)</td>
</tr>
<tr>
<td>2000 2000 - 2003 FFFF</td>
<td>Reserved Local I/O Space (24KB)</td>
</tr>
<tr>
<td>2008 0000 - 201F FFFF</td>
<td>Local Register I/O Space (1.5MB)</td>
</tr>
<tr>
<td>2020 0000 - 23FF FFFF</td>
<td>Reserved Local I/O Space (62.5MB)</td>
</tr>
<tr>
<td>2400 0000 - 27FF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>2008 0000 - 2BFF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>2C08 0000 - 2FFF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>3000 0000 - 303F FFFF</td>
<td>Local Q22-Bus Memory Space (4MB)</td>
</tr>
<tr>
<td>3040 0000 - 33FF FFFF</td>
<td>Reserved Local I/O Space (60MB)</td>
</tr>
<tr>
<td>3400 0000 - 37FF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>3800 0000 - 3BFF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>3C00 0000 - 3FFF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>E004 0000 - E007 FFFF</td>
<td>Local ROM Space</td>
</tr>
</tbody>
</table>
### A.2 KA50/51/55/56 Detailed Local Address Space Map

Local Memory Space (up to 128MB) 0000 0000 - 7FF FFFF
Q22-bus Map - top 32KB of Main Memory

**VAX I/O Space**

---

**Local Q22-bus I/O Space**
- **Reserved Q22-bus I/O Space** 2000 0000 - 2000 0007
- **Q22-bus Floating Address Space** 2000 0008 - 2000 07FF
- **User Reserved Q22-bus I/O Space** 2000 0800 - 2000 0FFF
- **Reserved Q22-bus I/O Space** 2000 1000 - 2000 1F3F
- **Interprocessor Comm Reg** 2000 1F40
- **Reserved Q22-bus I/O Space** 2000 1F44 - 2000 1FFF

**Local Register I/O Space** 2000 2000 - 2003 FFFF
- **Reserved Local Register I/O Space** 2000 4000 - 2000 422F
- **Reserved Local Register I/O Space** 2000 4280 - 2000 7FFF
- **Reserved Local Register I/O Space** 2000 40B0 - 2000 422F
- **NICSR0 - Vector Add, IPL, Sync/Async** 2000 8000
- **NICSR1 - Polling Demand Register** 2000 8004
- **NICSR2** - Reserved 2000 8008
- **NICSR3 - Receiver List Address** 2000 800C
- **NICSR4 - Transmitter List Address** 2000 8010
- **NICSR5 - Status Register** 2000 8014
- **NICSR6 - Command and Mode Register** 2000 8018
- **NICSR7 - System Base Address** 2000 801C
- **NICSR8** - Reserved 2000 8020*
- **NICSR9 - Watchdog Timers** 2000 8024*
- **NICSR10** - Reserved 2000 8028*
- **NICSR11 - Rev Num & Missed Frame Count** 2000 802C*
- **NICSR12** - Reserved 2000 8030*
- **NICSR13 - Breakpoint Address** 2000 8034*
- **NICSR14** - Reserved 2000 8038*
- **NICSR15 - Diagnostic Mode & Status** 2000 803C
- **Reserved Local Register I/O Space** 2000 8040 - 2003 FFFF
Address Assignments
A.2 KA50/51/55/56 Detailed Local Address Space Map

KA50/51/55/56 DETAILED LOCAL ADDRESS SPACE MAP (Cont.)

*******************************************************
*  *
* Q-22 Bus Local Register I/O Space  2008 0000 - 201F FFFF
* DMA System Configuration Register  2008 0000
* DMA System Error Register         2008 0004
* DMA Master Error Address Register 2008 0008
* DMA Slave Error Address Register  2008 000C
* Q22-bus Map Base Register         2008 0010
* Reserved Local Register I/O Space 2008 0014 - 2008 00FF
*  *
*******************************************************
  
Reserved Local Register I/O Space  2008 0194 - 2008 3FFF
Boot and Diagnostic Reg (32 Copies) 2008 4000 - 2008 407C
Reserved Local Register I/O Space  2008 4080 - 2008 7FFF

*******************************************************
*  *
* Q22-bus Map Registers  2008 8000 - 2008 FFFF
* Reserved Local Register I/O Space  2009 0000 - 2013 FFFF
*  *
*******************************************************

SSC CSRs

SSC Base Address Register  2014 0000
SSC Configuration Register  2014 0010
CP Bus Timeout Control Register  2014 0020
Diagnostic LED Register  2014 0030
Reserved Local Register I/O Space  2014 0034 - 2014 006B
Address Assignments
A.2 KA50/51/55/56 Detailed Local Address Space Map

KA50/51/55/56 DETAILED LOCAL ADDRESS SPACE MAP (Cont.)

VAX IPRs implemented by NCA

Interval Clock Control Status Reg 2100 0060
Next Interval Count Register 2100 0064
Interval Count Register 2100 0068

NMC CSRs

O-bit Data Registers 2101 0000 - 2101 7FFF
Main Memory Configuration Reg 0 2101 8000
Main Memory Configuration Reg 1 2101 8004
Main Memory Signature Register 0 2101 8020
Main Memory Signature Register 1 2101 8024
Main Memory Error Address Register 2101 8040
Main Memory Error Status Register 2101 8044
Main Memory Mode Control and Diagnostic Register
O-bit Address and Mode Register 2101 804C

NCA CSRs

Error Status Register 2102 0000
Mode Control and Diagnostic Reg 2102 0004
CP1 Slave Error Address Register 2102 0006
CP2 Slave Error Address Register 2102 000C
CP1 IO Error Address Register 2102 0010
CP2 IO Error Address Register 2102 0014
NDAL Error Address Register 2102 0018
Address Assignments
A.2 KA50/51/55/56 Detailed Local Address Space Map

KA50/51/55/56 DETAILED LOCAL ADDRESS SPACE MAP (Cont.)

******************************************************************************
* OPTIONAL KZDDA SCSI CONTROLLER
* *
*  ** SCSI DMA address register  21C00000  
*  ** SCSI DMA direction register  21C00004  
*  ** Interrupt mask register  21C00008  
*  ** Interrupt pending register  21C0000C  
*  ** SCSI Controller (53C94) registers  22000080 - 220000B0  
*      (13 byte regs (0:A,B,C) on LW boundary)
*  ** scsicr0  22000080  
*  ** scsicr1  22000084  
*  ** scsicr2  22000088  
*  ** scsicr3  2200008C  
*  ** scsicr4  22000090  
*  ** scsicr5  22000094  
*  ** scsicr6  22000098  
*  ** scsicr7  2200009C  
*  ** scsicr8  220000A0  
*  ** scsicr9  220000A4  
*  ** scsicra  220000A8  
*  ** scsicrb  220000AC  
*  ** scsicrc  220000B0  
*  ** SCSI DMA Map registers  23000000 - 23007FFF  
*       (8,192 32 bit registers)
******************************************************************************

EDAL BUS DEVICES

******************************************************************************
* OPTIONAL SYNC COMMUNICATION DEVICE
* *
*  ** Register sets of the SYNC ports  2400 0000 - 24FF FFFF  
*  ** Option ROM Space  ???? ???? - ???? ????  
* *
******************************************************************************

QUART (DC7085) Registers  2500 0000 - 2500 0007  
SCSI DMA Address Register  25C0 0000  
SCSI DMA Direction Register  25C0 0004  
Interrupt Mask Register  25C0 0008  
Interrupt Pending Register  25C0 000C  
SCSI Controller (53C94) Registers  2600 0080 - 2600 00BF  
SCSI DMA Map Registers  2700 0000 - 2700 7FFF
Address Assignments
A.2 KA50/51/55/56 Detailed Local Address Space Map

KA50/51/55/56 DETAILED LOCAL ADDRESS SPACE MAP (Cont.)
********************************************************************************
* OPTIONAL ASYNC COMMUNICATION DEVICE
*
* Register sets of the ASYNC ports 3E00 0000 - 3E00 000E
* Option ROM Space 3E01 0000 - 3E02 FFFF
*
********************************************************************************

Local FEPROM Space E004 0000 - E007 FFFF
VAX System Type Register (In ROM) E004 0004
Local FEPROM - (Halt Protected) E004 0000 - E007 FFFF

********************************************************************************
The following addresses allow those KA50/51/55/56 Internal Processor Registers that are implemented in the SSC chip (External, Internal Processor Registers) to be accessed via the local I/O page. These addresses are documented for diagnostic purposes only and should not be used by non-diagnostic programs.

Time Of Year Register 2014 006C
Console Storage Receiver Status 2014 0070*
Console Storage Receiver Data 2014 0074*
Console Storage Transmitter Status 2014 0078*
Console Storage Transmitter Data 2014 007C*
Console Receiver Control/Status 2014 0080
Console Receiver Data Buffer 2014 0084
Console Transmitter Control/Status 2014 0088
Console Transmitter Data Buffer 2014 008C
Reserved Local Register I/O Space 2014 0090 - 2014 00DB
I/O Bus Reset Register 2014 00DC
Reserved Local Register I/O Space 2014 00E0
Reserved Local Register I/O Space 2014 00FC - 2014 00FF

* These registers are not fully implemented, accesses yield UNPREDICTABLE results.

********************************************************************************
Address Assignments
A.2 KA50/51/55/56 Detailed Local Address Space Map

KA50/51/55/56 DETAILED LOCAL ADDRESS SPACE MAP (Cont.)

Local Register I/O Space (Cont.)
- Timer 0 Control Register 2014 0100
- Timer 0 Interval Register 2014 0104
- Timer 0 Next Interval Register 2014 0108
- Timer 0 Interrupt Vector 2014 010C
- Timer 1 Control Register 2014 0110
- Timer 1 Interval Register 2014 0114
- Timer 1 Next Interval Register 2014 0118
- Timer 1 Interrupt Vector 2014 011C
- Reserved Local Register I/O Space 2014 0120 - 2014 012F

BDR Address Decode Match Register 2014 0140
BDR Address Decode Mask Register 2014 0144
Reserved Local Register I/O Space 2014 0138 - 2014 03FF

Battery Backed-Up RAM 2014 0400 - 2014 07FF
Reserved Local Register I/O Space 2014 0800 - 201F FFFF

Reserved Local I/O Space 2020 0000 - 2FFF FFFF
Local Q22-bus Memory Space 3000 0000 - 303F FFFF
Reserved Local Register I/O Space 3040 0000 - 3FFF FFFF

A.3 External, Internal Processor Registers

Several of the Internal Processor Registers (IPR's) on the KA50/51/55/56 are implemented in the NCA or SSC chip rather than the CPU chip. These registers are referred to as External Internal Processor Registers and are listed below.

<table>
<thead>
<tr>
<th>IPR #</th>
<th>Register Name</th>
<th>Abbrev.</th>
</tr>
</thead>
<tbody>
<tr>
<td>27</td>
<td>Time of Year: Register</td>
<td>TOY</td>
</tr>
<tr>
<td>28</td>
<td>Console Storage Receiver Status</td>
<td>CSRS*</td>
</tr>
<tr>
<td>29</td>
<td>Console Storage Receiver Data</td>
<td>CSRD*</td>
</tr>
<tr>
<td>30</td>
<td>Console Storage Transmitter Status</td>
<td>CSTS*</td>
</tr>
<tr>
<td>31</td>
<td>Console Storage Transmitter Data</td>
<td>CSDB*</td>
</tr>
<tr>
<td>32</td>
<td>Console Receiver Control/Status</td>
<td>RXCS</td>
</tr>
<tr>
<td>33</td>
<td>Console Receiver Data Buffer</td>
<td>RXDB</td>
</tr>
<tr>
<td>34</td>
<td>Console Transmitter Control/Status</td>
<td>TXCS</td>
</tr>
<tr>
<td>35</td>
<td>Console Transmitter Data Buffer</td>
<td>TXDB</td>
</tr>
<tr>
<td>55</td>
<td>I/O System Reset Register</td>
<td>IORESET</td>
</tr>
</tbody>
</table>

* These registers are not fully implemented, accesses yield UNPREDICTABLE results.
A.4 Global Q22–bus Address Space Map

Q22–bus Memory Space

Q22–bus Memory Space (Octal) 0000 0000 - 1777 7777

Q22–bus I/O Space (BBS7 Asserted)

Q22–bus I/O Space (Octal) 1776 0000 - 1777 7777
  Reserved Q22–bus I/O Space 1776 0000 - 1776 0007
  Q22–bus Floating Address Space 1776 0010 - 1776 3777
  User Reserved Q22–bus I/O Space 1776 4000 - 1776 7777
  Reserved Q22–bus I/O Space 1777 0000 - 1777 7477
  Interprocessor Comm Reg 1777 7500
  Reserved Q22–bus I/O Space 1777 7502 - 1777 7777

A.5 Processor Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
<th>I/O Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kernel Stack Pointer</td>
<td>KSP</td>
<td>0</td>
<td>0</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Executive Stack Pointer</td>
<td>ESP</td>
<td>1</td>
<td>1</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Supervisor Stack Pointer</td>
<td>SSP</td>
<td>2</td>
<td>2</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>User Stack Pointer</td>
<td>USP</td>
<td>3</td>
<td>3</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Interrupt Stack Pointer</td>
<td>ISP</td>
<td>4</td>
<td>4</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>5–7</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td>E1000014</td>
</tr>
</tbody>
</table>

(continued on next page)
### Address Assignments

#### A.5 Processor Registers

**Table A-1 (Cont.) Processor Registers**

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
<th>I/O Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0 Base Register</td>
<td>P0BR</td>
<td>8</td>
<td>8</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>P0 Length Register</td>
<td>P0LR</td>
<td>9</td>
<td>9</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>P1 Base Register</td>
<td>P1BR</td>
<td>10</td>
<td>A</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>P1 Length Register</td>
<td>P1LR</td>
<td>11</td>
<td>B</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>System Base Register</td>
<td>SBR</td>
<td>12</td>
<td>C</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>System Length Register</td>
<td>SLR</td>
<td>13</td>
<td>D</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>CPU Identification</td>
<td>CPUID</td>
<td>14</td>
<td>E</td>
<td>RW</td>
<td>NVAX</td>
<td>2-1</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>15</td>
<td>F</td>
<td></td>
<td></td>
<td>3</td>
<td>E100003C</td>
</tr>
<tr>
<td>Process Control Block Base</td>
<td>PCBB</td>
<td>16</td>
<td>10</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>System Control Block Base</td>
<td>SCBB</td>
<td>17</td>
<td>11</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Interrupt Priority Level(^1)</td>
<td>IPL</td>
<td>18</td>
<td>12</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>AST Level(^1)</td>
<td>ASTLVL</td>
<td>19</td>
<td>13</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Software Interrupt Request Register</td>
<td>SIRR</td>
<td>20</td>
<td>14</td>
<td>W</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\)Initialized on reset

(continued on next page)
### Address Assignments

#### A.5 Processor Registers

**Table A-1 (Cont.) Processor Registers**

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
<th>I/O Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software Interrupt Summary Register¹</td>
<td>SISR</td>
<td>21</td>
<td>15</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interval Counter Control /Status</td>
<td>ICCS</td>
<td>24</td>
<td>18</td>
<td>RW</td>
<td>NCA</td>
<td>2-7</td>
<td>E1000060</td>
</tr>
<tr>
<td>Next Interval Count</td>
<td>NICR</td>
<td>25</td>
<td>19</td>
<td>RW</td>
<td>NCA</td>
<td>3-7</td>
<td>E1000064</td>
</tr>
<tr>
<td>Interval Count</td>
<td>ICR</td>
<td>26</td>
<td>1A</td>
<td>RW</td>
<td>NCA</td>
<td>3-7</td>
<td>E1000068</td>
</tr>
<tr>
<td>Time of Year Register</td>
<td>TODR</td>
<td>27</td>
<td>1B</td>
<td>RW</td>
<td>SSC</td>
<td>2-3</td>
<td>E100006C</td>
</tr>
<tr>
<td>Console Storage Receiver Status</td>
<td>CSRS</td>
<td>28</td>
<td>1C</td>
<td>RW</td>
<td>SSC</td>
<td>2-3</td>
<td>E1000070</td>
</tr>
<tr>
<td>Console Storage Receiver Data</td>
<td>CSRD</td>
<td>29</td>
<td>1D</td>
<td>R</td>
<td>SSC</td>
<td>2-3</td>
<td>E1000074</td>
</tr>
<tr>
<td>Console Storage Transmitter Status</td>
<td>CSTS</td>
<td>30</td>
<td>1E</td>
<td>RW</td>
<td>SSC</td>
<td>2-3</td>
<td>E1000078</td>
</tr>
<tr>
<td>Console Storage Transmitter Data</td>
<td>CSTD</td>
<td>31</td>
<td>1F</td>
<td>W</td>
<td>SSC</td>
<td>2-3</td>
<td>E100007C</td>
</tr>
</tbody>
</table>

¹ Initialized on reset

(continued on next page)
Address Assignments
A.5 Processor Registers

Table A–1 (Cont.) Processor Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>ImPL</th>
<th>Cat</th>
<th>I/O Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Console Receiver Control/Status</td>
<td>RXCS</td>
<td>32</td>
<td>20</td>
<td>RW</td>
<td>SSC</td>
<td>2-3</td>
<td>E1000080</td>
</tr>
<tr>
<td>Console Receiver Data Buffer</td>
<td>RXDB</td>
<td>33</td>
<td>21</td>
<td>R</td>
<td>SSC</td>
<td>2-3</td>
<td>E1000084</td>
</tr>
<tr>
<td>Console Transmitter Control/Status</td>
<td>TXCS</td>
<td>34</td>
<td>22</td>
<td>RW</td>
<td>SSC</td>
<td>2-3</td>
<td>E1000088</td>
</tr>
<tr>
<td>Console Transmitter Data Buffer</td>
<td>TXDB</td>
<td>35</td>
<td>23</td>
<td>W</td>
<td>SSC</td>
<td>2-3</td>
<td>E100008C</td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>36</td>
<td>24</td>
<td></td>
<td>3</td>
<td>E1000090</td>
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</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>37</td>
<td>25</td>
<td></td>
<td>3</td>
<td>E1000094</td>
<td></td>
</tr>
<tr>
<td>Machine Check Error Register</td>
<td>MCESR</td>
<td>38</td>
<td>26</td>
<td>W</td>
<td>NVAX</td>
<td>2-1</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>39</td>
<td>27</td>
<td></td>
<td>3</td>
<td>E100009C</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
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<td>28</td>
<td></td>
<td>3</td>
<td>E10000A0</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>41</td>
<td>29</td>
<td></td>
<td>3</td>
<td>E10000A4</td>
<td></td>
</tr>
<tr>
<td>Console Saved PC</td>
<td>SAVPC</td>
<td>42</td>
<td>2A</td>
<td>R</td>
<td>NVAX</td>
<td>2-1</td>
<td></td>
</tr>
<tr>
<td>Console Saved PSL</td>
<td>SAVPSL</td>
<td>43</td>
<td>2B</td>
<td>R</td>
<td>NVAX</td>
<td>2-1</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>44–54</td>
<td>2C</td>
<td></td>
<td>3</td>
<td>E10000B0</td>
<td></td>
</tr>
<tr>
<td>I/O System Reset Register</td>
<td>IORESET</td>
<td>55</td>
<td>37</td>
<td>W</td>
<td>SSC</td>
<td>2-3</td>
<td>E10000DC</td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
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$^1$Initialized on reset

$^2$Change broadcast to vector unit if present

$^3$Testability and diagnostic use only; not for software use in normal operation

(continued on next page)
Address Assignments
A.5 Processor Registers

Table A-1 (Cont.) Processor Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
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\(^3\)Testability and diagnostic use only; not for software use in normal operation

(continued on next page)
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## Address Assignments

### A.5 Processor Registers

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### Address Assignments
#### A.5 Processor Registers

**Table A-1 (Cont.) Processor Registers**

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<th>Register Name</th>
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<sup>3</sup>Testability and diagnostic use only; not for software use in normal operation

(continued on next page)
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#### A.5 Processor Registers

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<th>(Dec)</th>
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(continued on next page)
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<td>F5</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>246</td>
<td>F6</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>247</td>
<td>F7</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mbox</td>
<td>PCCTL</td>
<td>248</td>
<td>F8</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Pcache Control</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>249</td>
<td>F9</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>250</td>
<td>FA</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>251</td>
<td>FB</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>252</td>
<td>FC</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>253</td>
<td>FD</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>254</td>
<td>FE</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>255</td>
<td>FF</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Unimplemented 100-00FFFFFF

(continued on next page)
### Address Assignments
#### A.5 Processor Registers

**Table A-1 (Cont.) Processor Registers**

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
<th>I/O Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>See</td>
<td></td>
<td>01000000–</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>FFFFFFFF</td>
</tr>
<tr>
<td>Table A-2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Type:**
- R = Read-only register
- RW = Read-write register
- W = Write-only register

**Implemented:**
- NVAX = Implemented in the NVAX CPU chip
- System = Implemented in the system environment
- Vector = Implemented in the optional vector unit or its NDAL interface

**Category, class-subclass, where:**
- class is one of:
  - 1 = Implemented as per DEC standard 032
  - 2 = NVAX-specific implementation which is unique or different from the DEC standard 032 implementation
  - 3 = Not implemented internally; converted to I/O space read or write and passed to system environment

- subclass is one of:
  - 1 = Processed as appropriate by Ebox microcode
  - 2 = Converted to Mbox IPR number and processed via internal IPR command
  - 3 = Processed by internal IPR command, then converted to I/O space read or write and passed to system environment
  - 4 = If virtual machine option is implemented, processed as in 1, otherwise as in 3
  - 5 = Processed by internal IPR command
  - 6 = May be block decoded; reference causes UNDEFINED behavior
  - 7 = Full interval timer may be implemented in the system environment. Subset ICCS is implemented in NVAX CPU chip
  - 8 = Converted to MFVP MSYNC
### A.6 IPR Address Space Decoding

<table>
<thead>
<tr>
<th>IPR Group</th>
<th>Mnemonic</th>
<th>IPR Address Range (hex)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td></td>
<td>00000000..000000FF${}^1$</td>
<td>256 individual IPRs.</td>
</tr>
<tr>
<td>Bcache Tag</td>
<td>BCTAG</td>
<td>01000000..011FFFE0${}^1$</td>
<td>64k Bcache tag IPRs, each separated by 20(hex) from the previous one.</td>
</tr>
<tr>
<td>Bcache Deallocate</td>
<td>BCFLUSH</td>
<td>01400000..015FFFE0${}^1$</td>
<td>64k Bcache tag deallocate IPRs, each separated by 20(hex) from the previous one.</td>
</tr>
<tr>
<td>Pcache Tag</td>
<td>PCTAG</td>
<td>01800000..01801FE0${}^1$</td>
<td>256 Pcache tag IPRs, 128 for each Pcache set, each separated by 20(hex) from the previous one.</td>
</tr>
<tr>
<td>Pcache Data Parity</td>
<td>PCDAP</td>
<td>01C00000..01C01FF8${}^1$</td>
<td>1024 Pcache data parity IPRs, 512 for each Pcache set, each separated by 8(hex) from the previous one.</td>
</tr>
</tbody>
</table>

${}^1$Unused fields in the IPR addresses for these groups should be zero. Neither hardware nor microcode detects and faults on an address in which these bits are nonzero. Although noncontiguous address ranges are shown for these groups, the entire IPR address space maps into one of these groups. If these fields are nonzero, the operation of the CPU is UNDEFINED.

${}^2$The mnemonic is for the first IPR in the block.

Processor registers in all groups except the normal group are processed entirely by the NVAX CPU chip and will never appear on the NDAL. This is also true for a number of the IPRs in the normal group. IPRs in the normal group that are not processed by the NVAX CPU chip are converted into I/O space references and passed to the system environment via a read or write command on the NDAL.

Each of the 256 possible IPRs in the normal group are of longword length, so a 1-KB block of I/O space is required to convert each possible IPR to a unique I/O space longword. This block starts at address E1000000 (hex). Conversion of an IPR address to an I/O space address in this block is done by shifting the IPR address left into bits <9:2>, filling bits <1:0> with zeros, and merging in the base address of the block. This can be expressed by the equation:

\[
I/O \text{ ADDRESS} = E1000000 + (IPR \text{ NUMBER} \times 4)
\]
Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95, and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q–bus and DSSI, will appear on the console and/or printouts from time to time.

This section describes ROM partitioning and subroutine entry points that are public and are guaranteed to be compatible over future versions of the firmware. An entry point is the address at which any subroutine or subprogram will start execution.

B.1 Firmware EPROM Layout

The KA50/51/55/56 has 512 Kbytes of FEPROM. Unlike previous Q22–bus based processors, there is no duplicate decoding of the FEPROM into halt-protected and halt-unprotected spaces. The entire FEPROM is halt-protected. See Figure B–1 for the KA50/51/55/56 FEPROM layout.
The first instruction executed on halts is a branch around the System ID Extension (SIE) and the callback entry points. This allows these public data structures to reside in fixed locations in the FEPROM.

The callback area entry points provide a simple interface to the currently defined console for VMB and secondary bootstraps. This is documented further in the next section.

The fixed area checksum is the sum of longwords from 20040000 to the checksum, inclusive. This checksum is distinct from the checksum that the rest of the console uses.

The console, diagnostic and boot code constitute the bulk of the firmware. This code is field upgradable. The console checksum is from 20044000 to the checksum, inclusive.

The memory between the console checksum and the user area at the end of the FEPROM is reserved for Digital for future expansion of the firmware. The contents of this area is set to FF.

The last 4096 bytes of FEPROM are reserved for customer use and are not included in the console checksum. During a PROM bootstrap with PRB0 as the selected boot device, this block is tested for a PROM "signature block".
B.1.1 System Identification Registers

The firmware and operating system software reference two registers to determine the processor on which they are running. The first, the System Identification register (SID), is a NVAX internal processor register. The second, the System Identification Extension register (SIE), is a firmware register located in the FEPROM.

B.1.1.1 PRS_SID (IPR 62)

The SID longword can be read from IPR 62 using the MFPR instruction. This longword value is processor specific, however, the layout of this register is shown in Figure B–2. A description of each field is provided in Table B–1.

Figure B–2 SID : System Identification Register

<table>
<thead>
<tr>
<th>31</th>
<th>24</th>
<th>23</th>
<th>08</th>
<th>07</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_TYPE</td>
<td>Reserved</td>
<td>Version</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table B–1 System Identification Register

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>RW</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>CPU_TYPE</td>
<td>ro</td>
<td>CPU type is the processor specific identification code.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0A : CVAX</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0B : RIGEL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>13 : NVAX</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>14 : SOC</td>
</tr>
<tr>
<td>24:8</td>
<td>Reserved</td>
<td>ro</td>
<td>Reserved for future use.</td>
</tr>
<tr>
<td>7:0</td>
<td>VERSION</td>
<td>ro</td>
<td>Version of the microcode.</td>
</tr>
</tbody>
</table>

B.1.1.2 SIE (20040004)

The System Identification Extension register is an extension of the SID and is used to further differentiate between hardware configurations. The SID identifies which CPU and microcode are executing, and the SIE identifies which module and firmware revision are present. Note, the fields in this register are dependent on SID<31:24>(CPU_TYPE).
ROM Partitioning
B.1 Firmware EPROM Layout

By convention, all MicroVAX 3100 systems implement a longword at physical location 20040004 in the firmware EPROM for the SIE. The layout of the SIE is shown in Figure B–3. A description of each field is provided in Table B–2.

Figure B–3 SIE : System Identification Extension (20040004)

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>RW</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>SYS_TYPE</td>
<td>ro</td>
<td>This field identifies the type of system for a specific processor.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>03 : Bounded system.</td>
</tr>
<tr>
<td>23:16</td>
<td>VERSION</td>
<td>ro</td>
<td>This field identifies the resident version of the firmware encoded as two hexadecimal digits. For example, if the banner displays V5.0, then this field is 50 (hex).</td>
</tr>
<tr>
<td>15:8</td>
<td>SYS_SUB_TYPE</td>
<td>ro</td>
<td>This field identifies the particular system subtype.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>08 : KA50/KA55</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>09 : KA51/KA56</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0A : KA62</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0B : KA53</td>
</tr>
<tr>
<td>7:0</td>
<td>VARIANT</td>
<td>ro</td>
<td>This field identifies the particular system variant.</td>
</tr>
</tbody>
</table>

B.1.2 Call-Back Entry Points

The firmware provides several entry points that facilitate I/O to the designated console device. Users of these entry points do not need to be aware of the console device type, be it a video terminal or workstation.

The primary intent of these routines is to provide a simple console device to VMB and secondary bootstraps, before operating systems load their own terminal drivers.

These are JSB (subroutine as opposed to procedure) entry points located in fixed locations in the firmware. These locations branch to code that in turn calls the appropriate routines.
ROM Partitioning
B.1 Firmware EPROM Layout

All of the entry points are designed to run at IPL 31 on the interrupt stack in physical mode. Virtual mode is not supported. Due to internal firmware architectural restrictions, users are encouraged to only call into the halt-protected entry points. These entry points are listed in Table B-3.

### Table B-3 Call-Back Entry Points

<table>
<thead>
<tr>
<th>Entry Point</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP$GET_CHAR_R4</td>
<td>20040008</td>
</tr>
<tr>
<td>CP$MSG_OUT_NOLF_R4</td>
<td>2004000C</td>
</tr>
<tr>
<td>CP$READ_WTH_</td>
<td>20040010</td>
</tr>
<tr>
<td>PRMPT_R4</td>
<td></td>
</tr>
</tbody>
</table>

#### B.1.2.1 CP$GETCHAR_R4

This routine returns the next character entered by the operator in R0. A timeout interval can be specified. If the timeout interval is zero, no timeout is generated. If a timeout is specified and if timeout occurs, a value of 18 (CAN) is returned instead of normal input.

Registers R0,R1,R2,R3 and R4 are modified by this routine, all others are preserved.

```assembly
; -----------------------------------------------
; Usage with timeout:
movl $timeout_in_tenths_of_second, r0 ; Specify timeout.
jsb @@CP$GET_CHAR_R4 ; Call routine.
cmp rb, $x18 ; Check for timeout.
b eql timeout_handler ; Branch if timeout.
; Input is in R0.
; -----------------------------------------------

; -----------------------------------------------
; Usage without timeout:
clr rb ; Specify no timeout.
jsb @@CP$GET_CHAR_R4 ; Call routine.
; Input is in R0.
; -----------------------------------------------
```


ROM Partitioning

B.1 Firmware EPROM Layout

B.1.2.2 CP$MSG_OUT_NOLF_R4

This routine outputs a message to the console. The message is specified either by a message code or a string descriptor. The routine distinguishes between message codes and descriptors by requiring that any descriptor be located outside of the first page of memory. Hence, message codes are restricted to values between 0 and 511.

Registers R0,R1,R2,R3 and R4 are modified by this routine, all others are preserved.

;-----------------------------------------------
; Usage with message code:

movzbl  #console_message_code,r0        ; Specify message code.
jsb    @@CP$MSG_OUT_NOLF_R4            ; Call routine.

;-----------------------------------------------
; Usage with a message descriptor (position dependent).

movaq  5$,r0                           ; Specify address of desc.
jsb    @@CP$MSG_OUT_NOLF_R4            ; Call routine.

5$:    .ascid /This is a message/        ; Message with descriptor.

;-----------------------------------------------
; Usage with a message descriptor (position independent).

pushab 5$                               ; Generate message desc.
pushl  $105-5$                           ; on stack.
movl  sp,r0                              ; Pass desc. addr. in R0.
jsb    @@CP$MSG_OUT_NOLF_R4            ; Call routine.
clrq   (sp)+                             ; Purge desc. from stack.

5$:    .ascii /This is a message/        ; Message.
10$:    

;-----------------------------------------------

B.1.2.3 CP$READ_WTH_PRMPT_R4

This routine outputs a prompt message and then inputs a character string from the console. When the input is accepted, DELETE, CONTROL-U and CONTROL-R functions are supported.

As with CP$MSG_OUT_NOLF_R4, either a message code or the address of a string descriptor is passed in R0 to specify the prompt string. A value of zero results in no prompt. A time-out value in 10-millisecond ticks may be passed in R1. If R1 is zero, the prompt will not timeout.
A descriptor of the input string is returned in R0 and R1. R0 contains the length of the string and R1 contains the address. This routine inputs the string into the console program string buffer and therefore the caller need not provide an input buffer. Successive calls however destroy the previous contents of the input buffer.

Registers R0 and R1 are modified by this routine, all others are preserved.

;-------------------------------------------------------------
; Usage with a message descriptor (position independent).

pushab 5$                         ; Generate prompt desc.
pushl #10S-5$                      ; on stack.
movl sp,r0                         ; Pass desc. addr. in R0.
crl r1                              ; Specify no time-out.
jsb @CP$READ_WTH_PRMPT_R4          ; Call routine.
crq (sp)+                           ; Purge prompt desc.
                              ; Input desc in R0 and R1.

5$: ascii /Prompt> /               ; Prompt string.
10S:                                 
;-------------------------------------------------------------

B.1.3 Boot Information Pointers

Two longwords located in FEPROM are used as pointers to the default boot device descriptor and the default boot flags (Figure B-4), because the actual location of this data may change in successive versions of the firmware. Any software that uses these pointers should reference them at the addresses in halt-protected space.
The following macro defines the boot device descriptor format.

```
;---------------------------------------------------
; Default Boot Device Descriptor
;
.boot_device_descriptor::
    base = .
    . = base + dsc$w_length
    .word nvr$S_boot_device
    . = base + dsc$B_dtype
    .byte dsc$K_dtype_z
    . = base + dsc$B_class
    .byte dsc$K_class_z
    . = base + dsc$A_pointer
    .long nvr_base + nvr$B_boot_device
    . = base + dsc$S_dscdefl
;---------------------------------------------------
```
This appendix contains definitions of the key global data structures used by the CPU firmware.

---

**Note**

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95 and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q-bus and DSSI, will appear on the console and/or printouts from time to time.

---

### C.1 Halt Dispatch State Machine

The CPU halt dispatcher determines what actions the firmware will take on halt entry based on the machine state. The dispatcher is implemented as a state machine, which uses a single bitmap control word and the transition (see Table C-1) to process all halts. The transition table is sequentially searched for matches with the current state and control word. If there is a match, a transition occurs to the next state.

The control word comprises the following information:

- **Halt Type**, used for resolving external halts. Valid only if Halt Code is 00.

  - 000 : power-up state
  - 001 : halt in progress
  - 010 : negation of Q22-bus DCOK
  - 011 : console BREAK condition detected
  - 100 : Q22-bus BHALT
  - 101 : SGECH BOOT_L asserted (trigger boot)
Data Structures and Memory Layout
C.1 Halt Dispatch State Machine

- **Halt Code**, compressed form of $\text{SAVP}SL_{13:8}$(RESTART_CODE).
  
  00 : RESTART_CODE = 2, external halt
  01 : RESTART_CODE = 3, power-up/reset
  10 : RESTART_CODE = 6, halt instruction
  11 : RESTART_CODE = any other, error halts

- **Mailbox Action**, passed by an operating system in CPMBX$_{1:0}$(HALT_ACTION).
  
  00 : restart, boot, halt
  01 : restart, halt
  10 : boot, halt
  11 : halt

- **User Action**, specified with the SET HALT console command.
  
  000 : default
  001 : restart, halt
  010 : boot, halt
  011 : halt
  100 : restart, boot, halt

- **HEN**, Break (halt) Enable/Disable switch, BDR$_{07}$
- **ERR**, error status
- **TIP**, trace in progress
- **DIP**, diagnostics in progress
- **BIP**, bootstrap in progress CPMBX$_{2}$
- **RIP**, restart in progress CPMBX$_{3}$

A transition to a "next state" occurs if a match is found between the control word and a "current state" entry in the table. The firmware does a linear search through the table for a match. Therefore, the order of the entries in the transition table is important. The control longword is reassembled before each transition from the current machine state. The state machine transitions are shown in Table C.1.
### Data Structures and Memory Layout

#### C.1 Halt Dispatch State Machine

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Halt Type</th>
<th>Halt Code</th>
<th>Halt Action</th>
<th>User Action</th>
<th>HEN-ERR-TIP-DIP-BIP-RIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENTRY</td>
<td>-&gt;RESET INIT</td>
<td>xxx</td>
<td>01</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x - x</td>
</tr>
<tr>
<td>ENTRY</td>
<td>-&gt;BREAK INIT</td>
<td>011</td>
<td>00</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x - x</td>
</tr>
<tr>
<td>ENTRY</td>
<td>-&gt;TRACE INIT</td>
<td>xxx</td>
<td>10</td>
<td>xx</td>
<td>xxx</td>
<td>x - 0 - 1 - x - x - x</td>
</tr>
<tr>
<td>ENTRY</td>
<td>-&gt;OTHER INIT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
</tbody>
</table>

**Perform conditional initialization**

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Halt Type</th>
<th>Halt Code</th>
<th>Halt Action</th>
<th>User Action</th>
<th>HEN-ERR-TIP-DIP-BIP-RIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET INIT</td>
<td>-&gt;INIT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x - x</td>
</tr>
<tr>
<td>BREAK INIT</td>
<td>-&gt;INIT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x - x</td>
</tr>
<tr>
<td>TRACE INIT</td>
<td>-&gt;INIT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x - x</td>
</tr>
<tr>
<td>OTHER INIT</td>
<td>-&gt;INIT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x - x</td>
</tr>
</tbody>
</table>

**Perform common initialization**

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Halt Type</th>
<th>Halt Code</th>
<th>Halt Action</th>
<th>User Action</th>
<th>HEN-ERR-TIP-DIP-BIP-RIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>-&gt;BOOTSTRAP</td>
<td>101</td>
<td>00</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x - x</td>
</tr>
<tr>
<td>INIT</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>00</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x - x</td>
</tr>
</tbody>
</table>

**Check for external halts**

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Halt Type</th>
<th>Halt Code</th>
<th>Halt Action</th>
<th>User Action</th>
<th>HEN-ERR-TIP-DIP-BIP-RIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>-&gt;TRACE</td>
<td>xxx</td>
<td>10</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - 1 - x - x - x</td>
</tr>
</tbody>
</table>

---

1 Perform a unique initialization routine on entry. In particular, power-ups, BREAKs, and TRACEs require special initialization. Any other halt entry performs a default initialization.

2 After performing conditional initialization, complete common initialization.

3 Halt on all external halts, except:

- if DCOK (unlikely) and halts are disabled, bootstrap
- if SECC remote trigger, bootstrap

4 Unconditionally enter the TRACE state, if the TIP flag is set and the halt was due to a HALT instruction. From the TRACE state the firmware exits, if TIP is set and ERR is clear; otherwise it halts.

(continued on next page)
Data Structures and Memory Layout
C.1 Halt Dispatch State Machine

Table C-1 (Cont.) Firmware State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Halt Type</th>
<th>Halt Code</th>
<th>Mailbox Action</th>
<th>User Action</th>
<th>HEN-ERR-TIP-DIP-BIP-RIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRACE</td>
<td>-&gt;EXIT</td>
<td>xxx</td>
<td>10</td>
<td>xx</td>
<td>xxx</td>
<td>x - 0 - 1 - x - x - x</td>
</tr>
<tr>
<td>TRACE</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
</tbody>
</table>

Check for pending (NEXT) trace

| INIT          | -->BOOTSTRAP | xxx | 01 | xx | xxx | 0 - 0 - 0 - 0 - 0 - 0 |
| INIT          | -->BOOTSTRAP | xxx | 01 | xx | 010 | 1 - 0 - 0 - 0 - 0 - 0 |
| INIT          | -->BOOTSTRAP | xxx | 01 | xx | 100 | 1 - 0 - 0 - 0 - 0 - 0 |
| INIT          | -->BOOTSTRAP | xxx | 1x | 10 | xxx | x - 0 - 0 - 0 - 0 - 0 |
| INIT          | -->BOOTSTRAP | xxx | 1x | 00 | 010 | x - 0 - 0 - 0 - 0 - 0 |
| INIT          | -->BOOTSTRAP | xxx | 1x | 00 | 100 | x - 0 - 0 - 0 - 0 - 1 |
| INIT          | -->BOOTSTRAP | xxx | 1x | 00 | 100 | x - 1 - 0 - 0 - 0 - x |
| INIT          | -->BOOTSTRAP | xxx | 1x | 00 | 000 | 0 - 0 - 0 - 0 - 0 - 1 |
| RESTART       | -->BOOTSTRAP | xxx | 1x | 00 | 000 | 0 - 1 - 0 - 0 - 0 - x |

Check for bootstrap conditions

| INIT          | -->RESTART  | xxx | 1x | 01 | xxx | x - 0 - 0 - 0 - 0 - 0 |
| INIT          | -->RESTART  | xxx | 1x | 00 | 001 | x - 0 - 0 - 0 - 0 - 0 |
| INIT          | -->RESTART  | xxx | 1x | 00 | 100 | x - 0 - 0 - 0 - 0 - 0 |

Check for restart conditions

4 Unconditionally enter the TRACE state, if the TIP flag is set and the halt was due to a HALT instruction. From the TRACE state the firmware exits, if TIP is set and ERR is clear; otherwise it halts.

5 Bootstrap,

- if power-up and halts are disabled.
- if power-up and halts are enabled and user action is 2 or 4.
- if not power-up and mailbox is 2.
- if not power-up and mailbox is 0 and user action is 2.
- if not power-up and restart failed and mailbox is 0 and user action is 0 or 4.

6 Restart the operating system if not power-up and

- if mailbox is 1.
- if mailbox is 0 and user action is 1 or 4.
- if mailbox is 0 and user action is 0 and halts are disabled.

(continued on next page)
### Table C-1 (Cont.) Firmware State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Halt Type</th>
<th>Halt Code</th>
<th>Mailbx Action</th>
<th>User Action</th>
<th>HEN-ERR-TIP-DIP-BIP-RIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>-&gt;RESTART</td>
<td>xxx</td>
<td>1x</td>
<td>00</td>
<td>000</td>
<td>0 - 0 - 0 - 0 - 0 - 0</td>
</tr>
</tbody>
</table>

**Check for restart conditions**

**Perform common exit processing, if no errors**

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Halt Type</th>
<th>Halt Code</th>
<th>Mailbx Action</th>
<th>User Action</th>
<th>HEN-ERR-TIP-DIP-BIP-RIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOTSTRAP</td>
<td>-&gt;EXIT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - 0 - x - x - x - x</td>
</tr>
<tr>
<td>RESTART</td>
<td>-&gt;EXIT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - 0 - x - x - x - x</td>
</tr>
<tr>
<td>HALT</td>
<td>-&gt;EXIT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - 0 - x - x - x - x</td>
</tr>
</tbody>
</table>

**Exception transitions, just halt**

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Halt Type</th>
<th>Halt Code</th>
<th>Mailbx Action</th>
<th>User Action</th>
<th>HEN-ERR-TIP-DIP-BIP-RIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>BOOT</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>REST</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>HALT</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>TRACE</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>EXIT</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
</tbody>
</table>

---

6 Restart the operating system if not power-up and
   if mailbox is 1.
   if mailbox is 0 and user action is 1 or 4.
   if mailbox is 0 and user action is 0 and halts are disabled.

7 Exit after halts, bootstrap or restart. The exit state transitions to program I/O mode.

8 Guard block that catches all exception conditions. In all cases, just halt.

### C.2 Restart Parameter Block

VMB typically utilizes the low portion of memory unless there are bad pages in the first 128K bytes. The first page in its block is used for the Restart Parameter Block (RPB), through which it communicates to the operating system. Usually, this is page 0.
VMB will initialize the Restart Parameter Block (RPB) as shown in Table C–2.

<table>
<thead>
<tr>
<th>(R11)+</th>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00:</td>
<td>RPBS$L_BASE</td>
<td>Physical address of base of RPB.</td>
</tr>
<tr>
<td>04:</td>
<td>RPBS$L_RESTART</td>
<td>Cleared.</td>
</tr>
<tr>
<td>08:</td>
<td>RPBS$L_CHKSUM</td>
<td>-1</td>
</tr>
<tr>
<td>0C:</td>
<td>RPBS$L_RSTRTFLG</td>
<td>Cleared.</td>
</tr>
<tr>
<td>10:</td>
<td>RPBS$L_HALTPC</td>
<td>R10 on entry to VMB (HALT PC).</td>
</tr>
<tr>
<td>10:</td>
<td>RPBS$L_HALTPSL</td>
<td>PR$SAVPSL on entry to VMB (HALT PSL).</td>
</tr>
<tr>
<td>18:</td>
<td>RPBS$L_HALTCODE</td>
<td>AP on entry to VMB (HALT CODE).</td>
</tr>
<tr>
<td>1C:</td>
<td>RPBS$L_BOOTR0</td>
<td>R0 on entry to VMB.</td>
</tr>
</tbody>
</table>

**Note**

The field RPBSW_R0UBVEC, which overlaps the high-order word of RPBS$L_BOOTR0, is set by the boot device drivers to the SCB offset (in the second page of the SCB) of the interrupt vector for the boot device.

| 20:    | RPBS$L_BOOTR1   | VMB version number. The high-order word of the version is the major ID and the low-order word is the minor ID. |
| 24:    | RPBS$L_BOOTR2   | R2 on entry to VMB.                                   |
| 28:    | RPBS$L_BOOTR3   | R3 on entry to VMB.                                   |
| 2C:    | RPBS$L_BOOTR4   | R4 on entry to VMB.                                   |

**Note**

The 48-bit booting node address is stored in RPBS$L_BOOTR3 and RPBS$L_BOOTR4 for compatibility with ELN VX.X. (This field is only initialized this way when performing a network boot.)

| 30:    | RPBS$L_BOOTR5   | R5 on entry to VMB.                                   |
| 34:    | RPBS$L_IOVEC    | Physical address of boot driver’s I/O vector of transfer addresses. |

(continued on next page)
### Data Structures and Memory Layout

#### C.2 Restart Parameter Block

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPB$__IOVECSZ</td>
<td>Size of BOOT QIO routine.</td>
</tr>
<tr>
<td>RPB$__FILLBN</td>
<td>LBN of secondary bootstrap image.</td>
</tr>
<tr>
<td>RPB$__FILSIZ</td>
<td>Size of secondary bootstrap image in blocks.</td>
</tr>
<tr>
<td>RPB$__PFNMAP</td>
<td>The PFN bitmap is an array of bits, where each bit has the value &quot;1&quot; if the corresponding page of memory is valid, or has the value &quot;0&quot; if the corresponding page of memory contains a memory error. Through use of the PFNMAP, the operating system can avoid memory errors by avoiding known bad pages altogether. The memory bitmap is always page-aligned, and describes all the pages of memory from physical page #0 to the high end of memory, but excluding the PFN bitmap itself and the Q-bus map registers. If the high byte of the bitmap spans some pages available to the operating system and some pages of the PFN bitmap itself, the pages corresponding to the bitmap itself will be marked as bad pages. The first longword of the PFNMAP descriptor contains the number of bytes in the PFNMAP; the second longword contains the physical address of the bitmap.</td>
</tr>
<tr>
<td>RPB$__PFNCNT</td>
<td>Count of &quot;good&quot; pages of physical memory, but not including the pages allocated to the Q22-bus scatter/gather map, the console scratch area, and the PFN bitmap at the top of memory.</td>
</tr>
<tr>
<td>RPB$__SVASPT</td>
<td>0.</td>
</tr>
<tr>
<td>RPB$__CSRPHY</td>
<td>Physical address of CSR for boot device.</td>
</tr>
<tr>
<td>RPB$__CSRVIR</td>
<td>0.</td>
</tr>
<tr>
<td>RPB$__ADPPHY</td>
<td>Physical address of ADP (really the address of QMRs - ^x800 to look like a UBA adapter).</td>
</tr>
<tr>
<td>RPB$__ADPVIR</td>
<td>0.</td>
</tr>
<tr>
<td>RPB$__UNIT</td>
<td>Unit number of boot device.</td>
</tr>
<tr>
<td>RPB$__DEVTYPE</td>
<td>Device type code of boot device.</td>
</tr>
<tr>
<td>RPB$__SLAVE</td>
<td>Slave number of boot device.</td>
</tr>
</tbody>
</table>

(continued on next page)
### Table C–2 (Cont.) Restart Parameter Block Fields

<table>
<thead>
<tr>
<th>(R11)+</th>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>68:</td>
<td>RPB$T_FILE</td>
<td>Name of secondary bootstrap image (defaults to SYS0.SYSEXESYSBOOT.EXE). This field (up to 40 bytes) is overwritten with the input string on a &quot;solicit&quot; boot.</td>
</tr>
</tbody>
</table>

**Note**

1. For VAX/OpenVMS, the RPB$T_FILE must contain the root directory string "SYSn." on a non-network bootstrap. This string is parsed by SYSBOOT (SYSBOOT does not use the high nibble of BOOTR5).
2. The RPB$T_FILE is overwritten to contain the boot node name for compatibility with ELN VX.X (this field is only initialized this way when performing a network boot).

<table>
<thead>
<tr>
<th>90:</th>
<th>RPB$B_CONFREG</th>
<th>Array (16 bytes) of adapter types (NDT$_UB0 - UNIBUS).</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0:</td>
<td>RPB$B_HDRPGRNT</td>
<td>Count of header pages.</td>
</tr>
<tr>
<td>A1:</td>
<td>RPB$W_BOOTNDT</td>
<td>Boot adapter nexus device type. Used by SYSBOOT and INIADP (OF SYSLOA) to configure the adapter of the boot device (changed from a byte to a word field in Version 12 of VMB).</td>
</tr>
<tr>
<td>B0:</td>
<td>RPB$L_SCBB</td>
<td>Physical address of SCB.</td>
</tr>
<tr>
<td>BC:</td>
<td>RPB$L_MEMDSC</td>
<td>Count of pages in physical memory including both good and bad pages. The high 8 bits of this longword contain the TR #, which is always 0 for KA52.</td>
</tr>
<tr>
<td>C0:</td>
<td>RPB$L_MEMDSC+4</td>
<td>PFN of the first page of memory. This field is always 0 for KA50/51/55/56, even if page #0 is a bad page.</td>
</tr>
</tbody>
</table>

**Note**

No other memory descriptors are used.

| 104:   | RPB$L_BADPGS    | Count of "bad" pages of physical memory.                                                                                                    |

(continued on next page)
Table C–2 (Cont.) Restart Parameter Block Fields

<table>
<thead>
<tr>
<th>(R11)</th>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>108:</td>
<td>RPB$B_CTRLLLTR</td>
<td>Boot device controller number biased by 1. In VAX/OpenVMS, this field is used by INIT (in SYS) to construct the boot device's controller letter. A 0 implies this field has not been initialized, else if initialized, A=1, B=2, etc. (this field was added in Version 13 of VMB).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The rest of the RPB is zeroed.</td>
</tr>
</tbody>
</table>

C.3 VMB Argument List

The VMB code will also initialize an argument list as shown in Table C–3 (the address of the argument list is passed in the AP).

Table C–3 VMB Argument List

<table>
<thead>
<tr>
<th>(AP)</th>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04:</td>
<td>VMB$L_FILECPCHE</td>
<td>Quadword filename.</td>
</tr>
<tr>
<td>0C:</td>
<td>VMB$L_LO_PFN</td>
<td>PFN of first page of physical memory (always 0, regardless of where 128 Kbytes of “good” memory starts).</td>
</tr>
<tr>
<td>10:</td>
<td>VMB$L_HI_PFN</td>
<td>PFN of last page of physical memory.</td>
</tr>
<tr>
<td>14:</td>
<td>VMB$Q_PFNMAP</td>
<td>Descriptor of PFN bitmap. First longword contains count of bytes in bitmap. Second longword contains physical address of bitmap. (Same rules as for RPB$Q_PFNMAP listed above.)</td>
</tr>
<tr>
<td>1C:</td>
<td>VMB$Q_UCODE</td>
<td>Quadword.</td>
</tr>
<tr>
<td>24:</td>
<td>VMB$B_SYSTEMID</td>
<td>48-bit (actually a quadword is allocated) booting node address which is initialized when performing a network boot. This field is copied from the Target System Address parameter of the parameters message. (The DECnet HIORD value is added if the field was two bytes.)</td>
</tr>
<tr>
<td>2C:</td>
<td>VMB$L_FLAGS</td>
<td>Set as needed.</td>
</tr>
<tr>
<td>30:</td>
<td>VMB$L_CI_HIPFN</td>
<td>Cluster interface high PFN.</td>
</tr>
</tbody>
</table>

(continued on next page)
## Data Structures and Memory Layout
### C.3 VMB Argument List

<table>
<thead>
<tr>
<th>(AP)</th>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>34:</td>
<td>VMB$Q_NODENAME</td>
<td>Boot node name which is initialized when performing a network boot. This field is copied from the Target System Name parameter of the parameters message.</td>
</tr>
<tr>
<td>3C:</td>
<td>VMB$Q_HOSTADDR</td>
<td>Host node address (this value is only initialized when booting over the network). This field is copied from the Host System Address parameter of the parameters message.</td>
</tr>
<tr>
<td>44:</td>
<td>VMB$Q_HOSTNAME</td>
<td>Host node name (this value is only initialized when performing a network boot). This field is copied from the Host System Name parameter of the parameters message.</td>
</tr>
<tr>
<td>4C:</td>
<td>VMB$Q_TOD</td>
<td>Time of day (this value is only initialized when performing a network boot). The time of day is copied from the first eight bytes of the Host System Time parameter of the parameters message. (The time differential values are NOT copied.)</td>
</tr>
<tr>
<td>54:</td>
<td>VMB$L_XPARAM</td>
<td>Pointer to data retrieved from request of the parameter file.</td>
</tr>
<tr>
<td>58:</td>
<td></td>
<td>The rest of the argument list is zeroed.</td>
</tr>
</tbody>
</table>
Configurable Machine State

The KA50/51/55/56 CPU modules have many control registers that need to be configured for proper operation of the module. The following list shows the normal state of all configurable bits in the CPU module as they are left after the successful completion of power-up ROM diagnostics.

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95 and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q–bus and DSSI, will appear on the console and/or printouts from time to time.

Configuration Register Bit Settings (* = reset state)

NCA:

-----

NCA_CSR1: Mode Control and Diagnostic Status Register (2102 0004)

15:14: CP2 MT Timer Prescaler

11 = 144000 cycles* - needed for CQBIC 10ms No Grant timeout

13:12: CP1 MT Timer Prescaler

00 = 144 cycles - minimum for passive releases, no cycle should take longer than this.

11:10: NDAL Timeout Prescaler

00 = 3200 cycles* - this is longer than both NCA and NMC transactions timeouts, preserves timeout order.

9: CQBIC mode

0 = CQBIC not present* - this is to avoid the QBUS_TRANS deadlock.
Configurable Machine State

8: IO2 ID enable
   1 = enabled
7: Force wrong CP2 bus parity - off - diagnostic use only
6: Force wrong CP1 bus parity - off - diagnostic use only
5: Force wrong NDAI master parity - off - diagnostic use only
4: Force wrong NDAI slave parity - off - diagnostic use only
3: Enable prefetch
   1 = enable CP bus prefetch on DMA reads
2: Force write buffer hit - off - diagnostic use only
1: Force CP2 bus owner - diagnostic use only
   0 = disabled
0: Force CP1 bus owner - diagnostic use only
   0 = disabled

ICCS: Interval Clock Control and Status Register (2100 0060)
NOTE: OpenVMS sets ICCS, NICR to proper values.
6: Interrupt enable
   0 = disabled*
5: Single step - off
4: Transfer
   0 = disabled*
0: Run - increment every lusec - off

NICR: Next Interval Count Register (2100 0064)
31:0 Initial count value for ICR (FFFFD8FO* (10ms))

NMC:

NMC_CSR0-7: Memory Configuration Registers (2101 8000 thru 2101 801C)
NOTE: Diagnostics set these registers based on available memory
31: Base Address Valid
   0 = not valid*
   1 = valid
28:24: Base Address (0 on reset)
   1MB RAM - all address bits used
   4MB RAM - only <28:26> used
2:1 RAM size
   01 = 1MB RAM
   10 = 4MB RAM
   11 = non-existent bank
0: Mode
   1 = 64-bit mode

NMC_CSR18: Mode Control and Diagnostic Status Register (2101 8048)
31: Fast Diagnostic Mode (FDM)
   0 = disabled* - diagnostic use only
30: FDM Second pass
   0 = disabled* - diagnostic use only
Configurable Machine State

29: Diagnostic Checkbit mode
0 = disabled* - diagnostic use only

28: QBus on IO1
0 = QBus on IO2*

27: Enable soft error log (NDAL & memory related)
0 = disabled* - OpenVMS enables this

26: Flush BCache
0 = don’t flush*

24:17: Memory diagnostic check bits (0*) - may not be read as 0

8:7: NDAL Timeout Scaler
00 = 2600 cycles* - maximum to preserve timeout order

6: Disable memory error
0 = memory errors detected and corrected*

5: Refresh interval timer select
0 = 328 cycles*

4:2: Force wrong parity on NDAL transactions - off
- diagnostic use only

1: Disable memory refresh
0 = memory refreshed*

0: Force refresh
0 = normal refresh*

NMC_CSR19: 0-bit Address and Mode Register (2101 804C)

16: Ignore 0-bit mode
0 = 0-bits checked*

15: Disable 0-bit error
0 = 0-bit errors detected*

14:6: 0-bit segment address (0*) - not used in normal operation

5:3: 0-bit mask (0*) - not used in normal operation

2:0: 0-bit operation mode
X00 = reconstruction mode* - not used in normal operation

NMC_OSCR: 0-bit Data Registers (2101 0000 thru 2101 7FFF)

23:12: 0-bit field 1 (0 at reset)

11:0: 0-bit field 0 (0 at reset)

NVAX: __________

CPUID: CPU ID Register (IPR E)
7:0: CPU identification = 0 (for single processor config.)

SID: System Identification Register (IPR 3E)
NOTE: this register may only be written by microcode
Configurable Machine State

31:24: CPU type - 13hex (NVAX code)
13:8: Patch revision
7:0: Microcode revision

ICSR: IBox Control and Status Register (IPR D3)
0: VIC enable
   1 = enabled

ECR: EBox Control Register (IPR 7D)
13: FBox test enable
   0 = disable* - diagnostic use only
7: Interval time mode
   1 = full CPU implemented interval timer
5: S3 stall timeout
   0 = counts cycles w/ timeout_enable asserted (~3 sec)*
3: FBox stage 4 bypass
   1 = enabled - improves FBox latency
2: S3 external time base timeout
   0 = disabled* - use internal time base
1: FBox enable
   1 = enabled
0: Vector present
   0 = no* - no vector option available at this time

MMAPEN: Memory Map Enable Register (IPR E6)
0: Memory map enable
   0 = disabled* - OpenVMS enables this

PAMODE: Physical Address Mode Register (IPR E7)
0: Physical address mode
   0 = 30-bit physical address space*

PCCTL: PCache Control Register (IPR F8)
8: PCache Electrical disable
   0 = PCache enabled*
7:5 MBox performance monitor mode (0*) - diagnostic use only
4: PCache error enable
   1 = enables PCache error detection
3: Bank select during force hit mode
   0 = left bank selected if force hit mode enabled* - diagnostic use only
2: Force hit
   0 = disabled* - diagnostic use only
1: I enable
   1 = enable PCache for IREAD, INVAL, I_CF commands
Configurable Machine State

0: D_enable
   1 = enable PCache for INVAL, D-stream read/write/fill

CCTL: CBox Control Register (IPR A0)
30: Software ETM
   0 = disabled* - diagnostic use only
16: Force NDAL parity error - off - diagnostic use only
15:11: Performance monitoring bits (0*) - diagnostic use only
10: Disable CBox write packer
    0 = write packer enabled* - improves write latency
9: Read timeout time base
   0 = external time base
8: Software ECC
   0 = use correct ECC*
7: Disable BCache errors
   0 = BCache errors detected*
6: Force Hit
   0 = disabled* - diagnostic use only
5:4: BCache size
   00 = 128 KB* (KA50/52/55)
   10 = 512 KB (KA51/53/54/56)
3:2: Data store speed
   00 = 2 cycle read, 3 cycle write* (KA51/53/54/56)
   01 = 3 cycle read, 4 cycle write (KA50/52)
   10 = 4 cycle read, 5 cycle write (KA55)
1: Tag store speed
   0 = 3 cycle read, 3 cycle write* (KA51/53/54/56)
   1 = 4 cycle read, 4 cycle write (KA50/52/55)
0: Enable BCache
   1 = enabled

CQBIC: ------

SCR: System Configuration Register (2008 0000)
14: Halt enable
    1 = BHALT to CQBIC HALTIN pin to cause halts
12: Page prefetch disable
    1 = map prefetch disabled - historical latency reasons
7: Restart enable
   0 = QBus restart causes ARB power-up reset*
3:1: ICR offset address select bits
   0 = (AUX mode not supported)*
Configurable Machine State

ICR: Interprocessor Communication Register (2000 1F40)
8: AUX Halt
   0 = no halt - AUX mode not supported
6: ICR interrupt enable
   0 = interprocessor interrupts disabled - only
      uniprocessor config. allowed
5: Local memory external access enable
   0 = external access disabled* - OpenVMS configures map

QBMBR: Q-Bus Map Base Address Register (2008 0010)
28:15: address where 8K QBus mapping register are located
      (undefined at reset)

SHAC: ----
NOTE: all SHAC registers are set up by OpenVMS driver

PQBBR: Port Queue Block Base Register (2000 4248)
20:0: upper bits of physical address of base of Port Queue
      block. Contains HW version, FW version, shared host
      memory version and CI port maintenance ID at power-up.

PPR: Port Parameter Register (2000 4258)
31:29: Cluster size. For SHAC value = 0.
28:16: Internal buffer length = 0* (For SHAC value = 1010 hex)
    7:0: Port number. Same as SHAC’s DSSI ID.

PMCSR: Port Maintenance Control and Status Register (2000 425C)
2: Interrupt enable
   0 = disabled*
1: Maintenance timer disable
   0 = enabled*

SGEC: ----
NOTE: all SGEC registers are set up by OpenVMS driver

NICSRO: Vector Address, IPL, Synch/Asynch Register (2000 8000)
31:30: Interrupt priority
       00 = 14*
29: Synch/Asynch bus master operating mode
    0 = asynchronous
15:0: Interrupt vector = 0003hex*
Configurable Machine State

NicSR6: Command and Mode Register  (2000 8018)
30: Interrupt enable
   0 = disabled*
28:25: Burst limit mode
   maximum number of longwords transferred in a single
   DMA burst. 1*, 2, 4, 8 when NICSR<19> is clear; 1*, 4
   when set.
20: Boot message enable mode
   0 = disabled*
19: Single cycle enable mode
   0 = disabled*
11: Start/Stop transmission command
   0 = SGEc transmission process in stopped state*
10: Start/Stop reception command
   0 = SGEc reception process in stopped state*
9:8: Operating mode
   00 = normal mode*
7: Disable data chaining mode
   0 = frames too long for current receive buffer
   will be transferred to the next buffer(s)
   in receive list*
6: Force collision mode (internal loopback mode only)
   0 = no collision*
3: Pass bad frames mode
   0 = bad frames discarded*
2:1: Address filtering mode
   00 = normal mode*

NicSR7: System Base Register  (2000 801C)
29:0: System base address – physical starting address of
   the VAX system page table (unpredictable after reset)

NicSR9: Watchdog Timers Register  (2000 8024)
31:16: Receive watchdog timeout
   0 = never timeout*
   default = 1250 = 2 ms
   range = 72 µs (45) to 100 ms
15:0: Transmit watchdog timeout
   0 = never timeout*
   default = 1250 = 2 ms
   range = 72 µs (45) to 100 ms

SSC:
---

SSC BAR: SSC Base Address Register  (2014 0000)
29:0: Base Address (reset value = 20140000)

SSCCR: SSC Configuration Register  (2014 0010)
27: Interrupt vector disable
   0 = interrupt vector enabled*
Configurable Machine State

25:24: IPL Level
    00 = 14*

23: ROM access time
    0 = 350 ns*

22:20: ROM size
    110 = 512KB

18:16: Halt protected space
    110 = 20040000 - 200BFFFF (historical)

15: n/a

14:12: n/a

6: Programmable address strobe 1 ready enable (for BDR)
    1 = ready asserted after address strobe

5:4: Programmable address strobe 1 enable (for BDR)
    11 = read enabled, write enabled

2: Programmable address strobe 0 ready enable
    0 = no ready after address strobe* Used for FE-ROM programming

1:0: Programmable address strobe 0 enable
    00 = read disabled, write disabled* Used for FE-ROM programming

SSCBT: SSC Bus Time Out Register (2014 0020)
    23:0: Bus timeout interval = 4000hex (16.384 ms)
    range = 1 to FFFFFF (1 μs to 16.77 sec)

ADSO MAT: Programmable Address Strobe 0 Match Register (2014 0130)
    29:2: Match address
        0 = disabled*

ADSMAS: Programmable Address Strobe 0 Mask Register (2014 0134)
    29:2: Mask address bits

ADS1MAT: Programmable Address Strobe 1 Match Register (2014 0140)
    29:2: Match address = 20084000 (for BDR)

ADS1MAS: Programmable Address Strobe 1 Mask Register (2014 0144)
    29:2: Mask address bits = 7C (for BDR)

T1CR: Programmable Timer 0 Control Register (2014 0100)
    6: Interrupt enable
        0 = disabled*

    2: STP
        0 = run after overflow*

    0: RUN
        0 = counter not running* (historical)
Configurable Machine State

TlCR: Programmable Timer 1 Control Register (2014 0110)
  6:  Interrupt enable
       0 = disabled*
  2:  STP
       0 = run after overflow*
  0:  RUN
       1 = counter incrementing every microsecond (historical)

TNIR: Programmable Timer Next Interval Registers (2014 0108, 2014 0118)
  31:0:  Timer next interval count (use 2's complement)
        range = 0* to 1.2 hours

T0IV: Programmable Timer 0 Interrupt Vector Register (2014 010C)
  9:2:  Timer interrupt vector = 78hex

T1IV: Programmable Timer 1 Interrupt Vector Registers (2014 011C)
  9:2:  Timer interrupt vector = 7Chex

TOY: Time of Year Register (2014 006C)
  31:0:  Number of 10 ms intervals since written

DLEDR: Diagnostic LED Register (2014 0030)
  3:0:  Display bits
        0 = LEDs on* (historical)
This appendix describes how the CPU firmware partitions the SSC 1 KB battery-backed-up (BBU) RAM.

__________________________ Note ___________________________

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95 and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q–bus and DSSI, will appear on the console and/or printouts from time to time.

__________________________

E.1 SSC RAM Layout

The KA50/51/55/56 firmware uses the 1K byte of NVRAM on the SSC (see Figure E–1), for storage of firmware specific data structures and other information that must be preserved across power cycles. This NVRAM resides in the SSC chip starting at address 20140400. The NVRAM should not be used by the operating systems except as documented below. This NVRAM is not reflected in the bitmap built by the firmware.
NVRAM Partitioning
E.1 SSC RAM Layout

Figure E-1  KA50/51/55/56 SSC NVRAM Layout

<table>
<thead>
<tr>
<th>Field</th>
<th>Public Data Structures (CPMBX, etc.)</th>
<th>Service Vectors</th>
<th>Firmware Stack</th>
<th>Diagnostic State</th>
<th>Resvd for Customer Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>20140400</td>
<td>Public Data Structures (CPMBX, etc.)</td>
<td>Service Vectors</td>
<td>Firmware Stack</td>
<td>Diagnostic State</td>
<td>Resvd for Customer Use</td>
</tr>
<tr>
<td>201407FC</td>
<td>Public Data Structures (CPMBX, etc.)</td>
<td>Service Vectors</td>
<td>Firmware Stack</td>
<td>Diagnostic State</td>
<td>Resvd for Customer Use</td>
</tr>
</tbody>
</table>

E.1.1 Public Data Structures

Public data structures consist of three bytes, NVR0, NVR1, and NVR2. Their functions are described in Table E-1, Table E-2, and Table E-3.

E.1.1.1 Console Program MailBoX (CPMBX)

The Console Program MailBoX (CPMBX) comprised of NVR0, is a software data structure located at the beginning of NVRAM (20140400). The CPMBX is used to pass information between the CPU firmware and diagnostics, VMB, or an operating system.

Figure E-2  NVR0 (20140400) : Console Program MailBoX (CPMBX)

<table>
<thead>
<tr>
<th>Field</th>
<th>LANGUAGE</th>
<th>RIP</th>
<th>BIP</th>
<th>HLT_ACT</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:6</td>
<td>LANGUAGE</td>
<td>RIP</td>
<td>BIP</td>
<td>HLT_ACT</td>
</tr>
</tbody>
</table>

Table E-1  Bit Functions for NVR0

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:4</td>
<td>LANGUAGE</td>
<td>This field specifies the current selected language for displaying halt and error messages on terminals which support MCS.</td>
</tr>
<tr>
<td>3</td>
<td>RIP</td>
<td>If set, a restart attempt is in progress. This flag must be cleared by the operating system, if the restart succeeds. (continued on next page)</td>
</tr>
</tbody>
</table>
Table E–1 (Cont.) Bit Functions for NVR0

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>BIP</td>
<td>If set, a bootstrap attempt is in progress. This flag must be cleared by the operating system if the bootstrap succeeds.</td>
</tr>
<tr>
<td>1:0</td>
<td>HLT_ACT</td>
<td>Processor halt action - this field in conjunction with the conditions specified for system halts is used to control the automatic restart/bootstrapping procedure. HLT_ACT is normally written by the operating system.</td>
</tr>
</tbody>
</table>

- 0: Restart; if that fails, reboot; if that fails, halt.
- 1: Restart; if that fails, halt.
- 2: Reboot; if that fails, halt.
- 3: Halt.

---

E.1.1.2 Terminal Status

Figure E–3 NVR1 (20140401)

![Figure E–3](image)

Table E–2 Bit Functions for NVR1

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>MCS</td>
<td>If set, indicates that the attached terminal supports Multinational Character Set. If clear, MCS is not supported.</td>
</tr>
<tr>
<td>1</td>
<td>CRT</td>
<td>If set, indicates that the attached terminal is a CRT. If clear, indicates that the terminal is hardcopy.</td>
</tr>
</tbody>
</table>

---

E.1.1.3 Keyboard Status

Figure E–4 NVR2 (20140402)

![Figure E–4](image)
**NVRAM Partitioning**

**E.1 SSC RAM Layout**

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>KEYBOARD</td>
<td>This field indicates the national keyboard variant in use.</td>
</tr>
</tbody>
</table>

**E.1.2 Service Vectors**

Service vectors point to the routines for the reading or writing of characters by the console.

**E.1.3 Firmware Stack**

This section contains the stack that is used by all of the firmware, with the exception of VMB, which has its own built-in stack.

**E.1.4 Diagnostic State**

This area is used by the firmware resident diagnostics. It serves as the primary communications mechanism between the diagnostics and the console program.

**E.1.5 USER Area**

The KA50/51/55/56 console reserves the last longword (address 201407FC) of the NVRAM for customer use. This location is not tested by the console firmware. Its value is undefined.
MOP Counters

The following counters are kept for the Ethernet boot channel. All counters are unsigned integers. V4 counters rollover on overflow. All V3 counters "latch" at their maximum value to indicate overflow. Unless otherwise stated, all counters include both normal and multicast traffic. Furthermore, they include information for all protocol types. Frames received and bytes received counters do not include frames received with errors. Table F–1 displays the byte lengths and ordering of all the counters in both MOP Versions 3.0 and 4.0.

Table F–1 MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>V3 Off Len</th>
<th>V4 Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIME_SINCE_CREATION</td>
<td>00 2</td>
<td>00 16</td>
<td>Time since last zeroed. The time which has elapsed, since the counters were last zeroed. Provides a frame of reference for the other counters by indicating the amount of time they cover. For MOP V3, this time is the number of seconds. MOP V4 uses the UTC Binary Relative Time format.</td>
</tr>
</tbody>
</table>

(continued on next page)
### Table F-1 (Cont.) MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>Off</th>
<th>Len</th>
<th>Off</th>
<th>Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>V3</td>
<td></td>
<td></td>
<td>V4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rx_BYTES</td>
<td>02</td>
<td>4</td>
<td>10</td>
<td>8</td>
<td><strong>Bytes received.</strong> The total number of user data bytes successfully received. This does not include Ethernet data link headers. This number is the number of bytes in the Ethernet data field, which includes any padding or length fields when they are enabled. These are bytes from frames that passed hardware filtering. When the number of frames received is used to calculate protocol overhead, the overhead plus bytes received provides a measurement of the amount of Ethernet bandwidth (over time) consumed by frames addressed to the local system.</td>
</tr>
<tr>
<td>Tx_BYTES</td>
<td>06</td>
<td>4</td>
<td>18</td>
<td>8</td>
<td><strong>Bytes sent.</strong> The total number of user data bytes successfully transmitted. This does not include Ethernet data link headers or data link generated retransmissions. This number is the number of bytes in the Ethernet data field, which includes any padding or length fields when they are enabled. When the number of frames sent is used to calculate protocol overhead, the overhead plus bytes sent provides a measurement of the amount of Ethernet bandwidth (over time) consumed by frames sent by the local system.</td>
</tr>
</tbody>
</table>

(continued on next page)
### Table F–1 (Cont.) MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>V3 Off Len</th>
<th>V3 Len</th>
<th>V4 Off Len</th>
<th>V4 Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rx_FRAMES</td>
<td>0A 4</td>
<td>20 8</td>
<td></td>
<td></td>
<td><strong>Frames received.</strong> The total number of frames successfully received. These are frames that passed hardware filtering. Provides a gross measurement of incoming Ethernet usage by the local system. Provides information used to determine the ratio of the error counters to successful transmits.</td>
</tr>
<tr>
<td>Tx_FRAMES</td>
<td>0E 4</td>
<td>28 8</td>
<td></td>
<td></td>
<td><strong>Frames sent.</strong> The total number of frames successfully transmitted. This does not include data link generated retransmissions. Provides a gross measurement of outgoing Ethernet usage by the local system. Provides information used to determine the ratio of the error counters to successful transmits.</td>
</tr>
<tr>
<td>Rx_MCAST_BYTES</td>
<td>12 4</td>
<td>30 8</td>
<td></td>
<td></td>
<td><strong>Multicast bytes received.</strong> The total number of multicast data bytes successfully received. This does not include Ethernet data link headers. This number is the number of bytes in the Ethernet data field. In conjunction with total bytes received, provides a measurement of the percentage of this system's receive bandwidth (over time) that was consumed by multicast frames addressed to the local system.</td>
</tr>
<tr>
<td>Rx_MCAST_FRAMES</td>
<td>16 4</td>
<td>38 8</td>
<td></td>
<td></td>
<td><strong>Multicast frames received.</strong> The total number of multicast frames successfully received. In conjunction with total frames received, provides a gross percentage of the Ethernet usage for multicast frames addressed to this system.</td>
</tr>
</tbody>
</table>

(continued on next page)
## MOP Counters

### Table F-1 (Cont.) MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>V3 Off</th>
<th>Len</th>
<th>V4 Off</th>
<th>Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx_INIT_DEFERRED</td>
<td>1A</td>
<td>4</td>
<td>40</td>
<td>8</td>
<td><strong>Frames sent(^1), initially deferred.</strong> The total number of times that a frame transmission was deferred on its first transmission attempt. In conjunction with total frames sent, measures Ethernet contention with no collisions.</td>
</tr>
<tr>
<td>Tx_ONE_COLLISION</td>
<td>1E</td>
<td>4</td>
<td>48</td>
<td>8</td>
<td><strong>Frames sent(^1), single collision.</strong> The total number of times that a frame was successfully transmitted on the second attempt after a normal collision on the first attempt. In conjunction with total frames sent, measures Ethernet contention at a level where there are collisions but the backoff algorithm still operates efficiently.</td>
</tr>
<tr>
<td>Tx_MULTI_COLLISION</td>
<td>22</td>
<td>4</td>
<td>50</td>
<td>8</td>
<td><strong>Frames sent(^1), multiple collisions.</strong> The total number of times that a frame was successfully transmitted on the third or later attempt after normal collisions on previous attempts. In conjunction with total frames sent, measures Ethernet contention at a level where there are collisions and the backoff algorithm no longer operates efficiently. <strong>No single frame is counted in more than one of the above three counters.</strong></td>
</tr>
</tbody>
</table>

\(^1\)Only one of these three counters will be incremented for a given frame.

(continued on next page)
## MOP Counters

<table>
<thead>
<tr>
<th>Name</th>
<th>Off Len</th>
<th>Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TxFAIL_COUNT</td>
<td>26 2</td>
<td>-</td>
<td><strong>Send failure count</strong>&lt;sup&gt;2&lt;/sup&gt;. The total number of times a transmit attempt failed. Each time the counter is incremented, a type of failure is recorded. When Read-counter function reads the counter, the list of failures is also read. When the counter is set to zero, the list of failures is cleared. In conjunction with total frames sent, provides a measure of significant transmit problems. TxFAIL_BITMAP contains the possible reasons.</td>
</tr>
<tr>
<td>TxFAIL_BITMAP</td>
<td>2C 2</td>
<td>-</td>
<td><strong>Send failure reason bitmap</strong>&lt;sup&gt;2&lt;/sup&gt;. This bitmap lists the types of transmit failures that occurred as summarized below:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 - Excessive collisions</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 - Carrier detect failed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2 - Short circuit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3 - Open circuit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4 - Frame too long</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5 - Remote failure to defer</td>
</tr>
<tr>
<td>TxFAIL_EXCESS_COLLS</td>
<td>- -</td>
<td>58 8</td>
<td><strong>Send failure—Excessive collisions. Exceeded the maximum number of retransmissions due to collisions. Indicates an overload condition on the Ethernet.</strong></td>
</tr>
</tbody>
</table>

<sup>2</sup>V3 send/receive failures are collapsed into one counter with bitmap indicating which failures occurred.

(continued on next page)
### MOP Counters

#### Table F-1 (Cont.)  MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>V3</th>
<th>V4</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TxFAIL_CARRIER_CHECK</td>
<td>-</td>
<td>60</td>
<td>8</td>
</tr>
<tr>
<td>TxFAIL_SHORT_CIRCUIT</td>
<td>-</td>
<td>68</td>
<td>8</td>
</tr>
<tr>
<td>TxFAIL_OPEN_CIRCUIT</td>
<td>-</td>
<td>70</td>
<td>8</td>
</tr>
<tr>
<td>TxFAIL_LONG_FRAME</td>
<td>-</td>
<td>78</td>
<td>8</td>
</tr>
</tbody>
</table>

³Always zero.

(continued on next page)
## MOP Counters

### Table F-1 (Cont.) MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>Off</th>
<th>Len</th>
<th>Off</th>
<th>Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TxFail_REMOTE_DEFER</td>
<td>-</td>
<td>-</td>
<td>80</td>
<td>8</td>
<td><strong>Send failure—Remote failure to defer</strong>. A remote system began transmitting after the allowed window for collisions. This indicates either a problem with some other system’s carrier sense or a weak transmitter.</td>
</tr>
<tr>
<td>RxFAIL_COUNT</td>
<td>2A</td>
<td>2</td>
<td>-</td>
<td>-</td>
<td><strong>Receive failure count</strong>. The total number of frames received with some data error. Includes only data frames that passed either physical or multicast address comparison. This counter includes failure reasons in the same way as the send failure counter. In conjunction with total frames received, provides a measure of data related receive problems. RxFAIL_BITMAP contains the possible reasons.</td>
</tr>
<tr>
<td>RxFAIL_BITMAP</td>
<td>2C</td>
<td>2</td>
<td>-</td>
<td>-</td>
<td><strong>Receive failure reason bitmap</strong>. This bitmap lists the types of receive failures that occurred as summarized below:</td>
</tr>
</tbody>
</table>
|                       |     |     |     |     | 0 : Block check failure  
|                       |     |     |     | 1 : Framing error  
|                       |     |     |     | 2 : Frame too long |
| RxFAIL_BLOCK_CHECK    | -   | -   | 88  | 8   | **Receive failure—Block check error**. A frame failed the CRC check. This indicates several possible failures, such as EMI, late collisions, or improperly set hardware parameters. |

2V.3 send/receive failures are collapsed into one counter with bitmap indicating which failures occurred.

3Always zero.
### MOP Counters

#### Table F-1 (Cont.) MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>V3 Off Len</th>
<th>V4 Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RxFAIL_FRAMING_ERR</td>
<td>- -</td>
<td>90 8</td>
<td><strong>Receive failure—Framing error.</strong> The frame did not contain an integral number of 8 bit bytes. This indicates several possible failures, such as EMI, late collisions, or improperly set hardware parameters.</td>
</tr>
<tr>
<td>RxFAIL_LONG_FRAME</td>
<td>- -</td>
<td>98 8</td>
<td><strong>Receive failure—Frame too long</strong>. The frame was discarded because it was outside the Ethernet maximum length and could not be received. This indicates that a remote system is sending invalid length frames.</td>
</tr>
<tr>
<td>UNKNOWN_DESTINATION</td>
<td>2E 2</td>
<td>A0 8</td>
<td><strong>Unrecognized frame destination.</strong> The number of times a frame was discarded because there was no portal with the protocol type or multicast address enabled. This includes frames received for the physical address, the broadcast address, or a multicast address.</td>
</tr>
<tr>
<td>DATA_OVERRUN</td>
<td>30 2</td>
<td>A8 8</td>
<td><strong>Data overrun.</strong> The total number of times the hardware lost an incoming frame because it was unable to keep up with the data rate. In conjunction with total frames received, provides a measure of hardware resource failures. The problem reflected in this counter is also captured as an event.</td>
</tr>
</tbody>
</table>

---

3Always zero.

(continued on next page)
### MOP Counters

**Table F–1 (Cont.) MOP Counter Block**

<table>
<thead>
<tr>
<th>Name</th>
<th>V3 Oft Len</th>
<th>V3 Off Len</th>
<th>V4 Oft Len</th>
<th>V4 Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO_SYSTEM_BUFFER</td>
<td>32 2</td>
<td>B0 8</td>
<td></td>
<td></td>
<td><strong>System buffer unavailable</strong>&lt;sup&gt;3&lt;/sup&gt;. The total number of times no system buffer was available for an incoming frame. In conjunction with total frames received, provides a measure of system buffer related receive problems. The problem reflected in this counter is also captured as an event. This can be any buffer between the hardware and the user buffers (those supplied on Receive requests). Further information as to potential different buffer pools is implementation specific.</td>
</tr>
<tr>
<td>NO_USER_BUFFER</td>
<td>34 2</td>
<td>B8 8</td>
<td></td>
<td></td>
<td><strong>User buffer unavailable</strong>&lt;sup&gt;3&lt;/sup&gt;. The total number of times no user buffer was available for an incoming frame that passed all filtering. These are the buffers supplied by users on Receive requests. In conjunction with total frames received, provides a measure of user buffer related receive problems. The problem reflected in this counter is also captured as an event.</td>
</tr>
<tr>
<td>FAIL_COLLIS_DETECT</td>
<td>- -</td>
<td>C0 8</td>
<td></td>
<td></td>
<td><strong>Collision detect check failure.</strong> The approximate number of times that collision detect was not sensed after a transmission. If this counter contains a number roughly equal to the number of frames sent, either the collision detect circuitry is not working correctly or the test signal is not implemented.</td>
</tr>
</tbody>
</table>

<sup>3</sup>Always zero.
The error messages issued by the KA50/51/55/56 firmware fall into three categories: halt code messages, VMB error messages, and console messages.

G.1 Machine Check Register Dump

Some error conditions, such as machine check, generate an error summary register dump preceding the error message. For example, examining a nonexistent memory location results in the following display:

```
>>> e/p/1 20000000
MCSR=00000600  MEAR=08400610  MMCDSR=01111110  MDAB=00000000
CESR=80000200  CMCDSR=00001008  CSEX=00000000  CSEAR=00000000
CIOEAR1=00000000  CIOEAR2=00000000  CNEAR=00000000  ICISR=00000010
PCSTS=FFFF8000  PCADR=FFFFFF80  TBSTS=00000000  TBAADR=F5755754
NEDSR=0000000000  NECDSR=ED14066C  NECOMM=80000000  NEICMD=9000003FFF
NEATHI=FFFFFFF  NEATLO=FF7F8FF  CEFSTS=0001920A  CEFADR=50000000
BCEDSTS=00000000  BCEDIDX=FFFFFE00  BCETAG=FFFFFE00  BCEDSTS=00000000
QBEAR=00000000  QEAR=00000000  LPCR=00000000  ECR=00000000
SCSICSR4-00  SCSICSR6-CO  SCSICSR5-00
?7D MACHINE CHECK 80000000 00000000 20048C68 20048C59 20048C55 40110080
>>>```

G.2 Halt Code Messages

Except on power-up, which is not treated as an error condition, the following halt messages are issued by the firmware whenever the processor halts (Table G-1).

For example, if the processor encounters a .HALT instruction while in kernel mode, the processor halts and the firmware displays the following before entering console I/O mode:

```
?06 HLT INST
PC = 800050D3```
**Error Messages**

**G.2 Halt Code Messages**

The number preceding the halt message is the "halt code." This number is obtained from SAVPSL<13:8>(RESTART_CODE), IPR 43, which is saved on any processor restart operation.

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>02</td>
<td>EXT HLT</td>
<td>External halt, caused by either console BREAK condition, Q22–bus BHALT_L, or DBR&lt;AUX_HLT&gt; bit was set while enabled.</td>
</tr>
<tr>
<td>03</td>
<td>—</td>
<td>Power-up, no halt message is displayed. However, the presence of the firmware banner and diagnostic countdown indicates this halt reason.</td>
</tr>
<tr>
<td>04</td>
<td>ISP ERR</td>
<td>In attempting to push state onto the interrupt stack during an interrupt or exception, the processor discovered that the interrupt stack was mapped NO ACCESS or NOT VALID.</td>
</tr>
<tr>
<td>05</td>
<td>DBL ERR</td>
<td>The processor attempted to report a machine check to the operating system, and a second machine check occurred.</td>
</tr>
<tr>
<td>06</td>
<td>HLT INST</td>
<td>The processor executed a HALT instruction in kernel mode.</td>
</tr>
<tr>
<td>07</td>
<td>SCB ERR3</td>
<td>The SCB vector had bits &lt;1:0&gt; equal to 3.</td>
</tr>
<tr>
<td>08</td>
<td>SCB ERR2</td>
<td>The SCB vector had bits &lt;1:0&gt; equal to 2.</td>
</tr>
<tr>
<td>0A</td>
<td>CHM FR ISTK</td>
<td>A change mode instruction was executed when PSL&lt;IS&gt; was set.</td>
</tr>
<tr>
<td>0B</td>
<td>CHM TO ISTK</td>
<td>The SCB vector for a change mode had bit &lt;0&gt; set.</td>
</tr>
<tr>
<td>0C</td>
<td>SCB RD ERR</td>
<td>A hard memory error occurred while the processor was trying to read an exception or interrupt vector.</td>
</tr>
<tr>
<td>10</td>
<td>MCHK AV</td>
<td>An access violation or an invalid translation occurred during machine check exception processing.</td>
</tr>
<tr>
<td>11</td>
<td>KSP AV</td>
<td>An access violation or translation not valid occurred during processing of a kernel stack not valid exception.</td>
</tr>
<tr>
<td>12</td>
<td>DBL ERR2</td>
<td>Double machine check error. A machine check occurred while trying to service a machine check.</td>
</tr>
<tr>
<td>13</td>
<td>DBL ERR3</td>
<td>Double machine check error. A machine check occurred while trying to service a kernel stack not valid exception.</td>
</tr>
<tr>
<td>19</td>
<td>PSL EXCS1</td>
<td>PSL&lt;26:24&gt; = 5 on interrupt or exception.</td>
</tr>
</tbody>
</table>

1For the last six cases, the VAX architecture does not allow execution on the interrupt stack while in a mode other than kernel. In the first three cases, an interrupt is attempting to run on the interrupt stack while not in kernel mode. In the last three cases, an REI instruction is attempting to return to a mode other than kernel and still run on the interrupt stack.

(continued on next page)


**Error Messages**

**G.2 Halt Code Messages**

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?1A</td>
<td>PSL EXC6(^1)</td>
<td>PSL&lt;26:24&gt; = 6 on interrupt or exception.</td>
</tr>
<tr>
<td>?1B</td>
<td>PSL EXC7(^1)</td>
<td>PSL&lt;26:24&gt; = 7 on interrupt or exception.</td>
</tr>
<tr>
<td>?1D</td>
<td>PSL REI5(^1)</td>
<td>PSL&lt;26:24&gt; = 5 on an REI instruction</td>
</tr>
<tr>
<td>?1E</td>
<td>PSL REI6(^1)</td>
<td>PSL&lt;26:24&gt; = 6 on an REI instruction</td>
</tr>
<tr>
<td>?1F</td>
<td>PSL REI7(^1)</td>
<td>PSL&lt;26:24&gt; = 7 on an REI instruction</td>
</tr>
<tr>
<td>?3F</td>
<td>MICROVERIFY</td>
<td>Microcode power-up self-test failed.</td>
</tr>
<tr>
<td></td>
<td>FAILURE</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\)For the last six cases, the VAX architecture does not allow execution on the interrupt stack while in a mode other than kernel. In the first three cases, an interrupt is attempting to run on the interrupt stack while not in kernel mode. In the last three cases, an REI instruction is attempting to return to a mode other than kernel and still run on the interrupt stack.

**G.3 VMB Error Messages**

VMB issues the errors listed in Table G–2.

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?40</td>
<td>NOSUCHDEV</td>
<td>No bootable devices found.</td>
</tr>
<tr>
<td>?41</td>
<td>DEVAISSIGN</td>
<td>Device is not present.</td>
</tr>
<tr>
<td>?42</td>
<td>NOSUCHFILE</td>
<td>Program image not found.</td>
</tr>
<tr>
<td>?43</td>
<td>FILESTRUCT</td>
<td>Invalid boot device file structure.</td>
</tr>
<tr>
<td>?44</td>
<td>BADCHKSUM</td>
<td>Bad checksum on header file.</td>
</tr>
<tr>
<td>?45</td>
<td>BADFILEHDR</td>
<td>Bad file header.</td>
</tr>
<tr>
<td>?46</td>
<td>BADDIRECTORY</td>
<td>Bad directory file.</td>
</tr>
<tr>
<td>?47</td>
<td>FILNOTCNTG</td>
<td>Invalid program image format.</td>
</tr>
<tr>
<td>?48</td>
<td>ENDOFFILE</td>
<td>Premature end of file encountered.</td>
</tr>
<tr>
<td>?49</td>
<td>BADFILENAME</td>
<td>Bad filename given.</td>
</tr>
<tr>
<td>?4A</td>
<td>BUFFEROVF</td>
<td>Program image does not fit in available memory.</td>
</tr>
<tr>
<td>?4B</td>
<td>CTRLERR</td>
<td>Boot device I/O error.</td>
</tr>
</tbody>
</table>

(continued on next page)
Error Messages
G.3 VMB Error Messages

Table G–2 (Cont.) VMB Error Messages

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?4C</td>
<td>DEVINACT</td>
<td>Failed to initialize boot device.</td>
</tr>
<tr>
<td>?4D</td>
<td>DEVOFFLINE</td>
<td>Device is offline.</td>
</tr>
<tr>
<td>?4E</td>
<td>MEMERR</td>
<td>Memory initialization error.</td>
</tr>
<tr>
<td>?4F</td>
<td>SCBINT</td>
<td>Unexpected SCB exception or machine check.</td>
</tr>
<tr>
<td>?50</td>
<td>SCB2NDINT</td>
<td>Unexpected exception after starting program image.</td>
</tr>
<tr>
<td>?51</td>
<td>NOROM</td>
<td>No valid ROM image found.</td>
</tr>
<tr>
<td>?52</td>
<td>NOSUCHNODE</td>
<td>No response from load server.</td>
</tr>
<tr>
<td>?53</td>
<td>INSFMAPREG</td>
<td>The Q22–bus map initialization failed.</td>
</tr>
<tr>
<td>?54</td>
<td>RETRY</td>
<td>No devices bootable, retrying.</td>
</tr>
<tr>
<td>?55</td>
<td>IVDEVNAM</td>
<td>Invalid device name.</td>
</tr>
<tr>
<td>?56</td>
<td>DRVERR</td>
<td>Drive error.</td>
</tr>
</tbody>
</table>

G.4 Console Error Messages

The error messages listed in Table G–3 are issued in response to a console command that has error(s).

Table G–3 Console Error Messages

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?61</td>
<td>CORRUPTION</td>
<td>The console program database has been corrupted.</td>
</tr>
<tr>
<td>?62</td>
<td>ILLEGAL REFERENCE</td>
<td>Illegal reference. The requested reference would violate virtual memory protection, the address is not mapped, the reference is invalid in the specified address space, or the value is invalid in the specified destination.</td>
</tr>
<tr>
<td>?63</td>
<td>ILLEGAL COMMAND</td>
<td>The command string cannot be parsed.</td>
</tr>
<tr>
<td>?64</td>
<td>INVALID DIGIT</td>
<td>A number has an invalid digit.</td>
</tr>
<tr>
<td>?65</td>
<td>LINE TOO LONG</td>
<td>The command was too large for the console to buffer. The message is issued only after receipt of the terminating carriage return.</td>
</tr>
<tr>
<td>?66</td>
<td>ILLEGAL ADDRESS</td>
<td>The address specified falls outside the limits of the address space.</td>
</tr>
</tbody>
</table>

(continued on next page)
## Error Messages

### G.4 Console Error Messages

**Table G-3 (Cont.)  Console Error Messages**

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>767</td>
<td>VALUE TOO LARGE</td>
<td>The value specified does not fit in the destination.</td>
</tr>
<tr>
<td>768</td>
<td>QUALIFIER CONFLICT</td>
<td>Qualifier conflict; for example, two different data sizes are specified for an EXAMINE command.</td>
</tr>
<tr>
<td>769</td>
<td>UNKNOWN QUALIFIER</td>
<td>The switch is unrecognized.</td>
</tr>
<tr>
<td>76A</td>
<td>UNKNOWN SYMBOL</td>
<td>The symbolic address in an EXAMINE or DEPOSIT command is unrecognized.</td>
</tr>
<tr>
<td>76B</td>
<td>CHECKSUM</td>
<td>The command or data checksum of an X command is incorrect. If the data checksum is incorrect, this message is issued, and is not abbreviated to &quot;Illegal command&quot;.</td>
</tr>
<tr>
<td>76C</td>
<td>HALTED</td>
<td>The operator entered a HALT command.</td>
</tr>
<tr>
<td>76D</td>
<td>FIND ERROR</td>
<td>A FIND command failed either to find the RPB or 128 KB of good memory.</td>
</tr>
<tr>
<td>76E</td>
<td>TIME OUT</td>
<td>During an X command, data failed to arrive in the time expected (60 seconds).</td>
</tr>
<tr>
<td>76F</td>
<td>MEMORY ERROR</td>
<td>A machine check occurred with a code indicating a read or write memory error.</td>
</tr>
<tr>
<td>770</td>
<td>UNIMPLEMENTED</td>
<td>Unimplemented function.</td>
</tr>
<tr>
<td>771</td>
<td>NO VALUE QUALIFIER</td>
<td>Qualifier does not take a value.</td>
</tr>
<tr>
<td>772</td>
<td>AMBIGUOUS QUALIFIER</td>
<td>There were not enough unique characters to determine the qualifier.</td>
</tr>
<tr>
<td>773</td>
<td>VALUE QUALIFIER</td>
<td>Qualifier requires a value.</td>
</tr>
<tr>
<td>774</td>
<td>TOO MANY QUALIFIERS</td>
<td>Too many qualifiers supplied for this command.</td>
</tr>
<tr>
<td>775</td>
<td>TOO MANY ARGUMENTS</td>
<td>Too many arguments supplied for this command.</td>
</tr>
<tr>
<td>776</td>
<td>AMBIGUOUS COMMAND</td>
<td>There were not enough unique characters to determine the command.</td>
</tr>
<tr>
<td>777</td>
<td>TOO FEW ARGUMENTS</td>
<td>Insufficient arguments supplied for this command.</td>
</tr>
<tr>
<td>778</td>
<td>TYPEAHEAD OVERFLOW</td>
<td>The typeahead buffer overflowed.</td>
</tr>
<tr>
<td>779</td>
<td>FRAMING ERROR</td>
<td>A framing error was detected on the console serial line.</td>
</tr>
<tr>
<td>77A</td>
<td>OVERRUN ERROR</td>
<td>An overrun error was detected on the console serial line.</td>
</tr>
<tr>
<td>77B</td>
<td>SOFT ERROR</td>
<td>A soft error occurred.</td>
</tr>
<tr>
<td>77C</td>
<td>HARD ERROR</td>
<td>A hard error occurred.</td>
</tr>
<tr>
<td>77D</td>
<td>MACHINE CHECK</td>
<td>A machine check occurred.</td>
</tr>
</tbody>
</table>

(continued on next page)
## Error Messages
### G.4 Console Error Messages

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?7E</td>
<td>CONSOLE STACK OVERRUN</td>
<td>SSC RAM stack overflowed into NVR.</td>
</tr>
<tr>
<td>?7F</td>
<td>COMMAND NOT SUPPORTED</td>
<td>Command on similar modules not supported on this product.</td>
</tr>
<tr>
<td>?80</td>
<td>ILLEGAL PASSWORD</td>
<td>Password is not 16 characters in length.</td>
</tr>
<tr>
<td>?81</td>
<td>INCORRECT PASSWORD</td>
<td>Password entered does not match previously entered password.</td>
</tr>
<tr>
<td>?82</td>
<td>PASSWORD FACILITY NOT Enabled</td>
<td>A password has not been set.</td>
</tr>
</tbody>
</table>
Related Documents

The following documents contain information relating to the maintenance of systems that use the KA50/51/55/56 CPU modules.

<table>
<thead>
<tr>
<th>Title</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Guide to BA42B-Based MicroVAX 3100 Systems Service Information Kit</td>
<td>EK-M3100-IN</td>
</tr>
<tr>
<td>MicroVAX 3100 Models 30, 40, 80, 85, 90, 95, 96 System Illustrated Parts Breakdown</td>
<td>EK-MV310-IP</td>
</tr>
<tr>
<td>MicroVAX 3100 BA42B Enclosure Maintenance</td>
<td>EK-M3100-MG</td>
</tr>
<tr>
<td>MicroVAX 3100 BA42B Enclosure System Options</td>
<td>EK-M3100-OP</td>
</tr>
<tr>
<td>OpenVMS Factory Installed Software User Guide</td>
<td>EK-A0377-UG</td>
</tr>
</tbody>
</table>

¹# = current revision, which is always shipped.
ASCII
American standard code for information interchange.

BFLAG
Boot FLAG is the longword supplied in the SET BFLAG and BOOT /R5: commands that qualify the bootstrap operation. SHOW BFLAG displays the current value.

BHALT
Q22–bus Halt signal is usually tied to the front panel Halt switch.

BIP
Boot In Progress flag in CPMBX<2>

Bootstrap
A link between console mode (the system firmware) and programming mode (the operating system).

Bugcheck
Software or hardware error fatal to OpenVMS processor or system.

Cache memory
A small, high-speed memory placed between slower main memory and the processor. A cache increases effective memory transfer rates and processor speed.

CMOS
Complementary metal oxide semiconductor.
CPMBX
Console Program Mailbox is used to pass information between operating systems and the firmware.

CRC
Character code recognition. The use of pattern recognition techniques to identify characters by automatic means.

CQVIC
CVAX to Q22-bus interface chip.

CSR
Control status register. A register used to control the operation of a device and record the status of an operation or both.

CPU
Central processing unit. The main unit of a computer containing the circuits that control the interpretation and execution of instructions. The CPU holds the main storage, arithmetic unit, and special registers.

DCOK
Q22-bus signal indicating dc power is stable. This signal is tied to the Restart switch on the System Control Panel.

DE
Diagnostic Executive is a component of the ROM-based diagnostics responsible for set-up, execution, and clean-up of component diagnostic tests.

DMA
Direct memory access. A method of accessing a device's memory without interacting with the device's CPU.

DNA
Digital Network Architecture.

EPROM
Erasable programmable read-only memory. EPROM is a type of read-only memory that can be erased by using ultraviolet light, returning the device to a blank state.
ECC
Error Correction Code. Code that carries out automatic error correction by performing an exclusive "or" operation on the transferred data and applying a correction mask.

Factory Installed Software (FIS)
Operating system software loaded into a system disk during manufacture. On site, the FIS is bootstrapped in the system, prompting a predefined menu of questions on the final configuration.

FEPROM
Flash Erasable Programmable Read-Only Memory (FEPROM). FEPROMs use electrical (bulk) erasure rather than ultraviolet erasure.

FIFO
First-in/first-out. A method used for processing or recovering data in which the oldest item is processed or recovered first.

Firmware
Functionally it consists of diagnostics, bootstraps, console, and halt entry/exit code.

FPU
Floating-point unit. A unit that handles the automatic positioning of the decimal point during arithmetic operations.

FRU
Field replaceable unit.

GPR
General Purpose Registers. On the KA52/53, they are the sixteen standard VAX longword registers R0 through R15. The last four registers, R12 through R15, are also known by their unique mnemonics: AP (Argument Pointer), FP (Frame Pointer), SP (Stack Pointer), and PC (Program Counter), respectively.

Initialization
The sequence of steps that prepare the system to start. Initialization occurs after a system has been powered up.

IPL
Interrupt Priority Level ranges from 0 to 31 (0 to 1F hex).
IPR
Internal Processor Registers implemented by the processor chip set. These longword registers are only accessible with the instructions MTPR (Move To Processor Register) and MFPR (Move From Processor Register) and require kernel mode privileges. This document uses the prefix "PR$_" when referencing these registers.

ISE

IT
Interval timer.

LED
Light emitting diode.

Machine check
An operating system action triggered by certain system errors that can be fatal to system operation. Once triggered, machine check handler software analyzes the error, comparing it to predetermined failure scenarios. Three outcomes are possible: the system continues to run, the software program is halted, or the system crashes.

μs
Microsecond (10e-6 seconds)

MMJ
Modified modular jack.

MOP

ms
Millisecond (10e-3 seconds)

MSCP
Mass Storage Control Protocol is used in Digital disks and tapes.
NVR
Nonvolatile random access memory. A memory device that retains information in the absence of power.

NVRAM
Nonvolatile RAM. On the KA52/53, this is 1 Kb of battery backed-up RAM on the SSC.

PC
Program Counter or R15.

PCB
Process Control Block is a data structure pointed to by the PR$_PCBB register and contains the current process' hardware context.

PFN
Page Frame Number is an index of a page (512 bytes) of local memory. A PFN is derived from the bit field <23:09> of a physical address.

PR$_ICC
Interval Clock Control and Status, IPR 24.

PR$_IPL
Interrupt Priority Level, IPR 18.

PR$_MAPEN
Memory Management Mapping Enable, IPR 56.

PR$_PCBB
Process Control Block Base register, IPR 16.

PR$_RXCS
R(X)ceive Console Status, IPR 32.

PR$_RXDB
R(X)ceive Data Buffer, IPR 33.

PR$_SAVISP
SAVed Interrupt Stack Pointer, IPR 41.
PR$ _SAVPC
SAVed Program Counter, IPR 42.

PR$ _SAVPSL
SAVed Program Status Longword, IPR 43.

PR$ _SCBB
System Control Block Base register, IPR 17.

PR$ _SISR
Software Interrupt Summary Register, IPR 21.

PR$ _TODR
Time Of Day Register, IPR 27, is commonly referred to as the Time Of Year
register or TOY clock.

PR$ _TXCS
T(X)ransmit Console Status, IPR 34.

PR$ _TXDB
T(X)ransmit Data Buffer, IPR 35.

PROM
Programmable read-only memory. A read-only memory device that can be
programmed.

PSL, PSW
Processor Status Longword is the VAX extension of the PSW (Processor Status
Word). The PSW (lower word) contains instruction condition codes and is
accessible by nonprivileged users; however, the upper word contains system
status information and is accessible by privileged users.

QBMB
Q22–bus Map Base Register found in the CQBIC determines the base address
in local memory for the scatter/gather registers.

QDSS
Q22–bus video controller for workstations.

QMR
Q22–bus Map Register.
QNA
Q22-bus Ethernet controller module.

RAM
Random access memory. A read/write memory device.

RAP
Register address port.

RIP
Restart In Progress flag in CPMBX<3>.

ROM
Read-only memory. A memory device that cannot be altered during the normal use of the computer.

rPB
Restart parameter block.

SCB
System Control Block. A data structure pointed to by PR$_SCBB. It contains a list of longword exception and interrupt vectors.

SCSI
Small computer system interface. An interface designed for connecting disks and other peripheral devices to computer systems. SCSI is defined by an American National Standards Institute (ANSI) standard.

SDD
Symptom-Directed Diagnosis. Online analysis of nonfatal system errors in order to locate potential system fatal errors before they occur.

SGEC
Second Generation Ethernet Chip.

SHAC
Single Host Adapter Chip.
SP
Stack pointer. An address location that contains the address of the processor-defined stack. The processor-defined stack is an area of memory set aside for temporary storage or for procedure and interrupt service linkages.

SRM
Standard Reference Manual, as in VAX SRM.

SSC
System Support Chip.

TOY
Time of year.

VAXcluster configuration
A highly integrated organization of OpenVMS systems that communicate over a high-speed communications path. VAXcluster configurations have all the functions of single-node systems, plus the ability to share CPU resources, queues, and disk storage. Like a single-node system, the VAXcluster configuration provides a single security and management environment. Member nodes can share the same operating environment or serve specialized needs.

VMB
Virtual machine bootstrap. The VMB program loads and runs the operating system.

OpenVMS
Virtual memory system. The operating system for a VAX computer.
Index

A

Acceptance testing, 4-13 to 4-14
Algorithm
to find a valid RPB, 4-32
to restart operating system, 4-31
ANALYZE/ERROR, 5-14
interpreting CPU errors using, 5-15
interpreting DMA to host transaction faults using, 5-28
interpreting memory errors using, 5-18
interpreting system bus faults using, 5-26
ANALYZE/SYSTEM, 5-21
Asynchronous communications interfaces
support for, 2-4
Asynchronous communications options
list of, 2-4

B

Binary load and unload (X command), 3-35
Bits
RPB$V_DiAG, 4-24
RPB$V_SOLICT, 4-24
Block diagram, 1-3
Boot Block Format, 4-23
BOOT command, 3-13
Boot Flags
RPB$V_BBLOCK, 4-23
Bootstrap
conditions, 4-17
definition of, 4-17
disk and tape, 4-23

Bootstrap (cont’d)
failure, 4-18
initialization, 4-18
memory layout, 4-19
memory layout after successful bootstrap, 4-21
network, 4-24
preparing for, 4-18
primary, 4-20
secondary, 4-20

C

Comment command (!), 3-38
! (comment command), 3-38
Communications devices, 2-4
Communications options, 2-4
Configuration
memory, 1-9
Connectors
function of, 1-6
identification of, 1-5
Console command
LOGIN, 3-21
Console commands
address space control qualifiers, 3-9
address specifiers, 3-3
binary load and unload (X), 3-35
BOOT, 3-13
! (comment), 3-38
CONTINUE, 3-15
data control qualifiers, 3-9
DEPOSIT, 3-15
EXAMINE, 3-16
FIND, 3-17
Console commands (cont'd)
  HALT, 3–18
  HELP, 3–18
  INITIALIZE, 3–20
 keywords, 3–10
 list of, 3–11
 MOVE, 3–22
 NEXT, 3–23
 qualifier and argument conventions, 3–3
 qualifiers, 3–9
 REPEAT, 3–24
 SEARCH, 3–25
 SET, 3–27
 SHOW, 3–28
 START, 3–31
 symbolic addresses, 3–4
 syntax, 3–3
 TEST, 3–31
 UNJAM, 3–35
 X (binary load and unload), 3–35

Console error messages
 sample of, 5–41

Console I/O mode
 special characters, 3–2

Console port, testing, 5–58

Console security feature
 values, 3–28

CONTINUE command, 3–15

Controls
 function of, 1–6
 identification of, 1–5

DNA Maintenance Operations Protocol
 (MOP), 4–24

Documents
 related, H–1

E

Entry Point
 definition of, B–1

Error during UETP, 5–57
 diagnosing, 5–56

Error Log Utility
 relationship to UETP, 5–56

Error messages
 console, sample of, 5–41
 EXAMINE command, 3–16
 External mass storage devices, 2–2

F

FE utility, 5–47

Files–11 lookup, 4–23

FIND command, 3–17

Firmware
 power-up sequence, 4–1
 updating, 6–1

Flags
 restart in progress, 4–31

G

General purpose registers (GPRs)
 symbolic addresses for, 3–4

H

H3103 loopback connector, 5–58

H8572 loopback connector, 5–58

Halt
 dispatch, C–1

HALT command, 3–18

Halt protection, override, 5–48

HELP command, 3–18
Indicators
  function of, 1–6
  identification of, 1–5
INIT, 4–18
Initialization
  following a processor halt, 4–31
  prior to bootstrap, 4–18
INITIALIZE command, 3–20
Initial power-up test
  See IPR
Internal mass storage devices
  list of, 2–2
IPL_31, 4–19
iSYS$TEST logical name, 5–56

KA50/51/55/56 CPU module
  block diagram of, 1–3
KA50/55/56 system
  communications options, 2–4
  configurations of, 2–1
  mass storage device configurations, 2–1
  memory configurations, 2–1
KA50 CPU module
  features of, 1–1
KA50 system
  configurations of, 1–1
KA51 CPU module
  features of, 1–1
KA51 system
  configurations of, 1–1
KA55 CPU module
  features of, 1–1
KA55 system
  configurations of, 1–1

Language selection menu
  messages, list of, 4–2
Local Memory Partitioning, 4–19
Log file generated by UETP
  OLDUETP.LOG, 5–57
LOGIN command, 3–21
Loopback connectors
  H3103, 5–58
  H8572, 5–58
  list of, 5–59
Loopback tests, 5–58
  console port, 5–58
  Ethernet, 5–58

Mass storage devices, 2–1
  external, 2–2
  internal, 2–2
  SCSI ID assignments, 2–4
Memory
  acceptance testing of, 4–13
  configurations, 1–10
  expansion connector identification, 1–9
  expansion of, 1–9
  isolating FRU, 4–14, 5–48
  rules for adding, 1–9
  testing, 5–48
Memory configuration
  KA50/51/55/56 system, 2–1
Memory modules, 1–9
Memory option
  installation of, 1–11
Memory test, 1–13
MEM test, 1–13
MicroVAX data types
  support of, 1–4
MicroVAX instructions
  support of, 1–5
MOM$LOAD, 4–25
MOP, functions, 5–53
MOP functions, 4–26
MOP program load sequence, 4–25
MOVE command, 3–22
MS44 memory modules, 1–9

N
Network listening, 4–30
NEXT command, 3–23

NVRAM
CPMBX, E–2
partitioning, E–1

O
OLDUETPLOG file, 5–56
Onboard memory
location of, 1–9
OpenVMS
error handling, 5–4
event record translation, 5–14
Operating System
bootstrap, 4–17
restarting a halted, 4–31
Operating System Restart
definition of, 4–31

P
Parameters
for diagnostic tests, 4–9
in error display, 5–42
Patchable Control Store
Error messages, 6–8
PFN bitmap, 4–18
Ports
function of, 1–6
identification of, 1–5
POST
See Power-on self-tests

Power-on self-tests
description, 4–2
errors handled by, 4–5
kernel, 4–3
Power-on self-tests (cont’d)
mass storage, 4–5
power-up
machine state, 4–14
memory layout, 4–15
Power-up sequence, 4–1
Power-up tests, 4–1
Primary Bootstrap, 4–20

R
Registers
initializing the general purpose, 4–18
Related documents, H–1
REPEAT command, 3–24
REQ_PROGRAM, 4–30
Restart, 4–31
Restart Parameter Block (RPB)
RIP flag, 4–31
ROM-based diagnostics, 4–6 to 4–10
console display during, 5–41
isolating failures with, 5–43
list of, 4–6
parameters, 4–7
utilities, 4–6
RPB
initialization, C–5
locating, 4–32
RPB Signature Format, 4–32
RZ-series ISE
diagnostics, 4–5

S
Scripts, 4–11
list of, 4–12
SCSI ID assignments
recommendations for, 2–4
SEARCH command, 3–25
Secondary Bootstrap, 4–20
SET command, 3–27
SET HOST/DUP command, 3–27
SHOW command, 3–28
SICL messages, 5–34
  converting appended MEL files, 5–37
START command, 3–31
Symbolic addresses, 3–4
  for any address space, 3–7
  for GPRs, 3–4
Synchronous communications options
  list of, 2–5
Synchronous communications standards
  support for, 2–5
System hang, 5–58

Virtual Memory Boot (VMB), 4–21
  definition of, 4–20
  primary bootstrap, 4–20
  secondary bootstrap, 4–23

W
  Warmstart, 4–31

X
  X command (binary load and unload), 3–35

T
  TEST command, 3–31
  Tests, diagnostic
    list of, 4–6
    parameters for, 4–9
  Troubleshooting
    procedures, general, 5–2
    UETP, 5–57

U
  UETINIT01.EXE image, 5–57
  UETP
    interpreting OpenVMS failures with, 5–56
  UETPLOG file, 5–56
  UNJAM, 4–18
  UNJAM command, 3–35
  User Environment Test Package (UETP)
    interpreting output of, 5–56
    running multiple passes of, 5–56
    typical failures reported by, 5–57
  Utilities, diagnostic, 4–6

V
  VAXELN
    and VMB, 4–20
  VAXsimPLUS, 5–3, 5–32
    customizing, 5–39
    enabling SICL, 5–40
    installing, 5–38
MicroVAX 3100 Model 85, 90, 95, 96
KA50/51/55/56 CPU
System Maintenance

Order Number: EK–M3100–SM. B01

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This manual gives maintenance information for systems that use the KA50, KA51, KA55 or KA56 CPU module.
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## Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Pages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preface</td>
<td>xi</td>
</tr>
<tr>
<td>1 KA50/51/55/56 CPU Module Description</td>
<td>1–1</td>
</tr>
<tr>
<td>1.1 KA50/51/55/56 CPU Module</td>
<td>1–1</td>
</tr>
<tr>
<td>1.1.1 Physical Description</td>
<td>1–2</td>
</tr>
<tr>
<td>1.1.2 Functional Description</td>
<td>1–3</td>
</tr>
<tr>
<td>1.2 MS44 and MS44L Memory Modules</td>
<td>1–9</td>
</tr>
<tr>
<td>1.3 MS44 or MS44L Memory Option Installation</td>
<td>1–11</td>
</tr>
<tr>
<td>1.4 Memory Tests</td>
<td>1–13</td>
</tr>
<tr>
<td>2 Configuration</td>
<td>2–1</td>
</tr>
<tr>
<td>2.1 Memory Configurations</td>
<td>2–1</td>
</tr>
<tr>
<td>2.2 Mass Storage Devices</td>
<td>2–2</td>
</tr>
<tr>
<td>2.2.1 Internal Mass Storage Devices</td>
<td>2–2</td>
</tr>
<tr>
<td>2.2.2 External Mass Storage Devices</td>
<td>2–2</td>
</tr>
<tr>
<td>2.2.3 SCSI ID Numbers</td>
<td>2–4</td>
</tr>
<tr>
<td>2.3 Communications Options</td>
<td>2–4</td>
</tr>
<tr>
<td>2.3.1 Asynchronous Communications Options</td>
<td>2–4</td>
</tr>
<tr>
<td>2.3.2 Synchronous Communications Options</td>
<td>2–5</td>
</tr>
<tr>
<td>3 KA50/51/55/56 Firmware Commands</td>
<td>3–2</td>
</tr>
<tr>
<td>3.1 Console I/O Mode Control Characters</td>
<td>3–3</td>
</tr>
<tr>
<td>3.1.1 Command Syntax</td>
<td>3–3</td>
</tr>
<tr>
<td>3.1.2 Address Specifiers</td>
<td>3–4</td>
</tr>
<tr>
<td>3.1.3 Symbolic Addresses</td>
<td>3–4</td>
</tr>
<tr>
<td>3.1.4 Console Numeric Expression Radix Specifiers</td>
<td>3–8</td>
</tr>
<tr>
<td>3.1.5 Console Command Qualifiers</td>
<td>3–9</td>
</tr>
<tr>
<td>3.1.6 Console Command Keywords</td>
<td>3–10</td>
</tr>
<tr>
<td>3.2 Console Commands</td>
<td>3–13</td>
</tr>
<tr>
<td>3.2.1 BOOT</td>
<td>3–13</td>
</tr>
</tbody>
</table>
### 3.2 System Initialization and Acceptance Testing (Normal Operation)

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.2.2</td>
<td>CONTINUE</td>
<td>3-15</td>
</tr>
<tr>
<td>3.2.3</td>
<td>DEPOSIT</td>
<td>3-15</td>
</tr>
<tr>
<td>3.2.4</td>
<td>EXAMINE</td>
<td>3-16</td>
</tr>
<tr>
<td>3.2.5</td>
<td>FIND</td>
<td>3-17</td>
</tr>
<tr>
<td>3.2.6</td>
<td>HALT</td>
<td>3-18</td>
</tr>
<tr>
<td>3.2.7</td>
<td>HELP</td>
<td>3-18</td>
</tr>
<tr>
<td>3.2.8</td>
<td>INITIALIZE</td>
<td>3-20</td>
</tr>
<tr>
<td>3.2.9</td>
<td>LOGIN</td>
<td>3-21</td>
</tr>
<tr>
<td>3.2.10</td>
<td>MOVE</td>
<td>3-22</td>
</tr>
<tr>
<td>3.2.11</td>
<td>NEXT</td>
<td>3-23</td>
</tr>
<tr>
<td>3.2.12</td>
<td>REPEAT</td>
<td>3-24</td>
</tr>
<tr>
<td>3.2.13</td>
<td>SEARCH</td>
<td>3-25</td>
</tr>
<tr>
<td>3.2.14</td>
<td>SET</td>
<td>3-27</td>
</tr>
<tr>
<td>3.2.15</td>
<td>SHOW</td>
<td>3-28</td>
</tr>
<tr>
<td>3.2.16</td>
<td>START</td>
<td>3-31</td>
</tr>
<tr>
<td>3.2.17</td>
<td>TEST</td>
<td>3-31</td>
</tr>
<tr>
<td>3.2.18</td>
<td>UNJAM</td>
<td>3-35</td>
</tr>
<tr>
<td>3.2.19</td>
<td>X—Binary Load and Unload</td>
<td>3-35</td>
</tr>
<tr>
<td>3.2.20</td>
<td>! (Comment)</td>
<td>3-38</td>
</tr>
</tbody>
</table>

### 4 System Initialization and Acceptance Testing (Normal Operation)

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1</td>
<td>Basic Initialization Flow</td>
<td>4-1</td>
</tr>
<tr>
<td>4.2</td>
<td>Power-On Self-Tests (POST)</td>
<td>4-2</td>
</tr>
<tr>
<td>4.2.1</td>
<td>Power-Up Tests for Kernel</td>
<td>4-3</td>
</tr>
<tr>
<td>4.2.2</td>
<td>Power-Up Tests for Mass Storage Devices</td>
<td>4-5</td>
</tr>
<tr>
<td>4.3</td>
<td>CPU ROM-Based Diagnostics</td>
<td>4-6</td>
</tr>
<tr>
<td>4.3.1</td>
<td>Diagnostic Tests</td>
<td>4-6</td>
</tr>
<tr>
<td>4.3.2</td>
<td>Scripts</td>
<td>4-11</td>
</tr>
<tr>
<td>4.4</td>
<td>Basic Acceptance Test Procedure</td>
<td>4-13</td>
</tr>
<tr>
<td>4.5</td>
<td>Machine State on Power-Up</td>
<td>4-14</td>
</tr>
<tr>
<td>4.6</td>
<td>Main Memory Layout and State</td>
<td>4-14</td>
</tr>
<tr>
<td>4.6.1</td>
<td>Reserved Main Memory</td>
<td>4-15</td>
</tr>
<tr>
<td>4.6.1.1</td>
<td>PFN Bitmap</td>
<td>4-15</td>
</tr>
<tr>
<td>4.6.1.2</td>
<td>Scatter/Gather Map</td>
<td>4-16</td>
</tr>
<tr>
<td>4.6.1.3</td>
<td>Firmware “Scratch Memory”</td>
<td>4-16</td>
</tr>
<tr>
<td>4.6.2</td>
<td>Contents of Main Memory</td>
<td>4-16</td>
</tr>
<tr>
<td>4.6.3</td>
<td>Memory Controller Registers</td>
<td>4-17</td>
</tr>
<tr>
<td>4.6.4</td>
<td>On-Chip and Backup Caches</td>
<td>4-17</td>
</tr>
<tr>
<td>4.6.5</td>
<td>Translation Buffer</td>
<td>4-17</td>
</tr>
<tr>
<td>4.6.6</td>
<td>Halt-Protected Space</td>
<td>4-17</td>
</tr>
<tr>
<td>4.7</td>
<td>Operating System Bootstrap</td>
<td>4-17</td>
</tr>
<tr>
<td>Section</td>
<td>Title</td>
<td>Page</td>
</tr>
<tr>
<td>---------</td>
<td>-------</td>
<td>------</td>
</tr>
<tr>
<td>4.7.1</td>
<td>Preparing for the Bootstrap</td>
<td>4-18</td>
</tr>
<tr>
<td>4.7.2</td>
<td>Primary Bootstrap Procedures (VMB)</td>
<td>4-20</td>
</tr>
<tr>
<td>4.7.3</td>
<td>Device Dependent Secondary Bootstrap Procedures</td>
<td>4-23</td>
</tr>
<tr>
<td>4.7.3.1</td>
<td>Disk and Tape Bootstrap Procedure</td>
<td>4-23</td>
</tr>
<tr>
<td>4.7.3.2</td>
<td>MOP Ethernet Functions and Network Bootstrap Procedure</td>
<td>4-24</td>
</tr>
<tr>
<td>4.7.3.3</td>
<td>Network &quot;Listening&quot;</td>
<td>4-30</td>
</tr>
<tr>
<td>4.8</td>
<td>Operating System Restart</td>
<td>4-31</td>
</tr>
<tr>
<td>4.8.1</td>
<td>Locating the RPB</td>
<td>4-32</td>
</tr>
</tbody>
</table>

### 5 System Troubleshooting and Diagnostics

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1</td>
<td>Basic Troubleshooting Flow</td>
<td>5-1</td>
</tr>
<tr>
<td>5.2</td>
<td>Product Fault Management and Symptom-Directed Diagnosis</td>
<td>5-3</td>
</tr>
<tr>
<td>5.2.1</td>
<td>General Exception and Interrupt Handling</td>
<td>5-3</td>
</tr>
<tr>
<td>5.2.2</td>
<td>OpenVMS Error Handling</td>
<td>5-4</td>
</tr>
<tr>
<td>5.2.3</td>
<td>OpenVMS Error Logging and Event Log Entry Format</td>
<td>5-6</td>
</tr>
<tr>
<td>5.2.4</td>
<td>OpenVMS Event Record Translation</td>
<td>5-14</td>
</tr>
<tr>
<td>5.2.5</td>
<td>Interpreting CPU Faults Using ANALYZE/ERROR</td>
<td>5-15</td>
</tr>
<tr>
<td>5.2.6</td>
<td>Interpreting Memory Faults Using ANALYZE/ERROR</td>
<td>5-18</td>
</tr>
<tr>
<td>5.2.6.1</td>
<td>Uncorrectable ECC Errors</td>
<td>5-18</td>
</tr>
<tr>
<td>5.2.6.2</td>
<td>Correctable ECC Errors</td>
<td>5-22</td>
</tr>
<tr>
<td>5.2.7</td>
<td>Interpreting System Bus Faults Using ANALYZE/ERROR</td>
<td>5-26</td>
</tr>
<tr>
<td>5.2.8</td>
<td>Interpreting DMA ⇔ Host Transaction Faults Using ANALYZE/ERROR</td>
<td>5-28</td>
</tr>
<tr>
<td>5.2.9</td>
<td>VAXsimPLUS and System-Initiated Call Logging (SICL) Support</td>
<td>5-32</td>
</tr>
<tr>
<td>5.2.9.1</td>
<td>Converting the SICL Service Request MEL File</td>
<td>5-37</td>
</tr>
<tr>
<td>5.2.9.2</td>
<td>VAXsimPLUS Installation Tips</td>
<td>5-38</td>
</tr>
<tr>
<td>5.2.9.3</td>
<td>VAXsimPLUS Post-installation Tips</td>
<td>5-39</td>
</tr>
<tr>
<td>5.2.10</td>
<td>Repair Data for Returning FRUs</td>
<td>5-41</td>
</tr>
<tr>
<td>5.3</td>
<td>Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures</td>
<td>5-41</td>
</tr>
<tr>
<td>5.3.1</td>
<td>FE Utility</td>
<td>5-47</td>
</tr>
<tr>
<td>5.3.2</td>
<td>Overriding Halt Protection</td>
<td>5-48</td>
</tr>
<tr>
<td>5.3.3</td>
<td>Isolating Memory Failures</td>
<td>5-48</td>
</tr>
<tr>
<td>5.4</td>
<td>Using MOP Ethernet Functions to Isolate Failures</td>
<td>5-53</td>
</tr>
<tr>
<td>5.5</td>
<td>Interpreting User Environmental Test Package (UETP) OpenVMS Failures</td>
<td>5-56</td>
</tr>
<tr>
<td>5.5.1</td>
<td>Interpreting UETP Output</td>
<td>5-56</td>
</tr>
<tr>
<td>5.5.1.1</td>
<td>UETP Log Files</td>
<td>5-56</td>
</tr>
<tr>
<td>5.5.1.2</td>
<td>Possible UETP Errors</td>
<td>5-57</td>
</tr>
<tr>
<td>5.6</td>
<td>Using Loopback Tests to Isolate Failures</td>
<td>5-58</td>
</tr>
</tbody>
</table>
6 FEPROM Firmware Update

6.1 Preparing the Processor for a FEPROM Update .......................... 6-2
6.2 Updating Firmware via Ethernet ........................................... 6-3
6.3 Updating Firmware via Tape ............................................... 6-6
6.4 FEPROM Update Error Messages .......................................... 6-7

A Address Assignments

A.1 KA50/51/55/56 General Local Address Space Map ...................... A-1
A.2 KA50/51/55/56 Detailed Local Address Space Map ...................... A-3
A.3 External, Internal Processor Registers ................................. A-8
A.4 Global Q22–bus Address Space Map ..................................... A-9
A.5 Processor Registers .......................................................... A-9
A.6 IPR Address Space Decoding ................................................ A-21

B ROM Partitioning

B.1 Firmware EPROM Layout .................................................... B-1
B.1.1 System Identification Registers ....................................... B-3
B.1.1.1 PR$_SID$ (IPR 62) .................................................... B-3
B.1.1.2 SIE (00040004) ....................................................... B-3
B.1.2 Call-Back Entry Points .................................................. B-4
B.1.2.1 CP$GETCHAR_R4 .................................................... B-5
B.1.2.2 CP$MSG_OUT_NOLF_R4 .......................................... B-6
B.1.2.3 CP$READ_WTH_PRMPT_R4 ...................................... B-6
B.1.3 Boot Information Pointers ................................................. B-7

C Data Structures and Memory Layout

C.1 Halt Dispatch State Machine .............................................. C-1
C.2 Restart Parameter Block .................................................... C-5
C.3 VMB Argument List .......................................................... C-9
D Configurable Machine State

E NVRAM Partitioning

E.1 SSC RAM Layout .................................................. E-1
E.1.1 Public Data Structures ........................................... E-2
E.1.1.1 Console Program MailBox (CPMBX) ......................... E-2
E.1.1.2 Terminal Status ............................................... E-3
E.1.1.3 Keyboard Status .............................................. E-3
E.1.2 Service Vectors .................................................. E-4
E.1.3 Firmware Stack .................................................. E-4
E.1.4 Diagnostic State ................................................ E-4
E.1.5 USER Area ...................................................... E-4

F MOP Counters

G Error Messages

G.1 Machine Check Register Dump .................................... G-1
G.2 Halt Code Messages .............................................. G-1
G.3 VMB Error Messages .............................................. G-3
G.4 Console Error Messages .......................................... G-4

H Related Documents

Glossary

Index

Examples

1–1 Successful Running of Memory Test Script A8 .................. 1–13
1–2 Typical Failure After Running Memory Test Script A8 .......... 1–14
4–1 Successful Diagnostic Countdown ............................... 4–2
4–2 Successful Power-Up to List of Bootable Devices ............... 4–5
4–3 Test 9E ............................................................ 4–8
5–1 Error Log Entry Indicating CPU Error .......................... 5–16
5–2 SHOW ERROR Display Using the OpenVMS Operating System .................................................. 5–17
<table>
<thead>
<tr>
<th>Page</th>
<th>Title</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>5–3</td>
<td>Error Log Entry Indicating Uncorrectable ECC Error</td>
<td>5–20</td>
</tr>
<tr>
<td>5–4</td>
<td>SHOW MEMORY Display Under the OpenVMS Operating System</td>
<td>5–21</td>
</tr>
<tr>
<td>5–5</td>
<td>Using ANALYZE/SYSTEM to Check the Physical Address in Memory for a Replaced Page</td>
<td>5–22</td>
</tr>
<tr>
<td>5–6</td>
<td>Error Log Entry Indicating Correctable ECC Error</td>
<td>5–25</td>
</tr>
<tr>
<td>5–7</td>
<td>Error Log Entry Indicating Q-Bus Error</td>
<td>5–27</td>
</tr>
<tr>
<td>5–8</td>
<td>Error Log Entry Indicating Polled Error</td>
<td>5–29</td>
</tr>
<tr>
<td>5–9</td>
<td>Device Attention Entry</td>
<td>5–31</td>
</tr>
<tr>
<td>5–10</td>
<td>SICL Service Request with Appended MEL File</td>
<td>5–38</td>
</tr>
<tr>
<td>5–11</td>
<td>Sample Output with Errors</td>
<td>5–41</td>
</tr>
<tr>
<td>5–12</td>
<td>FE Utility Example</td>
<td>5–48</td>
</tr>
<tr>
<td>5–13</td>
<td>Failure Due to a Missing SIMM (One 16 Mbyte Set)</td>
<td>5–49</td>
</tr>
<tr>
<td>5–14</td>
<td>Failure Due to a Missing SIMM (Two 16 Mbyte Sets)</td>
<td>5–50</td>
</tr>
<tr>
<td>5–15</td>
<td>Failure Due to a Bad SIMM</td>
<td>5–51</td>
</tr>
<tr>
<td>5–16</td>
<td>SIMM Wrong Size</td>
<td>5–52</td>
</tr>
<tr>
<td>6–1</td>
<td>FEPROM Update via Ethernet</td>
<td>6–5</td>
</tr>
<tr>
<td>6–2</td>
<td>FEPROM Update via Tape</td>
<td>6–7</td>
</tr>
</tbody>
</table>

**Figures**

<table>
<thead>
<tr>
<th>Page</th>
<th>Title</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>1–1</td>
<td>KA50/51/55/56 CPU Module</td>
<td>1–2</td>
</tr>
<tr>
<td>1–2</td>
<td>KA50/51/55/56 CPU Module Block Diagram</td>
<td>1–4</td>
</tr>
<tr>
<td>1–3</td>
<td>KA50/51/55/56 Controls, Indicators, Ports, and Connectors</td>
<td>1–6</td>
</tr>
<tr>
<td>1–4</td>
<td>Memory Expansion Connectors</td>
<td>1–10</td>
</tr>
<tr>
<td>1–5</td>
<td>Memory Module Installation</td>
<td>1–12</td>
</tr>
<tr>
<td>2–1</td>
<td>SZ Expansion Box Numbering System</td>
<td>2–3</td>
</tr>
<tr>
<td>4–1</td>
<td>Console Banner</td>
<td>4–3</td>
</tr>
<tr>
<td>4–2</td>
<td>Memory Layout After Power-Up Diagnostics</td>
<td>4–15</td>
</tr>
<tr>
<td>4–3</td>
<td>Memory Layout Prior to VMB Entry</td>
<td>4–20</td>
</tr>
<tr>
<td>4–4</td>
<td>Memory Layout at VMB Exit</td>
<td>4–22</td>
</tr>
<tr>
<td>4–5</td>
<td>Boot Block Format</td>
<td>4–24</td>
</tr>
<tr>
<td>4–6</td>
<td>Locating the Restart Parameter Block</td>
<td>4–32</td>
</tr>
<tr>
<td>5–1</td>
<td>Event Log Entry Format</td>
<td>5–8</td>
</tr>
<tr>
<td>5–2</td>
<td>Machine Check Stack Frame Subpacket</td>
<td>5–9</td>
</tr>
<tr>
<td>5–3</td>
<td>Processor Register Subpacket</td>
<td>5–10</td>
</tr>
</tbody>
</table>
5–4 Memory Subpacket for ECC Memory Errors .......................... 5–11
5–5 Memory SBE Reduction Subpacket (Correctable Memory Errors) ........................................... 5–11
5–6 CRD Entry Subpacket Header ........................................ 5–12
5–7 Correctable Read Data (CRD) Entry ......................... 5–13
5–8 Trigger Flow for the VAXsimPLUS Monitor ................. 5–34
5–9 Five-Level VAXsimPLUS Monitor Display .................. 5–36
6–1 Firmware Update Utility Layout ............................... 6–2
6–2 W4 Jumper Setting for Updating Firmware .......................... 6–3
B–1 KA50/51/55/56 FEPROM Layout ............................... B–2
B–2 SID : System Identification Register ............................. B–3
B–3 SIE : System Identification Extension (20040004) .... B–4
B–4 Boot Information Pointers ........................................ B–8
E–1 KA50/51/55/56 SSC NVRAM Layout ......................... E–2
E–2 NVR0 (20140400) : Console Program MailBoX (CPMBX) ..... E–2
E–3 NVR1 (20140401) ............................................. E–3
E–4 NVR2 (20140402) ............................................. E–3

Tables

1–1 Functions of Controls, Indicators, Connectors ................ 1–6
1–2 KA50/51/55/56 CPU Module Memory Configurations .... 1–10
2–1 KA50/51/55/56 Internal Mass Storage Devices .......... 2–2
2–2 Supported Asynchronous Communications Options ........ 2–4
2–3 Supported Synchronous Communications Options ........ 2–5
2–4 DSW42-AA Communications Support ..................... 2–5
3–1 Console Symbolic Addresses .................................. 3–4
3–2 Symbolic Addresses Used in Any Address Space .......... 3–8
3–3 Console Radix Specifiers ................................... 3–8
3–4 Console Command Qualifiers ................................ 3–9
3–5 Command Keywords by Type .................................. 3–11
3–6 Console Command Summary ................................ 3–11
4–1 LED Codes ..................................................... 4–4
4–2 Scripts Available to Customer Services ................. 4–12
4–3 Network Maintenance Operations Summary ............... 4–26
4–4 Supported MOP Messages .................................. 4–27
4–5 MOP Multicast Addresses and Protocol Specifiers ....... 4–31
5-1 OpenVMS Error Handler Entry Types ..................... 5-7
5-2 Conditions That Trigger VAXsimPLUS Notification and Updating .................................................. 5-33
5-3 Five-Level VAXsimPLUS Monitor Screen Displays ........ 5-35
5-4 KA50/51/55/56 Console Displays as Pointers to FRUs .... 5-44
5-5 Loopback Connectors for Common Devices .................. 5-60
A-1 Processor Registers ..................................... A-9
A-2 IPR Address Space Decoding ................................ A-21
B-1 System Identification Register ........................... B-3
B-2 System Identification Extension ........................... B-4
B-3 Call-Back Entry Points .................................... B-5
C-1 Firmware State Transition Table ........................... C-3
C-2 Restart Parameter Block Fields ............................ C-6
C-3 VMB Argument List ....................................... C-9
E-1 Bit Functions for NVR0 ..................................... E-2
E-2 Bit Functions for NVR1 ..................................... E-3
E-3 Bit Functions for NVR2 ..................................... E-4
F-1 MOP Counter Block ........................................ F-1
G-1 HALT Messages ............................................. G-2
G-2 VMB Error Messages ....................................... G-3
G-3 Console Error Messages .................................... G-4
Preface

This manual describes the KA50 CPU module used in the MicroVAX 3100 Model 90, the KA51 CPU module used in the MicroVAX 3100 Model 95, the KA55 CPU module used in the MicroVAX 3100 Model 85, and the KA56 CPU module used in the MicroVAX 3100 Model 96 system. It provides the configuration guidelines, ROM-based diagnostic information, and troubleshooting information for systems containing the KA50/51/55/56 CPU modules.

Audience

This manual is for Digital Services personnel who provide support and maintenance for systems that use the KA50/51/55/56 CPU module. It is also for customers who have a self-maintenance agreement with Digital Equipment Corporation.

Structure of This Manual

This manual is divided into six chapters, eight appendixes, a glossary, and an index:

- Chapter 1 describes the KA50/51/55/56 CPU module.
- Chapter 2 describes the KA50/51/55/56 system configurations.
- Chapter 3 describes the console commands that you can enter at the console prompt.
- Chapter 4 describes the system initialization, testing and bootstrap process that occurs at power-up.
- Chapter 5 describes the error log interpretation of diagnostic testing, the ROM-based diagnostic testing, and troubleshooting procedures for the KA50/51/55/56 systems. Also, this chapter provides information on testing DSSI storage devices, using MOP Ethernet functions to isolate errors, and interpreting UEITP failures.
- Chapter 6 describes the FEPROM firmware.
• Appendix A gives the address assignments.

• Appendix B describes ROM partitioning and subroutine entry points.

• Appendix C gives definitions of the key global data structures used by the CPU firmware.

• Appendix D gives the normal state of all configurable bits in the CPU module as they are left after the successful completion of power-up ROM diagnostics.

• Appendix E describes how the CPU firmware partitions the SCC 1 KB battery-backed-up (BBU) RAM.

• Appendix F gives MOP counters.

• Appendix G describes the error codes and messages that the system exerciser test generates.

• Appendix H gives a list of related documents.

--------------------------------- Note ---------------------------------
Examples in this manual may vary slightly from your particular MicroVAX 3100 system, since they are from various VAX and MicroVAX systems which share common features, options, diagnostics, and so on.

---------------------------------
Conventions

The following conventions are used in this manual:

<table>
<thead>
<tr>
<th>Convention</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ctrl/x</td>
<td>Ctrl/x indicates that you hold down the Ctrl key while you press another key or mouse button (indicated here by x).</td>
</tr>
<tr>
<td>x</td>
<td>A lowercase italic x indicates the generic use of a letter. For example, xxx indicates any combination of three alphabetic characters.</td>
</tr>
<tr>
<td>n</td>
<td>A lowercase italic n indicates the generic use of a number. For example, 19nn indicates a 4-digit number in which the last 2 digits are unknown.</td>
</tr>
<tr>
<td>[]</td>
<td>In format descriptions, braces indicate required elements. You must choose one of the elements.</td>
</tr>
<tr>
<td>[]</td>
<td>In format descriptions, brackets indicate optional elements. You can choose none, one, or all of the options.</td>
</tr>
<tr>
<td>( )</td>
<td>In format descriptions, parentheses delimit the parameter or argument list.</td>
</tr>
<tr>
<td>...</td>
<td>In format descriptions, horizontal ellipsis points indicate one of the following:</td>
</tr>
<tr>
<td></td>
<td>• An item that is repeated</td>
</tr>
<tr>
<td></td>
<td>• An omission such as additional optional arguments</td>
</tr>
<tr>
<td></td>
<td>• Additional parameters, values, or other information that you can enter</td>
</tr>
<tr>
<td></td>
<td>In format descriptions, a vertical bar separates similar options, one of which you can choose.</td>
</tr>
<tr>
<td>italic type</td>
<td>Italic type emphasizes important information, indicates variables, and indicates the complete titles of manuals.</td>
</tr>
<tr>
<td>boldface type</td>
<td>Boldface type in examples indicates user input. Boldface type in text indicates the first instance of terms defined either in the text, in the glossary, or both.</td>
</tr>
<tr>
<td>n nnn.nnn nn</td>
<td>A space character separates groups of 3 digits in numerals with 5 or more digits. For example, 10 000 equals ten thousand.</td>
</tr>
<tr>
<td>n.nn</td>
<td>A period in numerals signals the decimal point indicator. For example, 1.75 equals one and three-fourths.</td>
</tr>
<tr>
<td>MONOSPACE</td>
<td>Text displayed on the screen is shown in monospace type.</td>
</tr>
<tr>
<td>Convention</td>
<td>Description</td>
</tr>
<tr>
<td>---------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Radix indicators</td>
<td>The radix of a number is written as a word enclosed in parentheses,</td>
</tr>
<tr>
<td></td>
<td>for example, 23(decimal) or 34(hexadecimal).</td>
</tr>
<tr>
<td>&gt;&gt;&gt;</td>
<td>Three right angle brackets indicate the console prompt.</td>
</tr>
<tr>
<td>UPPERCASE</td>
<td>A word in uppercase indicates a command.</td>
</tr>
<tr>
<td>Note</td>
<td>A note contains information that is of special importance to the user.</td>
</tr>
<tr>
<td>Caution</td>
<td>A caution contains information to prevent damage to the equipment.</td>
</tr>
<tr>
<td>Warning</td>
<td>A warning contains information to prevent personal injury.</td>
</tr>
</tbody>
</table>
1

KA50/51/55/56 CPU Module Description

This chapter describes the KA50 central processing unit (CPU) module that is used in the MicroVAX 3100 Model 90, the KA51 CPU module that is used in the MicroVAX 3100 Model 95, the KA55 CPU module that is used in the MicroVAX 3100 Model 85 system, and the KA56 CPU module that is used in the MicroVAX 3100 Model 96. It gives information on the following:

- KA50/51/55/56 CPU modules
- MS44 or MS44L memory modules

The KA50, KA51, KA55 and KA56 are similar in design, and the information in this document is applicable for each of them except where noted. The differences between the KA50, KA51, KA55, and KA56 CPUs are as follows:

<table>
<thead>
<tr>
<th></th>
<th>KA50</th>
<th>KA51</th>
<th>KA55</th>
<th>KA56</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed</td>
<td>286Mhz (14ns)</td>
<td>333Mhz (12ns)</td>
<td>250Mhz (16ns)</td>
<td>400Mhz (10ns)</td>
</tr>
<tr>
<td>VIC</td>
<td>2Kb</td>
<td>2Kb</td>
<td>disabled</td>
<td>2Kb</td>
</tr>
<tr>
<td>P-cache</td>
<td>8Kb</td>
<td>8Kb</td>
<td>8Kb</td>
<td>8Kb</td>
</tr>
<tr>
<td>B-cache</td>
<td>128Kb</td>
<td>512Kb</td>
<td>128Kb</td>
<td>512Kb</td>
</tr>
</tbody>
</table>

1.1 KA50/51/55/56 CPU Module

The KA50/51/55/56 CPU module is based on the NVAX chip set. It uses MS44 or MS44L memory modules and a set of supported small computer system interface (SCSI) devices. Figure 1-1 shows the KA50 CPU module; the KA51, KA55 and KA56 modules are similar.
KA50/51/55/56 CPU Module Description

1.1 KA50/51/55/56 CPU Module

1.1.1 Physical Description

The KA50/51/55/56 CPU module is the primary component of the MicroVAX 3100 system in which it is installed. The KA50/51/55/56 CPU module contains the following components:

- The NVAX processor chip—This chip is a complementary metal oxide semiconductor (CMOS) virtual memory microprocessor. The key features of the chip are as follows:
  - Support for the MicroVAX chip subset of the VAX instruction set
  - Support for the MicroVAX chip subset of the VAX data types
  - Full VAX memory management
  - 30-bit physical memory addressing

Figure 1–1 KA50/51/55/56 CPU Module

- DC244 NVAX memory controller (NMC) memory controller chip
- DC243 NVAX CP bus adapter (NMA) and input/output (I/O) control chip
- SCSI controller and SQWF buffer chip
- Time-of-year (TOY) clock SSC chip
KA50/51/55/56 CPU Module Description
1.1 KA50/51/55/56 CPU Module

- DC541 SGEC chip Ethernet controller for standard or ThinWire Ethernet
- DC7085 (QUART) serial line controller (4 serial lines, one with modem control)
- 128K bytes (KA50/55) or 512K bytes (KA51/56) of second level write-back cache memory
- Basic system memory (16M bytes of random-access memory (RAM) consisting of four MS44L-AA memory modules or 64M bytes of RAM consisting of four MS44-CA)
- Support for up to 128M bytes of RAM
- 512K bytes of read-only memory (ROM)—This ROM contains the boot and diagnostic firmware for the system.
- 32-byte network address ROM
- Four asynchronous communications ports as follows:
  - Three DEC423 ports—These ports are modified modular jack (MMJ) connectors.
  - One modem control port—This port is a D-sub 25-way connector.
- Provision for asynchronous communications options that provide one of the following:
  - Eight or 16 additional DEC423 ports
  - Eight additional modem ports
- Provision for synchronous communications options that provide:
  - Two synchronous ports

1.1.2 Functional Description

Figure 1–2 is block diagram of the CPU module. This example shows a KA51 and KA56. The diagrams for the KA50 and KA55 are the same except that there are only 128Kb of B-cache on those modules instead of the 512Kb shown.
The KA50/51/55/56 CPU module supports the following MicroVAX data types:

- Byte, word, longword, and quadword
- Character string
- Variable-length bit field
- Absolute queues
- Self-relative queues
- f-floating-point, d-floating-point, and g-floating-point
The operating system uses software emulation to support other MicroVAX data types. The KA50/51/55/56 CPU module supports the following MicroVAX instructions:

- Integer, arithmetic and logical
- Address
- Variable-length bit field
- Control
- Procedure call
- Miscellaneous
- Queue
- Character string instructions
- MOVC3/MOVCS
- CMPC3/CMPC5
- LOCC
- SCANC
- SKPC
- SPANC
- Operating system support
- f_floating-point, d_floating-point, and g_floating-point

The NVAX processor chip provides special microcode assistance to aid the macrocode emulation of the following instruction groups:

- Character string (other than those mentioned previously)
- Decimal string
- CRC
- EDITPC

The operating system uses software emulation to support other VAX instructions. Figure 1–3 shows the controls, indicators, ports, and connectors on the KA50/51/55/56 CPU module. Table 1–1 describes the functions of the controls, indicators, ports, and connectors.
Table 1–1 Functions of Controls, Indicators, Connectors

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal SCSI connector</td>
<td>A connector that provides a connection for SCSI devices mounted inside the system enclosure.</td>
</tr>
</tbody>
</table>

(continued on next page)
<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic system memory connectors</td>
<td>Four connectors for the basic system memory modules.</td>
</tr>
<tr>
<td>Memory expansion connectors</td>
<td>Four connectors for an additional memory option.</td>
</tr>
<tr>
<td>External SCSI connector</td>
<td>A connector that provides a connection to SCSI devices that are external to the system enclosure. (Only functional when the internal SCSI connector has a cable installed.)</td>
</tr>
<tr>
<td>Power connector</td>
<td>A connector for dc power.</td>
</tr>
<tr>
<td>ThinWire Ethernet port</td>
<td>A port that provides a connection to a ThinWire Ethernet network.</td>
</tr>
<tr>
<td>Ethernet switch</td>
<td>A two-position switch that determines the type of Ethernet that the system uses as follows:</td>
</tr>
<tr>
<td></td>
<td>• Left position—selects the standard Ethernet type</td>
</tr>
<tr>
<td></td>
<td>• Right position—selects the ThinWire Ethernet type</td>
</tr>
<tr>
<td>Standard Ethernet port</td>
<td>A port that provides a connection to a standard Ethernet network.</td>
</tr>
<tr>
<td>LED display</td>
<td>A set of six LEDs that provide power-up and self-test diagnostic code information.</td>
</tr>
<tr>
<td>Break/Enable LED</td>
<td>A LED indicator that shows the function of MMJ port 3 as follows:</td>
</tr>
<tr>
<td></td>
<td>• On—Break enable</td>
</tr>
<tr>
<td></td>
<td>• Off—Break disable on port 3</td>
</tr>
<tr>
<td>Break/Enable switch¹</td>
<td>A two-position switch that determines the function of MMJ port 3 as follows:</td>
</tr>
<tr>
<td></td>
<td>• Up position—MMJ port 3 functions as a console port; in this state, you can press the Break key on the keyboard of a terminal connected to MMJ port 3 to put the system in console mode.</td>
</tr>
<tr>
<td></td>
<td>• Down position—MMJ port 3 functions as a console port only, and the Break key is disabled.</td>
</tr>
</tbody>
</table>

¹The system recognizes the position of this switch only when the system is turned on.

(continued on next page)
### Table 1–1 (Cont.) Functions of Controls, Indicators, Connectors

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Halt button</td>
<td>A momentary-contact push button that puts the system in console mode.</td>
</tr>
<tr>
<td>Asynchronous modem control port 2</td>
<td>EIA-232 compatible asynchronous port with modem control.</td>
</tr>
<tr>
<td>MMJ port 3</td>
<td>DEC423 compatible asynchronous port. This port functions as the primary console port.</td>
</tr>
<tr>
<td>MMJ port 1</td>
<td>DEC423 compatible asynchronous port.</td>
</tr>
<tr>
<td>MMJ port 0</td>
<td>DEC423 compatible asynchronous port.</td>
</tr>
<tr>
<td>DSW42 I/O connector</td>
<td>A connector that provides a connection for the DSW42 input/output cable.</td>
</tr>
<tr>
<td>DHW42 I/O connector</td>
<td>A connector that provides a connection for the DHW42 input/output cable.</td>
</tr>
<tr>
<td>DSW42 logic board connectors</td>
<td>Two connectors that provide connections for a DSW42 logic board.</td>
</tr>
<tr>
<td>DHW42 logic board connectors</td>
<td>Two connectors that provide connections for a DHW42 logic board.</td>
</tr>
<tr>
<td>KZDDA SCSI connector option</td>
<td>Connector which provides a physical interface between the CPU module and external SCSI devices on an optional second SCSI bus (SCSI-B).</td>
</tr>
</tbody>
</table>
1.2 MS44 and MS44L Memory Modules

The MS44 and the MS44L memory modules provide memory expansion for the KA50/51/55/56 CPU module. The KA50/51/55/56 CPU module supports one variant of the MS44 memory option and one variant of the MS44L option as follows:

- The MS44L-BC (16M bytes), which contains four MS44L-AA (4M bytes) memory modules
- The MS44-DC (64M bytes), which contains four MS44-CA (16M bytes) memory modules

Note

Use only MS44 or MS44L memory modules qualified by Digital.

The rules for adding MS44 or MS44L memory options are as follows:

- You must install all four of the memory modules contained in a memory option. This means that you can expand memory in 16M byte or 64M byte increments only.
- You can install memory options only in a set of connectors that have the same numeral in the connector label. The sets are identified by the following labels:
  - 0A, 0B, 0C, 0D
  - 1E, 1F, 1G, 1H

Figure 1–4 shows the location of the basic memory (16M bytes or 64M bytes) and the memory expansion connectors. Table 1–2 lists the memory configurations.
Table 1–2 KA50/51/55/56 CPU Module Memory Configurations

<table>
<thead>
<tr>
<th>Total Memory (bytes)</th>
<th>Increment 1&lt;br&gt;(0A + 0B + 0C + 0D)&lt;sup&gt;2&lt;/sup&gt;</th>
<th>Increment 2&lt;br&gt;(1E + 1F + 1G + 1H)&lt;sup&gt;2&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>16M</td>
<td>MS44L-BC</td>
<td>MS44L-BC</td>
</tr>
<tr>
<td>32M</td>
<td>MS44L-BC</td>
<td>MS44L-BC</td>
</tr>
<tr>
<td>64M</td>
<td>MS44-DC</td>
<td>MS44L-BC</td>
</tr>
<tr>
<td>80M</td>
<td>MS44-DC</td>
<td>MS44L-BC</td>
</tr>
<tr>
<td>128M</td>
<td>MS44-DC</td>
<td>MS44-DC</td>
</tr>
</tbody>
</table>

<sup>1</sup> Basic system memory.

<sup>2</sup> 0A, 0B, 0C, 0D, 1E, 1F, 1G, and 1H are connector identifiers (see Figure 1–4).
1.3 MS44 or MS44L Memory Option Installation

The MS44 and MS44L memory options consist of four memory modules each. Install an MS44 or MS44L memory option on the KA50/51/55/56 CPU module as follows:

1. Position the KA50/51/55/56 CPU module, component side up, so that the edge connectors are facing away from you.

2. Identify the connectors on the KA50/51/55/56 CPU module into which you must install the memory option (see Figure 1–4 and Table 1–2).

3. Insert the first memory module, with the side containing the bar code facing away from you, into the connector on the KA50/51/55/56 CPU module (see Figure 1–5).

_________________________ Caution ________________________________

The connectors are keyed to ensure that you install the memory modules with the correct orientation. Do not force the modules into the connectors with an incorrect orientation.

_________________________ Caution ________________________________

Make sure that you fully install the memory module into the connector before you tilt the module toward the front of the enclosure.
4. Tilt the memory module toward the front of the enclosure until the metal locking clips on the connector lock the memory module in position.

5. Repeat the procedure in step 1 for the subsequent memory modules. Insert them into the other connectors in the set on the KA50/51/55/56 CPU module.

6. Run the MFM diagnostic test, refer to Section 1.4 after you reinstall the KA50/51/55/56 CPU module into the system enclosure to check that the memory is working correctly.

---

**Caution**

When removing memory modules, you must release the metal clips on the connectors of the CPU module.
1.4 Memory Tests

The memory tests check the system memory contained on the MS44 and/or MS44L memories. The tests run automatically as part of the power-up tests and initialization, when you turn on the system. The memory tests are a group of individual tests which can be called individually or normally as a group under a specific script number.

The recommended method to verify a new memory installation is to run the memory test script A8 which will call all of the memory tests and run them on all memory present.

Examples of successful and unsuccessful runs of memory test script A8 are shown in Example 1–1 and Example 1–2.

The individual memory tests are listed following the examples.

Example 1–1 Successful Running of Memory Test Script A8

```plaintext
>>> T A8
9D..31..3D..4F..4E..4D..4C..4B..4A..48..48..48..48..48..48..48..48..48..48..48..48
48..48..48..47..40..80..80..
>>> The failure is reported by the count bad pages test 40 at end of the script. Issuing the SHOW MEMORY command shows which memory set caused the failure. Bad pages were detected in memory set 0.

>>> SHOW MEMORY
16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 00000000 to 00FFFF, 16MB, 32256 good pages, 512 bad pages

16 MB RAM, SIMM Set (1E,1F,1G,1H) present
Memory Set 1: 01000000 to 01FFFF, 16MB, 32768 good pages, 0 bad pages

Total of 32MB, 65024 good pages, 512 bad pages, 112 reserved pages
>>>```
KA50/51/55/56 CPU Module Description

1.4 Memory Tests

Example 1–2 Typical Failure After Running Memory Test Script A8

```plaintext
>>> T A8
9D..31..30..4F..4E..4D..4C..4B..4A..48..48..48..48..48..48..48..48..48..48..48..
48..48..48..47..40..
```

Test DC - Check for No Memory Present

The only purpose of this test is to check for the specific condition of no valid memory present in the system. This occurs if no memory is present, or if memory is present and one or more SIMMs is missing or not plugged in correctly.

Test 31 - Size and Setup Memory CSRs

Find out how much memory is available and configure into consecutive memory starting at address 00000000. Verify proper configuration data in the CSRs.

Test 30 - Build a Bitmap In Memory

Set up a bitmap in RAM to be used by the memory tests. Test the area before setting up a bitmap.

This test looks for a 1 MB KB section of memory to be used for the bitmap, busmap and reserved console area and structures to run diagnostics. The test starts at the top of available memory and tests one section of memory at the top of each 4 MB section of memory until a good section is found for the maps or the bottom of memory is reached, in which case the test fails.

Test 4F - Data Pattern Tests

Verifies that each bit in the data path can be written to a one and a zero individually. This test also checks for shorts between individual paths. The test needs to be run once for each array of memory chips.

This test uses various fix patterns and also floating 1's and 0's patterns across all 72 data bits (64 data, 8 ECC). The test always checks both even and odd QW's of data so that all four SIMMs in a memory set are tested.

Test 4E - Masked Write Cycles with No Errors, BYTE, WORD

This test verifies masked write cycles to memory.
Test 4D - Address Uniqueness Test
The main purpose of the test is to verify that each set on each board can be uniquely addressed. The test writes a unique pattern to each location to be tested then verifies all locations.

Test 4C - MEMORY ECC, Verify Error Detection and Reporting
The main purpose of this test is to test ECC logic. It is not intended to test the memory RAMs explicitly.

The test verifies that single and double bit errors are reported and logged correctly in the MESR. It also verifies that single bit errors cause interrupts through vector 54 when enabled and that double bit errors cause a machine check.

In addition, the test also verifies that multiple bit errors can be detected using data patterns that generate all of the syndrome values for multiple bit errors.

Test 4B - MEMORY Verify Masked Write Cycles with Errors
The test verifies operation of masked write cycles when the location contains errors. In addition, it verifies that errors are reported and that single bit errors are corrected.

Test 4A - MEMORY ECC, Verify Ability to Correct Single Bit Errors
This test verifies the correct operation of the error correction logic (ECC). It does this by verifying that single bit errors can be detected and corrected in any of the 64 data bits and that single bit errors are detected in the eight check bits.

Test 48 - MEMORY Address/Shorts Test
This test verifies that all locations in each set can be uniquely written to and that each of the 64 data bits in each QW can be written to a one and to a zero. This test also writes all locations in memory with good ECC.

The test runs on a hexaword basis with all caches enabled to fully utilize caching to speed up the test. Two primary data patterns of AAAAAAAA_AAAAAAA and 55555555_55555555 are used by the test. The ECC checkbits for these patterns are complements of each other. By running this test, all data and ECC bits in all locations in memory will be written as a 1 and a 0. The test also detects addressing errors.

Test 47 - MEMORY Data Retention, Verify Refresh Logic
This test verifies that the refresh logic is working for all memory boards. The test loads patterns into memory, waits a specified amount of time, then verifies the patterns.
Test 40 - MEMORY Count Bad Pages Marked in Bitmap
This test is normally run last in a script of memory tests. Its only purpose is to read the bitmap when done and check to see if any pages in memory were marked bad, if so, report an error.

Note
If this test fails, do SHOW MEMORY to see which set has bad pages in it.
This chapter describes the KA50/51/55/56 system configurations. It gives information on the following:

- Memory configurations
- Mass storage devices
- Communications options

### 2.1 Memory Configurations

A KA50/51/55/56 system has a basic memory of 16M bytes or 64M bytes. This consists of four MS44L-AA memory modules or four MS44-CA memory modules. You can add memory in 16M byte or 64M byte increments, up to a maximum of 128M bytes. See Section 1.2 for information on the memory configurations.

### 2.2 Mass Storage Devices

A KA50/51/55/56 system supports mass storage devices in the following categories:

- Internal mass storage devices—These devices are mounted inside the system enclosure.
- External mass storage devices—These devices are self-contained units that you can connect to the system externally.
2.2 Mass Storage Devices

2.2.1 Internal Mass Storage Devices

Table 2–1 shows some of the internal mass storage devices that a KA50/51/55/56 system supports.

<table>
<thead>
<tr>
<th>Option Name</th>
<th>Description</th>
<th>Size(^1) (in)</th>
<th>Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>RZ23L</td>
<td>Disk drive</td>
<td>3.5</td>
<td>120-MB</td>
</tr>
<tr>
<td>RZ24</td>
<td>Disk drive</td>
<td>3.5</td>
<td>209-MB</td>
</tr>
<tr>
<td>RZ24L</td>
<td>Disk drive</td>
<td>3.5</td>
<td>245-MB</td>
</tr>
<tr>
<td>RZ25</td>
<td>Disk drive</td>
<td>3.5</td>
<td>400-MB</td>
</tr>
<tr>
<td>RZ25L</td>
<td>Disk drive</td>
<td>3.5</td>
<td>535-MB</td>
</tr>
<tr>
<td>RZ25M</td>
<td>Disk drive</td>
<td>3.5</td>
<td>545-MB</td>
</tr>
<tr>
<td>RZ26</td>
<td>Disk drive</td>
<td>3.5</td>
<td>1.05-GB</td>
</tr>
<tr>
<td>RZ26L</td>
<td>Disk drive</td>
<td>3.5</td>
<td>1.05-GB</td>
</tr>
<tr>
<td>RZ28</td>
<td>Disk drive</td>
<td>3.5</td>
<td>2.10-GB</td>
</tr>
<tr>
<td>TZ30(^2)</td>
<td>Tape drive</td>
<td>5.25</td>
<td>95-MB cartridge</td>
</tr>
<tr>
<td>TZK10/TZK11(^2)</td>
<td>Tape drive</td>
<td>5.25</td>
<td>Range of cartridges</td>
</tr>
<tr>
<td>TLZ06/TLZ07(^2)</td>
<td>Tape drive</td>
<td>5.25</td>
<td>Range of cassettes</td>
</tr>
<tr>
<td>RX23/RX28(^2)</td>
<td>Diskette drive</td>
<td>3.5</td>
<td>Range of diskettes</td>
</tr>
<tr>
<td>RRD42(^2)</td>
<td>CDROM drive</td>
<td>5.25</td>
<td>600-MB CDROM</td>
</tr>
<tr>
<td>RRD43(^2)</td>
<td>CDROM drive</td>
<td>5.25</td>
<td>600-MB CDROM</td>
</tr>
</tbody>
</table>

\(^1\text{Size of half-height device.}\)
\(^2\text{Removable media device.}\)

The system enclosure determines the combinations of internal mass storage devices in a KA50/51/55/56 system. See the MicroVAX 3100 BA42B Enclosure Maintenance manual for more information.

2.2.2 External Mass Storage Devices

The external mass storage devices connect to KA50/51/55/56 systems through the SCSI connector on the back of the system enclosure. In KA50/51/55/56 systems, the SCSI bus supports a maximum of seven mass storage devices. Therefore, the number of external mass storage devices that you can connect depends on the number of mass storage devices that are mounted inside the system enclosure.
Configuration
2.2 Mass Storage Devices

The maximum number of mass storage devices in the system enclosure is five. This means that you can connect at least two external mass storage devices.

A KA50/51/55/56 system supports the SZ series of mass storage expansion boxes. The SZ number defines the contents of each expansion box. Figure 2–1 shows the numbering system for SZ expansion boxes.

**Figure 2–1  SZ Expansion Box Numbering System**

```
SZ 1 n x – x x
```

<table>
<thead>
<tr>
<th>Enclosure Type</th>
<th>Power Cord Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 = BA42 Enclosure</td>
<td>A = 120 V ac</td>
</tr>
<tr>
<td>6 = BA46 Enclosure</td>
<td>B = 240 V ac</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Left Compartment</th>
<th>Right Compartment</th>
</tr>
</thead>
<tbody>
<tr>
<td>A = RZ55</td>
<td>A = RZ55</td>
</tr>
<tr>
<td>B = RZ56</td>
<td>B = RZ56</td>
</tr>
<tr>
<td>C = RZ57</td>
<td>C = RZ57</td>
</tr>
<tr>
<td>P = RZ25¹</td>
<td>D = TLZ04²</td>
</tr>
<tr>
<td>R = RZ58</td>
<td>E = T2Z10</td>
</tr>
<tr>
<td>X = Empty</td>
<td>F = RRD42</td>
</tr>
<tr>
<td></td>
<td>H = T230</td>
</tr>
<tr>
<td></td>
<td>L = RX23</td>
</tr>
<tr>
<td></td>
<td>M = RX33</td>
</tr>
<tr>
<td></td>
<td>P = RZ25¹</td>
</tr>
<tr>
<td></td>
<td>R = RZ58</td>
</tr>
<tr>
<td></td>
<td>X = Empty</td>
</tr>
</tbody>
</table>

¹ The RZ25 disk drive fits in the BA42 enclosure only.
² The TLZ04 tape drive fits in the BA46 enclosure only.

With the KZDDA SCSI option, a second SCSI connector, a KA50/51/55/56 system can support seven additional external devices on a second (external) SCSI bus.

A KA50/51/55/56 system also supports other types of external mass storage devices. See the latest Systems and Options Catalog (SOC) for a listing of supported external SCSI devices.

When you are adding mass storage devices, use these guidelines. Also, refer to documentation for your SCSI expander, if any.

- You can add a maximum of four external SCSI devices. A fully configured SZ12 enclosure contains two SCSI devices.
- You can add a maximum of two SCSI tape devices. Depending on the configuration, the system may support two TLZ04 tape drives.
Configuration

2.2 Mass Storage Devices

- The BA40 single drive expansion box contains one SCSI device.
- The RRD42 CDROM drive is a single SCSI device. You can add a maximum of three RRD42 CDROM drives.
- Terminate the SCSI bus correctly. Failure to do this can cause a system failure or corrupt data.
- Digital recommends that you connect all SCSI devices to the same ac power source.
- Do not add or remove devices that are connected to the SCSI bus while the power is on.
- Digital does not guarantee the correct operation of a SCSI bus that does not use the cables supplied by Digital or is not configured in accordance with Digital recommendations.

2.2.3 SCSI ID Numbers

Each mass storage device must have a unique SCSI ID number. SCSI ID 6 is typically used for the SCSI controller.

2.3 Communications Options

A KA50/51/55/56 system supports the following types of communications options:

- Asynchronous communications options
- Synchronous communications options

Each communications option has components that are installed in the system enclosure and components that connect to the system externally.

2.3.1 Asynchronous Communications Options

Table 2–2 lists the asynchronous communications options that KA50/51/55/56 systems support.

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DHW42-AA</td>
<td>Eight-line DEC423 asynchronous option</td>
</tr>
<tr>
<td>DHW42-BA</td>
<td>Sixteen-line DEC423 asynchronous module option</td>
</tr>
<tr>
<td>DHW42-CA</td>
<td>Eight-line EIA-232 modem asynchronous module option</td>
</tr>
<tr>
<td>DHW42-UP</td>
<td>Eight-line to 16-line DEC423 asynchronous upgrade option</td>
</tr>
</tbody>
</table>
2.3.2 Synchronous Communications Options

Table 2–3 lists the synchronous communications options that KA50/51/55/56 systems support.

**Table 2–3 Supported Synchronous Communications Options**

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model 100</td>
<td>DSW42-AA&lt;sup&gt;1&lt;/sup&gt; Two-line EIA-232/V.24 synchronous option with two external cables, BC19D-02 (17-01110-01)</td>
</tr>
</tbody>
</table>

<sup>1</sup>This option is supplied with two external cables that support the EIA-232/V.24 interface.

The DSW42-AA option also supports the communications interfaces listed in Table 2–4, but you must order the external cables separately.

**Table 2–4 DSW42-AA Communications Support**

<table>
<thead>
<tr>
<th>Communications Interface</th>
<th>External Cable</th>
</tr>
</thead>
<tbody>
<tr>
<td>EIA-423/V.10</td>
<td>BC19E-02&lt;sup&gt;1&lt;/sup&gt; (17-01111-01)</td>
</tr>
<tr>
<td>EIA-422/V.11</td>
<td>BC19B-02&lt;sup&gt;1&lt;/sup&gt; (17-01108-01)</td>
</tr>
</tbody>
</table>

<sup>1</sup>Two required for DSW42-AA.
KA50/51/55/56 Firmware Commands

This chapter describes the console mode control characters, the command syntax, the command modifiers, and all of the console commands. You can enter these commands when the system is in console mode. Console mode is indicated when the console prompt (>>>) is displayed. If the system is running the operating system software, refer to the MicroVAX 3100 Model 85 Customer Technical Information manual, the MicroVAX 3100 Model 90 Customer Technical Information manual, the MicroVAX 3100 Model 95 Customer Technical Information manual, or the MicroVAX 3100 Model 96 Customer Technical Information manual, for information on returning the system to console mode.

If the console security feature is enabled and a security password is set, you must log in to privileged console mode before using most of these commands. Refer to the appropriate MicroVAX 3100 Customer Technical Information manual (above) for information on the console security feature.

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95, and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q–bus and DSSI, will appear on the console and/or printouts from time to time.
3.1 Console I/O Mode Control Characters

In console I/O mode, several characters have special meaning:

\textbf{RETURN} 
Also \texttt{<CR>}. The carriage return ends a command line. No action is taken on a command until after it is terminated by a carriage return. A null line terminated by a carriage return is treated as a valid, null command. No action is taken, and the console prompts for input. Carriage return is echoed as carriage return, line feed (\texttt{<CR><LF>}).

\textbf{<DEL>}
When you press \texttt{<DEL>}, the console deletes the previously typed character. The resulting display differs, depending on whether the console is a video or a hardcopy terminal.

For hardcopy terminals, the console echoes a backslash (\textbackslash{}), followed by the deletion of the character. If you press additional rubouts, the additional deleted characters are echoed. If you type a nonrubout character, the console echoes another backslash, followed by the character typed. The result is to echo the characters deleted, surrounding them with backslashes. For example:

\texttt{EXAM\{E \texttt{<DEL><\textbackslash\textbackslash>\text{NE}<CR>}}

The console echoes: \texttt{EXAM\{E\textbackslash\textbackslash;\text{NE}<CR>}

The console sees the command line: \texttt{EXAMINE<CR>}

For video terminals, the previous character is erased and the cursor is restored to its previous position.

The console does not delete characters past the beginning of a command line. If you press more rubouts than there are characters on the line, the extra rubouts are ignored. A rubout entered on a blank line is ignored.

\textbf{\texttt{CTRL/A} and F14}
Toggle insertion/overstrike mode for command line editing. By default, the console powers up to overstrike mode.

\textbf{\texttt{CTRL/U} or up_{arrow} (or down_{arrow})}
Recalls previous command(s). Command recall is only operable if sufficient memory is available. This function may then be enabled and disabled using the SET RECALL command.

\textbf{\texttt{CTRL/H} and \texttt{F12}}
Move cursor left one position.

\textbf{\texttt{CTRL/F} and right arrow}
Moves cursor to the end of the line.

\textbf{\texttt{CTRL/H} backspace, and F12}
Move cursor to the beginning of the line.

\textbf{\texttt{CTRL/U}}
Echoes \texttt{^U<CR>} and deletes the entire line. Entered but otherwise ignored if typed on an empty line.

\textbf{\texttt{CTRL/S}}
Stops output to the console terminal until \texttt{CTRL/C} is typed. Not echoed.

\textbf{\texttt{CTRL/Q}}
Resumes output to the console terminal. Not echoed.
3.1 Console I/O Mode Control Characters

**CTRLR**
Echoes <CR><LF>, followed by the current command line. Can be used to improve the readability of a command line that has been heavily edited.

**CTRLC**
Echoes ^C<CR> and aborts processing of a command. When entered as part of a command line, deletes the line.

**CTRL/O**
Ignores transmissions to the console terminal until the next [CTRL/O] is entered. Echoes ^O when disabling output, not echoed when it re-enables output. Output is re-enabled if the console prints an error message, or if it prompts for a command from the terminal. Output is also enabled by entering console I/O mode, by pressing the [BREAK] key, and by pressing [CTRLC].

3.1.1 Command Syntax

The console accepts commands up to 80 characters long. Longer commands produce error messages. The character count does not include rubouts, rubbed-out characters, or the [RETURN] at the end of the command.

You can abbreviate a command by entering only as many characters as are required to make the command unique. Most commands can be recognized from their first character. See Table 3–5.

The console treats two or more consecutive spaces and tabs as a single space. Leading and trailing spaces and tabs are ignored. You can place command qualifiers after the command keyword or after any symbol or number in the command.

All numbers (addresses, data, counts) are hexadecimal (hex), but symbolic register names contain decimal register numbers. The hex digits are 0 through 9 and A through F. You can use uppercase and lowercase letters in hex numbers (A through F) and commands.

The following symbols are qualifier and argument conventions:

|   | An optional qualifier or argument
|   | A required qualifier or argument

3.1.2 Address Specifiers

Several commands take one or more addresses as arguments. An address defines the address space and the offset into that space. The console supports five address spaces:

- Physical memory
- Virtual memory
- General purpose registers (GPRs)
- Internal processor registers (IPRs)
- The PSL
KA50/51/55/56 Firmware Commands

3.1 Console I/O Mode Control Characters

The address space that the console references is inherited from the previous console reference, unless you explicitly specify another address space. The initial address space is physical memory.

3.1.3 Symbolic Addresses

The console supports symbolic references to addresses. A symbolic reference defines the address space and the offset into that space. Table 3–1 lists symbolic references supported by the console, grouped according to address space. You do not have to use an address space qualifier when using a symbolic address.

<table>
<thead>
<tr>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
</tr>
</thead>
<tbody>
<tr>
<td>/G—General Purpose Registers</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R0</td>
<td>00</td>
<td>R4</td>
<td>04</td>
<td>R8</td>
<td>08</td>
<td>R12  (AP)</td>
<td>0C</td>
</tr>
<tr>
<td>R1</td>
<td>01</td>
<td>R5</td>
<td>05</td>
<td>R9</td>
<td>09</td>
<td>R13  (FP)</td>
<td>0D</td>
</tr>
<tr>
<td>R2</td>
<td>02</td>
<td>R6</td>
<td>06</td>
<td>R10</td>
<td>0A</td>
<td>R14  (SP)</td>
<td>0E</td>
</tr>
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<td>03</td>
<td>R7</td>
<td>07</td>
<td>R11</td>
<td>0B</td>
<td>R15  (PC)</td>
<td>0F</td>
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<td>/I—Internal Processor Registers</td>
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<td>00</td>
<td>pr$ _chbb</td>
<td>10</td>
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<td>02</td>
<td>pr$ _ipl</td>
<td>12</td>
<td>pr$ _tc</td>
<td>22</td>
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<td>pr$ _usp</td>
<td>03</td>
<td>pr$ _astlv</td>
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<td>pr$ _txb</td>
<td>23</td>
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<td>33</td>
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<tr>
<td>pr$ _isp</td>
<td>04</td>
<td>pr$ _sir</td>
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<td>—</td>
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<td>—</td>
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<tr>
<td>—</td>
<td>06</td>
<td>—</td>
<td>16</td>
<td>pr$ _mces</td>
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<td>—</td>
<td>07</td>
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<td>pr$ _ioreset</td>
<td>37</td>
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</table>

Note: All symbolic values in this table are in hexadecimal.

(continued on next page)
### 3.1 Console I/O Mode Control Characters

**Table 3-1 (Cont.)** Console Symbolic Addresses

<table>
<thead>
<tr>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
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<td>18</td>
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<td>pr$_mapen</td>
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<td>09</td>
<td>pr$_nicr</td>
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<td>29</td>
<td>pr$_tbia</td>
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<tr>
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<td>pr$_icr</td>
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<td>pr$_savpc</td>
<td>2A</td>
<td>pr$_tbia</td>
<td>3A</td>
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<tr>
<td>pr$_p1lr</td>
<td>0B</td>
<td>pr$_todr</td>
<td>1B</td>
<td>pr$_savpel</td>
<td>2B</td>
<td>—</td>
<td>3B</td>
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<td>—</td>
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<td>—</td>
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<td>—</td>
<td>2E</td>
<td>pr$_sid</td>
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<td>pr$_vmar</td>
<td>D0</td>
<td>—</td>
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<td>B1</td>
<td>pr$_vtag</td>
<td>D1</td>
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<td>pr$_neocmd</td>
<td>B2</td>
<td>pr$_vdata</td>
<td>D2</td>
<td>pr$_pcadr</td>
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<td>pr$_icsr</td>
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<td>D4</td>
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<td>B5</td>
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<td>pr$_pamode</td>
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<td>—</td>
<td>E8</td>
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<td>—</td>
<td>E9</td>
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<td>—</td>
<td>FA</td>
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<td>—</td>
<td>BB</td>
<td>pr$_tbads</td>
<td>ED</td>
<td>—</td>
<td>FB</td>
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</table>

(continued on next page)
### KA50/51/55/56 Firmware Commands

#### 3.1 Console I/O Mode Control Characters

Table 3-1 (Cont.) Console Symbolic Addresses

<table>
<thead>
<tr>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
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<td>30000000</td>
<td>qbmbr</td>
<td>20000010</td>
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<td>---</td>
</tr>
<tr>
<td>mem or</td>
<td>20040000</td>
<td>---</td>
<td>20080000</td>
<td>br</td>
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<tr>
<td>prom</td>
<td></td>
<td></td>
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<td>qbear</td>
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<td>ectr</td>
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<td>20008018</td>
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<td>sgec_proc</td>
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<td>sgec_bpt</td>
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<td>sgec_pqbr</td>
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<td>sgec_par</td>
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<td>sgec_pmgqcr</td>
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<td>sgec_pdmcr</td>
<td>20004298</td>
<td>sgec_pdc0cr</td>
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<td>sgec_pqcr</td>
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<td>sgec_pmtcr</td>
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<td>sgec_pmc0cr</td>
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</tbody>
</table>

(continued on next page)
**Table 3–1 (Cont.) Console Symbolic Addresses**

<table>
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<tr>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
<th>Symb</th>
<th>Addr</th>
</tr>
</thead>
<tbody>
<tr>
<td>nmcwcb</td>
<td>21000110</td>
<td>modr</td>
<td>21010000</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>memcon0</td>
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<td>memcon1</td>
<td>21018004</td>
<td>memcon2</td>
<td>21018008</td>
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<td>scsicr5B</td>
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<td>scsicrb</td>
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</tr>
</tbody>
</table>

Table 3–2 lists symbolic addresses that you can use in any address space.
KA50/51/55/56 Firmware Commands
3.1 Console I/O Mode Control Characters

Table 3–2  Symbolic Addresses Used In Any Address Space

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>The location last referenced in an EXAMINE or DEPOSIT command.</td>
</tr>
<tr>
<td>+</td>
<td>The location immediately following the last location referenced in an EXAMINE or DEPOSIT command. For references to physical or virtual memory spaces, the location referenced is the last address, plus the size of the last reference (1 for byte, 2 for word, 4 for longword, 8 for quadword). For other address spaces, the address is the last address referenced plus one.</td>
</tr>
<tr>
<td>_</td>
<td>The location immediately preceding the last location referenced in an EXAMINE or DEPOSIT command. For references to physical or virtual memory spaces, the location referenced is the last address minus the size of this reference (1 for byte, 2 for word, 4 for longword, 8 for quadword). For other address spaces, the address is the last address referenced minus one.</td>
</tr>
<tr>
<td>@</td>
<td>The location addressed by the last location referenced in an EXAMINE or DEPOSIT command.</td>
</tr>
</tbody>
</table>

3.1.4 Console Numeric Expression Radix Specifiers

By default, the console treats any numeric expression used as an address or a datum as a hexadecimal integer. The user may override the default radix by using one of the specifiers listed in Table 3–3.

Table 3–3  Console Radix Specifiers

<table>
<thead>
<tr>
<th>Form 1</th>
<th>Form 2</th>
<th>Radix</th>
</tr>
</thead>
<tbody>
<tr>
<td>%b</td>
<td>^b</td>
<td>Binary</td>
</tr>
<tr>
<td>%o</td>
<td>^o</td>
<td>Octal</td>
</tr>
<tr>
<td>%d</td>
<td>^d</td>
<td>Decimal</td>
</tr>
<tr>
<td>%x</td>
<td>^x</td>
<td>Hexadecimal, default</td>
</tr>
</tbody>
</table>

For instance, the value 19 is by default hexadecimal, but it may also be represented as %b11001, %o31, %d25, and %x19 (or in the alternate form as ^b11001, ^o31, ^d25, and ^x19).
3.1.5 Console Command Qualifiers

You can enter console command qualifiers in any order on the command line after the command keyword. The three types of qualifiers are data control, address space control, and command specific. Table 3–4 lists and describes the data control and address space control qualifiers. Command specific qualifiers are listed in the descriptions of individual commands.

<table>
<thead>
<tr>
<th>Qualifier</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Control</strong></td>
<td></td>
</tr>
<tr>
<td>/B</td>
<td>The data size is byte.</td>
</tr>
<tr>
<td>/W</td>
<td>The data size is word.</td>
</tr>
<tr>
<td>/L</td>
<td>The data size is longword.</td>
</tr>
<tr>
<td>/Q</td>
<td>The data size is quadword.</td>
</tr>
<tr>
<td>/N:{count}</td>
<td>An unsigned hexadecimal integer that is evaluated into a longword. This qualifier determines the number of additional operations that are to take place on EXAMINE, DEPOSIT, MOVE, and SEARCH commands. An error message appears if the number overflows 32 bits.</td>
</tr>
<tr>
<td>/STEP:{size}</td>
<td>Step. Overrides the default increment of the console current reference. Commands that manipulate memory, such as EXAMINE, DEPOSIT, MOVE, and SEARCH, normally increment the console current reference by the size of the data being used.</td>
</tr>
<tr>
<td>/WRONG</td>
<td>Wrong. On writes, 3 is used as the value of the ECC bits, which always generates double bit errors. Ignores ECC errors on main memory reads.</td>
</tr>
</tbody>
</table>

(continued on next page)
Table 3-4 (Cont.) Console Command Qualifiers

<table>
<thead>
<tr>
<th>Qualifier</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>/G</td>
<td>General purpose register (GPR) address space, R0–R15. The data size is always longword.</td>
</tr>
<tr>
<td>/I</td>
<td>Internal processor register (IPR) address space. Accessible only by the MTPR and MFPR instructions. The data size is always longword.</td>
</tr>
<tr>
<td>/V</td>
<td>Virtual memory address space. All access and protection checking occur. If access to a program running with the current PSL is not allowed, the console issues an error message. Deposits to virtual space cause the PTE&lt;M&gt; bit to be set. If memory mapping is not enabled, virtual addresses are equal to physical addresses. Note that when you examine virtual memory, the address space and address in the response is the physical address of the virtual address.</td>
</tr>
<tr>
<td>/P</td>
<td>Physical memory address space.</td>
</tr>
<tr>
<td>/M</td>
<td>Processor status longword (PSL) address space. The data size is always longword.</td>
</tr>
<tr>
<td>/U</td>
<td>Access to console private memory is allowed. This qualifier also disables virtual address protection checks. On virtual address writes, the PTE&lt;M&gt; bit is not set if the /U qualifier is present. This qualifier is not inherited; it must be respecified on each command.</td>
</tr>
</tbody>
</table>

3.1.6 Console Command Keywords

Table 3-5 lists command keywords by type. Table 3-6 lists the parameters, qualifiers, and arguments for each console command. Parameters, used with the SET and SHOW commands only, are listed in the first column along with the command.

You should not use abbreviations in programs. Although it is possible to abbreviate by using the minimum number of characters required to uniquely identify a command or parameter, these abbreviations may become ambiguous at a later time if an updated version of the firmware contains new commands or parameters.
### Table 3–5  Command Keywords by Type

<table>
<thead>
<tr>
<th>Processor Control</th>
<th>Data Transfer</th>
<th>Console Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOT</td>
<td>DEPOSIT</td>
<td>CONFIGURE</td>
</tr>
<tr>
<td>CONTINUE</td>
<td>EXAMINE</td>
<td>FIND</td>
</tr>
<tr>
<td>HALT</td>
<td>MOVE</td>
<td>REPEAT</td>
</tr>
<tr>
<td>INITIALIZE</td>
<td>SEARCH</td>
<td>SET</td>
</tr>
<tr>
<td>NEXT</td>
<td>X</td>
<td>SHOW</td>
</tr>
<tr>
<td>START</td>
<td></td>
<td>TEST</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LOGIN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>!</td>
</tr>
</tbody>
</table>

### Table 3–6  Console Command Summary

<table>
<thead>
<tr>
<th>Command</th>
<th>Qualifiers</th>
<th>Argument</th>
<th>Other(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOT</td>
<td>/R5:(boot_flags) /([boot_flags]</td>
<td></td>
<td>[(boot_device)],</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[boot_device]</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[...]</td>
<td></td>
</tr>
<tr>
<td>CONFIGURE</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>CONTINUE</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>DEPOSIT</td>
<td>/B /W /L /Q — /G /I /V /P /M /U</td>
<td>[address]</td>
<td>[data]</td>
</tr>
<tr>
<td></td>
<td>/N:(count) /STEP:[size] /WRONG</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EXAMINE</td>
<td>/B /W /L /Q — /G /I /V /P /M /U</td>
<td>[address]</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>/N:(count) /STEP:[size] /WRONG /INSTRUCTION</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FIND</td>
<td>/MEM /RPB</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>HALT</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>HELP</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>INITIALIZE</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>LOGIN</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

(continued on next page)
### Table 3-6 (Cont.) Console Command Summary

<table>
<thead>
<tr>
<th>Command</th>
<th>Qualifiers</th>
<th>Argument</th>
<th>Other(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOVE</td>
<td>/B /W /L /Q — /N /P /U /N:[count] /STEP:[size] /WRONG</td>
<td>[src_address]</td>
<td>[dest_address]</td>
</tr>
<tr>
<td>NEXT</td>
<td>—</td>
<td>[count]</td>
<td>—</td>
</tr>
<tr>
<td>REPEAT</td>
<td>—</td>
<td>[command]</td>
<td>—</td>
</tr>
<tr>
<td>SEARCH</td>
<td>/B /W /L /Q — /N /P /U /N:[count] /STEP:[size] /WRONG /NOT</td>
<td>[start_address]</td>
<td>[pattern] [mask]</td>
</tr>
<tr>
<td>SET BFLAG</td>
<td>—</td>
<td>[bitmap]</td>
<td>—</td>
</tr>
<tr>
<td>SET BOOT</td>
<td>—</td>
<td>[[boot_device]], [boot_device]...</td>
<td>—</td>
</tr>
<tr>
<td>SET CONTROLP</td>
<td>—</td>
<td>[0/1]</td>
<td>—</td>
</tr>
<tr>
<td>SET HALT</td>
<td>—</td>
<td>[halt_action]</td>
<td>—</td>
</tr>
<tr>
<td>SCSI_ID</td>
<td>—</td>
<td>[bus1 id]</td>
<td>—</td>
</tr>
<tr>
<td>SET HOST</td>
<td>/DUP /DSSI /BUS:[0/1]</td>
<td>[node_number]</td>
<td>[task]</td>
</tr>
<tr>
<td>SET HOST</td>
<td>/DUP /UQSSP /DISK ! /TAPE</td>
<td>[controller_number]</td>
<td>[task]</td>
</tr>
<tr>
<td>SET HOST</td>
<td>/DUP /UQSSP</td>
<td>[csr_address]</td>
<td>[task]</td>
</tr>
<tr>
<td>SET HOST</td>
<td>/MAINTENANCE /UQSSP /SERVICE /MAINTENANCE /UQSSP</td>
<td>[controller_number]</td>
<td>[csr_address]</td>
</tr>
<tr>
<td>SET LANGUAGE</td>
<td>—</td>
<td>[language_type]</td>
<td>—</td>
</tr>
<tr>
<td>SET RECALL</td>
<td>—</td>
<td>[0/1]</td>
<td>—</td>
</tr>
<tr>
<td>SHOW BFLAG</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SHOW BOOT</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SHOW CONTROLP</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SHOW DSSI</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SHOW HALT</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SHOW LANGUAGE</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

1For Open VMS version 1.3 and earlier, only one argument, the id, is used. For later versions, two arguments are accepted; the first refers to the bus, the second to the id; if only one argument is supplied, the system defaults to bus 0, and the argument is taken as the id.

(continued on next page)
Table 3-6 (Cont.) Console Command Summary

<table>
<thead>
<tr>
<th>Command</th>
<th>Qualifiers</th>
<th>Argument</th>
<th>Other(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHOW MEMORY</td>
<td>/FULL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHOW QBUS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHOW RECALL</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SH( w RLV12</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHOW SCSI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHOW SCSI:_ID</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHOW TRANSLATION</td>
<td></td>
<td>(phys_address)</td>
<td></td>
</tr>
<tr>
<td>SHOW UQSSP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHOW VERSION</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>START</td>
<td></td>
<td>{address}</td>
<td></td>
</tr>
<tr>
<td>TEST</td>
<td></td>
<td>(test_number)</td>
<td>(parameters)</td>
</tr>
<tr>
<td>UNJAM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X</td>
<td></td>
<td>{address}</td>
<td>(count)</td>
</tr>
</tbody>
</table>

3.2 Console Commands

The following sections describe all the console commands, give the command formats with their qualifiers, and describe the significance of each qualifier.

3.2.1 BOOT

The BOOT command initializes the processor and transfers execution to Virtual Memory Boot (VMB). VMB attempts to boot the operating system from the specified device or list of devices, or from the default boot device if none is specified. The console qualifies the bootstrap operation by passing a boot flags bitmap to VMB in R5.

Format:

BOOT [qualifier-list] [(boot_dev1), (boot_dev2), ...]

If you do not enter either the qualifier or the device name, the default value is used. Explicitly stating the boot flags overrules the boot device overrides, but does not permanently change the corresponding default value.
KA50/51/55/56 Firmware Commands

3.2 Console Commands

When specifying a list of boot devices (up to 32 characters, with devices separated by commas and no spaces), the system checks the devices in the order specified and boots from the first one that contains bootable software.

______________________________ Note ______________________________

If included in a string of boot devices, the Ethernet device, EZA0, should be placed only as the last device of the string. The system will continuously attempt to boot from EZA0.

____________________________

Set the default boot device and boot flags with the SET BOOT and SET BFLAG commands. If you do not set a default boot device, the processor times out after 30 seconds and attempts to boot from the Ethernet device, EZA0.

Qualifiers:

Command specific:

/R5:[boot_flags] A 32-bit hex value passed to VMB in R5. The console does not interpret this value. Use the SET BFLAG command to specify a default boot flags longword. Use the SHOW BFLAG command to display the longword.

/[boot_flags] Same as /R5:[boot_flags]

/device_name] A character string of up to 32 characters. When specifying a list of boot devices, the device names should be separated by commas and no spaces. Apart from checking the length, the console does not interpret or validate the device name. The console converts the string to uppercase, then passes VMB a string descriptor to this device name in R0. Use the SET BOOT command to specify a default boot device or list of devices. Use the SHOW BOOT command to display the default boot device. The factory default device is the Ethernet device, EZA0. Refer to the MicroVAX 3100 Customer Technical Information manuals for a list of the boot devices supported by the system.

Examples:

>>>SHOW BOOT
DKA300

>>>SHOW BFLAG
00000000

>>>B 'Boot using default boot flags and device.
(BOOT/R5:0 DKA300)

2.

-DKA300
3.2.2 CONTINUE

The CONTINUE command causes the processor to begin instruction execution at the address currently contained in the program counter (PC). This address is the address stored in the PC when the system entered console mode or an address that the user specifies using the DEPOSIT command. The CONTINUE command does not perform a processor initialization. The console enters program I/O mode.

Format:

CONTINUE

Example:

>>>CONTINUE
$ !OpenVMS DCL prompt

3.2.3 DEPOSIT

The DEPOSIT command deposits data into the address specified. If you do not specify an address space or data size qualifier, the console uses the last address space and data size used in a DEPOSIT, EXAMINE, MOVE, or SEARCH command. After processor initialization, the default address space is physical memory and the default data size is longword. If you specify conflicting address space or data sizes, the console ignores the command and issues an error message.

Format:

DEPOSIT [qualifier-list] (address) [data] [data...]

Qualifiers:

Data control: /B, /W, /L, /Q, /N:[count], /STEP:[size], /WRONG

Address space control: /G, /I, /M, /P, /N, /U

Arguments:

[address] A longword address that specifies the first location into which data is deposited. The address can be an actual address or a symbolic address.

[data] The data to be deposited. If the specified data is larger than the deposit data size, the firmware ignores the command and issues an error response. If the specified data is smaller than the deposit data size, it is extended on the left with zeros.

[[data]] Additional data to be deposited (as much as can fit on the command line).
3.2 Console Commands

Examples:

>>>D/P/B:N:1FF 0 0          ! Clear first 512 bytes of physical memory.
>>>D/V/L:N:3 1234 5         ! Deposit 5 into four longwords starting at virtual memory address 1234.
>>>D/N:8 R0 FFFFFFFF        ! Loads GPRs R0 through R8 with -1.
>>>D/L/P/N:10/ST:200 0 8    ! Deposit 8 in the first longword of the first 17 pages in physical memory.
>>>D/N:200 - 0             ! Starting at previous address, clear 513 longwords or 2052 bytes.

3.2.4 EXAMINE

The EXAMINE command examines the contents of the memory location or register specified by the address. If no address is specified, + is assumed. The display line consists of a single character address specifier, the physical address to be examined, and the examined data.

EXAMINE uses the same qualifiers as DEPOSIT. However, the /WRONG qualifier causes EXAMINE to ignore ECC errors on reads from physical memory. The EXAMINE command also supports an /INSTRUCTION qualifier, which will disassemble the instructions at the current address.

Format:

EXAMINE [qualifier-list] [address]

Qualifiers:

Data control: /B, /W, /L, /Q, /N: (count), /STEP: (size), /WRONG
Address space control: /G, /I, /M, /P, /N, /U
Command specific:

/INSTRUCTION Disassembles and displays the VAX MACRO-32 instruction at the specified address.

Arguments:

[[address]] A longword address that specifies the first location to be examined. The address can be an actual or a symbolic address. If no address is specified, + is assumed.
Examples:

```plaintext
>>>EX PC
   G 00000000 FFFFFFFC
>>>EX SP
   G 00000000 00000200
>>>EX PSL
   M 00000000 041F0000
>>>E/M
   M 00000000 041F0000
>>>E R4/N:5
   G 00000004 00000000
   G 00000005 00000000
   G 00000006 00000000
   G 00000007 00000000
   G 00000008 00000000
   G 00000009 801D9000
>>>EX PRS SCBB
   i 00000011 2004A000
   EExamine the SCBB, IPR 17
   i (decimal).
>>>E/P 0
   P 00000000 00000000
>>>EX /INS 20040000
   P 20040000 11 BRB 20040019
>>>EX /INS/N:5 20040019
   P 20040019 D0 MOVL I^#20140000,#20140000
   P 20040024 D2 MCOML @#20140030,#20140002
   P 2004002F D2 MCOML S^#0E,#20140030
   P 20040036 7D MOVQ R0,#201404B2
   P 2004003D D0 MOVL I^#201404B2,R1
   P 20040044 DB MFPR S^#2A,B^44(R1)
>>>E/INS
   P 20040048 DB MFPR S^#2B,B^48(R1)
>>>```

3.2.5 FIND

The FIND command searches main memory, starting at address zero for a page-aligned 128-Kbyte segment of good memory, or a restart parameter block (RPB). If the command finds the segment or RPB, its address plus 512 is left in Stack Pointer (SP) R14. If it does not find the segment or RPB, the console issues an error message and preserves the contents of SP. If you do not specify a qualifier, /RPB is assumed.

Format:

```
FIND [qualifier-list]
```
KA50/51/55/56 Firmware Commands

3.2 Console Commands

Qualifiers:

Command specific:

/MEMORY Searches memory for a page-aligned block of good memory, 128K bytes in length. The search looks only at memory that is deemed usable by the bitmap. This command leaves the contents of memory unchanged.

/RPB Searches all physical memory for an RPB. The search does not use the bitmap to qualify which pages are looked at. The command leaves the contents of memory unchanged.

Examples:

>>>EX SP            ! Check the SP.
   G 00000000E 00000000

>>>FIND /MEM        ! Look for a valid 128 Kbytes.
>>>EX SP            ! Note where it was found.
   G 00000000E 00000200

>>>FIND /RPB        ! Check for valid RPB.
?2C FND ERR 00000004  ! None to be found here.

3.2.6 HALT

The HALT command has no effect. It is included for compatibility with other VAX consoles.

Format:

HALT

Example:

>>>HALT           ! Pretend to halt.

3.2.7 HELP

The HELP command provides information about command syntax and usage.

Format:

HELP

Example:
>>>HELP
Following is a brief summary of all the commands supported by the console:

UPPERCASE denotes a keyword that you must type in
| denotes an OR condition
[ ] denotes optional parameters
<> denotes a field specifying a syntactically correct value
.. denotes one of an inclusive range of integers
... denotes that the previous item may be repeated

Valid qualifiers:
/B |W |L |Q |/INSTRUCTION
/G |T |V |P |/M
/STEP: /N: /NOT
/WRONG /U

Valid commands:
BOOT [[/R5:][boot_flags]] [boot_device]
CONTINUE
DEPOSIT [qualifiers] <address> <datum> [<datum>...]
EXAMINE [qualifiers]' [address]
FIND [/MEMORY | /RPB]
HALT
HELP
INITIALIZE
LOGIN
MOVE [qualifiers] <address> <address>
NEXT [count]
REPEAT <command>
SEARCH [qualifiers] <address> <pattern> [<mask>]
SET BFLG <boot_flags>
SET BOOT <boot_device>
SET DSI_ID <bus_number> <id>
SET HALT <0..4 | DEFAULT | RESTART | REBOOT | HALT | RESTART_REBOOT>
SET HOST/DUP/DSII/BUS:<0..3> <node_number> [task]
SET LANGUAGE <1..15>
SET PSE <0..1 | DISABLED | ENABLED>
SET PSWD <password>
SET RECALL <0..1 | DISABLED | ENABLED>
SET SCSI ID <0..7>
SHOW BFLG
SHOW BOOT
SHOW CONFIG
SHOW DEVICE
SHOW DSI [0..3]
SHOW DSSI ID
SHOW ERRORS
SHOW ESTAT
SHOW ETHERNET
SHOW HALT
SHOW LANGUAGE
SHOW MEMORY [/FULL]
KA50/51/55/56 Firmware Commands

3.2 Console Commands

SHOW PSE
SHOW RECALL
SHOW SAVED_STATE
SHOW SCSI
SHOW SCSI_ID
SHOW TESTS
SHOW TRANSLATION <physical_address>
SHOW VERSION
START <address>
TEST [<test_code> [<parameters>]]
UNJAM
X <address> <count>

>>> 3.2.8 INITIALIZE

The INITIALIZE command performs a processor initialization.

Format:

INITIALIZE

The following registers are initialized:

<table>
<thead>
<tr>
<th>Register</th>
<th>State at Initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSL</td>
<td>041F0000</td>
</tr>
<tr>
<td>IPL</td>
<td>1F</td>
</tr>
<tr>
<td>ASTLVL</td>
<td>4</td>
</tr>
<tr>
<td>SISR</td>
<td>0</td>
</tr>
<tr>
<td>ICCS</td>
<td>Bits &lt;6&gt; and &lt;0&gt; clear; the rest are unpredictable.</td>
</tr>
<tr>
<td>RXCS</td>
<td>0</td>
</tr>
<tr>
<td>TXCS</td>
<td>80</td>
</tr>
<tr>
<td>MAPEN</td>
<td>0</td>
</tr>
<tr>
<td>Caches</td>
<td>Flushed</td>
</tr>
<tr>
<td>Instruction buffer</td>
<td>Unaffected</td>
</tr>
<tr>
<td>Console previous reference</td>
<td>Longword, physical, address 0</td>
</tr>
<tr>
<td>TODR</td>
<td>Unaffected</td>
</tr>
<tr>
<td>Main memory</td>
<td>Unaffected</td>
</tr>
<tr>
<td>General registers</td>
<td>Unaffected</td>
</tr>
<tr>
<td>Halt code</td>
<td>Unaffected</td>
</tr>
</tbody>
</table>

3-20 KA50/51/55/56 Firmware Commands
<table>
<thead>
<tr>
<th>Register</th>
<th>State at Initialization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bootstrap-in-progress flag</td>
<td>Unaffected</td>
</tr>
<tr>
<td>Internal restart-in-progress flag</td>
<td>Unaffected</td>
</tr>
</tbody>
</table>

The firmware clears all error status bits and initializes the following:

- CDAL bus timer
- Address decode and match registers
- Programmable timer interrupt vectors
- The QUART LPR register is set to 9600 baud
- All error status bits are cleared

Example:

```
>>>INIT
>>>
```

### 3.2.9 LOGIN

Allows you to put the system in privileged console mode. When the console security feature is enabled and when you put the system in secure console mode, the system operates in unprivileged console mode. You can access only a subset of the console commands. To access the full range of console commands, you must use this command. This command may only be executed in secure console mode. The format of this command is as follows:

```
LOG(IN)G
```

When you enter the command, the system prompts you for a password as follows:

Password:

You must enter the current console security password. If you do not enter the correct password, the system displays the error message, INCORRECT PASSWORD. When you enter the console security password, the system operates in privileged console mode. In this mode, you can use all the console commands. The system exits from privileged console mode when you enter one of the following console commands:

- BOOT
- CONTINUE
- HALT
KA50/51/55/56 Firmware Commands
3.2 Console Commands

- START

3.2.10 MOVE

The MOVE command copies the block of memory starting at the source address to a block beginning at the destination address. Typically, this command has an /N qualifier so that more than one datum is transferred. The destination correctly reflects the contents of the source, regardless of the overlap between the source and the data.

The MOVE command actually performs byte, word, longword, and quadword reads and writes as needed in the process of moving the data. Moves are supported only for the physical and virtual address spaces.

Format:

MOVE [qualifier-list] [src_address] [dest_address]

Qualifiers:

Data control: /B, /W, /L, /Q, /N:[count], /STEP:[size], /WRONG

Address space control: /N, /U, /P

Arguments:

[src_address] A longword address that specifies the first location of the source data to be copied.

[dest_address] A longword address that specifies the destination of the first byte of data. These addresses may be an actual address or a symbolic address. If no address is specified, + is assumed.

Examples:

>>>EX/N: 4 0 ! Observe destination.
P 00000000 00000000
P 00000004 00000000
P 00000008 00000000
P 0000000C 00000000
P 00000010 00000000

>>>EX/N: 4 200 ! Observe source data.
P 00000200 5BDD0520
P 00000204 585E04C1
P 00000208 00FF8FB8
P 0000020C 5208A8D0
P 00000210 540CA8DE

>>>MOV/N: 4 200 0 ! Move the data.
3.2.11 NEXT

The NEXT command executes the specified number of macro instructions. If no count is specified, 1 is assumed.

After the last macro instruction is executed, the console reenters console I/O mode.

Format:

NEXT [count]

The console implements the NEXT command, using the trace trap enable and trace pending bits in the PSL and the trace pending vector in the SCB.

The console enters the "Spacebar Step Mode". In this mode, subsequent spacebar strokes initiate single steps and a carriage return forces a return to the console prompt.

The following restrictions apply:

- If memory management is enabled, the NEXT command works only if the first page in SSC RAM is mapped in S0 (system) space.
- Overhead associated with the NEXT command affects execution time of an instruction.
- The NEXT command elevates the IPL to 31 for long periods of time (milliseconds) while single-stepping over several commands.
- Unpredictable results occur if the macro instruction being stepped over modifies either the SCBB or the trace trap entry. This means that you cannot use the NEXT command in conjunction with other debuggers.

Arguments:

[count] A value representing the number of macro instructions to execute.
KA50/51/55/56 Firmware Commands
3.2 Console Commands

Examples:

>>>DEP 1000 50D650D4
>>>DEP 1004 125005D1
>>>DEP 1008 00FE11F9
>>>EX /INSTRUCTION /N:5 1000
   P 00001000  D4 CLRL   R0
   P 00001002  D6 INCL   R0
   P 00001004  D1 CMPL  S#05,R0
   P 00001007  12 BNEQ   00001002
   P 00001009  11 BRB   00001009
   P 0000100B  00 HALT
>>>DEP PR$ SCBB 200
>>>DEP PC 1000
   ! List it.
   ! Set up a user SCBB...
   ! ...and the PC.
   ! Single step...
   ! or multiple step the program.
   ! ...
   P 00001000  D4 CLRL   R0
   P 00001002  D6 INCL   R0
   P 00001004  D1 CMPL  S#05,R0
   P 00001007  12 BNEQ   00001002
   P 00001009  11 BRB   00001009
   P 0000100B  00 HALT
>>>N 5
>>>N 7
>>>N
   P 00001000  D4 CLRL   R0
   P 00001002  D6 INCL   R0
   P 00001004  D1 CMPL  S#05,R0
   P 00001007  12 BNEQ   00001002
   P 00001009  11 BRB   00001009
   P 0000100B  00 HALT

3.2.12 REPEAT

The REPEAT command repeatedly displays and executes the specified command. Press [Ctrl+C] to stop the command. You can specify any valid console command except the REPEAT command.

Format:

REPEAT [command]
Arguments:
(command) A valid console command other than REPEAT.

Examples:

```plaintext
>>> REPEAT EX PR$ TCDR  !Watch the clock.
1 0000001B 5AFE78CE
1 0000001B 5AFE78D1
1 0000001B 5AFE78FD
1 0000001B 5AFE7900
1 0000001B 5AFE7903
1 0000001B 5AFE7907
1 0000001B 5AFE790A
1 0000001B 5AFE790D
1 0000001B 5AFE7910
1 0000001B 5AFE793C
1 0000001B 5AFE793F
1 0000001B 5AFE7942
1 0000001B 5AFE7946
1 0000001B 5AFE7949
1 0000001B 5AFE794C
1 0000001B 5AFE794F
1 0000001B 57'C
```
KA50/51/55/56 Firmware Commands
3.2 Console Commands

SEARCH reports the address under the following conditions:

<table>
<thead>
<tr>
<th>/NOT Qualifier</th>
<th>Match Condition</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>Absent</td>
<td>True</td>
<td>Report address</td>
</tr>
<tr>
<td>Absent</td>
<td>False</td>
<td>No report</td>
</tr>
<tr>
<td>Present</td>
<td>True</td>
<td>No report</td>
</tr>
<tr>
<td>Present</td>
<td>False</td>
<td>Report address</td>
</tr>
</tbody>
</table>

The address is advanced by the size of the pattern (byte, word, longword, or quadword), unless overridden by the /STEP qualifier.

Qualifiers:

Data control: /B, /W, /L, /Q, /N:[count], /STEP:[size], /WRONG

Address space control: /P, /N, /U

Command specific:

/NOT Inverts the sense of the match.

Arguments:

[start_address] A longword address that specifies the first location subject to the search. This address can be an actual address or a symbolic address. If no address is specified, + is assumed.

(pattern) The target data.

[mask] A mask of the bits desired in the comparison.

Examples:
3.2 Console Commands

KA50/51/55/56 Firmware Commands

3.2.14 SET

The SET command sets the parameter to the value you specify.

**Format:**

```
SET [parameter] [value]
```

**Parameters:**

- **BFLAG**
  
  Sets the default R5 boot flags. The value must be a hex number of up to eight digits.

- **BOOT**

  Sets the default boot device. The value must be a valid device name or list of device names as specified in the BOOT command description in Section 3.2.1.

- **HALT**

  Sets the user-defined halt action. Acceptable values are the keywords "default", "restart", "reboot", "halt", "restart_reboot", or a number in the range 0 to 4 inclusive.
KA50/51/55/56 Firmware Commands

3.2 Console Commands

HOST
Invoke the DUP or MAINTENANCE driver on the selected node. Only SET HOST/DUP accepts a value parameter. The hierarchy of the SET HOST qualifiers listed below suggests the appropriate usage. Each qualifier only supports additional qualifiers at levels below it.

LANGUAGE
Sets console language and keyboard type. If the current console terminal does not support the multinational character set (MCS), then this command has no effect and the console message appears in English. Values are 1 through 15.

PSE
Allows you to enable or disable the console security feature of the system. The SET PSE command accepts the following values:

- 0—Console security disabled
- 1—Console security enabled

When the console security feature is enabled, only a subset of the console commands is available to the user. To enable the complete set of console commands once the console security feature is enabled, you must use the LOGIN command (see Section 3.2.9).

PSWD
Allows you to set or change the console security password.

RECALL
Sets command recall state to either ENABLED (1) or DISABLED (0).

SCSI_ID
Sets the SCSI ID of the SCSI controller to a number in the range 0 to 7. The SCSI ID of the SCSI controller is set to 6 before the system is shipped. For the KZDDA option second SCSI bus, You must enter two arguments; the bus, then the id.

Qualifiers: Listed in the parameter descriptions above.

Examples:

>>> SET BLFAG 220
>>> SET BOOT DUA0
>>> SET LANGUAGE 5
>>> SET HALT RESTART

3.2.15 SHOW

The SHOW command displays the console parameter you specify.

Format:

SHOW {parameter}
Parameters:

BFLAG
Displays the default R5 boot flags.

BOOT
Displays the default boot device.

CONFIG
Displays the system configuration. The command displays information about the devices that the firmware has tested. It also displays the device errors that the most recent device test detected.

DEVICE
Displays all devices in the system.

HALT
Shows the user-defined halt action.

ESTAT
Shows results from last run of the system exerciser, tests 100 to 107. Data is volatile and is destroyed by running other tests or boots, etc. SHOW ESTAT normally done immediately after running the system test.

ERRORS
Shows saved data on tests which failed.

ETHERNET
Displays hardware Ethernet address for all Ethernet adapters that can be found. Displays as blank if no Ethernet adapter is present.

LANGUAGE
Displays console language and keyboard type. Refer to the corresponding SET LANGUAGE command for the meaning.

MEMORY
Displays main memory configuration.
/FULL—Additionally, displays the normally inaccessible areas of memory, such as the PFN bitmap pages, and the console scratch memory pages. Also reports the addresses of bad pages, as defined by the bitmap.

PSE
Displays the condition of the console security feature of the system.

RECALL
Shows the current state of command recall, either ENABLED or DISABLED.

This information is obtained from the media type field of the MSCP command GET UNIT STATUS. The console does not display device information if a node is not running (or cannot run) an MSCP server.

SCSI
Shows any SCSI devices in the system.

TRANSLATION
Shows any virtual addresses that map to the specified physical address. The firmware uses the current values of page table base and length registers to perform its search; it is assumed that page tables have been properly built.

VERSION
Displays the current firmware version.

Qualifiers: Listed in the parameter descriptions above.
KA50/51/55/56 Firmware Commands
3.2 Console Commands

Examples:

>>> SHOW BFLAG
00000220
>>> SHOW BOOT
DUA0
>>> SHOW CONTROLP
>>> SHOW ETHERNET
Ethernet Adapter
-2E0 (08-00-2B-08-29-14)
>>> SHOW HALT
restart
>>> SHOW LANGUAGE
English (United States/Canada)
>>> show memory

16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 04000000 to 04FFFFFF, 16MB, 32768 good pages, 0 bad pages

64 MB RAM, SIMM Set (1E,1F,1G,1H) present
Memory Set 1: 00000000 to 03FFFFFF, 64MB, 131072 good pages, 0 bad pages
Total of 80MB, 163840 good pages, 0 bad pages, 136 reserved pages
>>> show memory / full
>>> show mem/full

16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 00000000 to 00FFFFFF, 16MB, 32768 good pages, 0 bad pages
Total of 16MB, 32768 good pages, 0 bad pages, 104 reserved pages

Memory Bitmap
-00FF3000 to 00FF3FFF, 8 pages
Console Scratch Area
-00FF4000 to 00FF7FFF, 32 pages
Scan of Bad Pages
>>>
3.2.16 START

The START command starts instruction execution at the address you specify. If no address is given, the current PC is used. If memory mapping is enabled, macro instructions are executed from virtual memory, and the address is treated as a virtual address. The START command is equivalent to a DEPOSIT to PC, followed by a CONTINUE. It does not perform a processor initialization.

Format:
START [[address]]

Arguments:

[address] The address at which to begin execution. This address is loaded into the user's PC.

Example:
>>>START 1000

3.2.17 TEST

The TEST command invokes a diagnostic test program specified by the test number. If you enter a test number of 0 (zero), the power-up diagnostics are executed. The console accepts an optional list of up to five additional hexadecimal arguments.

Refer to Chapter 5 for a detailed explanation of the diagnostics.

Format:
TEST [[test_number] [[test_arguments]]]

Arguments:

[test_number] A two-digit hex number specifying the test to be executed. No meaning to console, but meaning to tests themselves. T 9E lists arguments used by applicable tests.
KA50/51/55/56 Firmware Commands
3.2 Console Commands

(test_arguments)  Up to five additional test arguments. These arguments are accepted, but
they have no meaning to the console.

Example:

>>>TEST 0
72..71..70..69..68..67..66..65..64..63..62..61..60..59..58..57..
56..55..54..53..52..51..50..49..48..47..46..45..44..43..42..41..
40..39..38..37..36..35..34..33..32..31..30..29..28..27..26..25..
24..23..22..21..20..19..18..17..16..15..14..13..12..11..10..09..
08..07..06..05..04..03..
Tests completed.

Example:

>>> 9C

savpc=20048C68  savpsl=20048C68  sbr=03FA0000  slr=00003040
p0br=80000000  p0lr=001B2000  plbr=00000000  pllr=00000000
sid=13001401  sie=03020A01  mapen=00000000
bcrl=00000000  txr=00000000  tnir=00000000  tivr=0000007B
bcr=00000001  tirl=02AF768E  tnr=00000000  tivr=0000007C
bdr=3F8B00F  ssccr=00D05070  scbb=20053400
DZ csr=0020  tcr=0008  msr=0F75
scr=0000D000  dser=00000000  qbear=00000000F  dear=00000000
qmb=03FF8000  ipcr=0000
nicr0=1FF0003  3=00004030  4=00004050  5=0B390000  6=83800000  7=00000000
nicr9=04E204E2  10=00040000  11=00000000  12=00000000  13=00000000  15=000000FF
NISA-08-00-2B-29-1C-7A  intmask=00  intreq=00  scaddr=00000000  scddir=0
SCSI_CSRs 0=01 1=00 2=00 3=00 4=00 5=05 6=05 7=00 8=16 9=5B A=5B B=00 C=04
V1C........icsr=00000001  vmar=00007E00  ecr=000000CA
PC......pctl=FFFFC13  pcsts=FFFF8000  paddr=FFFFC12
BC_128K...cctl=00000007  bcetstd=00003E00  bcetidx=FFFFFE00  bcetag=FFFFFE00
...bcetstd=0000F000  bcetidx=01FFFFF  bcetdec=00000000
.............bcest=00000000  bcedidx=01FFFFF  bcetdecc=00000000
..............bcest=00000000  neomdr=E005F700  neomcmd=8000FF04  neicmd=000003FF
..............neomdr=FFFFFE00  nedatol=FFFFFE00  cefasa=00192000  cefadr=E000020C
MEMORY.....mesr=00060000  mear=08406010...Add=21018040  mncsr=00000000
..............memcon=080000005  memcon1=00000007  moamr=00000000  ssr=COCE
NCA........ces=00000000  cmcdsr=0000C108  cnewr=00000000
..............csear=00000000  csear=00000000  cioear=00000000  cioear=00000000
..............cisr=00000000  nicr=FFFFBD8F0  icr=FFFFBD8F0  todr=00000000

3-32  KA50/51/55/56 Firmware Commands
**Example:**

```plaintext
>>> ! list diagnostics and scripts
>>> TEST
```

<table>
<thead>
<tr>
<th>Test</th>
<th>Address</th>
<th>Name</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20052200</td>
<td>SCB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20055B50</td>
<td>De_executive</td>
<td>*** mark_Hard_SBES ******</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>2006A53C</td>
<td>Memory_Init_Bitmap</td>
<td>**</td>
</tr>
<tr>
<td>31</td>
<td>2006AB34</td>
<td>Memory_Setup_CSRs</td>
<td>**</td>
</tr>
<tr>
<td>32</td>
<td>2005D14B</td>
<td>NMC_registers</td>
<td>**</td>
</tr>
<tr>
<td>33</td>
<td>2005D324</td>
<td>NMC_powerup</td>
<td>**</td>
</tr>
<tr>
<td>34</td>
<td>2005E6D8</td>
<td>SSC ROM</td>
<td>**</td>
</tr>
<tr>
<td>35</td>
<td>2005F990</td>
<td>B_Cache_diag_mode</td>
<td>bypass_test_mask **</td>
</tr>
<tr>
<td>37</td>
<td>20061390</td>
<td>Cache_w_Memory</td>
<td>bypass_test_mask **</td>
</tr>
<tr>
<td>40</td>
<td>2006B5E0</td>
<td>Memory_count_pages</td>
<td>SIMM_set0 SIMM_set1 Soft_errs_allowed *****</td>
</tr>
<tr>
<td>41</td>
<td></td>
<td>Board_Reset</td>
<td>*</td>
</tr>
<tr>
<td>42</td>
<td></td>
<td>Chk_for_Interrupts</td>
<td>**</td>
</tr>
<tr>
<td>46</td>
<td>200610C4</td>
<td>P_Cache_diag_mode</td>
<td>bypass_test_mask **</td>
</tr>
<tr>
<td>47</td>
<td>2006AD04</td>
<td>Memory_Refresh</td>
<td>start a end incr cont_on_err time_seconds *****</td>
</tr>
<tr>
<td>48</td>
<td>2006B028</td>
<td>Memory.Addr shorts</td>
<td>start_add end_add * cont_on_err pat2 pat3 *****</td>
</tr>
<tr>
<td>4A</td>
<td>2006A23C</td>
<td>Memory_ECC_FBEs</td>
<td>start_add end_add add incr cont_on_err *****</td>
</tr>
<tr>
<td>4B</td>
<td>2006940C</td>
<td>Memory_Byte_Errors</td>
<td>start_add end_add add incr cont_on_err *****</td>
</tr>
<tr>
<td>4C</td>
<td>20069B40</td>
<td>Memory_ECC_Logic</td>
<td>start_add end_add add incr cont_on_err *****</td>
</tr>
<tr>
<td>4D</td>
<td>20068F6B</td>
<td>Memory_Address</td>
<td>start_add end_add add incr cont_on_err *****</td>
</tr>
<tr>
<td>4E</td>
<td>20069B88</td>
<td>Memory_Byte</td>
<td>start_add end_add add incr cont_on_err *****</td>
</tr>
<tr>
<td>4F</td>
<td>2006B7F4</td>
<td>Memory_Data</td>
<td>start_add end_add add incr cont_on_err *****</td>
</tr>
<tr>
<td>51</td>
<td>2005B03C</td>
<td>FPA</td>
<td>**</td>
</tr>
<tr>
<td>52</td>
<td></td>
<td></td>
<td>**</td>
</tr>
<tr>
<td>53</td>
<td>2005B530</td>
<td>SSC_Prog_timers</td>
<td>which_timer wait_time us ***</td>
</tr>
<tr>
<td>54</td>
<td>2005B818</td>
<td>SSC_TOY_Clock</td>
<td>repeat_test_250ms ea Tolerance ***</td>
</tr>
<tr>
<td>55</td>
<td>2005C18</td>
<td>Virtual_Mode</td>
<td>**</td>
</tr>
<tr>
<td>56</td>
<td>20055B6C</td>
<td>Interval_Timer</td>
<td>***</td>
</tr>
<tr>
<td>58</td>
<td>200507C</td>
<td>SHAC_LPCHK</td>
<td>From_bus To_bus passes *****</td>
</tr>
<tr>
<td>59</td>
<td>2005D24</td>
<td>SHAC_RESET</td>
<td>dssi_bus port_number time_secs not_pres **</td>
</tr>
<tr>
<td>59</td>
<td>2006778</td>
<td>SGEC_LPCHK_ASSIST</td>
<td>time_secs **</td>
</tr>
<tr>
<td>5C</td>
<td>2006D010</td>
<td>SHAC</td>
<td>SHAC_number **</td>
</tr>
<tr>
<td>5F</td>
<td>200619B8</td>
<td>SGEC</td>
<td>loopback_type no ram tests *****</td>
</tr>
<tr>
<td>62</td>
<td>2005B1C</td>
<td>console_QDSS</td>
<td>mark_not_present selftest_r0 selftest_r1 *****</td>
</tr>
<tr>
<td>63</td>
<td>2005CA4</td>
<td>QDSS any</td>
<td>input_ctrl selftest_r0 selftest_r1 *****</td>
</tr>
<tr>
<td>80</td>
<td>2005D3C0</td>
<td>CQBIC_memory</td>
<td>bypass_test_mask **</td>
</tr>
<tr>
<td>81</td>
<td>200596CC</td>
<td>Qbus_MSCP</td>
<td>IP_ctrl *****</td>
</tr>
<tr>
<td>82</td>
<td>20059AC</td>
<td>Qbus_DELQA</td>
<td>device_num_addr ****</td>
</tr>
<tr>
<td>83</td>
<td>2005AB5C</td>
<td>Q&amp;A_Intlpbck1</td>
<td>controller_number ***</td>
</tr>
<tr>
<td>84</td>
<td>2005F1C</td>
<td>Q&amp;A_Intlpbck2</td>
<td>controller_number ***</td>
</tr>
<tr>
<td>85</td>
<td>2005A9C</td>
<td>Q&amp;A_memory</td>
<td>incr_test_pattern controller_number *****</td>
</tr>
<tr>
<td>86</td>
<td>2005F44</td>
<td>Q&amp;A_DMA</td>
<td>Controller_number main_mem_buf *****</td>
</tr>
<tr>
<td>90</td>
<td>20058494</td>
<td>CQBIC_registers</td>
<td>*</td>
</tr>
</tbody>
</table>
3.2 Console Commands

Scripts

A0 User defined scripts
A1 Powerup tests, Functional Verify, continue on error, numeric countdown
A3 Functional Verify, stop on error, test # announcements
A4 Loop on A3, Functional Verify
A6 Memory tests, mark only multiple bit errors
A7 Memory tests
A8 Memory acceptance tests, mark single and multi-bit errors, call A7
A9 Memory tests, stop on error
B2 Extended tests plus BF, then loop
B5 Extended tests, then loop
BF D2, SYNC, ASYNC with loopbacks
3.2.18 UNJAM

The UNJAM command performs an I/O bus reset, by writing a 1 (one) to IPR 55 (decimal). SHAC and SGEC are explicitly reset, EDAL_INTREQ register error bits are cleared and SCSI_DMA map registers are cleared.

Format:

UNJAM

Example:

>>>UNJAM

>>> 3.2.19 X—Binary Load and Unload

The X command is for use by automatic systems communicating with the console.

The X command loads or unloads (that is, writes to memory, or reads from memory) the specified number of data bytes through the console serial line (regardless of console type) starting at the specified address.

Format:

X [address] [count] CR [line_checksum] [data] [data_checksum]

If bit 31 of the count is clear, data is received by the console and deposited into memory. If bit 31 is set, data is read from memory and sent by the console. The remaining bits in the count are a positive number indicating the number of bytes to load or unload.

The console accepts the command upon receiving the carriage return. The next byte the console receives is the command checksum, which is not echoed. The command checksum is verified by adding all command characters, including the checksum and separating space (but not including the terminating carriage return, rubouts, or characters deleted by rubout), into an 8-bit register initially set to zero. If no errors occur, the result is zero. If the command checksum
is correct, the console responds with the input prompt and either sends
data to the requester or prepares to receive data. If the command checksum
is in error, the console responds with an error message. The intent is to
prevent inadvertent operator entry into a mode where the console is accepting
characters from the keyboard as data, with no escape mechanism possible.

If the command is a load (bit 31 of the count is clear), the console responds
with the input prompt (>>>), then accepts the specified number of bytes of data
for depositing to memory, and an additional byte of received data checksum.
The data is verified by adding all data characters and the checksum character
into an 8-bit register initially set to zero. If the final content of the register is
nonzero, the data or checksum are in error, and the console responds with an
error message.

If the command is a binary unload (bit 31 of the count is set), the console
responds with the input prompt (>>>), followed by the specified number of
bytes of binary data. As each byte is sent, it is added to a checksum register
initially set to zero. At the end of the transmission, the two’s complement of
the low byte of the register is sent.

If the data checksum is incorrect on a load, or if memory or line errors occur
during the transmission of data, the entire transmission is completed, then the
console issues an error message. If an error occurs during loading, the contents
of the memory being loaded are unpredictable.

The console represses echo while it is receiving the data string and checksums.

The console terminates all flow control when it receives the carriage return at
the end of the command line in order to avoid treating flow control characters
from the terminal as valid command line checksums.

You can control the console serial line during a binary unload using control
characters (Ctrl-C, Ctrl-S, Ctrl-O, and so on). You cannot control the console
serial line during a binary load, since all received characters are valid binary
data.

The console has the following timing requirements:
• It must receive data being loaded with a binary load command at a rate of
  at least one byte every 60 seconds.
• It must receive the command checksum that precedes the data within 60
  seconds of the carriage return that terminates the command line.
• It must receive the data checksum within 60 seconds of the last data byte.

If any of these timing requirements are not met, then the console aborts the
transmission by issuing an error message and returning to the console prompt.
The entire command, including the checksum, can be sent to the console as a single burst of characters at the specified character rate of the console serial line. The console is able to receive at least 4 Kbytes of data in a single X command.
3.2.20  ! (Comment)

The comment character (an exclamation point) is used to document command sequences. It can appear anywhere on the command line. All characters following the comment character are ignored.

Format:  

Example:

>>>! The console ignores this line.
>>>
This chapter describes the system initialization, testing, and bootstrap processes that occur at power-up. In addition, the acceptance test procedure to be performed when installing a system or whenever adding or replacing FRUs is described.

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95 and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q-bus and DSSI, will appear on the console and/or printouts from time to time.

4.1 Basic Initialization Flow

On power-up, the firmware identifies the console device, optionally performs a language inquiry, and runs the diagnostics.

The firmware waits for power to stabilize by monitoring SCR<15>(POK). Once power is stable, the firmware verifies that the console battery backup RAM (BBU RAM) is valid (backup battery is charged) by checking SSSCR<31>(BLO). If it is invalid or zero (battery is discharged), the BBU RAM is initialized.

After the battery check, the firmware tries to determine the type of terminal attached to the console serial line. It uses this information to determine if multinational support is appropriate.

The console uses the saved console language if the contents of the BBUJ RAM are valid.
System Initialization and Acceptance Testing (Normal Operation)

4.1 Basic Initialization Flow

If the firmware detects that the contents of the BBU RAM are invalid, the firmware prompts you for the language to be used for displaying the following system messages (if the console terminal supports the multinational character set):

Loading system software.
Failure.
Restarting system software.
Performing normal system tests.
Tests completed.
Normal operation not possible.
Bootfile.
Memory configuration error.
No default boot device has been specified.
Available devices.
Device?
Retrying network bootstrap.

The position of the Break Enable/Disable switch has no effect on these conditions. The firmware will not prompt for a language if the console terminal, such as the VT100, does not support the multinational character set (MCS).

Following a successful diagnostic countdown (see Example 4–1), the console may prompt you for a default boot device.

Example 4–1 Successful Diagnostic Countdown

KAS0-A VX.X, VMB 2.14
Performing normal system tests.
12...71...70...69...68...67...66...65...64...63...62...61...60...59...58...57...
56...55...54...53...52...51...50...49...48...47...46...45...44...43...42...41...
40...39...38...37...36...35...34...33...32...31...30...29...28...27...26...25...
24...23...22...21...20...19...18...17...16...15...14...13...12...11...10...09...
08...07...06...05...04...03...
Tests completed.
>>>
4.2.1 Power-Up Tests for Kernel

In a nonmanufacturing environment where the intended console device is the serial line unit (SLU), the console program performs the following actions at power-up:

1. Checks for POK.
2. Establishes SLU as console device.
3. Prints banner message.
   
   The banner message contains the processor name, the version of the firmware, and the version of VMB. The letter code in the firmware version indicates if the firmware is pre-field test, field test, or official release. The first digit indicates the major release number and the trailing digit indicates the minor release number (Figure 4–1).

**Figure 4–1 Console Banner**

```
KA52-A V n.n, VMB n.n
   \-- minor release of VMB
          \-- major release of VMB
               \-- minor release of firmware
                    \-- major release of firmware
                         \-- type of release: X - engineering release
                                      T - field test release
                                      V - volume release
               \-- processor type
```

4. Displays language inquiry menu on console if console supports multinational character set (MCS) and any of the following are true:
   - Battery is dead.
   - Contents of SSC RAM are invalid.

5. Calls the diagnostic executive (DE) with Test Code = 0.
   a. DE executes script A1 (Tests system module and memory).
System Initialization and Acceptance Testing (Normal Operation)
4.2 Power-On Self-Tests (POST)

While the diagnostics are running, the LEDs display a test code. A different countdown appears on the console terminal. Refer to Table 5-4 for a complete explanation of the power-up test display. Table 4-1 lists the LED codes and the associated actions performed at power-up. Example 4-2 shows a successful power-up to a list of bootable devices.

b. DE passes control back to the console program.

6. Issues end message and >>> prompt.

<table>
<thead>
<tr>
<th>LED Value</th>
<th>Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>Initial state on power-up, no code has executed</td>
</tr>
<tr>
<td>E</td>
<td>Entered ROM space, some instructions have executed</td>
</tr>
<tr>
<td>D</td>
<td>Waiting for power to stabilize (POK)</td>
</tr>
<tr>
<td>C</td>
<td>SSC RAM, SSC registers, and ROM checksum tests</td>
</tr>
<tr>
<td>B</td>
<td>O-bit memory, interval timer, and virtual mode tests</td>
</tr>
<tr>
<td>A</td>
<td>FPA tests</td>
</tr>
<tr>
<td>9</td>
<td>Backup cache tests</td>
</tr>
<tr>
<td>8</td>
<td>NMC, NCA, memory, and I/O interaction tests</td>
</tr>
<tr>
<td>7</td>
<td>CQBIC, SYNC, and ASYNC tests</td>
</tr>
<tr>
<td>6</td>
<td>Console and QUART tests</td>
</tr>
<tr>
<td>5</td>
<td>SCSI tests</td>
</tr>
<tr>
<td>4</td>
<td>SGEC Ethernet subsystem tests</td>
</tr>
<tr>
<td>3</td>
<td>“Console I/O” mode</td>
</tr>
<tr>
<td>2</td>
<td>Control passed to VMB</td>
</tr>
<tr>
<td>1</td>
<td>Control passed to secondary bootstrap</td>
</tr>
<tr>
<td>0</td>
<td>“Program I/O” mode, control passed to operating system</td>
</tr>
</tbody>
</table>
Example 4-2  Successful Power-Up to List of Bootable Devices

KA50-A VX.X, VMB 2.14
Performing normal system tests.
72..71..70..69..68..67..66..65..64..63..62..61..60..59..58..57..
56..55..54..53..52..51..50..49..48..47..46..45..44..43..42..41..
40..39..38..37..36..35..34..33..32..31..30..29..28..27..26..25..
24..23..22..21..20..19..18..17..16..15..14..13..12..11..10..09..
08..07..06..05..04..03..
Tests completed.
Loading system software.
No default boot device has been specified.
Available devices.
-DIA0 (RF73)
-DIA1 (RF73)
-MIA5 (TF85)
-EZAO (08-00-2B-06-10-42)
Device? [EZA0]:

4.2.2 Power-Up Tests for Mass Storage Devices

An RZ-series ISE may fail either during initial power-up or during normal operation. In both cases, the failure is indicated by the lighting of the red fault LED on the drive's front panel. The ISE also has a red fault LED, but it is not visible from the outside of the system enclosure.

If the drive is unable to execute the Power-On Self-Test (POST) successfully, the red fault LED remains lit and the ready LED does not come on, or both LEDs remain on.

POST is also used to handle two types of error conditions in the drive:

- **Controller errors** are caused by the hardware associated with the controller function of the drive module. A controller error is fatal to the operation of the drive, since the controller cannot establish a logical connection to the host. The red fault LED lights. If this occurs, replace the drive module.

- **Drive errors** are caused by the hardware associated with the drive control function of the drive module. These errors are not fatal to the drive, since the drive can establish a logical connection and report the error to the host. Both LEDs go out for about 1 second, then the red fault LED lights.
4.3 CPU ROM-Based Diagnostics

The KA50/51/55/56 ROM-based diagnostic facility is the primary diagnostic tool for troubleshooting and testing of the CPU, memory, and Ethernet. ROM-based diagnostics have significant advantages:

- Load time is virtually nonexistent.
- The boot path is more reliable.
- Diagnosis is done in a more primitive state.

The ROM-based diagnostics can detect failures in field-replaceable units (FRUs) other than the CPU module. For example, they can isolate to two memory SIMMS. (Table 5–4 lists the FRUs indicated by ROM-based diagnostic error messages.)

The diagnostics run automatically on power-up. While the diagnostics are running, the LED displays a hexadecimal number; while booting the operating system, 2 through 0 display.

The ROM-based diagnostics are a collection of individual tests with parameters that you can specify. A data structure called a script points to the tests (see Section 4.3.2). There are several field and manufacturing scripts.

A program called the diagnostic executive determines which of the available scripts to invoke. The script sequence varies if the system is in the manufacturing environment. The diagnostic executive interprets the script to determine what tests to run, the correct order to run the tests, and the correct parameters to use for each test.

The diagnostic executive also controls tests so that errors can be detected and reported. It ensures that when the tests are run, the machine is left in a consistent and well-defined state.

4.3.1 Diagnostic Tests

Example 4–3 shows a list of the ROM-based tests and utilities. To get this listing, enter T 9E at the console prompt (T is the abbreviation of TEST). The column headings have the following meanings:

<table>
<thead>
<tr>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base addresses shown in this document may not be the same as the addresses you see when you run T 9E. Run T 9E to get a list of actual addresses. See Example 4–3.</td>
</tr>
</tbody>
</table>
System Initialization and Acceptance Testing (Normal Operation)
4.3 CPU ROM-Based Diagnostics

- Test is the test number or utility code.
- Address is the base address of where the test or utility starts in ROM. If a test fails, entering T FE displays diagnostic state to the console. You can subtract the base address of the failing test from the last_exception_pc to find the index into the failing test's diagnostic listing.
- Name is a brief description of the test or utility.
- Parameters shows the parameters for each diagnostic test or utility. These parameters are encoded in ROM and are provided by the diagnostic executive. Tests accept up to 10 parameters. The asterisks (*) represent parameters that are used by the tests but that you cannot specify individually. These parameters are displayed in error messages, each one preceded by identifiers P1 through P10.
## System Initialization and Acceptance Testing (Normal Operation)

### 4.3 CPU ROM-Based Diagnostics

**Example 4-3  Test 9E**

<table>
<thead>
<tr>
<th>#</th>
<th>Address</th>
<th>Name</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>20051200</td>
<td>SCB</td>
<td>De executive</td>
<td></td>
</tr>
<tr>
<td>20054128</td>
<td>Memory_Init_Bitmap</td>
<td>*** mark Hard_SBEs ***</td>
<td></td>
</tr>
<tr>
<td>20065A9C</td>
<td>Memory_Setup_CSRs</td>
<td>***************</td>
<td></td>
</tr>
<tr>
<td>20065288</td>
<td>NMC Registers</td>
<td>***************</td>
<td></td>
</tr>
<tr>
<td>20065440</td>
<td>NMC Powerup</td>
<td>**</td>
<td></td>
</tr>
<tr>
<td>2005D6B0</td>
<td>SSC ROM</td>
<td>***</td>
<td></td>
</tr>
<tr>
<td>200652F4</td>
<td>B_Cache диагоме</td>
<td>bypass_test_mask ***************</td>
<td></td>
</tr>
<tr>
<td>200651EC</td>
<td>Cache w Memory</td>
<td>bypass_test_mask ***************</td>
<td></td>
</tr>
<tr>
<td>200651F4</td>
<td>Memory Count pages</td>
<td>SIMM_set0 SIMM_set1 Soft errs_allowed *****</td>
<td></td>
</tr>
<tr>
<td>200581F9</td>
<td>Board Reset</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2005B6F0</td>
<td>Chk for Interrupts</td>
<td>***************</td>
<td></td>
</tr>
<tr>
<td>20065B84</td>
<td>P_Cache диагоме</td>
<td>bypass_test_mask ***************</td>
<td></td>
</tr>
<tr>
<td>20065B84</td>
<td>Memory Refresh</td>
<td>start_a end incr cont_on_err time_seconds *****</td>
<td></td>
</tr>
<tr>
<td>20065B24</td>
<td>Memory Addr shorts</td>
<td>start_add end add * cont_on_err pat2 pat3 ****</td>
<td></td>
</tr>
<tr>
<td>20065B24</td>
<td>Memory ECC_SBEs</td>
<td>start_add end add incr cont_on_err *****</td>
<td></td>
</tr>
<tr>
<td>20065B24</td>
<td>Memory Byte Errors</td>
<td>start_add end add incr cont_on_err *****</td>
<td></td>
</tr>
<tr>
<td>20065B70</td>
<td>Memory ECC Logic</td>
<td>start_add end add incr cont_on_err *****</td>
<td></td>
</tr>
<tr>
<td>20065B14</td>
<td>Memory Address</td>
<td>start_add end add incr cont_on_err *****</td>
<td></td>
</tr>
<tr>
<td>20065B10</td>
<td>Memory Byte</td>
<td>start_add end add incr cont_on_err *****</td>
<td></td>
</tr>
<tr>
<td>20065B10</td>
<td>Memory Data</td>
<td>start_add end add incr cont_on_err *****</td>
<td></td>
</tr>
<tr>
<td>2005C408</td>
<td>FPA</td>
<td>***************</td>
<td></td>
</tr>
<tr>
<td>2005C8C4</td>
<td>SSC Prog timers</td>
<td>which timer wait time us ***</td>
<td></td>
</tr>
<tr>
<td>2005C8B8</td>
<td>SSC TOY Clock</td>
<td>repeat test 250ms ea Tolerance ***</td>
<td></td>
</tr>
<tr>
<td>2005C008</td>
<td>Virtual Mode</td>
<td>***************</td>
<td></td>
</tr>
<tr>
<td>2005C074</td>
<td>Interval Timer</td>
<td>*****</td>
<td></td>
</tr>
<tr>
<td>20060100</td>
<td>SHAC RESET</td>
<td>port_number time_secs not pres</td>
<td></td>
</tr>
<tr>
<td>200602AC</td>
<td>SHAC LFBCK ASSIST</td>
<td>time_secs **</td>
<td></td>
</tr>
<tr>
<td>2006682C</td>
<td>SHAC</td>
<td>bypass_test_mask ***************</td>
<td></td>
</tr>
<tr>
<td>20065524</td>
<td>SHAC loopback_type no_ram_tests *****</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2005D9C</td>
<td>QDSS any</td>
<td>input csr selftest_r0 selftest_r1 *****</td>
<td></td>
</tr>
<tr>
<td>20065B84</td>
<td>QBIC memory</td>
<td>bypass_test_mask ***************</td>
<td></td>
</tr>
<tr>
<td>2005D5D0</td>
<td>Qbus MSCP</td>
<td>IP csr********</td>
<td></td>
</tr>
<tr>
<td>2005D7AC</td>
<td>Qbus DELQ</td>
<td>device num addr ****</td>
<td></td>
</tr>
<tr>
<td>20055700</td>
<td>QZA Intipbck1</td>
<td>controller_number ***********</td>
<td></td>
</tr>
<tr>
<td>2005A7C4</td>
<td>QZA Intipbck2</td>
<td>controller_number ***********</td>
<td></td>
</tr>
<tr>
<td>2005B7C</td>
<td>QZA memory</td>
<td>incr test_pattern controller_number ***********</td>
<td></td>
</tr>
<tr>
<td>2005C714</td>
<td>QZA DMA</td>
<td>controller_number main_mem_buf ***********</td>
<td></td>
</tr>
<tr>
<td>2005C7C</td>
<td>QBIC registers</td>
<td>*</td>
<td></td>
</tr>
<tr>
<td>2005C7BA</td>
<td>QBIC powerup</td>
<td>**</td>
<td></td>
</tr>
<tr>
<td>20065644</td>
<td>Flush Ena Caches</td>
<td>dis_flush_VIC dis_flush_BC dis_flush_PC</td>
<td></td>
</tr>
<tr>
<td>20065C4B</td>
<td>INTERACTION</td>
<td>pass count disable_device ****</td>
<td></td>
</tr>
<tr>
<td>200654DC</td>
<td>Init memory</td>
<td>***</td>
<td></td>
</tr>
<tr>
<td>2005C8B0</td>
<td>List CPU registers</td>
<td>*</td>
<td></td>
</tr>
<tr>
<td>2005E660</td>
<td>Utility</td>
<td>Modify CPU type ***********</td>
<td></td>
</tr>
<tr>
<td>2005C4F0</td>
<td>List diagnostics</td>
<td>script_number *</td>
<td></td>
</tr>
<tr>
<td>20061610</td>
<td>Create A0_Script</td>
<td>***************</td>
<td></td>
</tr>
</tbody>
</table>

(continued on next page)
System Initialization and Acceptance Testing (Normal Operation)
4.3 CPU ROM-Based Diagnostics

<table>
<thead>
<tr>
<th>Example 4–3 (Cont.) Test 9E</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1 20058F8 SSC RAM Data</td>
</tr>
<tr>
<td>C2 20058F8 SSC RAM Data Addr</td>
</tr>
<tr>
<td>C5 2005F814 SSC registers</td>
</tr>
<tr>
<td>C6 20058120 SSC powerup</td>
</tr>
<tr>
<td>D0 20068C8 V Cache diag mode bypass test mask *********</td>
</tr>
<tr>
<td>D2 200660C8 O Bit diag mode bypass test mask *********</td>
</tr>
<tr>
<td>DA 20068FDC Panic Flush Cache **********</td>
</tr>
<tr>
<td>DB 20066908 Speed print speed *********</td>
</tr>
<tr>
<td>DC 200650C8 NO Memory present *</td>
</tr>
<tr>
<td>DD 20067118 R Cache Data debug start add end add incr *********</td>
</tr>
<tr>
<td>DE 20066CD8 R Cache Tag Debug start add end add incr *********</td>
</tr>
<tr>
<td>DF 200664F0 O BIT DEBUG start add end add incr seq incr ******</td>
</tr>
<tr>
<td>E0 200694D8 SCSI environment reset bus time s *********</td>
</tr>
<tr>
<td>E1 200695D8 SCSI Utility environment util nbr target ID lun ******</td>
</tr>
<tr>
<td>E2 200696A4 SCSI MAP bypass test addr incr data list *********</td>
</tr>
<tr>
<td>E4 20069A60 DZ environment *********</td>
</tr>
<tr>
<td>E8 20069BF0 SYNC environment *********</td>
</tr>
<tr>
<td>E9 20069CC0 SYNC Utility environment *********</td>
</tr>
<tr>
<td>EC 20069DA8 ASYNC environment *********</td>
</tr>
</tbody>
</table>

Scripts

<table>
<thead>
<tr>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0 User defined scripts</td>
</tr>
<tr>
<td>A1 Powerup tests, Functional Verify, continue on error, numeric countdown</td>
</tr>
<tr>
<td>A3 Functional Verify, stop on error, test 1 announcements</td>
</tr>
<tr>
<td>A4 Loop on A3 Functional Verify</td>
</tr>
<tr>
<td>A6 Memory tests, mark only multiple bit errors</td>
</tr>
<tr>
<td>A7 Memory tests</td>
</tr>
<tr>
<td>A8 Memory acceptance tests, mark single and multi-bit errors, call A7</td>
</tr>
<tr>
<td>A9 Memory tests, stop on error</td>
</tr>
<tr>
<td>B2 Extended tests plus BP, then loop</td>
</tr>
<tr>
<td>B5 Extended tests, then loop</td>
</tr>
<tr>
<td>DF DZ, SYNC, ASYNC with loopbacks</td>
</tr>
</tbody>
</table>

Load & start system exerciser

| Customer mode, 2 passes |
| CSSF mode, 2 passes |
| CSSE mode, continuous until °C |
| Manuf mode, continuous until °C |
| TINA mode, continuous until °C |
| Manuf mode, 2 passes |
| CSSF mode, select tests, continuous until °C |
| Manuf mode, select tests, continuous until °C |

User Determined Parameters

Parameters that you can specify are written out, as shown in the following examples:

30 2005C33C Memory_INIT_Bitmap *** mark Hard_SBEs ******
54 20055181 Virtual_Mode **********
System Initialization and Acceptance Testing (Normal Operation)
4.3 CPU ROM-Based Diagnostics

For example, the virtual mode test contains several parameters, but you cannot specify any that appear in the table as asterisks. To run this test individually, enter:

```plaintext
>>>T 54
```

The MEM_bitmap test, for example, accepts 10 parameters, but you can only specify mark_hard_SBEs because the rest are asterisks. To map out solid, single-bit ECC memory errors, type:

```plaintext
>>>T 30 0 0 0 1
```

Even though you cannot change the first three parameters, you need to enter zeros (0) as placeholders. The zeros are placeholders for parameters 1 through 3, which allows the program to parse the command line correctly. The diagnostic executive then provides the proper value for the test.

You enter 1 for parameter 4 to indicate that the test should map out solid, single-bit as well as multibit ECC memory errors. You then terminate the command line by pressing [RETURN]. You do not need to specify parameters 5 through 10; placeholders are needed only for parameters that precede the user-definable parameter.

For the most part tests and scripts can be run without any special setup. If a test or script is run interactively without an intervening power up, such as after a system crash or shutdown, enter the UNJAM and INIT commands before running the tests or script. This will ensure that the CPU is in a well known state. If the commands are not entered, misleading errors may occur.

Other considerations to be aware of when running individual tests or scripts interactively:

- When using the TEST or REPEAT TEST commands, you must specify a test number, test code or script number following the TEST command before pressing [RETURN].
- The memory bitmap and Q–bus scatter-gather map are created in main memory and the memory tests are run with these data structures left intact. Therefore, the upper portion of memory should not be accessed to avoid corrupting these data structures. The location of the maps is displayed using the SHOW MEMORY/FULL command.
4.3.2 Scripts

Most of the tests shown by utility 9E are arranged into scripts. A script is a data structure that points to various tests and defines the order in which they are run. Scripts should be thought of as diagnostic tables—these tables do not contain the actual diagnostic tests themselves, instead scripts simply define what tests or scripts should be run, the order that the tests or scripts should be run, and any input parameters to be parsed by the Diagnostic Executive.

Different scripts can run the same set of tests, but these tests can be run in a different order and/or with different parameters and flags. A script also contains the following information:

- The parameters and flags that need to be passed to the test.
- The locations from which the tests can be run. For example, certain tests can be run only from the FEPROM. Other tests are program-independent code, and can be run from FEPROM or main memory to enhance execution speed.
- What is to be shown, if anything, on the console.
- What is to be shown, if anything, in the LED display.
- What action to take on errors (halt, repeat, continue).

The power-up script runs every time the system is powered on. You can also invoke the power-up script at any time by entering T 0.

Additional scripts are included in the FEPROMs for use in manufacturing and engineering environments. Customer Services personnel can run these scripts and tests individually, using the T command. When doing so, note that certain tests may be dependent upon a state set up from a previous test. For this reason, use the UNJAM and INITIALIZE commands before running an individual test. You do not need these commands on system power-up because the system power-up leaves the machine in a defined state.

Customer Services Engineers (CSE) with a detailed knowledge of the system hardware and firmware can also create their own scripts by using the 9F User Script Utility. Table 4–2 lists the scripts available to Customer Services.

System Initialization and Acceptance Testing (Normal Operation) 4–11
# System Initialization and Acceptance Testing (Normal Operation)
## 4.3 CPU ROM-Based Diagnostics

<table>
<thead>
<tr>
<th>Script</th>
<th>Enter with TEST Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>A0</td>
<td>Runs user-defined script. Enter T 9F to create.</td>
</tr>
<tr>
<td>A1</td>
<td>A1, 0</td>
<td>Primary power-up script; builds memory bitmap; marks hard single-bit errors and multi-bit errors. Continues or error.</td>
</tr>
<tr>
<td>A3</td>
<td>A3, A4</td>
<td>Runs power-up tests, halts on first error.</td>
</tr>
<tr>
<td>A6</td>
<td>A6</td>
<td>Memory test script; initializes memory bitmap and marks only multiple bit errors.</td>
</tr>
<tr>
<td>A7</td>
<td>A7, A8</td>
<td>Memory test portion invoked by script A8. Reruns the memory tests without rebuilding and reinitializing the bitmap. Run script A8 once before running script A7 separately to allow mapping out of both single-bit and double-bit main memory ECC errors.</td>
</tr>
<tr>
<td>A8</td>
<td>A8</td>
<td>Memory acceptance. Running script A8 with script A7 tests main memory more extensively. It enables hard single-bit and multibit main memory ECC errors to be marked bad in the bitmap. Invokes script A7 when it has completed its tests.</td>
</tr>
<tr>
<td>A9</td>
<td>A9</td>
<td>Memory tests. Halts and reports the first error. Does not reset the bitmap or busmap. It is a quick way to specify which test caused a failure when a hard error is present.</td>
</tr>
<tr>
<td>AD</td>
<td>AD</td>
<td>Console program. Runs memory tests, marks bitmap, resets busmap, and resets caches. Calls script AE.</td>
</tr>
<tr>
<td>AE</td>
<td>AE, AD</td>
<td>Console program. Resets memory CSRs and resets caches. Also called by the INIT command.</td>
</tr>
<tr>
<td>AF</td>
<td>AF</td>
<td>Console program. Resets busmap and resets caches.</td>
</tr>
<tr>
<td>B2(^2)</td>
<td>B2</td>
<td>Runs extended tests, calls the BF script, then loops. Press [Ctrl] C to exit.</td>
</tr>
<tr>
<td>B5</td>
<td>B5</td>
<td>Runs extended tests, then loops. Press [Ctrl] C to exit.</td>
</tr>
<tr>
<td>BF(^2)</td>
<td>BF</td>
<td>Runs tests requiring loopback connectors for QUART, SYNC, and, ASYNC options if present. Press [Ctrl] C to exit.</td>
</tr>
</tbody>
</table>

\(^1\)Scripts AD, AE, and AF exist primarily for console program; error displays and progress messages are suppressed (not recommended for CSE use).

\(^2\)B2 and BF require loopback connectors.
4.4 Basic Acceptance Test Procedure

Perform the acceptance testing procedure listed below, after installing a system, or whenever adding or replacing the following:

- CPU module
- MS44 memory SIMM
- SCSI device
- SYNC device
- ASYNC device

1. Run two error-free passes of the power-up scripts by entering the following command:

```
>>>T B5
```

Script B5 will halt on an error so that the error message will not scroll off the screen.

Press [Ctrl+C] to terminate the scripts. Refer to Chapter 5 if failures occur.

To check the memory configuration and to ensure there are no bad pages, enter the following command line:

```
>>>SHOW MEM/FULL
```

16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 00000000 to 00FFFFFF, 16MB, 32768 good pages, 0 bad pages
Total of 16MB, 32768 good pages, 0 bad pages, 104 reserved pages

Memory Bitmap
-000F3000 to 00FF3FFF, 8 pages

Console Scratch Area
-00FF4000 to 00FF7FFF, 32 pages

Scan of Bad Pages

Q-bus Map
-01FF8000 to 01FFFF00, 64 pages

Scan of Bad Pages

The Q22–bus map always spans the top 32 Kbytes of good memory. The memory bitmap always spans two pages (1 Kbyte) for each 4 Mbytes of memory configured. Each bit within the memory bit map represents a page of memory.

To identify registers and register bit fields, see the KA50/51/55/56 CPU Technical Manual.
System Initialization and Acceptance Testing (Normal Operation)
4.4 Basic Acceptance Test Procedure

Examine MEMCON 0–1 to verify the memory configuration. Each pair of MEMCONs maps one memory module as follows:

MEMCON0: Set 0; 0A, 0B, 0C, 0D
MEMCON1: Set 1; 1E, 1F, 1G, 1H

4.5 Machine State on Power-Up

This section describes the state of the kernel after a power-up halt.

The descriptions in this section assume the system has just powered-up and the power-up diagnostics have successfully completed. The state of the machine is not defined if individual diagnostics are run or for any other halts other than a power-up halt (SAVPSL<13:8>(RESTART_CODE) = 3). Refer to Appendix D for a description of the normal state of CPU configurable bits following completion of power-up tests.

4.6 Main Memory Layout and State

Main memory is tested and initialized by the firmware on power-up. Figure 4–2 is a diagram of how main memory is partitioned after diagnostics.
4.6.1 Reserved Main Memory

In order to build the scatter/gather map and the bitmap, the firmware attempts to find a physically contiguous page-aligned 1M byte block of memory at the highest possible address.

Of the 1M byte, the upper 32 KB is dedicated to the Q22–bus scatter/gather map, as shown in Figure 4–2. Of the lower portion, up to 32K bytes at the bottom of the block is allocated to the Page Frame Number (PFN) bitmap. The size of the PFN bitmap is dependent on the extent of physical memory. Each bit in the bitmap maps one page (512 bytes) of memory. The remainder of the block between the bitmap and scatter/gather map (minimally 16 KB) is allocated for the firmware.

4.6.1.1 PFN Bitmap

The PFN bitmap is a data structure that indicates which pages in memory are deemed usable by operating systems. The bitmap is built by the diagnostics as a side effect of the memory tests on power-up. The bitmap always starts on a page boundary. The bitmap requires 1 KB for every 4 MB of main memory, hence, a 8 MB system requires 2 KB, 16 MB requires 4 KB, 32 MB requires 8 KB, and a 64 MB requires 16 KB. There may be memory above the bitmap which has both good and bad pages.
System Initialization and Acceptance Testing (Normal Operation)

4.6 Main Memory Layout and State

Each bit in thePFN bitmap corresponds to a page in main memory. There is a one to one correspondence between a page frame number (origin 0) and a bit index in the bitmap. A one in the bitmap indicates that the page is "good" and can be used. A zero indicates that the page is "bad" and should not be used.

The PFN bitmap is protected by a checksum stored in the NVRAM. The checksum is a simple byte wide, two's complement checksum. The sum of all bytes in the bitmap and the bitmap checksum should result in zero.

4.6.1.2 Scatter/Gather Map

On power-up, the scatter/gather map is initialized by the firmware to map to the first 4M bytes of main memory. Main memory pages will not be mapped if there is a corresponding page in Q22–bus memory.

On a processor halt other than power-up, the contents of the scatter/gather map is undefined, and is dependent on operating system usage.

Operating systems should not move the location of the scatter/gather map, and should access the map only on aligned longwords through the local I/O space of 20088000 to 2008FFFF, inclusive. The Q22–bus map base register (QMBR), is set up by the firmware to point to this area, and should not be changed by software.

4.6.1.3 Firmware "Scratch Memory"

This section of memory is reserved for the firmware. However, it is only used after successful execution of the memory diagnostics and initialization of the PFN bitmap and scatter/gather map. This memory is primarily used for diagnostic purposes.

4.6.2 Contents of Main Memory

The contents of main memory are undefined after the diagnostics have run. Typically, nonzero test patterns will be left in memory.

The diagnostics will "scrub" all of main memory, so that no power-up induced errors remain in the memory system. On the KA50/51/55/56 memory subsystem, the state of the ECC bits and the data bits are undefined on initial power-up. This can result in single and multiple bit errors if the locations are read before written, because the ECC bits are not in agreement with their corresponding data bits. An aligned longword write to every location (done by diagnostics) eliminates all power-up induced errors.
4.6.3 Memory Controller Registers

The SHOW MEMORY command defines the mapping of addresses to specific SIMM sets as follows:

- MEMCON0 is used with SIMM bank 0 (the 0A, 0B, 0C, and 0D memory slots)
- MEMCON1 is used with SIMM bank 1 (the 1E, 1F, 1G, and 1H memory slots)

Additional information should be captured from the NMCDSR, MOAMR, MSER, and MEAR as needed.

4.6.4 On-Chip and Backup Caches

All three caches are tested.

4.6.5 Translation Buffer

The CPU translation buffer is tested by diagnostics on power-up, but not used by the firmware because it runs in physical mode. The translation buffer can be invalidated by using PR$_TBIA, IPR 57.

4.6.6 Halt-Protected Space

On the KA50/51/55/56, halt-protected space spans the first half of the 512K byte FEPROM from 20040000 to 2007FFFF. The second half of the FEPROM has data which is loaded into memory and run.

The firmware always runs in halt-protected space. When passing control to the bootstrap, the firmware exits the halt-protected space, so if halts are enabled, and the halt line is asserted, the processor will then halt before booting.

4.7 Operating System Bootstrap

Bootstrapping is the process by which an operating system loads and assumes control of the system. The KA50/51/55/56 supports bootstrap of the VAX/OpenVMS and VAXELN operating systems. Additionally, the KA50/51/55 will boot MDM diagnostics and any user application image which conforms to the boot formats described herein.

On the KA50/51/55/56 a bootstrap occurs whenever a BOOT command is issued at the console or whenever the processor halts and the conditions specified in Table G–1 for automatic bootstrap are satisfied.
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstrap

4.7.1 Preparing for the Bootstrap

Prior to dispatching to the primary bootstrap (VMB), the firmware initializes the system to a known state. The initialization sequence follows:

1. Check the console program mailbox "bootstrap in progress" bit (CPMBX<2>(BIP)). If it is set, bootstrap fails.

2. If this is an automatic bootstrap, display the message "Loading system software." on the console terminal.

3. Set CPMBX<2>(BIP).

4. Validate the Page Frame Number (PFN) bitmap. If PFN bitmap checksum is invalid, then:
   a. Perform an UNJAM.
   b. Perform an INIT.
   c. Retest memory and rebuild PFN bitmap.

5. Validate the boot device name. If none exists, supply a list of available devices and prompt user for a device. If no device is entered within 30 seconds, use EZA0.

6. Write a form of this BOOT request including the active boot flags and boot device on the console, for example "(BOOT/R5:0 DUA0)".

7. Initialize the Q22–bus scatter/gather map.
   a. Set IPCR<8>(AUX_HLT).
   b. Clear IPCR<5>(LMEA).
   c. Perform an UNJAM.
   d. Perform an INIT.
   e. If an arbiter, map all vacant Q22–bus pages to the corresponding page in local memory and validate each entry if that page is "good".
   f. Set IPCR<5>(LMEA).

8. Search for a 128K byte contiguous block of good memory as defined by the PFN bitmap. If 128K bytes cannot be found, the bootstrap fails.

9. Initialize the general purpose registers as follows:
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstrap

R0          Address of descriptor of boot device name; 0 if none specified
R2          Length of PFN bitmap in bytes
R3          Address of PFN bitmap
R4          Time-of-day of bootstrap from PR$_{TODR}$
R5          Boot flags
R10         Halt PC value
R11         Halt PSL value (without halt code and map enable)
AP           Halt code
SP           Base of 128-Kbyte good memory block + 512
PC           Base of 128-Kbyte good memory block + 512
R1, R6, R7, R8,  0
R9, FP

10. Copy the VMB image from FEPROM to local memory beginning at the base of the 128 KB good memory block + 512.

11. Exit from the firmware to memory resident VMB.

On entry to VMB the processor is running at IPL 31 on the interrupt stack with memory management disabled. Also, local memory is partitioned as shown in Figure 4–3.
4.7.2 Primary Bootstrap Procedures (VMB)

Virtual Memory Boot (VMB) is the primary bootstrap for booting VAX processors. On the KA50/51/55/56 module, VMB is resident in the firmware and is copied into main memory before control is transferred to it. VMB then loads the secondary bootstrap image and transfers control to it.

In certain cases, such as VAXELN, VMB actually loads the operating system directly. However, for the purpose of this discussion "secondary bootstrap" refers to any VMB loadable image.
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstrap

VMB inherits a well defined environment and is responsible for further initialization. The following summarizes the operation of VMB.

1. Initialize a two-page SCB on the first-page boundary above VMB.
2. Allocate a three-page stack above the SCB.
3. Initialize the Restart Parameter Block (RPB).
4. Initialize the secondary bootstrap argument list.
5. If not a PROM boot, locate a minimum of three consecutive valid QMRs.
6. Write "2" to the diagnostic LEDs and display "2.." on the console to indicate that VMB is searching for the device.
7. Optionally, solicit from the console a "Bootfile: " name.
8. Write the name of the boot device from which VMB will attempt to boot on the console, for example, "-DIA0".
9. Copy the secondary bootstrap from the boot device into local memory above the stack. If this fails, the bootstrap fails.
10. Write "1" to the diagnostic LEDs and display "1.." on the console to indicate that VMB has found the secondary bootstrap image on the boot device and has loaded the image into local memory.
11. Clear CPMBX<2> (BIP) and CPMBX<3> (RIP).
12. Write "0" to the diagnostic LEDs and display "0.." on the console to indicate that VMB is now transferring control to the loaded image.
13. Transfer control to the loaded image with the following register usage.

<table>
<thead>
<tr>
<th>Register</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>R5</td>
<td>Transfer address in secondary bootstrap image</td>
</tr>
<tr>
<td>R10</td>
<td>Base address of secondary bootstrap memory</td>
</tr>
<tr>
<td>R11</td>
<td>Base address of RPB</td>
</tr>
<tr>
<td>AP</td>
<td>Base address of secondary boot parameter block</td>
</tr>
<tr>
<td>SP</td>
<td>Base address of secondary boot parameter block</td>
</tr>
</tbody>
</table>
In the event that an operating system has an extraordinarily large secondary bootstrap which overflows the 128 KB of "good" memory, VMB loads the remainder of the image in memory above the "good" block. However, if there are not enough contiguous "good" pages above the block to load the remainder of the image, the bootstrap fails.
4.7.3 Device Dependent Secondary Bootstrap Procedures

The following sections describe the various device dependent boot procedures.

4.7.3.1 Disk and Tape Bootstrap Procedure

The disk and tape bootstrap supports Files–11 lookup (supporting only the ODS level 2 file structure) or the boot block mechanism (used in PROM boot also). Of the standard DEC operating systems, OpenVMS and ELN use the Files–11 bootstrap procedure, and Ultrix-32 uses the boot block mechanism.

VMB first attempts a Files–11 lookup, unless the RPB$V_BBLOCK boot flag is set. If VMB determines that the designated boot disk is a Files–11 volume, it searches the volume for the designated boot program, usually [SYS0.SYSEXE]SYSBOOT.EXE. However, VMB can request a diagnostic image or prompt the user for an alternate file specification. If the boot image cannot be found, VMB fails.

If the volume is not a Files–11 volume or the RPB$V_BBLOCK boot flag was set, the boot block mechanism proceeds as follows:

1. Read logical block 0 of the selected boot device (this is the boot block).
2. Validate that the contents of the boot block conform to the boot block format (see below).
3. Use the boot block to find and read in the secondary bootstrap.
4. Transfer control to the secondary bootstrap image, just as for a Files–11 boot.

The format of the boot block must conform to that shown in Figure 4–5.
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstrap

Figure 4-5 Boot Block Format

<table>
<thead>
<tr>
<th></th>
<th>31</th>
<th>24</th>
<th>23</th>
<th>16</th>
<th>15</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BB-0:</td>
<td></td>
<td>n</td>
<td>1</td>
<td>any value</td>
<td>low LBN</td>
<td>high LBN</td>
</tr>
</tbody>
</table>

(The next segment is also used as a PROM "signature block.")

<table>
<thead>
<tr>
<th></th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BB+(2*n)+0:</td>
<td>CHK</td>
</tr>
<tr>
<td></td>
<td>any value, most likely 0</td>
</tr>
<tr>
<td>BB+(2*n)+8:</td>
<td>size in blocks of the image</td>
</tr>
<tr>
<td>BB+(2*n)+12:</td>
<td>load offset</td>
</tr>
<tr>
<td>BB+(2*n)+16:</td>
<td>offset into image to start</td>
</tr>
<tr>
<td>BB+(2*n)+20:</td>
<td>sum of the previous three longwords</td>
</tr>
</tbody>
</table>

Where:
1) the 18 (hex) indicates this is a VAX instruction set
2) 18 (hex) + "k" = the one's complement if "CHK"

4.7.3.2 MOP Ethernet Functions and Network Bootstrap Procedure

Whenever a network bootstrap is selected on the KA50/51/55/56, the VMB code makes continuous attempts to boot from the network. VMB uses the DNA Maintenance Operations Protocol (MOP) as the transport protocol for network bootstraps and other network operations. Once a network boot has been invoked, VMB turns on the designated network link and repeats load attempt, until either a successful boot occurs, a fatal controller error occurs, or VMB is halted from the operator console.

The KA50/51/55/56 supports the load of a standard operating system, a diagnostic image, or a user-designated program via network bootstraps. The default image is the standard operating system, however, a user may select an alternate image by setting either the RPB$V_DIAG bit or the RPB$V_SOLICT bit in the boot flag longword R5. Note that the RPB$V_SOLICT bit has precedence over the RPB$V_DIAG bit. Hence, if both bits are set, then the solicited file is requested.
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstrap

Note

VMB accepts a maximum 39 characters for a file specification for solicited boots. However, MOP V3 only supports a 15-character file name. If the network server is running the OpenVMS operating system, the following defaults apply to the file specification: the directory MOM$LOAD:, and the extension .SYS. Therefore, the file specification need only consist of the filename if the default directory and extension attributes are used.

The KA50/51/55/56 VMB uses the MOP program load sequence for bootstrapping the module and the MOP "dump/load" protocol type for load related message exchanges. The types of MOP message used in the exchange are listed in Table 4–3 and Table 4–4.
### System Initialization and Acceptance Testing (Normal Operation)

#### 4.7 Operating System Bootstrap

#### Table 4-3 Network Maintenance Operations Summary

<table>
<thead>
<tr>
<th>Function</th>
<th>Role</th>
<th>Transmit</th>
<th>Receive</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MOP Ethernet and IEEE 802.3 Messages&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dump</td>
<td>Requester</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Server</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Load</td>
<td>Requester</td>
<td>REQ_PROGRAM&lt;sup&gt;2&lt;/sup&gt; to solicit</td>
<td>VOLUNTEER</td>
</tr>
<tr>
<td></td>
<td></td>
<td>REQ_MEM_LOAD</td>
<td>MEM_LOAD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>or</td>
<td>MEM_LOAD_w_XFER</td>
</tr>
<tr>
<td></td>
<td></td>
<td>or</td>
<td>PARAM_LOAD_w_XFER</td>
</tr>
<tr>
<td></td>
<td>Server</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Console</td>
<td>Requester</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Server</td>
<td>COUNTERS</td>
<td>in response to</td>
<td>REQ_COUNTERS</td>
</tr>
<tr>
<td></td>
<td>SYSTEM_ID&lt;sup&gt;3&lt;/sup&gt;</td>
<td>in response to</td>
<td>REQUEST_ID</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>BOOT</td>
</tr>
<tr>
<td>Loopback</td>
<td>Requester</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Server</td>
<td>LOOPED_DATA&lt;sup&gt;4&lt;/sup&gt;</td>
<td>in response to</td>
<td>LOOP_DATA</td>
</tr>
</tbody>
</table>

#### IEEE 802.3 Messages<sup>5</sup>

<table>
<thead>
<tr>
<th>Function</th>
<th>Role</th>
<th>Transmit</th>
<th>Receive</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exchange</td>
<td>Requester</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Server</td>
<td>XID_RSP</td>
<td>in response to</td>
<td>XID_CMD</td>
</tr>
<tr>
<td>Test</td>
<td>Requester</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

---

<sup>1</sup> All unsolicited messages are sent in Ethernet (MOP V3) and IEEE 802.2 (MOP V4), until the MOP version of the server is known. All solicited messages are sent in the format used for the request.

<sup>2</sup>The initial REQ_PROGRAM message is sent to the dumpload multicast address. If an assistance VOLUNTEER message is received, then the responder’s address is used as the destination to repeat the REQ_PROGRAM message and for all subsequent REQ_MEM_LOAD messages.

<sup>3</sup>SYSTEM_ID messages are sent out every 8 to 12 minutes to the remote console multicast address and, on receipt of a REQUEST_ID message, they are sent to the initiator.

<sup>4</sup> LOOPED_DATA messages are sent out in response to LOOP_DATA messages. These messages are actually in Ethernet LOOP TEST format, not in MOP format, and when sent in Ethernet frames, omit the additional length field (padding is disabled).

<sup>5</sup>IEEE 802.2 support of XID and TEST is limited to Class 1 operations.

(continued on next page)
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstraps

Table 4–3 (Cont.) Network Maintenance Operations Summary

<table>
<thead>
<tr>
<th>Function</th>
<th>Role</th>
<th>Transmit</th>
<th>Receive</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>IEEE 802.3 Messages⁵</td>
<td></td>
</tr>
<tr>
<td>Server</td>
<td></td>
<td>TEST_RSP in response to TEST_CMD</td>
<td></td>
</tr>
</tbody>
</table>

⁵IEEE 802.2 support of XID and TEST is limited to Class 1 operations.

Table 4–4 Supported MOP Messages

<table>
<thead>
<tr>
<th>Message Type</th>
<th>Message Fields</th>
</tr>
</thead>
<tbody>
<tr>
<td>DUMP/LOAD</td>
<td></td>
</tr>
</tbody>
</table>

MEM_LOAD_w_XFER
Code  00
Load # nn
Load addr aa-aa-aa-aa
Image data None
Xfer addr aa-aa-aa-aa

MEM_LOAD
Code  02
Load # nn
Load addr aa-aa-aa-aa
Image data dd...

REQ_PROGRAM
Code  08
Device 25 LQA
49 SGEC
Format 01 V3
04 V4
Program 02 Sys
SW ID⁵ C-17¹
C-128²
If C[1] >00 Len
00 No
ID
FF OS
FE
Maint
Procesr 00 Sys
Info (see SYSTEM_ID)

REQ_MEM_LOAD
Code  0A
Load # nn
Error ee

¹MOP V3.0 only.
²MOP x4.0 only.
³Software ID field is loaded from the string stored in the 40-byte field, RPB$T_FILE, of the RPB on a solicited boot.

(continued on next page)
System Initialization and Acceptance Testing (Normal Operation)
4.7 Operating System Bootstrap

Table 4-4 (Cont.) Supported MOP Messages

<table>
<thead>
<tr>
<th>Message Type</th>
<th>Code</th>
<th>Load #</th>
<th>Prm typ</th>
<th>Prm len</th>
<th>Prm val</th>
<th>Xfer addr</th>
</tr>
</thead>
<tbody>
<tr>
<td>PARM_LOAD_w_ XFER</td>
<td>14</td>
<td>nn</td>
<td>01</td>
<td>I-16</td>
<td>Target name (^1)</td>
<td>aa-aa-aa-aa</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>02</td>
<td>I-06</td>
<td>Target addr (^1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>03</td>
<td>I-16</td>
<td>Host name (^1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>04</td>
<td>I-06</td>
<td>Host addr (^1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>05</td>
<td>0A</td>
<td>Host time (^1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>06</td>
<td>08</td>
<td>Host time (^2)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00</td>
<td>End</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VOLUNTEER**

| Code | 03 |

**REMOTE CONSOLE**

<table>
<thead>
<tr>
<th>REQUEST_ID</th>
<th>Code</th>
<th>Rsrvd</th>
<th>Recpt #</th>
<th>Info type</th>
<th>Info len</th>
<th>Info value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>05</td>
<td>xx</td>
<td>nn-nn</td>
<td>01-00 Version</td>
<td>03</td>
<td>04-00-00</td>
</tr>
<tr>
<td>SYSTEM_ID</td>
<td>Code</td>
<td>Rsrvd</td>
<td>Recpt #</td>
<td>Info type</td>
<td>Info len</td>
<td>Info value</td>
</tr>
<tr>
<td></td>
<td>07</td>
<td>xx</td>
<td>nn-nn</td>
<td>02-00 Functions</td>
<td>02</td>
<td>00-59</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>nn-nn</td>
<td>00-00</td>
<td>06</td>
<td>ee-ee-ee-ee-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>07-00</td>
<td>HW addr</td>
<td>01</td>
<td>ee-ee-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>64-00</td>
<td>Device</td>
<td>01</td>
<td>25 or 49</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>90-01</td>
<td>Datalink</td>
<td>01</td>
<td>01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>91-01</td>
<td>Bufr size</td>
<td>02</td>
<td>06-04</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REQ_COUNTERS</td>
<td>Code</td>
<td>Recpt #</td>
<td>Counter block</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>09</td>
<td>nn-nn</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>COUNTERS</td>
<td>Code</td>
<td>Recpt #</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0B</td>
<td>nn-nn</td>
<td>Counter block</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**BOOT**

<table>
<thead>
<tr>
<th>Code</th>
<th>Verification</th>
<th>Process</th>
<th>Control</th>
<th>Dev ID</th>
<th>SW ID (^3)</th>
<th>Script ID (^2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>06</td>
<td>vv-vv-</td>
<td>00 Sys</td>
<td>xx</td>
<td>C-17</td>
<td>(see REQ_ PROGRAM)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>vv-vv-</td>
<td></td>
<td></td>
<td></td>
<td>C-128</td>
<td></td>
</tr>
</tbody>
</table>

---

\(^1\) MOP V3.0 only.

\(^2\) MOP x4.0 only.

\(^3\) Software ID field is loaded from the string stored in the 40-byte field, RPBS_FILE, of the RPB on a solicited boot.

\(^4\) A BOOT message is not verified, because in this context, a boot is already in progress. However, a received BOOT message will cause the boot backoff timer to be reset to its minimum value.

(continued on next page)
VMB, the requester, starts by sending a REQ_PROGRAM message to the MOP 'dump/load' multicast address. It then waits for a response in the form of a VOLUNTEER message from another node on the network, the MOP server. If a response is received, then the destination address is changed from the multicast address to the node address of the server and the same REQ_PROGRAM message is retransmitted to the server as an Acknowledge.

Next, VMB begins sending REQ_MEM_LOAD messages to the server. The server responds with either:

- `MEM_LOAD` message, while there is still more to load.
- `MEM_LOAD_w_XFER`, if it is the end of the image.
- `PARAM_LOAD_w_XFER`, if it is the end of the image and operating system parameters are required.

The "load number" field in the load messages is used to synchronize the load sequence. At the beginning of the exchange, both the requester and server initialize the load number. The requester only increments the load number if a load packet has been successfully received and loaded. This forms the Acknowledge to each exchange. The server will resend a packet with a specific load number, until it sees the load number incremented. The final Acknowledge is sent by the requester and has a load number equivalent to the load number of the appropriate LOAD_w_XFER message + 1.
System Initialization and Acceptance Testing (Normal Operation)

4.7 Operating System Bootstrap

Because the request for load assistance is a MOP "must transact" operation, the network bootstrap continues indefinitely until a volunteer is found. The REQ_PROGRAM message is sent out in bursts of eight at four second intervals, the first four in MOP Version four IEEE 802.3 format and the last four in MOP Version 3 Ethernet format. The backoff period between bursts doubles each cycle from an initial value of four seconds, to eight seconds,... up to a maximum of five minutes. However, to reduce the likelihood of many nodes posting requests in lock-step, a random "jitter" is applied to the backoff period. The actual backoff time is computed as \((.75+.5\cdot RND(x))\cdot BACKOFF\), where \(0 \leq x < 1\).

4.7.3.3 Network "Listening"

While the CPU module is waiting for a load volunteer during bootstrap, it "listens" on the network for other maintenance messages directed to the node and periodically identifies itself at the end of each 8- to 12-minute interval before a bootstrap retry. In particular, this "listener" supplements the Maintenance Operation Protocol (MOP) functions of the VMB load requester typically found in bootstrap firmware and supports:

- A remote console server that generates COUNTERS messages in response to REQ_COUNTERS messages, unsolicited SYSTEM_ID messages every 8 to 12 minutes, and solicited SYSTEM_ID messages in response to REQUEST_ID messages, as well as recognition of BOOT messages.
- A loopback server that responds to Ethernet loopback messages by echoing the message to the requester.
- An IEEE 802.2 responder that replies to both XID and TEST messages.

During network bootstrap operation, the KA50/51/55/56 complies with the requirements defined in the "NI Node Architecture Specification" for a primitive node. The firmware listens only to MOP "Load/Dump", MOP "Remote Console", Ethernet "Loopback Assistance", and IEEE 802.3 XID/TEST messages (listed in Table 4–5) directed to the Ethernet physical address of the node. All other Ethernet protocols are filtered by the network device driver.

The MOP functions and message types, which are supported by the KA50/51/55/56, are summarized in Tables 4–3 and 4–5.
Table 4–5  MOP Multicast Addresses and Protocol Specifiers

<table>
<thead>
<tr>
<th>Function</th>
<th>Address</th>
<th>IEEE Prefix1</th>
<th>Protocol</th>
<th>Owner</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dump/Load</td>
<td>AB-00-00-01-00-00</td>
<td>08-00-2B</td>
<td>60-01</td>
<td>Digital</td>
</tr>
<tr>
<td>Remote console</td>
<td>AB-00-00-02-00-00</td>
<td>08-00-2B</td>
<td>60-02</td>
<td>Digital</td>
</tr>
<tr>
<td>Loopback assistance</td>
<td>CF-00-00-00-00-002</td>
<td>08-00-2B</td>
<td>90-00</td>
<td>Digital</td>
</tr>
</tbody>
</table>

1MOP V4.0 only.
2Not used.

4.8 Operating System Restart

An operating system restart is the process of bringing up the operating system from a known initialization state following a processor halt. This procedure is often called restart or warmstart, and should not be confused with a processor restart which results in firmware entry.

On the KA50/51/55/56, a restart occurs if the conditions specified in Table G–1 are satisfied.

To restart a halted operating system, the firmware searches system memory for the Restart Parameter Block (RPB), a data structure constructed for this purpose by VMB. (Refer to Table C–2 in Appendix C for a detailed description of this data structure.) If a valid RPB is found, the firmware passes control to the operating system at an address specified in the RPB.

The firmware keeps a "restart in progress" (RIP) flag in CPMBX which it uses to avoid repeated attempts to restart a failing operating system. An additional "restart in progress" flag is maintained by the operating system in the RPB.

The firmware uses the following algorithm to restart the operating system:

1. Check CPMBX<3>(RIP). If it is set, restart fails.
2. Print the message "Restarting system software." on the console terminal.
3. Set CPMBX<3>(RIP).
4. Search for a valid RPB. If none is found, restart fails.
5. Check the operating system RPB$L_RSTRTFLG<0>(RIP) flag. If it is set, restart fails.
6. Write "0" on the diagnostic LEDs.
System Initialization and Acceptance Testing (Normal Operation)
4.8 Operating System Restart

7. Dispatch to the restart address, RPB$\_RESTART, with:

SP Physical address of the RPB plus 512
AP Halt code
PSL 041F0000
PR$\_MAPEN 0

If the restart is successful, the operating system must clear CPMBX<3>(RIP).
If restart fails, the firmware prints "Restart failure." on the system console.

4.8.1 Locating the RPB

The RPB is a page-aligned control block which can be identified by the first three longwords. The format of the RPB "signature" is shown in Figure 4–6. (Refer to Table C–2 in Appendix C for a complete description of the RPB.)

Figure 4–6 Locating the Restart Parameter Block

<table>
<thead>
<tr>
<th>Location</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPB +00</td>
<td>Physical address of the RPB</td>
</tr>
<tr>
<td>+04</td>
<td>Physical address of the restart routine</td>
</tr>
<tr>
<td>+08</td>
<td>Checksum of first 31 longwords of restart routine</td>
</tr>
</tbody>
</table>

The firmware uses the following algorithm to find a valid RPB:

1. Search for a page of memory that contains its address in the first longword. If none is found, the search for a valid RPB has failed.

2. Read the second longword in the page (the physical address of the restart routine). If it is not a valid physical address, or if it is zero, return to step 1. The check for zero is necessary to ensure that a page of zeros does not pass the test for a valid RPB.

3. Calculate the 32 bit twos-complement sum (ignoring overflows) of the first 31 longwords of the restart routine. If the sum does not match the third longword of the RPB, return to step 1.

4. A valid RPB has been found.
System Troubleshooting and Diagnostics

This chapter provides troubleshooting information for the two primary diagnostic methods: online, interpreting error logs to isolate the FRU; and offline, interpreting ROM-based diagnostic messages to isolate the FRU.

In addition, the chapter provides information on using MOP Ethernet functions to isolate errors, and interpreting UETP failures.

The chapter concludes with a section on running loopback tests to test the console port and embedded Ethernet ports.

Note

The firmware and diagnosties for MicroVAX 3100 Models 85, 90, 95, and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q–bus and DSSI, may appear on the console and/or printouts from time to time.

5.1 Basic Troubleshooting Flow

Before troubleshooting any system problem, check the site maintenance log for the system’s service history. Be sure to ask the system manager the following questions:

• Has the system been used before and did it work correctly?
• Have changes (changes to hardware, updates to firmware or software) been made to the system recently?
• What is the state of the system—is it on line or off line?

If the system is off line and you are not able to bring it up, use the offline diagnostic tools, such as RBDs, MDM, and LEDs.
System Troubleshooting and Diagnostics
5.1 Basic Troubleshooting Flow

If the system is on line, use the online diagnostic tools, such as error logs, crash dumps, UETP, and other log files.

Four common problems occur when you make a change to the system:

- Incorrect cabling
- Module configuration errors (incorrect CSR addresses and interrupt vectors)
- Incorrect grant continuity
- Incorrect bus node ID plugs

In addition, check the following:

- If you have received error notification using VAXsimPLUS, check the mail messages and error logs as described in Section 5.2.

- If the operating system fails to boot (or appears to fail), check the console terminal screen for an error message. If the terminal displays an error message, see Section 5.3.

- Check the LEDs on the device you suspect is bad. If no errors are indicated by the device LEDs, run the ROM-based diagnostics described in this chapter.

- If the system boots successfully, but a device seems to fail or an intermittent failure occurs, check the error log ([SYSERR]ERRLOG.SYS) as described in Section 5.2.

- For fatal errors, check that the crash dump file exists for further analysis ([ SYSEXE] SYSDUMP.DMP).

- Check other log files, such as OPERATOR.LOG, OPCOM.LOG, SETHOST.LOG, etc. Many of these can be found in the [SYSMGR] account. SETHOST.LOG is useful in comparing the console output with event logs and crash dumps in order to see what the system was doing at the time of the error.

Use the following command to create SETHOST.LOG files, then log into the system account.

$ SET HOST/LOG 0

After logging out this file will reside in the [SYSMGR] account.

If the system is failing in the boot or start-up phase, it may be useful to include the command SET VERIFY in the front of various start-up .COM files to obtain a trace of the start-up commands and procedures.
When troubleshooting, note the status of cables and connectors before you perform each step. Label cables before you disconnect them. This step saves you time and prevents you from introducing new problems.

Most communications modules use floating CSR addresses and interrupt vectors. If you remove a module from the system, you may have to change the addresses and vectors of other modules.

If you change the system configuration, run the CONFIGURE utility at the console I/O prompt (>>>) to determine the CSR addresses and interrupt vectors recommended by Digital.

5.2 Product Fault Management and Symptom-Directed Diagnosis

This section describes how errors are handled by the microcode and software, how the errors are logged, and how, through the Symptom-Directed Diagnosis (SDD) tool, VAXsimPLUS, errors are brought to the attention of the user. This section also provides the service theory used to interpret error logs to isolate the FRU. Interpreting error logs to isolate the FRU is the primary method of diagnosis.

5.2.1 General Exception and Interrupt Handling

This section describes the first step of error notification: the errors are first handled by the microcode and then are dispatched to the OpenVMS error handler.

The kernel uses the NVAX core chipset: NVAX CPU, NVAX Memory Controller (NMC), and NDAL to CDAL adapter (NCA).

Internal errors within the NVAX CPU result in machine check exceptions, through System Control Block (SCB) vector 004, or soft error interrupts at Interrupt Priority Level (IPL) 1A, SCB vector 054 hex.

External errors to the NVAX CPU, which are detected by the NMC or NDAL to CDAL adapter (NCA), usually result in these chips posting an error condition to the NVAX CPU. The NVAX CPU will then generate a machine check exception through SCB vector 004, hard error interrupt, IPL 1D, through SCB vector 060 (hex), or a soft error interrupt through SCB vector 054.

External errors to the NMC and NCA, which are detected by chips on the CDAL busses for transactions which originated by the NVAX CPU, are typically signaled back to the NCA adapter. The NCA adapter will post an error signal back to the NVAX CPU which generates a machine check or high level interrupt.
In the case of Direct Memory Access (DMA) transactions where the NCA or NMC detects the error, the errors are typically signaled back to the CDAL-Bus device, but not posted to the NVAX CPU. In these cases the CDAL-Bus device typically posts a device level interrupt to the NVAX CPU via the NCA. In almost all cases, error state is latched by the NMC and NCA. Although these errors will not result in a machine check exception or high level interrupt (i.e. results in device level IPL 14–17 versus error level IPL 1A, 1D), the OpenVMS machine check handler has a polling routine that will search for this state at one-second intervals. This will result in the host logging a polled error entry.

These conditions cover all of the cases that will eventually be handled by the OpenVMS error handler. The OpenVMS error handler will generate entries that correspond to the machine check exception, hard or soft error interrupt type, or polled error.

5.2.2 OpenVMS Error Handling

Upon detection of a machine check exception, hard error interrupt, soft error interrupt or polled error, the OpenVMS operating system will perform the following actions:

- Snapshot the state of the kernel.
- In most entry points, disable the caches.
- If it is a machine check and if the machine check is recoverable, determine if instruction retry is possible.

Instruction retry is possible if one of the following conditions is true:

- If PCSTS <10>PTE_ER = 0:
  Check that (ISTATE2 <07>VR = 1) or (PSL <27> FPD = 1)
  Otherwise crash the system or process depending on PSL <25:24> Current Mode.
- If PCSTS <10>PTE_ER = 1:
  Check that (ISTATE2 <07>VR = 1) and (PSL <27> FPD = 0) and (PCSTS <09>PTE_ER_WR = 0)
  Otherwise crash the system.

ISTATE2 is a longword in the machine check stack frame at offset (SP)+24; PSL is a longword in the machine check stack frame at offset (SP)+32; VR is the VAX Restart flag; and FPD is the First Part Done flag.

- Check to see if the threshold has been exceeded for various errors (typically the threshold is exceeded if 3 errors occur within a 10 minute interval).
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

- If the threshold has been exceeded for a particular type of cache error, mark a flag that will signify that this resource is to be disabled (the cache will be disabled in most, but not all, cases).
- Update the SYSTAT software register with results of error/fault handling.
- For memory uncorrectable Error Correction Code (ECC) errors:
  - If machine check, mark page bad and attempt to replace page.
  - Fill in MEMCON software register with memory configuration and error status for use in FRU isolation.
- For memory single-bit correctable ECC errors:
  - Fill in Corrected Read Data (CRD) entry FOOTPRINT with set, bank, and syndrome information for use in FRU isolation.
  - Update the CRD entry for time, address range, and count; fill the MEMCON software register with memory configuration information.
  - Scrub memory location for first occurrence of error within a particular footprint. If second or more occurrence within a footprint, mark page bad in hopes that page will be replaced later. Disable soft error logging for 10 minutes if threshold is exceeded.
  - Signify that CRD buffer be logged for the following events: system shutdown (operator shutdown or crash), hard single-cell address within footprint, multiple addresses within footprint, memory uncorrectable ECC error, or CRD buffer full.
- For ownership memory correctable ECC error, scrub location.
- Log error.
- Crash process or system, dependent upon PSL (Current Mode) with a fatal bugcheck for the following situations:
  - Retry is not possible.
  - Memory page could not be replaced for uncorrectable ECC memory error.
  - Uncorrectable tag store ECC errors present in writeback cache.
  - Uncorrectable data store ECC errors present in writeback cache for locations marked as OWNED.
  - Most INT60 errors.
  - Threshold is exceeded (except for cache errors).
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

- A few other errors of the sort considered nonrecoverable are present.
- Disable cache(s) permanently if error threshold is exceeded.
- Flush and re-enable those caches which have been marked as good.
- Clear the error flags.
- Perform Return from Exception or Interrupt (REI) to recover and restart or continue the instruction stream for the following situations:
  - Most INT54 errors.
  - Those INT60 and INT54 errors which result in bad ECC written to a memory location. (These errors can provide clues that the problem is not memory related.)
  - Machine check conditions where instruction retry is possible.
  - Memory uncorrectable ECC error where page replacement is possible and instruction retry is possible.
  - Threshold exceeded (for cache errors only).
  - Return from Subroutine (RSB) and return from all polled errors.

Note
The results of the OpenVMS error handler may be preserved within the operating system session (for example, disabling a cache) but not across reboots.

Although the system can recover with cache disabled, the system performance will be degraded, since access time increases as available cache decreases.

5.2.3 OpenVMS Error Logging and Event Log Entry Format

The OpenVMS error handler for the kernel can generate six different entry types, as shown in Table 5-1. All error entry types, with the exception of correctable ECC memory errors, are logged immediately.
### Table 5-1 OpenVMS Error Handler Entry Types

<table>
<thead>
<tr>
<th>OpenVMS Entry Type</th>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
</table>
| EMB$C_MC           | (002.) | Machine Check Exception  
                     |       | SCB Vector 4, IPL 1F  |
| EMB$C_SE           | (006.) | Soft Error Interrupt  
                     |       | Correctable ECC Memory Error  
                     |       | SCB Vector 54, IPL 1A  |
| EMB$C_INT54        | (026.) | Soft Error Interrupt  
                     |       | SCB Vector 54, IPL 1A  |
| EMB$C_INT60        | (027.) | Hard Error Interrupt 60  
                     |       | SCB Vector 60, IPL 1D  |
| EMB$C_POLLED       | (044.) | Polled Errors  
                     |       | No exception or interrupt generated by hardware.  |
| EMB$C_BUGCHECK     |      | Fatal bugcheck  
                     |       | Bugcheck Types:  
                     |       | MACHINECHK  
                     |       | ASYNCWRTER  
                     |       | BADMCKCOD  
                     |       | INCONSTATE  
                     |       | UNXINTEXC  |

Each entry consists of an OpenVMS operating system header, a packet header, and one or more subpackets (Figure 5-1). Entries can be of variable length based on the number of subpackets within the entry. The FLAGS software register in the packet header shows which subpackets are included within a given entry.

Refer to Section 5.2.4 for actual examples of the error and event logs described throughout this section.
Machine check exception entries contain, at a minimum, a Machine Check Stack Frame subpacket (Figure 5–2).
### System Troubleshooting and Diagnostics

#### 5.2 Product Fault Management and Symptom-Directed Diagnosis

**Figure 5–2 Machine Check Stack Frame Subpacket**

<table>
<thead>
<tr>
<th>31</th>
<th>24 23</th>
<th>16 15</th>
<th>08 07</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td>AST LVL</td>
<td>xxxxx</td>
<td>Machine Check Code</td>
<td>xxxxxxxxx</td>
<td>CPU ID</td>
</tr>
<tr>
<td>INT. SYS register</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SAVEPC register</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VA register</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q register</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RN</td>
<td>Mode</td>
<td>Opcode</td>
<td>xxxxxxxxx</td>
<td>V</td>
</tr>
<tr>
<td>PC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

INT54, INT60, Polled, and some Machine Check entries contain a processor Register subpacket (Figure 5–3), which consists of some 40 plus hardware registers.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Figure 5-3 Processor Register Subpacket

<table>
<thead>
<tr>
<th>Address (IPR)</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>BPCR (IPR D4)</td>
<td>0</td>
</tr>
<tr>
<td>PAMODE (IPR E7)</td>
<td>4</td>
</tr>
<tr>
<td>MMEPTE (IPR E9)</td>
<td>8</td>
</tr>
<tr>
<td>MMESTS (IPR EA)</td>
<td>12</td>
</tr>
<tr>
<td>PCSCR (IPR 7C)</td>
<td>16</td>
</tr>
<tr>
<td>ICSR (IPR D3)</td>
<td>20</td>
</tr>
<tr>
<td>ECR (IPR 7D)</td>
<td>24</td>
</tr>
<tr>
<td>TBSTS (IPR ED)</td>
<td>28</td>
</tr>
<tr>
<td>PCCSTL (IPR F8)</td>
<td>32</td>
</tr>
<tr>
<td>PCSTS (IPR F4)</td>
<td>36</td>
</tr>
<tr>
<td>CCTL (IPR A0)</td>
<td>40</td>
</tr>
<tr>
<td>BCEDSTS (IPR A6)</td>
<td>44</td>
</tr>
<tr>
<td>BCTETS (IPR A3)</td>
<td>48</td>
</tr>
<tr>
<td>MESR (2101.8044)</td>
<td>52</td>
</tr>
<tr>
<td>MMCDSR (2101.8048)</td>
<td>56</td>
</tr>
<tr>
<td>CESR (2102.0000)</td>
<td>60</td>
</tr>
<tr>
<td>CMCDSR (2102.0004)</td>
<td>64</td>
</tr>
<tr>
<td>CEFSTS (IPR AC)</td>
<td>68</td>
</tr>
<tr>
<td>NESTS (IPR AE)</td>
<td>72</td>
</tr>
<tr>
<td>NEOCMD (IPR B2)</td>
<td>76</td>
</tr>
<tr>
<td>NEICMD (IPR B8)</td>
<td>80</td>
</tr>
<tr>
<td>DSER (2008.0004)</td>
<td>84</td>
</tr>
<tr>
<td>CBTCR (2014.0020)</td>
<td>88</td>
</tr>
<tr>
<td>MMEADR (IPR E8)</td>
<td>92</td>
</tr>
<tr>
<td>VMAR (IPR D0)</td>
<td>96</td>
</tr>
<tr>
<td>TBADR (IPR EC)</td>
<td>100</td>
</tr>
<tr>
<td>PCDAR (IPR F2)</td>
<td>104</td>
</tr>
<tr>
<td>BCEIDIX (IPR A7)</td>
<td>108</td>
</tr>
<tr>
<td>BCEDECC (IPR A8)</td>
<td>112</td>
</tr>
<tr>
<td>BCETIDX (IPR A4)</td>
<td>116</td>
</tr>
<tr>
<td>BCETAG (IPR A5)</td>
<td>120</td>
</tr>
<tr>
<td>MEAR (2101.8040)</td>
<td>124</td>
</tr>
<tr>
<td>MOAMR (2101.804C)</td>
<td>128</td>
</tr>
<tr>
<td>CSEAR1 (2102.0008)</td>
<td>132</td>
</tr>
<tr>
<td>CSEAR2 (2102.000C)</td>
<td>136</td>
</tr>
<tr>
<td>CIOEAR1 (2102.0010)</td>
<td>140</td>
</tr>
<tr>
<td>CIOEAR2 (2102.0014)</td>
<td>144</td>
</tr>
<tr>
<td>CNEAR (2102.0018)</td>
<td>148</td>
</tr>
<tr>
<td>CFEDAR (IPR AB)</td>
<td>152</td>
</tr>
<tr>
<td>NEOADR (IPR B0)</td>
<td>156</td>
</tr>
<tr>
<td>NEDATHI (IPR B4)</td>
<td>160</td>
</tr>
<tr>
<td>NEDATLO (IPR B6)</td>
<td>164</td>
</tr>
<tr>
<td>QBEAR (2008.0008)</td>
<td>168</td>
</tr>
<tr>
<td>DEAR (2008.000C)</td>
<td>172</td>
</tr>
<tr>
<td>IPCR0 (2000.1F40)</td>
<td>176</td>
</tr>
</tbody>
</table>

Note

The byte count, although part of the stack frame, is not included in the error log entry itself.

Bugcheck entries generated by the OpenVMS kernel error handler include the first 23 registers from the processor Register subpacket along with the Time of Day Register (TODR) and other software context states.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Uncorrectable ECC memory error entries include a Memory subpacket (Figure 5-4). The memory subpacket consists of MEMCON, which is a software register containing the memory configuration and error status used for FRU isolation, and MEMCONn, the hardware register that matched the error address in MEAR.

Figure 5-4 Memory Subpacket for ECC Memory Errors

Correctable Memory Error entries have a Memory (Single-Bit Error) SBE Reduction subpacket (Figure 5-5). This subpacket, unlike all others, is of variable length. It consists solely of software registers from state maintained by the error handler, as well as hardware state transformed into a more usable format.

Figure 5-5 Memory SBE Reduction Subpacket (Correctable Memory Errors)

The OpenVMS error handler maintains a Correctable Read Data (CRD) buffer internally within memory that is flushed asynchronously for high-level events to the error log file. The CRD buffer and resultant error log entry are maintained and organized as follows.

- Each entry has a subpacket header (Figure 5-6) consisting of LOGGING
  REASON, PAGE MAPOUT CNT, MEMCON, VALID ENTRY CNT, and
CURRENT ENTRY. MEMCON contains memory configuration information, but no error status as is done for the Memory subpacket.

Figure 5–6 CRD Entry Subpacket Header

- Following the subpacket header are 1 to 16 fixed-length Memory CRD Entries (Figure 5–7). The number of Memory CRD entries is shown in VALID ENTRY CNT. The entry which caused the report to be generated is in CURRENT ENTRY.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Figure 5–7 Correctable Read Data (CRD) Entry

<table>
<thead>
<tr>
<th>Field</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Footprint</td>
<td>31</td>
</tr>
<tr>
<td>Status</td>
<td>4</td>
</tr>
<tr>
<td>CRD_CNT</td>
<td>8</td>
</tr>
<tr>
<td>Pages Marked Bad_CNT</td>
<td>12</td>
</tr>
<tr>
<td>First Event</td>
<td>16</td>
</tr>
<tr>
<td>Last Event</td>
<td>24</td>
</tr>
<tr>
<td>Lowest Address</td>
<td>32</td>
</tr>
<tr>
<td>Highest Address</td>
<td>36</td>
</tr>
</tbody>
</table>

Each Memory CRD Entry represents one unique DRAM within the memory subsystem. A unique set, bank, and syndrome are stored in footprint to construct a unique ID for the DRAM.

Rather than logging an error for each occurrence of a single symbol correctable ECC memory error, the OpenVMS error handler maintains the CRD buffer—it creates a Memory CRD Entry for new footprints and updates an existing Memory CRD Entry for errors that occur within the range specified by the ID in FOOTPRINT. This reduces the amount of data logged overall without losing important information—errors are logged per unique failure mode rather than on a per error basis.

Each Memory CRD entry consists of a FOOTPRINT, STATUS, CRD_CNT, PAGE_MAPOUT_CNT, FIRST_EVENT, LAST_EVENT, LOWEST_ADDRESS and HIGHEST_ADDRESS.

FIRST_EVENT, LAST_EVENT, LOWEST_ADDRESS and HIGHEST_ADDRESS are updated to show the range of time and addresses of errors which have occurred for a DRAM. CRD_CNT is simply the total count per footprint. PAGE_MAPOUT_CNT is the number of pages that have been marked bad for a particular DRAM.
5.2 Product Fault Management and Symptom-Directed Diagnosis

STATUS contains a record of the failure mode status of a particular DRAM over time. This in turn determines whether or not the CRD buffer is logged. For the first occurrence of an error within a particular DRAM, the memory location will be scrubbed (corrected read data is read, then written back to the memory location) and CRD CNT will be set to 1. Since most memory single-bit errors are transient due to alpha particles, logging of the CRD buffer will not be done immediately for the first occurrence of an error within a DRAM. The CRD buffer will, however, be logged at the time of system shutdown (operator or crash induced), or when a more severe memory subsystem error occurs.

If the FOOTPRINT/DRAM experiences another error (CRD CNT > 1), the OpenVMS operating system will set HARD SINGLE ADDRESS or MULTIPLE ADDRESSES along with SCRUBBED in STATUS. Scrubbing is no longer performed; instead, pages are marked bad. In this case, the OpenVMS operating system will log the CRD buffer immediately. The CRD Buffer will also be logged immediately if PAGE MAPOUT THRESHOLD EXCEEDED is set in SYSTAT as a result of pages being marked bad. The threshold is reached if more than one page per Mbyte of system memory is marked bad.

Note

CURRENT ENTRY will be zero in the Memory SBE Reduction subpacket header if the CRD buffer was logged, not as a result of a HARD SINGLE ADDRESS or MULTIPLE ADDRESSES error in STATUS, but as a result of a memory uncorrectable ECC error shown as RELATED ERROR, or as a result of CRD BUFFER FULL or SYSTEM SHUTDOWN, all of which are shown under LOGGING REASON.

5.2.4 OpenVMS Event Record Translation

The kernel error log entries are translated from binary to ASCII using the ANALYZE/ERROR command. To invoke the error log utility, enter the DCL command ANALYZE/ERROR_LOG.

Format:

ANALYZE_ERROR_LOG [/qualifier(s)] [file-spec] [...]

Example:

$ ANALYZE/ERROR_LOG/INCLUDE=(CPU,MEMORY)/SINCE=TODAY
The error log utility translates the entry into the traditional three-column format. The first column shows the register mnemonics, the second column depicts the data in hex, and the last column shows the actual English translations.

As in the above example, the OpenVMS error handler also provides support for the /INCLUDE qualifier, such that CPU and MEMORY error entries can be selectively translated.

Since most kernel errors are bounded to either the processor module/system board or memory modules, the individual error flags and fields are not covered by the service theory. Although these flags are generally not required to diagnose a system to the FRU (Field Replaceable Unit), this information can be useful for component isolation.

ERF bit to text translation highlights all error flags that are set, and other significant state—these are displayed in capital letters in the third column. Otherwise, nothing is shown in the translation column. The translation rules also have qualifiers such that if the setting of an error flag causes other registers to be latched, the other registers will be translated as well. For example, if a memory ECC error occurs, the syndrome and error address fields will be latched as well. If such a field is valid, the translation will be shown (e.g. MEMORY ERROR ADDRESS); otherwise, no translation is provided.

### 5.2.5 Interpreting CPU faults using ANALYZE/ERROR

If the following three conditions are satisfied, the most likely FRU is the CPU module. Example 5–1 shows an abbreviated error log with numbers to highlight the key registers.

1. No memory subpacket is listed in the third column of the FLAGS register.

2. CESR register bit <09>, CP2 IO Error, is equal to zero in the KA50/51/55 /56 Register Subpacket.

3. DSER register bits <07>, Q22 Bus NXM, <05>, Q22 Bus Device Parity Error, or <02>, Q-22 Bus No Grant, are equal to zero in the KA50/51/55/56 Register Subpacket.

The FLAGS register is located in the packet header, which immediately follows the system identification header; the CESR and DSER registers are listed under the KA50/51/55/56 Register Subpacket.

CPU errors will increment an OpenVMS global counter, which can be viewed using the DCL command SHOW ERROR, as shown in Example 5–2.
To determine if any resources have been disabled, for example, if cache has been disabled for the duration of the OpenVMS session, examine the flags for the SYSTAT register in the packet header.

In Example 5–1, a translation buffer data parity error latched in the TBSTS register caused a machine check exception error.

Example 5–1 Error Log Entry Indicating CPU Error

PAGE 1.

ERROR SEQUENCE 11.
SYSTEM UPTIME: 0 DAYS 00:12:12
SCS NODE: OMEGA

MACHINE CHECK KA50 CPU Microcode Rev # 1. CONSOLE FW REV# 1.1

REVISION 00000000
SYSTAT 00000001

FLAGS 00000003 ATTEMPTING RECOVERY

machine check stack frame
KA50 subpacket

STACK FRAME SUBPACKET

ISTATE_1 80050000

MACHINE CHECK FAULT CODE = 05(x)
Current AST level = 4(X)
ASYNCHRONOUS HARDWARE ERROR

PSL 04140001 c-bit
executing on interrupt stack
PSL previous mode = kernel
PSL current mode = kernel
first part done set

KA50 REGISTER SUBPACKET

(continued on next page)
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5–1 (Cont.) Error Log Entry Indicating CPU Error

BPCR    ECCB0024

TBSTS    800001D3

LOCK SET
TRANSLATION BUFFER DATA PARITY ERROR
em latch invalid
s5 command = 1D(X)
valid Ibox specifier ref. error stored

CSEP     00000000  ●

DSEP     00000000  ●

IPCR0    00000020

LOCAL MEMORY EXTERNAL ACCESS ENABLED

Note
Ownership (0-bit) memory correctable or fatal errors (MESR <04> or MESR <03> of the processor Register S:abacket set equal to 1) are processor module errors, NOT memory errors.

Example 5–2 SHOW ERROR Display Using the OpenVMS Operating System

$ SHOW ERROR
Device  Error Count
CPU     1
MEMORY  1
PAB0:   1
PBA0:   1
PTA0:   1
RTA2:   1

$
5.2.6 Interpreting Memory Faults Using ANALYZE/ERROR

If "memory subpacket" or "memory sub packet" is listed in the third column of the FLAGS register, there is a problem with one or more of the memory modules, CPU module, or backplane.

- The "memory subpacket" message indicates an uncorrectable ECC error. Refer to Section 5.2.6.1 for instructions in isolating uncorrectable ECC error problems.

- The "memory sub packet" message indicates correctable ECC errors. Refer to Section 5.2.6.2 for instructions in isolating correctable ECC error problems.

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Note

The memory fault interpretation procedures work only if the memory modules have been properly installed and configured. For example, memory modules should start in backplane slot 4 (next to the processor module in slot 5) and proceed to slot 1 with no gaps.

_________________________________________________________

Note

Although the OpenVMS error handler has built-in features to aid Services in memory repair, good judgment is needed by the Service Engineer. It is essential to understand that in many, if not most cases, correctable ECC errors are transient in nature. No amount of repair will fix them, as generally there is nothing to be fixed.

Memory modules can represent a great expense to the Corporation when they are sent back to Repair with no errors. If one disagrees with the strategy in this section or has questions or suggestions, please contact Corporate Support.

_________________________________________________________

5.2.6.1 Uncorrectable ECC Errors

Refer to Example 5–3, which provides an abbreviated error log for uncorrectable ECC errors.

For uncorrectable ECC errors, a memory subpacket will be logged as indicated by "memory sub packet" listed in the third column of the FLAGS software register ( ). Also, the hardware register MESR <11> ( ) of the processor Register Subpacket will be set equal to 1, and MEAR will latch the error address ( ).
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Examine the MEMCON software register (1) under the memory subpacket. The MEMCON register provides memory configuration information.

The OpenVMS error handler will mark each page bad and attempt page replacement, indicated in SYSTAT (1). The DCL command SHOW MEMORY (Example 5–4) will also indicate the result of OpenVMS page replacement.

Uncorrectable memory errors will increment the OpenVMS global counter, which can be viewed using the DCL command SHOW ERROR.

______________________________

Note

If register MESR <11> was set equal to 1, but MESR <19:12> syndrome equals 07, no memory subpacket will be logged as a result of incorrect check bits written to memory because of an NDAL bus parity error detected by the NMC. In short, this indicates a problem with the CPU module, not memory. There should be a previous entry with MESR <22>, NDAL Data Parity Error set equal to 1.

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Note

One type of uncorrectable ECC error, that due to a “disown write”, will result in a CRD entry like those for correctable ECC errors. The FOOTPRINT longword for this entry contains the message “Uncorrectable ECC errors due to disown write”. The failing module should be replaced for this error.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5-3  Error Log Entry Indicating Uncorrectable ECC Error

VAX / VMS  SYSTEM ERROR REPORT  COMPIL 6-MAY-1991 10:16:49
PAGE 25.
ERROR SEQUENCE 2.
DATE/TIME 4-OCT-1991 09:14:29.86
SYSTEM UPTIME: 0 DAYS 00:01:39
SCS NODE: OMEGA1

INT54 ERROR  KA50  CPU Microcode Rev #1  CONSOLE FW REV#1.1

REVISION  00000000
SYSTAT  00000601

FLAGS  00000006

ATTEMPTING RECOVERY
PAGE MARKED BAD
PAGE REPLACED

memory subpacket
KA50 subpacket

KA50 REGISTER SUBPACKET

RPCR  ECCB0000
.
.

MFSR  80006800

UNCORRECTABLE MEMORY ECC ERROR

ERROR SUMMARY
MEMORY ERROR SYNDROME = 06(X)
.
.

MEAR  02FFDC00
main memory error address = 0B0F7000

ncal commander id = 00(X)
.
.

IPCR0  00000020
LOCAL MEMORY EXTERNAL ACCESS ENABLED

MEMORY SUBPACKET

MEMCON  000FFFF2
MEMORY CONFIGURATION:
MS44-AA SIM Memory Module 4 MB location 1E
MS44-AA SIM Memory Module 4 MB location 1F
MS44-AA SIM Memory Module 4 MB location 1G
MS44-AA SIM Memory Module 4 MB location 1H
_total memory = 16MB

(continued on next page)
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5–3 (Cont.) Error Log Entry Indicating Uncorrectable ECC Error

MEMCON3 8B000003

64 bit mode
Base address valid
RAM size = 1MB
base address = 0B(X)

Example 5–4 SHOW MEMORY Display Under the OpenVMS Operating System

$ SHOW MEMORY
System Memory Resources on 21-FEB-1992 05:58:52.58

Physical Memory Usage (pages):
Main Memory (128.00Mb) 262144 224527 28759 8858
Bad Pages 1 1 0 0
Slot Usage (slots):
Process Entry Slots 360 347 13 0
Balance Set Slots 324 313 11 0
Fixed-Size Pool Areas (packets):
Small Packet (SRP) List 3067 2724 343 128
I/O Request Packet (IRP) List 2263 2070 193 176
Large Packet (LRP) List 87 61 26 1856
Dynamic Memory Usage (bytes):
Nonpaged Dynamic Memory 1037824 503920 533904 473184
Paged Dynamic Memory 1468416 561584 906832 560624
Paging File Usage (pages):
DISK/VMS054-0:SYSG.SCX|PAGEFILE.SYS 300000 266070 300000

Of the physical pages in use, 24120 pages are permanently allocated to OpenVMS.

$ Using the OpenVMS command ANALYZE/SYSEM, you can associate a page that had been replaced (Bad Pages in SHOW MEMORY display) with the physical address in memory.

In Example 5–5, 5ff8 (under the Page Frame Number (PFN) column) is identified as the single page that has been replaced. The command EVAL 5ff8 * 200 converts the PFN to a physical page address. The result is 0bff7000, which is the MEAR address translated in Example 5–3. (Bits <8:0> of the addresses may differ since the page address from EVAL always shows bits <8:0> as 0.)
Example 5–5 Using ANALYZE/SYSTEM to Check the Physical Address in Memory for a Replaced Page

$ ANALYZE/SYSTEM
VAX/OpenVMS System analyzer
SDA> SHOW PTH /BAD
Bad page list
----------
Count: 1
Lolimit: -1
High limit: 1073741824

PFN  PTE ADDRESS  BAK  REFCNT  FLINK  BLINK  TYPE   STATE
----- ----------  ----  ------  -----  -----  ------  ------
0005FFB8  00000000  00000000  0  00000000  00000000  20 PROCESS 02 BADLIST

SDA> EVAL 5ffb8 * 200
Hex = 0BFF7000  Decimal = 201289728
SDA> EXIT
$

5.2.6.2 Correctable ECC Errors

Refer to Example 5–6, which provides an error log showing correctable ECC errors.

For correctable ECC errors, a Single-Bit Error (SBE) Memory Subpacket will be logged as indicated by "memory sbe reduction subpacket" listed in the third column of the FLAGS software register (●).

The Memory SBE Reduction Subpacket header contains a CURRENT ENTRY register (●) that displays the number of the Memory CRD Entry that caused the error notification. If CURRENT ENTRY > 0, examine which bits are set in the STATUS register (●) for this entry—GENERATE REPORT should be set.

Note

If CURRENT ENTRY = 0, then the entry was logged for something other than a single-bit memory correctable error Footprint. You will need to examine all of the Memory CRD Entries and Footprints to try to determine the likely FRU.

Check for the following:

- SCRUBBED (●)—If SCRUBBED is the only bit set in the STATUS register, memory modules should NOT generally be replaced.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

The kernel performs memory scrubbing of DRAM memory cells that may flip due to transient alpha particles. Scrubbing simply reads the corrected data and writes it back to the memory location. Returning memory modules that only have SCRUBBED set in STATUS will cost the corporation money, since the repair centers will generally not find a problem.

Unlike uncorrectable ECC errors, the error handling code cannot indicate if the page has been replaced. To get some idea, use DCL command, SHOW MEMORY. If the page mapout threshold has not been reached ("PAGE MAPOUT THRESHOLD EXCEEDED" is not set in SYSTAT packet header register (5)), the system should be restarted at a convenient time to allow the power-up self-test and ROM-based diagnostics to map out these pages. This can be done by entering TEST 0 at the console prompt, running an extended script TEST A9, or by powering down then powering up the system. In all cases, the diagnostic code will mark the page bad for hard single address errors, as well as any uncorrectable ECC error by default.

If there are many locations affected by hard single-cell errors, on the order of one or more pages per MB of system memory, the memory module should be replaced. The console command SHOW MEMORY will indicate the number of bad pages per module. For example, if the system contains 64 MB of main memory and there are 64 or more bad pages, the affected memory should be replaced.

Note

Under the OpenVMS operating system, the page mapout threshold is calculated automatically. If "PAGE MAPOUT THRESHOLD EXCEEDED" is set in SYSTAT (5), the failing memory module should be replaced.

In cases of a new memory module used for repair or as part of system installation, one may elect to replace the module rather than having diagnostics map them out, even if the threshold has not been reached for hard single-address errors.

- MULTIPLE ADDRESSES (6)—If the second occurrence of an error within a footprint is at a different address (LOWEST ADDRESS not equal to HIGHEST ADDRESS (6)), MULTIPLE ADDRESSES will be set in STATUS along with SCRUBBED. Scrubbing will not be attempted for this situation. In most cases, the failing memory module should be replaced regardless of the page mapout threshold.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

If CRD BUFFER FULL is set in LOGGING REASON (1) (located in the subpacket header) or PAGE MAPOUT THRESHOLD EXCEEDED is set in SYSTAT (2), the failing memory module should be replaced regardless of any thresholds.

For all cases (except when SCRUBBED is the only flag set in STATUS) isolate the offending memory by examining the translation in FOOTPRINT called MEMORY ERROR STATUS (3): The memory module is identified by its backplane position. In Example 5–6, SIMM memory modules in locations 0A and 0B are identified as failing.

The Memory SBE Reduction Subpacket header translates the MEMCON register (4) for memory subsystem configuration information.

Unlike uncorrectable memory and CPU errors, the OpenVMS global counter, as shown by the DCL command SHOW ERROR, is not incremented for correctable ECC errors unless it results in an error log entry for reasons other than system shutdown.

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Note ______________________

If footprints are being generated for more than one memory module, especially if they all have the same bit in error, the processor module, backplane, or other component may be the cause.

________________________
Note ______________________

One type of uncorrectable ECC error, that due to a "disown write", will result in a CRD entry like those for correctable ECC errors. The FOOTPRINT longword for this entry contains the message "Uncorrectable ECC errors due to disown write". The failing module should be replaced for this error.

________________________
Example 5–6 Error Log Entry Indicating Correctable ECC Error

PAGE 1.

ERROR SEQUENCE 2.
SYSTEM UPTIME: 0 DAYS 00:05:06
SCS NODE: OMega1

CORRECTABLE MEMORY ERROR KA50 CPU Microcode Rev # 1. CONSOLE FW REV 1.1

REVISON 00000000
SYSTAT 00000040
FLAGS 00000008

memory sbe reduction subpacket

MEMORY SBE REDUCTION SUBPACKET

LOGGING REASON 00000004

PAGE MAPOUT CNT 00000000
MEMCON 00FFDD01

MEMORY CONFIGURATION:
MS44-AA SIM Memory Module (4MB) Loc QA
MS44-AA SIM Memory Module (4MB) Loc OB
MS44-AA SIM Memory Module (4MB) Loc QC
MS44-AA SIM Memory Module (4MB) Loc OD
Total memory = 16MB
Sets enabled = 000000001

MEMORY ERROR STATUS:
SIMM MEMORY MODULES: LOCATIONS QA & OB
Set = 0 (X)
Bank = A

VALID ENTRY CNT 00000001
CURRENT ENTRY 00000000

MEMORY CRD ENTRY 1.

FOOTPRINT 00000073

(continued on next page)
System Troubleshooting and Diagnostics

5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5–6 (Cont.) Error Log Entry Indicating Correctable ECC Error

MEMORY ERROR STATUS:
SIMM MEMORY MODULE: LOCATION QA
set = 0
bank = 0.
ECC SYNDROME = 73(X)
CORRECTED DATA BIT = 0.

STATUS 00000010
scrubbed 1

CRD CNT 00000001
1.

PAGE MAPOUT CNT 00000000
0.

FIRST EVENT 16B0F640
009622CB
16-OCT-1992 11:03:36.10

LAST EVENT 16B0F640
009622CB
16-OCT-1992 11:03:36.10

LOWEST ADDRESS 0BF4000
HIGHEST ADDRESS 0BF4000

Note

Ownership (O-bit) memory correctable or fatal errors (MESR <04> or MESR <03> of the processor Register Subpacket set equal to 1) are processor module errors, NOT memory errors.

5.2.7 Interpreting System Bus Faults Using ANALYZE/ERROR

If hardware register CESR <09> (☑) and/or CQBIC hardware register DSER <07>, <05>, or <02> (☑) is set equal to 1, there may be a problem with the Q–bus or Q–bus option.

When CESR <09> is set equal to 1, examine the hardware register CIOEAR2 (☑) to determine the address of the offending option.

Example 5–7 provides an error log showing a faulty Q–bus option. The CIOEAR2 error register indicates the first UQSSP controller as the offending address.
Example 5-7  Error Log Entry Indicating Q-Bus Error

PAGE 1.
***************************************** ENTRY 75. ****************************
ERROR SEQUENCE 1852.  LOGGED ON:  SID 13001401
SYSTEM UPTIME: 12 DAYS 20:04:19  VAX/OpenVMS V5.5-2
SCS NODE:

MACHINE CHECK KA50  CPU Microcode Rev # 1.  CONSOLE FW REV# 1.1

REVISION 00000000
SYSTAT 00000001

FLAGS 00000003  ATTEMPTING RECOVERY

machine check stack frame
KA50 subpacket

STACK FRAME SUBPACKET

ISTATE_1 80060000
.
.
PSEL 03C00000

PSL previous mode = user
PSL current mode = user
first part done set

KA50 REGISTER SUBPACKET

(continued on next page)
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5–7 (Cont.) Error Log Entry Indicating Q-Bus Error

BPCR       ECC80024
.
.
CESR       80000200 •
             CP2 IO ERROR
             ERROR SUMMARY
.
.
DSER       00000080 •
             Q-22 BUS NXM
.
.
CIOEAR2    00001468 •
             cp2 IO error address = 20001468
             NDAL command id (cp2 transac) = 0(X)
.
.
IPCRO      00000020
             LOCAL MEMORY EXTERNAL ACCESS ENABLED

5.2.8 Interpreting DMA ↔ Host Transaction Faults Using ANALYZE/ERROR

Some kernel errors may result in two or more entries being logged. If the SGEC Ethernet controller or other CDAL device (residing on the processor module) encounter host main memory uncorrectable ECC errors, main memory NXM's or CDAL parity errors or timeouts, more than one entry results. Usually there will be one Polled Error entry logged by the host, and one or more Device Attention and other assorted entries logged by the device drivers.

In these cases the processor module or one of the four memory modules are the most likely cause of the errors. Therefore, it is essential to analyze Polled Error entries, since a polled entry usually represents the source of the error versus other entries, which are simply aftereffects of the original error.

Example 5–8 provides an abbreviated error log for a polled error. Example 5–9 provides an example of a device attention entry.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5-8  Error Log Entry Indicating Polled Error

VAX/VMS SYSTEM ERROR REPORT  COMPIL. 17-FEB-1992 05:32:21
PAGE 1.

ERROR SEQUENCE 15.
DATE/TIME 17-FEB-1992 05:22:00.90
SYSTEM UPTIME: 0 DAYS 02:27:48

LOGGED ON: SID 13001401
SYS.TYPE 00310A01

SCS NODE: VAX/OpenVMS V5.5-2

POLLED ERROR KA50 CPU Microcode Rev 1. CONSOLE FW REV 1.1
Standard Microcode Patch Patch Rev 1.10.

REVISION 00000000
SYSTAT 00000001

FLAGS 00000006 ATTEMPTING RECOVERY
memory subpacket

KA50 subpacket

KA50 REGISTER SUBPACKET

APCR ECC80024
.
.
MESR 8001B0D0 UNCORRECTABLE MEMORY ECC ERROR
ERROR SUMMARY
MEMORY ERROR SYNDROME = 1B(X)
.
.
MEAR 50000410 main memory error address = 00001040
ndal commander ld = 05(X)

.
.
IPCR0 00000020 LOCAL MEMORY EXTERNAL ACCESS ENABLED

MEMORY SUBPACKET

MEMCON 000FFFF02 MEMORY CONFIGURATION:
MS44-AA SIM Memory Module 4 MB location 1E
MS44-AA SIM Memory Module 4 MB location 1F
MS44-AA SIM Memory Module 4 MB location 1G
MS44-AA SIM Memory Module 4 MB location 1H
_total memory = 16MB

(continued on next page)
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5–8 (Cont.) Error Log Entry Indicating Polled Error

MEMCON0 80000003

64 bit mode
Base address valid
RAM size = 1MB
base address = 00(X)

ANAL/ERR/OUT- T81 T81.ZPD
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Example 5–9 Device Attention Entry

VA X / VM S SYSTEM ERROR REPORT

****************************************************************************** ENTRY
2.******************************************************************************

ERROR SEQUENCE 15.
DATE/TIME 17-FEB-1992 05:22:00.90
SYSTEM UPTIME: 0 DAYS 00:27:48
SCS NODE:

DEVICE ATTENTION KA50 CPU Microcode Rev # 1. CONSOLE FW REV # 1.1

OSSI SUB-SYSTEM, PABO: - PORT WILL BE RE-STARTED
PORT TIMEOUT, DRIVER RESETING PORT

CNF 03060022

PMCSR 00000000
PSR 80010000

PFAR 40001044
PESR 00010000
PPR 00000000

UCB5B_ERCNT 2C
UCB5B_ERMX 32
UCB5L_CHAN 0C450000

UCB5W_STS 0010
UCB5W_ERRCNT 0007

ANAL/ERR/ENTRY (ST:2, END:3)/OUT=POLL SHM
5.2.9 VAXsimPLUS and System-Initiated Call Logging (SICL) Support

Symptom-Directed Diagnostic (SDD) toolkit support for KA50/51/55/56 kernels is provided in version 2.0 of the toolkit. If version 2.0 is not available, you should install the previous version, as it provides support for many existing options.

MicroVAX 3100 systems use Symptom-Directed Diagnosis tools primarily for notification. The VAX System Integrity Monitor Plus (VAXsimPLUS) interactive reporting tool triggers notification for high-level events recorded in SYSSTAT and LOGGING REASON.

The VAXsimPLUS monitor simply parses for a handful of SYSSTAT flags and LOGGING reason codes. The VAXsimPLUS monitor display is updated and triggering occurs if the threshold has been reached. Some flags have a threshold of one; for example, SYSSTAT <08> ERROR THRESHOLD EXCEEDED will trigger VAXsimPLUS upon the first occurrence, since at least three errors would have already occurred and been handled by the OpenVMS operating system.

All lower level errors will ultimately set one of the conditions shown in Table 5–2. VAXsimPLUS will examine the conditions within a 24-hour period—thresholds are typically one or two flags or logging reason codes within that period.

Table 5–2 lists the conditions that will trigger VAXsimPLUS notification and updating. Figure 5–8 shows the flow for the VAXsimPLUS monitor trigger (for decision blocks with only one branch, the alternative is treated as an ignore condition). The entries ultimately are classified as either hard or soft. Errors that require corrective maintenance are classified as hard; while errors potentially requiring corrective maintenance are classified as soft.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Table 5-2  Conditions That Trigger VAXsimPLUS Notification and Updating

<table>
<thead>
<tr>
<th>Condition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYSTAT &lt;00&gt; = 1</td>
<td>&quot;Attempting recovery&quot;</td>
</tr>
<tr>
<td>SYSTAT &lt;00&gt; = 0</td>
<td>&quot;Full recovery or retry not possible&quot;</td>
</tr>
<tr>
<td>SYSTAT &lt;08&gt; = 1</td>
<td>&quot;Error threshold exceeded&quot;</td>
</tr>
<tr>
<td>SYSTAT &lt;09&gt; = 1</td>
<td>&quot;Page marked bad for uncorrectable ECC error in main memory&quot;</td>
</tr>
<tr>
<td>SYSTAT &lt;11&gt; = 1</td>
<td>&quot;Page mapout threshold for single bit ECC errors in main memory exceeded&quot;</td>
</tr>
<tr>
<td>LOGGING REASON &lt;3:0&gt; = 1</td>
<td>&quot;Memory CRD buffer full&quot;</td>
</tr>
<tr>
<td>LOGGING REASON &lt;3:0&gt; = 2</td>
<td>&quot;Generate report as a result of hard single address or multiple address DRAM memory fault&quot;</td>
</tr>
<tr>
<td>LOGGING REASON &lt;3:0&gt; = 0, 3, 5–F</td>
<td>&quot;Illegal LOGGING REASON&quot;</td>
</tr>
</tbody>
</table>
VAXsimPLUS triggering notifies the customer and Services using three message types: HARD, SOFT, and SICL Service Request. Each message contains the single STARS article theory number, as well as the SYSTAT or LOGGING REASON state. In addition, the SICL Service Request will have a Merged Error Log (MEL) datafile appended. Both hard and soft triggers will generate SICL Service Request messages.
Figure 5–9 shows the five VAXsimPLUS monitor screen displays. Table 5–3 provides a brief explanation of the five levels of screen displays.

Table 5–3  Five-Level VAXsimPLUS Monitor Screen Displays

<table>
<thead>
<tr>
<th>Level</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. System</td>
<td>The system level screen provides one box for each system being analyzed (in Figure 5–9 a single system is being analyzed). As with each screen level, the number of reported errors is displayed in the box. The boxes blink when the hard error thresholds are reached; the boxes are highlighted when the soft error thresholds are reached.</td>
</tr>
<tr>
<td>2. Subsystem</td>
<td>The subsystem level screen provides separate boxes for the kernel and node information. Other boxes that may be displayed are bus, disk, tape, etc.</td>
</tr>
<tr>
<td>3. Unit</td>
<td>The unit level screen provides a box for the kernel. If the subsystem has more than one unit or device with errors, those will be displayed as well.</td>
</tr>
<tr>
<td>4. Error Class</td>
<td>The error class level screen provides a box for both hard and soft errors.</td>
</tr>
<tr>
<td>5. Error Detail</td>
<td>Two error detail level screens (hard and soft) provide the number of reported errors along with a brief error description.</td>
</tr>
</tbody>
</table>
Once notification occurs, the service engineer should examine the error log file (after using the ANALYZE/ERROR command) or read the appended Merged Error Log (MEL) file in the SICL service request message. (The MEL file is encrypted, refer to Section 5.2.9.1 for instructions in converting these files.)
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-directed Diagnosis

Using the theory of interpretation provided in the previous sections, you can manually interpret the error logs.

__________________________ Note ______________________

The interpretation theory provided in this manual is also a STARS article and can be accessed via the Decoder Kit. (Theory 30B01.xxx reproduces in full, Section 5.2 of this manual).

In summary, a service engineer should use VAXsimPLUS notification as follows:

1. Make sure all four message types are sent to the Field and System accounts.
2. Log into the Field or System account.
3. Read mail (look for the SICL service request message with its appended MEL file).
4. Convert the encrypted MEL file and use the theory provided in this manual to interpret the error log file.

5.2.9.1 Converting the SICL Service Request MEL File

Use the following procedure to convert the encrypted MEL file that is appended to the SICL service request message (MEL files can be converted on site or at a support center). Example 5–10 shows a sample SICL service request message and appended MEL file.

1. Extract the SICL mail message from mail.
2. Edit the extracted file to obtain the appended MEL file. The MEL file is the encrypted code that appears between the rows of asterisks and includes the words “SICL” and “end.”
3. Convert the encrypted code to a binary file using the VAXsimPLUS decode command file as follows:

   $ MCR SDD$EXE:FMGR$SICL DECODE [MEL filename] [binary filename]

4. Use the ANALYZE/ERROR command to produce an error log entry.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

$ ANALYZE/ERROR [binary filename]

Example 5-10 SICL Service Request with Appended MEL File

To: SYSTEM
CC:
Subj: SDD T2.0 Service Request - Analysis:[30B01.200]

VAXsimPLUS Notification Message

VAXsimPLUS has detected that the following device needs attention:

DEVICE: ABIX$KERNEL (NVAX4000)
NODE: ABIX
SYSTEM SERIAL NUMBER: KA136H1520
SYSTEM TYPE: VAX 4000-600

VAXsimPLUS Diagnosis Information

Attn: Field Service
Device: ABIX$KERNEL (NVAX4000)
Count: 1.
Theory: [30B01.200]
Evidence: Urgent action required - ABIX$KERNEL Hard error(s):

SYSTAT <9> = 1 - Page Marked Bad For Uncorrectable ECC Error In Main Memory

%% SDDSPROFILE is defined to be NONE, no Customer Profile included in message %%

*****************************************************************************
SICL

134
M 0 S 0 0=0 0 A$24U3$9\( % @ G!::G*Y5
M 0 034N=2U,-2 7 60\( @ !P !6 : 0 "<<
M !Fp| " %/,%S P # RO R.P \%31.03 !P @ !
M H 0 O* /S_S$I\#X _A : F 6 /CA*0 (P0
H=A( % "!P 0 'Q0. ' ""% 0
M (5+5)P1Z P P 0 % " " S ,13
POE: \ " 0 % " !D/ 04 (}
end
*****************************************************************************

5.2.9.2 VAXsimPLUS Installation Tips

When installing VAXsimPLUS, the system will prompt you for information.
You will need to know the serial number and system model number for the
system on which you are installing VAXsimPLUS. The serial number is located
on the front of the chassis at the bottom and to the left (the front door must be
open). The system model number is attached to the outside of the door.
System Troubleshooting and Diagnostics
5.2 Product Fault Management and Symptom-Directed Diagnosis

Also, if the system does not have dialout capability, you should answer no when asked if you want to enable SICL—if you enter yes, the system will attempt to send mail via DSNLink resulting in error messages. After VAXsimPLUS is installed you can activate SICL and customize the VAXsimPLUS mailing lists so that SICL messages are sent to an appropriate destination(s) on site. This way, SICL messages are received onsite without incurring error messages regarding remote link failures.

5.2.9.3 VAXsimPLUS Post-Installation Tips

Once VAXsimPLUS is installed, you can set up mailing lists to direct VAXsimPLUS messages to the appropriate destinations. If the system has no dialout capability, SICL messages should be directed to the System and/or Field account—this is good practice for systems with dialout and service center support as well.

In the example that follows, the four types of mailing lists are displayed and System and Field accounts are added to all four mailing lists using VAXSIM /FAULT_MANAGER commands.

-------------------- Note ----------------------

The commands can be abbreviated.

DSN%SICL appears under the SICL mailing list if you enabled SICL during installation.

-------------------- End Note ----------------------
$ VAXSIM/FAULT SHOW MAIL
-- FSE mailing list --
FIELD
-- CUSTOMER mailing list --
SYSTEM
-- MONITOR mailing list is empty --
-- SICL mailing list --
DSN%SICL
$ VAXSIM/FAULT ADD SYSTEM ALL
$ VAXSIM/FAULT ADD FIELD ALL
$ VAXSIM/FAULT SHOW MAIL
-- FSE mailing list --
FIELD
SYSTEM
-- CUSTOMER mailing list --
FIELD
SYSTEM
-- MONITOR mailing list --
FIELD
SYSTEM
-- SICL mailing list --
DSN%SICL
FIELD
SYSTEM

To activate SICL after installation, use the following command:

$ VAXSIM/FAULT SET SICL ON

VAXsimPLUS customer notification messages should display a phone number for the customer to call in the event the system needs service. Use the following commands to examine and set the phone number parameter:

$ VAXSIM/FAULT SHOW PARAMETER

(SET parameter) (Parameter settings)
PHONE NUMBER Customer Service Phone Number is unknown
COPY Automatic copying is OFF
SICL System Initiated Call Logging is ON
SYSTEM_INFO System info for A81X
Serial number KA136H1520
System type VAX 4000-600
$ VAXSIM/FAULT SET PHONE 1-800-DIGITAL

Finally, the VAXSIMPLUS/MERGE command is useful in examining how a device is functioning in a cluster. The merge command collects the messages that are being sent to the other CPUs in the cluster.

5.2.10 Repair Data for Returning FRUs

When sending back an FRU for repair, include as much of the error log information as possible. If one or more error flags are set in a particular entry, record the mnemonic(s) of the register(s), the hex data, and error flag translation(s) on the repair tag. If an error address is valid, include the mnemonic, hex data, and translation on the repair tag as well. For memory and cache errors, include the syndrome and corrected-bit/bit-in-error information, along with the register mnemonic and hex data. Other registers which should be recorded for any entry type are SYSTAT, MEMCON and FOOTPRINT.

5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

If any of the tests fail, the test code displays on the console LED and, if specified in the firmware script, a diagnostic console printout displays in the format shown in Example 5–11.

Example 5–11 Sample Output with Errors

```plaintext
1 2  3  4  5
Test_Subtest=40  Subtest=00  Err_Type=FF  DE_Memory_count_pages.llis

Vec=0000  Prev_Err=0004  P1=00000001  P2=00000002  P3=00000001  P4=00000000
P5=00000020  P6=00000000  P7=00000020  P8=00000000  P9=00000000  P10=00FC44B
r0=00FF4000  r1=00000007  r2=00000000  r3=FFFFFFF  r4=00000000  r5=00000000
r6=00000000  r7=00000000  r8=00FF4000  r9=20140758  r10=FFFFFFFE  r11=FFFFFFF
ds=0000  ccr=00000000  intmsk=00  lcs=01  pc=00000000  paddr=FFFFFE0B  pctrl=FC13
ccntt=00000021  bcets=0000  bcets=0000  bcs=00000200  bcs=00
mocs=00110000  mdr=00000000

>>>
```

Several lines are printed in the error display. The first line has eight column headings:

1 Test identifies the diagnostic test, test ?40 in Example 5–11. Using Table 5–4, you can use the test number to point to possible problems in field replaceable units (FRUs).
System Troubleshooting and Diagnostics
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

2 Subtest log is two hex digits identifying, usually within 10 instructions, where in the diagnostic the error occurred.

3 Loop_subtest_log is an additional log generated out of the current test specified by the current test number and subtestlog. Usually these logs occur in common subroutines called from a diagnostic test.

4 Error_type (diagnostic executive error) signals the diagnostic's state and any illegal behavior. This field indicates a condition that the diagnostic expects on detecting a failure. FE or EF in this field means that an unexpected exception or interrupt was detected. FF indicates an error as a result of normal testing, such as a miscompare. The possible codes are:

<table>
<thead>
<tr>
<th>Error Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF</td>
<td>Normal error exit from diagnostic</td>
</tr>
<tr>
<td>FE</td>
<td>Unanticipated interrupt</td>
</tr>
<tr>
<td>FD</td>
<td>Interrupt in cleanup routine</td>
</tr>
<tr>
<td>FC</td>
<td>Interrupt in interrupt handler</td>
</tr>
<tr>
<td>FB</td>
<td>Script requirements not met</td>
</tr>
<tr>
<td>FA</td>
<td>No such diagnostic</td>
</tr>
<tr>
<td>EF</td>
<td>Unanticipated exception in executive</td>
</tr>
</tbody>
</table>

5 ASCII messages Shows the name of the listing file that contains the failed diagnostic.

6 Vec identifies the SCB vector through which the unexpected exception or interrupt trapped, when the de_error field detects an unexpected exception or interrupt (FE or EF).

7 Prev_errs is four hex digits showing the number of previous errors that have occurred (four in Example 5–11).

Lines 2 and 3 of the error printout are parameters 1 through 10. When the diagnostics are running normally, these parameters are the same parameters listed in Example 4–3.

When returning a module for repair, always record the the test number, subtest, and Err_type from line 1 of the printout. Also record the Vec from line 2. If possible, record additional information. If the error can be saved onto a printer, then enclose the full printout with the failing module.
System Troubleshooting and Diagnostics
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Note

Do not confuse the countdown pattern of powerup tests with the test number. In the following the last countdown was 58; this number should not be reported! The test number was 31.

The countdown pattern is used to indicate progress in the power-up tests. The actual true test number associated with a countdown value can change from one release of the ROM code to another. For example:

```
RA50-A T1.2-156, VMB 2.14
Performing normal system tests.
72..71..70..69..68..67..66..65..64..63..62..61..60..59..58..

? Test Subtest_31_06 Loop_Subtest=05 Err_Type=FF DE Memory_Setup_CSRs.lis
Vec=0000 Prev_Errs=0000  P1=C94AC94A  P2=01000000  P3=00000002  P4=00000000
```

Minimum recording for this error is:

Test = 31
Subtest = 6
Loop_Subtest = 5
Err_type = FF
Vec = 0.

Table 5-4 lists the hex LED display, the default action on errors, and the most likely unit that needs replacing reading from left to right. Example, 1,4 indicates 1 is most likely, then 4. The Default on Error column refers to the action taken by the diagnostic executive when the test fails in the script.

Memory tests are usually treated differently; when an error occurs, the memory tests usually try to continue and mark the bitmap. Test 40 reports failing pages in the bitmap.

When any memory test fails, always do a SHOW MEMORY to help identify the FRU. SHOW MEMORY will identify the FRU to a SET of SIMMs or to an individual SIMM if possible.

If a single set of SIMMs is present, and replacing a suspected bad SIMM or set does not fix the problem, assume that the system board is bad. Always check the seating of SIMMs before replacing. If nonvolatile data is lost after powerup or you always get a request to select a language at powerup, the battery may be bad.

Table 5-4 shows the various LED values and console terminal displays as they point to problems in field-replaceable units (FRUs).
System Troubleshooting and Diagnostics
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Table 5-4  KA50/51/55/56 Console Displays as Pointers to FRUs

<table>
<thead>
<tr>
<th>On Error Hex LED</th>
<th>Normal Console Display</th>
<th>Default Action on Error</th>
<th>Falling Test Number</th>
<th>Test Description</th>
<th>FRU¹</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power-Up Tests (Script A1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>None</td>
<td>Loop</td>
<td>None</td>
<td>Power up</td>
<td>1, 4</td>
</tr>
<tr>
<td>E</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>ROM code execution begun</td>
<td>1, 4</td>
</tr>
<tr>
<td>D</td>
<td>None</td>
<td>Loop</td>
<td>None</td>
<td>Wait for power</td>
<td>1, 4</td>
</tr>
<tr>
<td>B</td>
<td>72</td>
<td>Cont</td>
<td>9D</td>
<td>Utility</td>
<td>1, 4</td>
</tr>
<tr>
<td>B</td>
<td>71</td>
<td>Cont</td>
<td>42</td>
<td>Chk_for_interrupts</td>
<td>1, 3</td>
</tr>
<tr>
<td>9</td>
<td>70</td>
<td>Cont</td>
<td>35</td>
<td>B_Cache_diag_mode</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>69</td>
<td>Cont</td>
<td>33</td>
<td>NMC_powerup</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>68</td>
<td>Cont</td>
<td>32</td>
<td>NMC_registers</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>67</td>
<td>Cont</td>
<td>D0</td>
<td>V_Cache_diag_mode</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>66</td>
<td>Cont</td>
<td>D2</td>
<td>O_bit_Diag_mode</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>65</td>
<td>Cont</td>
<td>DF</td>
<td>O_bit_debug</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>64</td>
<td>Cont</td>
<td>46</td>
<td>P_cache_diag_mode</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>63</td>
<td>Cont</td>
<td>35</td>
<td>B_cache_diag_mode</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>62</td>
<td>Cont</td>
<td>DE</td>
<td>B_Cache_tag_debug</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>61</td>
<td>Cont</td>
<td>DD</td>
<td>B_Cache_data_debug</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>60</td>
<td>Cont</td>
<td>DA</td>
<td>PB_Flush_cache</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>59</td>
<td>Halt</td>
<td>DC</td>
<td>NO_Memory_present</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>58</td>
<td>Cont</td>
<td>31</td>
<td>Memory_Setup_CSRs</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>57</td>
<td>Halt</td>
<td>30</td>
<td>Memory_Init_Bitmap</td>
<td>2, 1</td>
</tr>
<tr>
<td>7</td>
<td>56</td>
<td>Cont</td>
<td>91</td>
<td>CQBIC_powerup</td>
<td>1, 3</td>
</tr>
</tbody>
</table>

¹Field-replaceable unit key:

1 = KA50
2 = MS44
3 = Q22-bus option
4 = System power supply
5 = SCSI device or 2 devices with same target id
6 = ASYNC option board
7 = COMM option board (SYNC)
8 = SHAC option board

(continued on next page)
System Troubleshooting and Diagnostics
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Table 5-4 (Cont.)  KA50/51/55/56 Console Displays as Pointers to FRUs

<table>
<thead>
<tr>
<th>Error Hex LED</th>
<th>Normal Console Display</th>
<th>Default Action on Error</th>
<th>Falling Test Number</th>
<th>Test Description</th>
<th>FRU¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>55</td>
<td>Cont</td>
<td>90</td>
<td>CQBIC_registers</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>54</td>
<td>Cont</td>
<td>C6</td>
<td>SSC_powerup</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>53</td>
<td>Cont</td>
<td>52</td>
<td>SSC_Prog_timers</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>52</td>
<td>Cont</td>
<td>52</td>
<td>SSC_Prog_timers</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>51</td>
<td>Cont</td>
<td>53</td>
<td>SSC_TOY_Clock</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>50</td>
<td>Cont</td>
<td>C1</td>
<td>SSC_RAM_Data</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>49</td>
<td>Cont</td>
<td>34</td>
<td>SSC_ROM</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>48</td>
<td>Cont</td>
<td>C5</td>
<td>SSC_registers</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>47</td>
<td>Cont</td>
<td>55</td>
<td>Interval_Timer</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>46</td>
<td>Cont</td>
<td>4F</td>
<td>Memory_Data</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>45</td>
<td>Cont</td>
<td>4E</td>
<td>Memory_Byte</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>44</td>
<td>Cont</td>
<td>4B</td>
<td>Memory_Byte_Errors</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>43</td>
<td>Cont</td>
<td>4A</td>
<td>Memory_ECC_SBEs</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>42</td>
<td>Cont</td>
<td>4C</td>
<td>Memory_ECC_Logic</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>41</td>
<td>Cont</td>
<td>48</td>
<td>Memory_Addr_shorts</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>40</td>
<td>Cont</td>
<td>48</td>
<td>Memory_addr_shorts</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>39</td>
<td>Cont</td>
<td>48</td>
<td>Memory_addr_shorts</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>38</td>
<td>Cont</td>
<td>48</td>
<td>Memory_addr_shorts</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>37</td>
<td>Cont</td>
<td>48</td>
<td>Memory_addr_shorts</td>
<td>2, 1</td>
</tr>
<tr>
<td>8</td>
<td>36</td>
<td>Cont</td>
<td>48</td>
<td>Memory_addr_shorts</td>
<td>2, 1</td>
</tr>
</tbody>
</table>

¹Field-replaceable unit key:
1 = KA50
2 = M344
3 = Q22-bus option
4 = System power supply
5 = SCSI device or 2 devices with same target id
6 = ASYNC option board
7 = COMM option board (SYNC)
8 = SHAC option board

(continued on next page)
### System Troubleshooting and Diagnostics

#### 5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

**Table 5–4 (Cont.) KA50/51/55/56 Console Displays as Pointers to FRUs**

<table>
<thead>
<tr>
<th>Error Hex LED</th>
<th>Normal Console Display</th>
<th>Default Action on Error</th>
<th>Failing Test Number</th>
<th>Test Description</th>
<th>FRU¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>Cont</td>
<td>48</td>
<td>Memory_addr_shorts</td>
<td>2, 1</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Cont</td>
<td>48</td>
<td>Memory_addr_shorts</td>
<td>2, 1</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Cont</td>
<td>4D</td>
<td>Memory_address</td>
<td>2, 1</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Cont</td>
<td>47</td>
<td>Memory_Refresh</td>
<td>2, 1</td>
<td></td>
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<tr>
<td>8</td>
<td>Halt</td>
<td>40</td>
<td>Memory_count_pages</td>
<td>2, 1</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Cont</td>
<td>40</td>
<td>Memory_count_pages</td>
<td>2, 1</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Cont</td>
<td>E4</td>
<td>DZ</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>Cont</td>
<td>54</td>
<td>Virtual_Mode</td>
<td>1</td>
<td></td>
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<tr>
<td>9</td>
<td>Cont</td>
<td>37</td>
<td>Cache_w_memory</td>
<td>1, 2</td>
<td></td>
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<tr>
<td>C</td>
<td>Cont</td>
<td>C2</td>
<td>SSC_RAM_Data_Addr</td>
<td>1</td>
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<tr>
<td>7</td>
<td>Cont</td>
<td>80</td>
<td>CQBC_memory</td>
<td>1, 2</td>
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<td>9</td>
<td>Cont</td>
<td>37</td>
<td>Cache_w_memory</td>
<td>1, 2</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>Cont</td>
<td>51</td>
<td>FPA</td>
<td>1</td>
<td></td>
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<td>5</td>
<td>Cont</td>
<td>E2</td>
<td>SCSI_MAP</td>
<td>1</td>
<td></td>
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<tr>
<td>5</td>
<td>Cont</td>
<td>E0</td>
<td>SCSI</td>
<td>1, 5</td>
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<td>4</td>
<td>Cont</td>
<td>5F</td>
<td>SGEC</td>
<td>1</td>
<td></td>
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<tr>
<td>5</td>
<td>Cont</td>
<td>5C</td>
<td>SHAC</td>
<td>8, 1</td>
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<tr>
<td>B</td>
<td>Cont</td>
<td>9A</td>
<td>INTERACTION</td>
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<tr>
<td>7</td>
<td>Cont</td>
<td>83</td>
<td>QZA_Intlpbk1</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Cont</td>
<td>84</td>
<td>QZA_Intlpbk2</td>
<td>3</td>
<td></td>
</tr>
</tbody>
</table>

¹Field-replaceable unit key:

1 = KA50
2 = MS44
3 = Q22-bus option
4 = System power supply
5 = SCSI device or 2 devices with same target id
6 = ASYNC option board
7 = COMM option board (SYNC)
8 = SHAC option board

(continued on next page)
System Troubleshooting and Diagnostics

5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Table 5-4 (Cont.)  KA50/51/55/56 Console Displays as Pointers to FRUs

<table>
<thead>
<tr>
<th>On Error Hex LED</th>
<th>Normal Console Display</th>
<th>Default Action on Error</th>
<th>Failing Test Number</th>
<th>Test Description</th>
<th>FRU 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-Up Tests (Script A1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>15</td>
<td>Cont</td>
<td>85</td>
<td>QZA_memory</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>14</td>
<td>Cont</td>
<td>86</td>
<td>QZA_DMA</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>13</td>
<td>Cont</td>
<td>63</td>
<td>QDSS_any</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>12</td>
<td>Cont</td>
<td>63</td>
<td>QDSS_any</td>
<td>3</td>
</tr>
<tr>
<td>B</td>
<td>11</td>
<td>Cont</td>
<td>DB</td>
<td>Speed</td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>10</td>
<td>Cont</td>
<td>EC</td>
<td>ASYNC</td>
<td>6, 1</td>
</tr>
<tr>
<td>7</td>
<td>09</td>
<td>Cont</td>
<td>E8</td>
<td>SYNC</td>
<td>7, 1</td>
</tr>
<tr>
<td>C</td>
<td>08</td>
<td>Cont</td>
<td>52</td>
<td>SSC_Prog_timers</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>07</td>
<td>Cont</td>
<td>52</td>
<td>SSC_Prog_timers</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>06</td>
<td>Cont</td>
<td>53</td>
<td>SSC_TOY_Clock</td>
<td>1</td>
</tr>
<tr>
<td>C</td>
<td>05</td>
<td>Cont</td>
<td>C1</td>
<td>SSC_RAM_Data</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>04</td>
<td>Cont</td>
<td>55</td>
<td>Interval_Timer</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>03</td>
<td>Cont</td>
<td>41</td>
<td>Board_Reset</td>
<td>1, 3</td>
</tr>
</tbody>
</table>

1Field-replaceable unit key:

1 = KA50
2 = MS44
3 = Q22-bus option
4 = System power supply
5 = SCSI device or 2 devices with same target id
6 = ASYNC option board
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8 = SHAC option board

5.3.1 FE Utility

In addition to the diagnostic console display and the LED code, the FE utility dumps the diagnostic state to the console (Example 5–12). This state indicates the major and minor test code of the test that failed, the 10 parameters associated with the test, and additional diagnostic state information.
System Troubleshooting and Diagnostics

5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Example 5–12 FE Utility Example

```plaintext
>>> FE

Bitmap=00FF3000, Length=00001000, Checksum=807F, Busmap=00FF8000
Test_number=00, Subtest=00, Loop Subtest=00, Error_type=00
Error_vector=0060, Severity=02, Last_exception_PC=20057C37
Total error_count=0004, Led display=08, Console display=81, save_mchk_code=00
parameter 1=00000002 2=00000000 3=2000146A 4=00000000 5=20057400
parameter 6=00000001 7=00000000 8=00000020 9=00000000 10=00000000
previous errors, Test Subtest Loop Subtest Error_Type
Test 81 02 00 FE Test 40 06 00 FF Test 03 00 FF Test E4 02 00 FF
Flags=FFF FFFFFF 0408443E BCACHE Disable=06 KA50 128KB BC 14.0 ns
Return_stack=201406CC, Subtest_pc=2005D7FF, Timeout=000007D0

>>>```

5.3.2 Overriding Halt Protection

The ROM diagnostics are run in halt-protected space during execution after power-up of the system. During this time they cannot normally be halted with the BREAK key or the HALT button. After power-up is complete, all diagnostics including the power-up script (A1) or (0) are run with halts enabled allowing a user to stop a script or test. The preferred method to stop scripts is to use CONTROL C first.

5.3.3 Isolating Memory Failures

This section describes procedures for isolating memory subsystem failures.

Memory tests numbers are DC, 31, 30, 4F, 4E, 4B, 4A, 4C, 48, 4D, 47 and 40. All of these tests are run during power-up.

Normally, if one or more of these tests fail during power-up at the end of power-up the diagnostic executive will execute the SHOW MEMORY command automatically to help identify the memory failure. In all cases of a memory failure, the primary means to isolate to the FRU is to use the SHOW MEMORY command.

Example 5–13 shows a memory failure due to a missing SIMM. In this case only one 16-MB set (4 SIMMs of 4 MB each) is present, and one of these is missing. Because of this, test DC fails and the power-up script is halted because no usable memory is present. At the end, SHOW MEMORY is automatically executed before the test is halted. In this example, SIMM set 1 (1E,1F,1G,1H) is present but SIMM 1F is either missing or not correctly installed in its socket.
System Troubleshooting and Diagnostics

5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Example 5–13  Failure Due to a Missing SIMM (One 16 Mbyte Set)

KA50-A V1.2, VMB 2.14
Performing normal system tests.
72..71..69..68..67..66..65..64..63..62..61..60..59..

? Test Subtest_DC_88  Loop_Subtest=05  Err_Type=FF  DE NO Memory present.lis
Vec=0000  Prev_Errs=0000  P1=C90AC90A  P2=00000000  P3=00000000  P4=00000006
P5=00000000  P6=7F7FFF33  P7=00000000  P8=00000000  P9=FFFFF000  P10=200636E4
r0=00000000  r1=21018000  r2=C90AC90A  r3=00000000  r4=01000000  r5=04000000
r6=00000000  r7=00000000  r8=00000000  r9=20140758  r10=FFFFFFFE  r11=FFFFFFFE

dser=0000  cesr=00000000  intmsk=00  icsr=01  pcsts=FA00  pcadr=FFFFFFF8  pcctl=FE13
ctcl=00000000  bcetst=03E0  bcddst=0000  cefst=0001EC20  ncest=00
nmcdst=01FE40  mesr=00000000

Error: SIMM Set 1 (1E,1F,1G,1H), SSR = C90A
SIMM_1E = 16MB  SIMM_1F = 00MB ??  SIMM_1G = 16MB  SIMM_1H = 16MB

Total of OMB, 0 good pages, 0 bad pages, 0 reserved pages
Normal operation not possible.

>>> ________________________________ Note ________________________________

The value listed by each SIMM is either 16 MB or 64 MB which indicates the full size of the set of SIMMs if all are present.

____________________ ACTION: _______________________

• If SIMM 1F is missing, install a SIMM.
• If SIMM 1F is present in socket, reseat the SIMM.
• If reseating SIMM 1F does not fix the problem, replace the SIMM with a new SIMM.
• At this point the system board is probably bad. If no new system board is available, try moving the SIMMs to the other set of sockets.

Example 5–14 shows a memory failure due to a missing SIMM. In this case two 16-MB sets (4 SIMMs of 4 MB each) are present with one SIMM missing in Set 1. Since one of memory is fully usable, all testing is completed. At the end SHOW MEMORY is automatically executed as before. SIMM 1H is missing or not installed correctly. The system is usable but with only 16 MB of memory instead of 32 MB.
System Troubleshooting and Diagnostics

5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Example 5–14  Failure Due to a Missing SIMM (Two 16 Mbyte Sets)

KA50-A T1.2-156, VMB 2.14
Performing normal system tests.
72..71..70..69..68..67..66..65..64..63..62..61..60..59..58..

? Test Subtest 31.06 Loop Subtest=05 Err Type=FF DE Memory Setup CSRs lis
Vec=0000 Prev Errs=0000 P1=C94AC94A P2=01000000 P3=00000002 P4=00000000
P5=25800000 P6=FFFFFFFF P7=00000000 P8=00000000 P9=0000C94A P10=C94AC14A
r0=00000008 r1=21018000 r2=C94AC94A r3=81000000 r4=01000000 r5=04000000
r6=00000002 r7=21018048 r8=00000000 r9=20140758 r10=FFFFFFFE r11=FFFFFFFF

dser=0000 cesr=00000000 intmsk=00 icsr=01 pcsts=FA00 pcadr=FFFFFF8F pcctl=FE13
cc1=00000006 bcetsts=0360 bcedsts=0F00 cefststs=00206E20 nest=00
mmcsr=01FFFE00 mesr=00000000

57..56..55..54..53..52..51..50..49..48..47..46..45..44..43..42..
41..40..39..38..37..36..35..34..33..32..31..30..29..28..27..26..
25..24..23..22..21..20..19..18..17..16..15..14..13..12..11..10..
09..08..07..06..05..04..03..

16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 00000000 to 00FFFFFF, 16MB, 32768 good pages, 0 bad pages

Error: SIMM Set 1 (1E,1F,1G,1H), SSR = C94A
SIMM_IE = 16MB SIMM_IF = 16MB SIMM_1G = 16MB SIMM_1H = 00MB ??

Total of 16MB, 32768 good pages, 0 bad pages, 104 reserved pages
Normal operation not possible.

ACTION:

• If SIMM 1H is missing, install a SIMM.
• If SIMM 1H is present in socket, reseat the SIMM.
• If reseating SIMM 1H does not fix the problem then replace the SIMM with a new SIMM.
• At this point the system board is probably bad.

Example 5–15 shows a memory failure due to a bad SIMM. In this case two 16-MB sets (4 SIMMs of 4 MB each) are present with one bad SIMM. SIMM 1H is marked as being bad.
System Troubleshooting and Diagnostics
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Example 5–15  Failure Due to a Bad SIMM

KA50-A V1.2, VMB 2.14
Performing normal system tests.
72..71..70..69..68..67..66..65..64..63..62..61..60..59..58..57..
56..55..54..53..52..51..50..49..48..47..46..45..44..43..42..41..
40..39..38..37..36..35..34..33..32..31..30..

? Test_Subtest_40_06  Loop_Subtest=00  Err_Type=FF  DE_Memory_count_pages.lis
29..28..27..26..25..24..23..22..21..20..19..18..17..16..15..14..
13..12..11..10..09..08..07..06..05..04..03..

16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 00000000 to 00FFFFFF, 16MB, 32768 good pages, 0 bad pages

Error: SIMM Set 1 (1E,1F,1G,1H), SSR = C14A
SIMM_1E = 16MB  SIMM_1F = 16MB  SIMM_1G = 16MB  SIMM_1H = 16MB ??
Memory Set 1: 01000000 to 01FFFFFF, 16MB, 0 good pages, 32768 bad pages

Total of 32MB, 32768 good pages, 32768 bad pages, 112 reserved pages

>>> ACTION

• Reseat the SIMM 1H.
• If reseating SIMM 1H does not fix the problem then replace the SIMM with a new SIMM.
• At this point the system board is probably bad.

Example 5–16 indicates that a large SIMM is mixed in with a set of small SIMMs. If a full set of SIMMs is present and one or more is the incorrect size then the diagnostic code will configure the set as a small set and run the tests. In this example, SIMM 1G is the wrong size SIMM. Because the set is configured as a small set, it is usable as a 16-MB set.
System Troubleshooting and Diagnostics
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

Example 5-16 SIMM Wrong Size

Error: SIMM Set 1 (1E,1F,1G,1H), SSR = C14A
SIMM 1E = 16MB SIMM 1F = 16MB SIMM 1G = 64MB ?? SIMM 1H = 16MB
Memory Set 1: 01000000 to 01FFFFFF, 16MB, 32768 good pages, 0 bad pages

ACTION:
Replace SIMM 1G with one of the correct size.
The diagnostics cannot always determine which SIMM caused a failure. If this occurs and more than one set is present, usually the failing set can be identified by using the SHOW MEMORY command.

>>>SHOW MEMORY

16 MB RAM, SIMM Set (0A,0B,0C,0D) present
Memory Set 0: 00000000 to 00FFFFFF, 16MB, 32768 good pages, 0 bad pages

16 MB RAM, SIMM Set (1E,1F,1G,1H) present
Memory Set 1: 01000000 to 01FFFFFF, 16MB, 32768 good pages, 32768 bad pages
Total of 32MB, 32768 good pages, 32768 bad pages, 112 reserved pages

ACTION:
Replace SIMM set 1 (1E,1F,1G,1H).
After installing a new set of SIMMs and successfully running power-up tests, run memory test script A8.

>>>T A8

Note

Script A9 is another memory test script. This script will stop on the first occurrence of any error. It will also stop on a soft error. If a failure occurs in A9 and if A9 then runs successfully 10 times and script A8 runs without error the problem is a soft error and does not require action.

Note

If a memory failure is marked in the bitmap, it will not be erased until either the system is powered up or the bitmap placing test is run with
5.3 Power-On Self-Test (POST) and ROM-Based Diagnostic (RBD) Failures

parameter P4 set to 0 to rebuild the bitmap.

To force rebuilding the bitmap to all good memory, enter the following commands:

T 30 0 0 0 0 ; T 30 will not work by itself.
T 0 ; rerun powerup script

5.4 Using MOP Ethernet Functions to Isolate Failures

The console requester can receive LOOPED_DATA messages from the server by sending out a LOOP_DATA message using NCP to set this up. An example follows.

Identify the Ethernet adapter address for the system under test (system 1) and attempt to boot over the network.

***system 1 (system under test)***

>>>SHOW ETHERNET
Ethernet Adapter
-EXA0 (08-00-2B-28-18-2C)
>>>BOOT EXA0
(RBOOT/R5:2 EXA0)

2..
-EXA0
Retrying network bootstrap.

Unless the system is able to boot, the “Retrying network bootstrap” message will display every 8–12 minutes.

Identify the system's Ethernet circuit and circuit state, enter the SHOW KNOWN CIRCUITS command from the system conducting the test (system 2).

***system 2 (system conducting test)***

5 MCR NCP
NCP>SHOW KNOWN CIRCUITS

Known Circuit Volatile Summary as of 14-NOV-1991 16:01:53

<table>
<thead>
<tr>
<th>Circuit</th>
<th>State</th>
<th>Loopback</th>
<th>Adjacent Routing Node</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISA-0</td>
<td>on</td>
<td></td>
<td>25.1023 (LAR25)</td>
</tr>
</tbody>
</table>
System Troubleshooting and Diagnostics
5.4 Using MOP Ethernet Functions to Isolate Failures

NCP> SET CIRCUIT ISA-0 STATE OFF
NCP> SET CIRCUIT ISA-0 SERVICE ENABLED
NCP> SET CIRCUIT ISA-0 STATE ON
NCP> LOOP CIRCUIT ISA-0 PHYSICAL ADDRESS 08-00-2B-28-18-2C WITH ERRORS
NCP> EXIT

If the loopback message was received successfully, the NCP prompt will reappear with no messages.

The following two examples show how to perform the Loopback Assist Function using another node on the network as an assistant (system 3) and the system under test as the destination. Both the assistant and the system under test are attempting to boot from the network. We will also need the physical address of the assistant node.

***system #3 (loopback assistant)***

>>> SHOW ETHERNET
Ethernet Adapter
-EZAO (08-00-2B-1E-76-9E)
>>> b ezao
(BOOT/R5:2 EZAO)

...
-EZAO
Retrying network bootstrap.

***system 2***

NCP> LOOP CIRCUIT ISA-0 PHYSICAL ADDRESS 08-00-2B-28-18-2C ASSISTANT PHYSICAL ADDRESS 08-00-2B-1E-76-9E WITH MIXED COUNT 20 LENGTH 200 HELP FULL
NCP>

Instead of using the physical address, you could use the assistant node's area address. When using the area address, system 3 is running the OpenVMS operating system.

***system 3***

SNCR NCP

NCP> SHOW NODE KITCH

Executor node = 25.900 (KITCH)
State = on
Identification = DECnet-VAX V5.4-1, OpenVMS V5.4-2
Active links = 2

NCP> SHOW KNOWN LINES CHARACTERISTICS

Known Line Volatile Characteristics as of 27-FEB-1992 11:20:50
Line = ISA-0
System Troubleshooting and Diagnostics

5.4 Using MOP Ethernet Functions to Isolate Failures

Receive buffers = 6
Controller = normal
Protocol = Ethernet
Service timer = 4000
Hardware address = 08-00-28-18-2C-9E
Device buffer size = 1498

NCP>SET CIRCUIT ISA-0 STATE OFF
NCP>SET CIRCUIT ISA-0 SERVICE ENABLED
NCP>SET CIRCUIT ISA-0 STATE ON
NCP>EXIT
$

***system 2***
NCP>EXIT
$

Note

The kernel's Ethernet buffer is 1024 bytes deep for the LOOP functions and will not support the maximum 1500-byte transfer length.

In order to verify that the address is reaching this node, a remote node can examine the status of the periodic SYSTEM_IDs sent by the KA50/51/55/56 Ethernet server. The SYSTEM_ID is sent every 8–12 minutes using NCP as in the following example:

***system 2***

NCP>EXIT

5 TYPE ETHER.LIS

Circuit name = ISA-0
Surveillance flag = enabled
Elapsed time = 00:09:37
Physical address = 08-00-28-18-2C
Time of last report = 27-Feb-11:50:34
Maintenance version = V4.0.0
Function list = Loop, Multi-block loader, Boot, Data link counters
Hardware address = 08-00-28-18-2C
Device type = ISA

Depending on your network, the file used to receive the output from the SHOW MODULE CONFIGURATOR command may contain many entries, most of which do not apply to the system you are testing. It is helpful to use an editor to search the file for the Ethernet hardware address of the system under test.
System Troubleshooting and Diagnostics
5.4 Using MOP Ethernet Functions to Isolate Failures

Existence of the hardware address verifies that you are able to receive the address from the system under test.

5.5 Interpreting User Environmental Test Package (UETP) OpenVMS Failures

When UETP encounters an error, it reacts like a user program. It either returns an error message and continues, or it reports a fatal error and terminates the image or phase. In either case, UETP assumes the hardware is operating properly and it does not attempt to diagnose the error.

If the cause of an error is not readily apparent, use the following methods to diagnose the error:

- **OpenVMS Error Log Utility**—Run the Error Log Utility to obtain a detailed report of hardware and system errors. Error log reports provide information about the state of the hardware device and I/O request at the time of each error. For information about running the Error Log Utility, refer to the *OpenVMS Error Log Utility Manual* and Section 5.2 of this manual.

- **Diagnostic facilities**—Use the diagnostic facilities to test exhaustively a device or medium to isolate the source of the error.

5.5.1 Interpreting UETP Output

You can monitor the progress of UETP tests at the terminal from which they were started. This terminal always displays status information, such as messages that announce the beginning and end of each phase and messages that signal an error.

The tests send other types of output to various log files, depending on how you started the tests. The log files contain output generated by the test procedures. Even if UETP completes successfully, with no errors displayed at the terminal, it is good practice to check these log files for errors. Furthermore, when errors are displayed at the terminal, check the log files for more information about their origin and nature.

5.5.1.1 UETP Log Files

UETP stores all information generated by all UETP tests and phases from its current run in one or more UETP.LOG files, and it stores the information from the previous run in one or more OLDUETP.LOG files. If a run of UETP involves multiple passes, there will be one UETP.LOG or one OLDUETP.LOG file for each pass.
At the beginning of a run, UETP deletes all OLĐUETPLOG files, and renames any UETPLOG files to OLDUETPLOG. Then UETP creates a new UETPLOG file and stores the information from the current pass in the new file. Subsequent passes of UETP create higher versions of UETPLOG. Thus, at the end of a run of UETP that involves multiple passes, there is one UETPLOG file for each pass. In producing the files UETPLOG and OLĐUETPLOG, UETP provides the output from the two most recent runs.

If the run involves multiple passes, UETPLOG contains information from all the passes. However, only information from the latest run is stored in this file. Information from the previous run is stored in a file named OLĐUETPLOG. Using these two files, UETP provides the output from its tests and phases from the two most recent runs.

The cluster test creates a NETSERVERLOG file in SYS$TEST for each pass on each system included in the run. If the test is unable to report errors (for example, if the connection to another node is lost), the NETSERVERLOG file on that node contains the result of the test run on that node. UETP does not purge or delete NETSERVERLOG files; therefore, you must delete them occasionally to recover disk space.

If a UETP run does not complete normally, SYS$TEST might contain other log files. Ordinarily these log files are concatenated and placed within UETPLOG. You can use any log files that appear on the system disk for error checking, but you must delete these log files before you run any new tests. You may delete these log files yourself or rerun the entire UETP, which checks for old UETPLOG files and deletes them.

5.5.1.2 Possible UETP Errors
This section is intended to help you identify problems you might encounter running UETP.

The following are the most common failures encountered while running UETP:

- Wrong quotas, privileges, or account
- UETINIT01 failure
- Ethernet device allocated or in use by another application
- Insufficient disk space
- Incorrect VAXcluster setup
- Problems during the load test
- DECnet–VAX error
- Lack of default access for the FAL object
System Troubleshooting and Diagnostics
5.5 Interpreting User Environmental Test Package (UETP) OpenVMS Failures

- Errors logged but not displayed
- No PCB or swap slots
- Hangs
- Bug checks and machine checks

For more information refer to the *VAX 3520, 3540 OpenVMS Installation and Operations (ZKS166)* manual.

5.6 Using Loopback Tests to Isolate Failures

You can use external loopback tests to isolate problems with the console port, and Ethernet controller (SGEC chip).

5.6.1 Testing the Console Port

To test the console port at power-up, set the Power-Up Mode switch on the console module to the Loop Back Test Mode position (bottom) and install an H3103 loopback connector into the MMJ. The H3103 connects the console port transmit and receive lines. At power-up, the SLU_EXT_LOOPBACK test then runs a continuous loopback test.

While the test is running, the LED display on the console module should alternate between 6 and 3. A value of 6 latched in the display indicates a test failure. If the test fails, one of the following parts is faulty: the KA50/51/55/56 or the cabling.

To test out to the end of the console terminal cable:
1. Plug the MMJ end of the console terminal cable into the back BA42B.
2. Disconnect the other end of the cable from the terminal.
3. Place an H8572 adapter into the disconnected end of the cable.
4. Connect the H3103 to the H8572.
5. Cycle power and observe the LED.

5.6.2 Embedded Ethernet Loopback Testing

Note

Before running Ethernet loopback tests, check that the problem is not due to a missing terminator on a ThinWire T-connector.

5–58 System Troubleshooting and Diagnostics
Test 5F is the internal loopback test for SGEC (Ethernet controller).

>>> T 5F

For an external SGEC loopback, enter "1".

>>> T 5F 1

Before running test 5F on the ThinWire Ethernet port, connect an H8223 T-connector with two H8225 terminators.

Before running test 5F on the standard Ethernet port, you must have a 12-22196-02 loopback connector installed.

----------------------------------------------- Note -----------------------------------------------

Make sure the Ethernet Connector Switch is set for the correct Ethernet port.

-----------------------------------------------

T 59 polls other nodes on Ethernet to verify SGEC functionality. The Ethernet cable must be connected to a functioning Ethernet. A series of MOP messages are generated; look for response messages from other nodes.

>>> T 59

Reply received from node: AA-00-04-00-FC-64
Total responses: 1
Reply received from node: AA-00-04-00-47-16
Total responses: 2
Reply received from node: 08-00-28-15-48-70
Total responses: 3

.
.
.

Reply received from node: AA-00-04-00-17-14
Total responses: 25
>>>
### System Troubleshooting and Diagnostics
#### 5.6 Using Loopback Tests to Isolate Failures

#### Table 5-5 Loopback Connectors for Common Devices

<table>
<thead>
<tr>
<th>Device</th>
<th>Module Loopback</th>
<th>Cable Loopback</th>
</tr>
</thead>
<tbody>
<tr>
<td>CXA16/CXB16</td>
<td>H3103 + H8572&lt;sup&gt;1&lt;/sup&gt;</td>
<td>–</td>
</tr>
<tr>
<td>CXY08</td>
<td>H3046 (50-pin)</td>
<td>H3197 (25-pin)</td>
</tr>
<tr>
<td>DIV32</td>
<td>H3072</td>
<td>–</td>
</tr>
<tr>
<td>DPV11</td>
<td>12-15336-10 or H325</td>
<td>H329 (12-27351-01)</td>
</tr>
<tr>
<td>DRQB3</td>
<td>–</td>
<td>17-01481-01 (from port 1 to port 2)</td>
</tr>
<tr>
<td>DRV1W</td>
<td>70-24767-01</td>
<td>–</td>
</tr>
<tr>
<td>DZQ11</td>
<td>12-15336-10 or H325</td>
<td>H329 (12-27351-01)</td>
</tr>
<tr>
<td>Ethernet&lt;sup&gt;2&lt;/sup&gt;</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>IBQ01</td>
<td>IBQ01-TA</td>
<td>–</td>
</tr>
<tr>
<td>IEQ11</td>
<td>17-01988-01</td>
<td>–</td>
</tr>
<tr>
<td>KMOV1A</td>
<td>H3255</td>
<td>H3251</td>
</tr>
<tr>
<td>KZQSA</td>
<td>12-30552-01</td>
<td>–</td>
</tr>
<tr>
<td>LPV11</td>
<td>12-15336-11</td>
<td>–</td>
</tr>
</tbody>
</table>

<sup>1</sup>Use the appropriate cable to connect transmit-to-receive lines. H3101 and H3103 are double-ended cable connectors.

<sup>2</sup>For ThinWire, use H8223-00 plus two H8225-00 terminators. For standard Ethernet, use 12-22196-02.
FEPROM Firmware Update

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95, and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q-bus and DSSI, will appear on the console and/or printouts from time to time.

KA50/51/55/56 firmware is located on four chips, each 128 K by 8 bits of FLASH programmable EPROMs, for a total of 512 Kbytes of ROM. (A FLASH EPROM (FEPROM) is a programmable read-only memory that uses electrical (bulk) erasure rather than ultraviolet erasure.)

FEPROMs provide nonvolatile storage of the CPU power-up diagnostics, console interface, and operating system primary bootstrap (VMB). An advantage of this technology is that the entire image in the FEPROMs may be erased, reprogrammed, and verified in place without removing the CPU module or replacing components.

A slight disadvantage to the FEPROM technology is that the entire part must be erased before reprogramming. Hence, there is a small "window of vulnerability" when the CPU has inoperable firmware. Normally, this window is less than 30 seconds. Nonetheless, an update should be allowed to execute undisturbed.

Firmware updates are provided through a package called the Firmware Update Utility. A Firmware Update Utility contains a bootable image, which can be booted from tape or Ethernet, that performs the FEPROM update. Firmware update packages, like software, are distributed through Digital's SSB. Service engineers are notified of updates through a service blitz or Engineering Change Order (ECO)/Field Change Order (FCO) notification.
FEPROM Firmware Update

Note

The NVAX CPU chip has an area called the Patchable Control Store (PCS), which can be used to update the microcode for the CPU chip. Updates to the PCS require a new version of the firmware.

A Firmware Update Utility image consists of two parts, the update program and the new firmware, as shown in Figure 6–1. The update program uniformly programs, erases, reprograms, and verifies the entire FEPROM.

Figure 6–1  Firmware Update Utility Layout

<table>
<thead>
<tr>
<th>Update Program</th>
</tr>
</thead>
<tbody>
<tr>
<td>New Firmware Image</td>
</tr>
</tbody>
</table>

MLQ-007271

Once the update has completed successfully, normal operation of the system may continue. The operator may then either halt or reset the system and reboot the operating system.

6.1 Preparing the Processor for a FEPROM Update

Complete the following steps to prepare the processor for a FEPROM update:

1. The system manager should perform operating system shutdown.

2. Enter console mode by pressing the Halt button once to halt the system. If the Break Enable/Disable switch on the console module is set to enable (indicated by 1), you can halt the system by pressing the Break key on the console terminal.
6.2 Updating Firmware via Ethernet

To update firmware via the Ethernet, the "client" system (the target system to be updated) and the "server" system (the system that serves boot requests) must be on the same Ethernet segment. The Maintenance Operation Protocol (MOP) is the transport used to copy the network image.

Use the following procedure to update firmware via the Ethernet:

1. Enable the server system's NCP circuit using the following OpenVMS commands:

   $ MCR NCP
   NCP>SET CIRCUIT <circuit> STATE OFF
   NCP>SET CIRCUIT <circuit> SERVICE ENABLED
   NCP>SET CIRCUIT <circuit> STATE ON
FEPROM Firmware Update
6.2 Updating Firmware via Ethernet

Where <circuit> is the system Ethernet circuit. Use the SHOW KNOWN CIRCUITS command to find the name of the circuit.

_________________________ Note _______________________

The SET CIRCUIT STATE OFF command will bring down the system's network.

_________________________ Note _______________________

2. Copy the file containing the updated code to the MOM$LOAD area on the server (this procedure may require system privileges). Refer to the Firmware Update Utility Release Notes for the Ethernet bootable filename. Use the following command to copy the file:

    $ COPY <filename>.SYS MOM$LOAD:*.*

    Where <filename> is the Ethernet bootable filename provided in the release notes.

3. On the client system, enter the command BOOT/100 EZ at the console prompt (>>>).

    The system then prompts you for the name of the file.

_________________________ Note _______________________

    Do NOT type the "SYS" suffix when entering the Ethernet bootfile name. The MOP load protocol only supports 15 character filenames.

_________________________ Caution _______________________

4. After the FEPROM upgrade program is loaded, simply type "Y" at the prompt to start the FEPROM blast. Example 6–1 provides a console display of the FEPROM update program.

_________________________ Caution _______________________

    Once you enter the bootfile name, do not interrupt the FEPROM blasting program, as this can damage the CPU module. The program takes several minutes to complete.
Example 6–1  FEPROM Update via Ethernet

***** On Server System *****

$ MCR NCP
NCP>SET CIRCUIT ISA-0 STATE OFF
NCP>SET CIRCUIT ISA-0 SERVICE ENABLED
NCP>SET CIRCUIT ISA-0 STATE ON
NCP>EXIT

$ COPY KA50_V41_R1.SYS MOM$LOAD:*.*

$ 6

***** On Client System *****

>>>b/100 eza0
(BOOT/R5:100 EZA0)
2.. Bootfile: ka50_v12
-EZA0
1..0..

FEPROM update program

---CAUTION---

--- Executing this program will change your current FEPROM ---

Do you want to continue [Y/N] ? : y

Blasting in V1.2-41. The program will take at most several minutes.

DO NOT ATTEMPT TO INTERRUPT PROGRAM EXECUTION
For this may result in loss of operable state !!!

10987654321

FEPROM Programming successful

706 HLT INST

PC = 00008E24

>>>

Note

If the update does not work, check to be sure the "write enable"
on-board jumper is installed (see Figure 6–2).

5. Recycle power or enter "T 0" at the console prompt (>>>).

6. If the customer requires, return the jumper on the module to the "write
   disable mode" setting.
6.3 Updating Firmware via Tape

To update firmware via tape, the system must have a TZ30, TF85, TK70, TK50 or TLZ04 tape drive.

If you need to make a bootable tape, copy the bootable image file to a tape as shown in the following example. Refer to the release notes for the name of the file.

```
$ INIT MKA500:"VOLUME_NAME"
$ MOUNT/BLOCK_SIZE = 512  MKA500:"VOLUME_NAME"
$ COPY/CONTIG<file_name> MKA500:<file_name>
$ DISMOUNT MKA500
$
```

Use the following procedure to update firmware via tape:

1. Be sure the on board jumper is in the correct ("write enable mode") position (Section 6.1).

2. At the console prompt (>>>, enter the BOOT/100 command for the tape device, for example: BOOT/100 MKA500.

   Use the SHOW DEVICE command if you are not sure of the device name for the tape drive.

   The system prompts you for the name of the file. Enter the bootfile name.

3. After the FEPROM upgrade program is loaded, simply type "Y" at the prompt to start the FEPROM blast. Example 6–2 provides a console display of the FEPROM update program.

   ----------------------------------------------------------------------------------
   Caution
   ----------------------------------------------------------------------------------

   Once you enter the bootfile name, do not interrupt the FEPROM blasting program, as this can damage the CPU module. The program takes several minutes to complete.

   ----------------------------------------------------------------------------------

4. Press the Restart button on the SCP or enter "T 0" at the console prompt (>>).

5. If the customer requires, return the jumper on the CPU module to the "write disable mode" setting.
Example 6-2  FEPROM Update via Tape

```plaintext
>>> BOOT/100 MKA500
(BOOT/R5:100 MKA500)

2.
Boot file: MKA50_V41_12
-WMA500

1..0..
FEPROM update program

---CAUTION---

--- Executing this program will change your current FEPROM ---

Do you want to continue [Y/N] ? : y

Blasting in V1.2-41. The program will take at most several minutes.

DO NOT ATTEMPT TO INTERRUPT PROGRAM EXECUTION
Doing so may result in loss of operable state!!!

+-------------------------------------
10...9...8...7...6...5...4...3...2...1...0

FEPROM Programming successful

206 HLT INST
    PC = 0000BE24

>>>```

6.4 FEPROM Update Error Messages

The following is a list of error messages generated by the FEPROM update program and actions to take if the errors occur.

**MESSAGE:**
?? ERROR update enable jumper is disconnected
unable to blast ROMs...

**ACTION:**
Reposition update enable jumper (Section 6.1).

**MESSAGE:**
?? ERROR, FEPROM programming failed

**ACTION:**
Turn off the system, then turn it on. If you see the banner message as expected, reenter console mode and try booting the update program again.
If you do not see the usual banner message, replace the CPU module.
Patchable Control Store (PCS) Loading Error Messages

The following is a list of error messages that may appear if there is a problem with the PCS. The PCS is loaded as part of the power-up stream (before ROM-based diagnostics are executed).

MESSAGE:
CPU is not an NVAX
COMMENT:
CPU_TYPE as read in NVAX SID is not = 19 (decimal), as is should be for an NVAX processor.

MESSAGE:
Microcode patch/CPU rev mismatch
COMMENT:
Header in microcode patch does not match MICROCODE_REV as read in NVAX SID.

MESSAGE:
PCS Diagnostic failed
COMMENT:
Something is wrong with the PCS. Replace the NVAX chip (or CPU module).
A

Address Assignments

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95 and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q-bus and DSSI, will appear on the console and/or printouts from time to time.

A.1 KA50/51/55/56 General Local Address Space Map
### Address Assignments

#### A.1 KA50/51/55/56 General Local Address Space Map

**VAX Memory Space**

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 0000 - 1FFFF FFFF</td>
<td>Local Memory Space (512MB)</td>
</tr>
</tbody>
</table>

**VAX I/O Space**

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 0000 - 2000 1FFFF</td>
<td>Local Q22-Bus I/O Space (8KB)</td>
</tr>
<tr>
<td>2000 2000 - 2003 FFFF</td>
<td>Reserved Local I/O Space (24KB)</td>
</tr>
<tr>
<td>2008 0000 - 201F FFFF</td>
<td>Local Register I/O Space (1.5MB)</td>
</tr>
<tr>
<td>2020 0000 - 23FF FFFF</td>
<td>Reserved Local I/O Space (62.5MB)</td>
</tr>
<tr>
<td>2400 0000 - 27FF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>2008 0000 - 2BFF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>2C00 0000 - 2FFF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>3000 0000 - 303F FFFF</td>
<td>Local Q22-Bus Memory Space (4MB)</td>
</tr>
<tr>
<td>3040 0000 - 33FF FFFF</td>
<td>Reserved Local I/O Space (60MB)</td>
</tr>
<tr>
<td>3400 0000 - 37FF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>3800 0000 - 3BFF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>3C00 0000 - 3FFF FFFF</td>
<td>Reserved Local I/O Space (64MB)</td>
</tr>
<tr>
<td>E004 0000 - E007 FFFF</td>
<td>Local ROM Space</td>
</tr>
</tbody>
</table>
## A.2 KA50/51/55/56 Detailed Local Address Space Map

### Local Memory Space (up to 128MB)

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 0000 - 7FF FFFF</td>
</tr>
</tbody>
</table>

**Q22-bus Map - top 32KB of Main Memory**

### VAX I/O Space

**----------------**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 0000 - 2000 1FFF</td>
</tr>
</tbody>
</table>

### Local Q22-bus I/O Space

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 0000 - 2000 0007</td>
</tr>
</tbody>
</table>

**Q22-bus Floating Address Space**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 0008 - 2000 07FF</td>
</tr>
</tbody>
</table>

**User Reserved Q22-bus I/O Space**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 0800 - 2000 0FFF</td>
</tr>
</tbody>
</table>

**Reserved Q22-bus I/O Space**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 1000 - 2000 1F3F</td>
</tr>
</tbody>
</table>

**Interprocessor Comm Reg**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 1F40</td>
</tr>
</tbody>
</table>

**Reserved Q22-bus I/O Space**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 1F44 - 2000 1FFF</td>
</tr>
</tbody>
</table>

### Local Register I/O Space

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 2000 - 2003 FFFF</td>
</tr>
</tbody>
</table>

**Reserved Local Register I/O Space**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 4000 - 2000 422F</td>
</tr>
</tbody>
</table>

**Reserved Local Register I/O Space**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 42B0 - 2000 7FFF</td>
</tr>
</tbody>
</table>

**Reserved Local Register I/O Space**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 40B0 - 2000 422F</td>
</tr>
</tbody>
</table>

**NICSR0 - Vector Add, IPL, Sync/Async**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 8000</td>
</tr>
</tbody>
</table>

**NICSR1 - Polling Demand Register**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 8004</td>
</tr>
</tbody>
</table>

**NICSR2 - Reserved**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 8008</td>
</tr>
</tbody>
</table>

**NICSR3 - Receiver List Address**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 800C</td>
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</tbody>
</table>

**NICSR4 - Transmitter List Address**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 8010</td>
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</tbody>
</table>

**NICSR5 - Status Register**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 8014</td>
</tr>
</tbody>
</table>

**NICSR6 - Command and Mode Register**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 8018</td>
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**NICSR7 - System Base Address**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
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<tr>
<td>2000 801C</td>
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**NICSR8 - Reserved**

<table>
<thead>
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<th>Address Range</th>
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<tbody>
<tr>
<td>2000 8020*</td>
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</tbody>
</table>

**NICSR9 - Watchdog Timers**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 8024*</td>
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</tbody>
</table>

**NICSR10 - Reserved**

<table>
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<tr>
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<tbody>
<tr>
<td>2000 8028*</td>
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</table>

**NICSR11 - Rev Num & Missed Frame Count**

<table>
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<tbody>
<tr>
<td>2000 802C*</td>
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</tbody>
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**NICSR12 - Reserved**

<table>
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**NICSR13 - Breakpoint Address**

<table>
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**NICSR14 - Reserved**

<table>
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**NICSR15 - Diagnostic Mode & Status**

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>2000 803C</td>
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</table>

**Reserved Local Register I/O Space**

<table>
<thead>
<tr>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 8040 - 2003 FFFF</td>
</tr>
</tbody>
</table>
# Address Assignments

## A.2 KA50/51/55/56 Detailed Local Address Space Map

### KA50/51/55/56 Detailed Local Address Space Map (Cont.)

<table>
<thead>
<tr>
<th>Address Assignment</th>
<th>Base Address</th>
<th>End Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q22 Bus Local Register I/O Space</td>
<td>2008 0000</td>
<td>201F FFFF</td>
</tr>
<tr>
<td>DMA System Configuration Register</td>
<td>2008 0000</td>
<td></td>
</tr>
<tr>
<td>DMA System Error Register</td>
<td>2008 0004</td>
<td></td>
</tr>
<tr>
<td>DMA Master Error Address Register</td>
<td>2008 0008</td>
<td></td>
</tr>
<tr>
<td>DMA Slave Error Address Register</td>
<td>2008 000C</td>
<td></td>
</tr>
<tr>
<td>Q22-bus Map Base Register</td>
<td>2008 0010</td>
<td></td>
</tr>
<tr>
<td>Reserved Local Register I/O Space</td>
<td>2008 0014</td>
<td>2008 00FF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Address Assignment</th>
<th>Base Address</th>
<th>End Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved Local Register I/O Space</td>
<td>2008 0194</td>
<td>2008 3FFF</td>
</tr>
<tr>
<td>Boot and Diagnostic Reg (32 Copies)</td>
<td>2008 4000</td>
<td>2008 407C</td>
</tr>
<tr>
<td>Reserved Local Register I/O Space</td>
<td>2008 4080</td>
<td>2008 7FFF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Address Assignment</th>
<th>Base Address</th>
<th>End Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q22-bus Map Registers</td>
<td>2008 8000</td>
<td>2008 FFFF</td>
</tr>
<tr>
<td>Reserved Local Register I/O Space</td>
<td>2009 0000</td>
<td>2013 FFFF</td>
</tr>
</tbody>
</table>

### SSC CSRs

<table>
<thead>
<tr>
<th>Address Assignment</th>
<th>Base Address</th>
<th>End Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSC Base Address Register</td>
<td>2014 0000</td>
<td></td>
</tr>
<tr>
<td>SSC Configuration Register</td>
<td>2014 0010</td>
<td></td>
</tr>
<tr>
<td>CP Bus Timeout Control Register</td>
<td>2014 0020</td>
<td></td>
</tr>
<tr>
<td>Diagnostic LED Register</td>
<td>2014 0030</td>
<td></td>
</tr>
<tr>
<td>Reserved Local Register I/O Space</td>
<td>2014 0034</td>
<td>2014 006B</td>
</tr>
</tbody>
</table>
Address Assignments
A.2 KA50/51/55/56 Detailed Local Address Space Map

KA50/51/55/56 DETAILED LOCAL ADDRESS SPACE MAP (Cont.)

VAX IPRs implemented by NCA

<table>
<thead>
<tr>
<th>Description</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interval Clock Control Status Reg</td>
<td>2100 0060</td>
</tr>
<tr>
<td>Next Interval Count Register</td>
<td>2100 0064</td>
</tr>
<tr>
<td>Interval Count Register</td>
<td>2100 0068</td>
</tr>
</tbody>
</table>

NMC CSRs

<table>
<thead>
<tr>
<th>Description</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>O-bit Data Registers</td>
<td>2101 0000 - 2101 7FFF</td>
</tr>
<tr>
<td>Main Memory Configuration Reg 0</td>
<td>2101 8000</td>
</tr>
<tr>
<td>Main Memory Configuration Reg 1</td>
<td>2101 8004</td>
</tr>
<tr>
<td>Main Memory Signature Register 0</td>
<td>2101 8020</td>
</tr>
<tr>
<td>Main Memory Signature Register 1</td>
<td>2101 8024</td>
</tr>
<tr>
<td>Main Memory Error Address Register</td>
<td>2101 8040</td>
</tr>
<tr>
<td>Main Memory Error Status Register</td>
<td>2101 8044</td>
</tr>
<tr>
<td>Main Memory Mode Control and</td>
<td>2101 8048</td>
</tr>
<tr>
<td>Diagnostic Register</td>
<td></td>
</tr>
<tr>
<td>O-bit Address and Mode Register</td>
<td>2101 804C</td>
</tr>
</tbody>
</table>

NCA CSRs

<table>
<thead>
<tr>
<th>Description</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Error Status Register</td>
<td>2102 0000</td>
</tr>
<tr>
<td>Mode Control and Diagnostic Reg</td>
<td>2102 0004</td>
</tr>
<tr>
<td>CP1 Slave Error Address Register</td>
<td>2102 0006</td>
</tr>
<tr>
<td>CP2 Slave Error Address Register</td>
<td>2102 000C</td>
</tr>
<tr>
<td>CP1 IO Error Address Register</td>
<td>2102 0010</td>
</tr>
<tr>
<td>CP2 IO Error Address Register</td>
<td>2102 0014</td>
</tr>
<tr>
<td>NDAL Error Address Register</td>
<td>2102 0018</td>
</tr>
</tbody>
</table>
Address Assignments
A.2 KA50/51/55/56 Detailed Local Address Space Map

KA50/51/55/56 DETAILED LOCAL ADDRESS SPACE MAP (Cont.)

******************************************************************************
* OPTIONAL KZDDA SCSI CONTROLLER
   *
   * SCSI DMA address register        21C00000
   * SCSI DMA direction register      21C00004
   * Interrupt mask register          21C00008
   * Interrupt pending register       21C0000C
   * SCSI Controller (53C94) registers 220000B0 - 220000F0
         (13 byte regs (0:9,A,B,C) on LW boundary)
         scsicr0  220000B0
         scsicr1  220000B4
         scsicr2  220000B8
         scsicr3  220000BC
         scsicr4  22000000
         scsicr5  22000094
         scsicr6  22000098
         scsicr7  2200009C
         scsicr8  220000A0
         scsicr9  220000A4
         scsicra  220000A8
         scsicrb  220000AC
         scsicrc  220000B0
   * SCSI DMA Map registers            23000000 - 23007FFF
* (8,192 32 bit registers)
******************************************************************************

EDAL BUS DEVICES

******************************************************************************
* OPTIONAL SYNC COMMUNICATION DEVICE
   *
   * Register sets of the SYNC ports  2400 0000 - 24FF FFFF
   * Option ROM Space                  ???? ???? - ???? ????
   *
******************************************************************************

QUART (DC7085) Registers            2500 0000 - 2500 0007
SCSI DMA Address Register           25C0 0000
SCSI DMA Direction Register         25C0 0004
Interrupt Mask Register             25C0 0008
Interrupt Pending Register          25C0 000C
SCSI Controller (53C94) Registers   2600 0080 - 2600 00BF
SCSI DMA Map Registers              2700 0000 - 2700 7FFF

A-6 Address Assignments
Address Assignments

A.2 KA50/51/55/56 Detailed Local Address Space Map

KA50/51/55/56 DETAILED LOCAL ADDRESS SPACE MAP (Cont.)

* OPTIONAL ASYNC COMMUNICATION DEVICE

* Register sets of the ASYNC ports  3E00 0000 - 3E00 000E
* Option ROM Space  3E01 0000 - 3E02 FFFF
* 

*************************************************************

Local FEPROM Space  E004 0000 - E007 FFFF
VAX System Type Register (In ROM)  E004 0004
Local FEPROM - (Halt Protected)  E004 0000 - E007 FFFF

*************************************************************

The following addresses allow those KA50/51/55/56 Internal Processor Registers that are implemented in the SSC chip (External, Internal Processor Registers) to be accessed via the local I/O page. These addresses are documented for diagnostic purposes only and should not be used by non-diagnostic programs.

Time Of Year Register  2014 006C
Console Storage Receiver Status  2014 0070*
Console Storage Receiver Data  2014 0074*
Console Storage Transmitter Status  2014 0078*
Console Storage Transmitter Data  2014 007C*
Console Receiver Control/Status  2014 0080
Console Receiver Data Buffer  2014 0084
Console Transmitter Control/Status  2014 0088
Console Transmitter Data Buffer  2014 008C
Reserved Local Register I/O Space  2014 0090 - 2014 00DB
I/O Bus Reset Register  2014 00DC
Reserved Local Register I/O Space  2014 00E0
Reserved Local Register I/O Space  2014 00FC - 2014 00FF

* These registers are not fully implemented, accesses yield UNPREDICTABLE results.

*************************************************************
Address Assignments
A.2 KA50/51/55/56 Detailed Local Address Space Map

KA50/51/55/56 DETAILED LOCAL ADDRESS SPACE MAP (Cont.)

<table>
<thead>
<tr>
<th>Local Register I/O Space (Cont.)</th>
<th>Address Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer 0 Control Register</td>
<td>2014 0100</td>
</tr>
<tr>
<td>Timer 0 Interval Register</td>
<td>2014 0104</td>
</tr>
<tr>
<td>Timer 0 Next Interval Register</td>
<td>2014 0108</td>
</tr>
<tr>
<td>Timer 0 Interrupt Vector</td>
<td>2014 010C</td>
</tr>
<tr>
<td>Timer 1 Control Register</td>
<td>2014 0110</td>
</tr>
<tr>
<td>Timer 1 Interval Register</td>
<td>2014 0114</td>
</tr>
<tr>
<td>Timer 1 Next Interval Register</td>
<td>2014 0118</td>
</tr>
<tr>
<td>Timer 1 Interrupt Vector</td>
<td>2014 011C</td>
</tr>
<tr>
<td>Reserved Local Register I/O Space</td>
<td>2014 0120 - 2014 012F</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>BDR Address Decode Match Register</th>
<th>2014 0140</th>
</tr>
</thead>
<tbody>
<tr>
<td>BDR Address Decode Mask Register</td>
<td>2014 0144</td>
</tr>
<tr>
<td>Reserved Local Register I/O Space</td>
<td>2014 0138 - 2014 03FF</td>
</tr>
</tbody>
</table>

| Battery Backed-Up RAM             | 2014 0400 - 2014 07FF |
| Reserved Local Register I/O Space | 2014 0800 - 2014 FFFF |

| Reserved Local I/O Space          | 2020 0000 - FFFF |
| Local Q22-bus Memory Space        | 3000 0000 - 303F FFFF |
| Reserved Local Register I/O Space | 3040 0000 - 3FFF FFFF |

A.3 External, Internal Processor Registers

Several of the Internal Processor Registers (IPR's) on the KA50/51/55/56 are implemented in the NCA or SSC chip rather than the CPU chip. These registers are referred to as External Internal Processor Registers and are listed below.

<table>
<thead>
<tr>
<th>IPR #</th>
<th>Register Name</th>
<th>Abbrev.</th>
</tr>
</thead>
<tbody>
<tr>
<td>27</td>
<td>Time of Year Register</td>
<td>TOY</td>
</tr>
<tr>
<td>28</td>
<td>Console Storage Receiver Status</td>
<td>CSRS*</td>
</tr>
<tr>
<td>29</td>
<td>Console Storage Receiver Data</td>
<td>CSRD*</td>
</tr>
<tr>
<td>30</td>
<td>Console Storage Transmitter Status</td>
<td>CSTS*</td>
</tr>
<tr>
<td>31</td>
<td>Console Storage Transmitter Data</td>
<td>CSDB*</td>
</tr>
<tr>
<td>32</td>
<td>Console Receiver Control/Status</td>
<td>RXCS</td>
</tr>
<tr>
<td>33</td>
<td>Console Receiver Data Buffer</td>
<td>RXDB</td>
</tr>
<tr>
<td>34</td>
<td>Console Transmitter Control/Status</td>
<td>TXCS</td>
</tr>
<tr>
<td>35</td>
<td>Console Transmitter Data Buffer</td>
<td>TXDB</td>
</tr>
<tr>
<td>55</td>
<td>I/O System Reset Register</td>
<td>IORESET</td>
</tr>
</tbody>
</table>

* These registers are not fully implemented, accesses yield UNPREDICTABLE results.
A.4 Global Q22–bus Address Space Map

Q22–bus Memory Space
-------------------------------
Q22–bus Memory Space (Octal) 0000 0000 – 1777 7777

Q22–bus I/O Space (BBS7 Asserted)
-------------------------------
Q22–bus I/O Space (Octal) 1776 0000 – 1777 7777
Reserved Q22–bus I/O Space 1776 0000 – 1776 0007
Q22–bus Floating Address Space 1776 0010 – 1776 3777
User Reserved Q22–bus I/O Space 1776 4000 – 1776 7777
Reserved Q22–bus I/O Space 1777 0000 – 1777 7777
Interprocessor Comm Reg 1777 7500
Reserved Q22–bus I/O Space 1777 7502 – 1777 7777

A.5 Processor Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
<th>I/O Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kernel Stack Pointer</td>
<td>KSP</td>
<td>0</td>
<td>0</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Executive Stack Pointer</td>
<td>ESP</td>
<td>1</td>
<td>1</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Supervisor Stack Pointer</td>
<td>SSP</td>
<td>2</td>
<td>2</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>User Stack Pointer</td>
<td>USP</td>
<td>3</td>
<td>3</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Interrupt Stack Pointer</td>
<td>ISP</td>
<td>4</td>
<td>4</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
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<tr>
<td>Reserved</td>
<td></td>
<td>5–7</td>
<td>5</td>
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<td></td>
<td></td>
<td>E1000014</td>
</tr>
</tbody>
</table>

(continued on next page)
Address Assignments
A.5 Processor Registers

Table A-1 (Cont.) Processor Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
<th>I/O Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0 Base Register</td>
<td>P0BR</td>
<td>8</td>
<td>8</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>P0 Length Register</td>
<td>P0LR</td>
<td>9</td>
<td>9</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>P1 Base Register</td>
<td>P1BR</td>
<td>10</td>
<td>A</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>P1 Length Register</td>
<td>P1LR</td>
<td>11</td>
<td>B</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>System Base Register</td>
<td>SBR</td>
<td>12</td>
<td>C</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>System Length Register</td>
<td>SLR</td>
<td>13</td>
<td>D</td>
<td>RW</td>
<td>NVAX</td>
<td>1-2</td>
<td></td>
</tr>
<tr>
<td>CPU Identification</td>
<td>CPUID</td>
<td>14</td>
<td>E</td>
<td>RW</td>
<td>NVAX</td>
<td>2-1</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
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<td>E100003C</td>
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<tr>
<td>Process Control Block Base</td>
<td>PCBB</td>
<td>16</td>
<td>10</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>System Control Block Base</td>
<td>SCBB</td>
<td>17</td>
<td>11</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Interrupt Priority Level</td>
<td>IPL</td>
<td>18</td>
<td>12</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>AST Level</td>
<td>ASTLVL</td>
<td>19</td>
<td>13</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Software Interrupt Request Register</td>
<td>SIRR</td>
<td>20</td>
<td>14</td>
<td>W</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
</tbody>
</table>

1Initialized on reset

(continued on next page)
### Address Assignments

#### A.5 Processor Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
<th>I/O Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software Interrupt Summary Register</td>
<td>SISR</td>
<td>21</td>
<td>15</td>
<td>RW</td>
<td>NVAX</td>
<td>1-1</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>22-23</td>
<td>16</td>
<td></td>
<td></td>
<td>3</td>
<td>E1000058</td>
</tr>
<tr>
<td>Interval Counter Control / Status</td>
<td>ICCS</td>
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1Initialized on reset

(continued on next page)
### Address Assignments

#### A.5 Processor Registers

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## Address Assignments
### A.5 Processor Registers

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<sup>1</sup>Initialized on reset
<sup>2</sup>Change broadcast to vector unit if present
<sup>3</sup>Testability and diagnostic use only; not for software use in normal operation

(continued on next page)
### Address Assignments
#### A.5 Processor Registers

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<thead>
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<th>Register Name</th>
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*Testability and diagnostic use only; not for software use in normal operation*

(continued on next page)
### Address Assignments
#### A.5 Processor Registers

**Table A-1 (Cont.) Processor Registers**

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Address Assignments
A.5 Processor Registers

Table A–1 (Cont.) Processor Registers

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### Address Assignments
#### A.5 Processor Registers

#### Table A-1 (Cont.) Processor Registers

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<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>216–223</td>
<td>D8</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
<tr>
<td>Mbox P0 Base Register</td>
<td>MP0BR</td>
<td>224</td>
<td>E0</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Mbox P0 Length Register</td>
<td>MP0LR</td>
<td>225</td>
<td>E1</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Mbox P1 Base Register</td>
<td>MP1BR</td>
<td>226</td>
<td>E2</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Mbox P1 Length Register</td>
<td>MP1LR</td>
<td>227</td>
<td>E3</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Mbox System Base Register</td>
<td>MSBR</td>
<td>228</td>
<td>E4</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
</tbody>
</table>

<sup>3</sup>Testability and diagnostic use only; not for software use in normal operation

(continued on next page)
Address Assignments
A.5 Processor Registers

Table A–1 (Cont.) Processor Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
<th>I/O Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mbox System Length Register&lt;sup&gt;3&lt;/sup&gt;</td>
<td>MSLR</td>
<td>229</td>
<td>E5</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Mbox Memory Management Enable&lt;sup&gt;2&lt;/sup&gt;</td>
<td>MMAPEN</td>
<td>230</td>
<td>E6</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Mbox Physical Address Mode</td>
<td>PAMODE</td>
<td>231</td>
<td>E7</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Mbox MME Address</td>
<td>MMEADR</td>
<td>232</td>
<td>E8</td>
<td>R</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Mbox MME PTE Address</td>
<td>MMEPTE</td>
<td>233</td>
<td>E9</td>
<td>R</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Mbox MME Status</td>
<td>MMESTS</td>
<td>234</td>
<td>EA</td>
<td>R</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>235</td>
<td>EB</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mbox TB Parity Address</td>
<td>TBADR</td>
<td>236</td>
<td>EC</td>
<td>R</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Mbox TB Parity Status</td>
<td>TBSTS</td>
<td>237</td>
<td>ED</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>238</td>
<td>EE</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>239</td>
<td>EF</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>240</td>
<td>F0</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td>241</td>
<td>F1</td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<sup>3</sup>Testability and diagnostic use only; not for software use in normal operation

(continued on next page)
### Table A-1 (Cont.) Processor Registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
<th>I/O Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mbox PCADR</td>
<td>PCADDR</td>
<td>242</td>
<td>F2</td>
<td>R</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Pcach Parity Address</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>243</td>
<td>F3</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
<tr>
<td>Mbox PCache Status</td>
<td>PCSTS</td>
<td>241</td>
<td>F4</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>245</td>
<td>F5</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>246</td>
<td>F6</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>247</td>
<td>F7</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
<tr>
<td>Mbox PCache Control</td>
<td>PCCTL</td>
<td>248</td>
<td>F8</td>
<td>RW</td>
<td>NVAX</td>
<td>2-5</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>249</td>
<td>F9</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>250</td>
<td>FA</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>251</td>
<td>FB</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>252</td>
<td>FC</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>253</td>
<td>FD</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>254</td>
<td>FE</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>255</td>
<td>FF</td>
<td></td>
<td>NVAX</td>
<td>2-6</td>
<td></td>
</tr>
</tbody>
</table>

Unimplemented 100-00FFFFFF 3

(continued on next page)
## Address Assignments
### A.5 Processor Registers

**Table A-1 (Cont.) Processor Registers**

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Mnemonic</th>
<th>(Dec)</th>
<th>(Hex)</th>
<th>Type</th>
<th>Impl</th>
<th>Cat</th>
<th>I/O Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>See</td>
<td></td>
<td></td>
<td>01000000-</td>
<td></td>
<td></td>
<td>2</td>
<td>FFFFFFFF</td>
</tr>
<tr>
<td>Table A-2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Type:**

- R = Read-only register
- RW = Read-write register
- W = Write-only register

**Implemented:**

- NVAX = Implemented in the NVAX CPU chip
- System = Implemented in the system environment
- Vector = Implemented in the optional vector unit or its NDAL interface

**Category (egory), class-subclass, where:**

- **class** is one of:
  - 1 = Implemented as per DEC standard 032
  - 2 = NVAX-specific implementation which is unique or different from the DEC standard 032 implementation
  - 3 = Not implemented internally; converted to I/O space read or write and passed to system environment

- **subclass** is one of:
  - 1 = Processed as appropriate by Ebox microcode
  - 2 = Converted to Mbox IPR number and processed via internal IPR command
  - 3 = Processed by internal IPR command, then converted to I/O space read or write and passed to system environment
  - 4 = If virtual machine option is implemented, processed as in 1, otherwise as in 3
  - 5 = Processed by internal IPR command
  - 6 = May be block decoded; reference causes UNDEFINED behavior
  - 7 = Full interval timer may be implemented in the system environment. Subset ICCS is implemented in NVAX CPU chip
  - 8 = Converted to MFVP MSYNC
A.6 IPR Address Space Decoding

Table A-2  IPR Address Space Decoding

<table>
<thead>
<tr>
<th>IPR Group</th>
<th>Mnemonic2</th>
<th>IPR Address Range (hex)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>BCTAG</td>
<td>00000000..000000FF01</td>
<td>256 individual IPRs.</td>
</tr>
<tr>
<td>Bcache Tag</td>
<td>BCFLUSH</td>
<td>01000000..011FFFE01</td>
<td>64k Bcache tag IPRs, each separated by 20(hex) from the previous one.</td>
</tr>
<tr>
<td>Bcache Deallocate</td>
<td>PCTAG</td>
<td>01400000..015FFFE01</td>
<td>64k Bcache tag deallocate IPRs, each separated by 20(hex) from the previous one.</td>
</tr>
<tr>
<td>Pcache Tag</td>
<td>PCDAP</td>
<td>01800000..01801FE01</td>
<td>256 Pcache tag IPRs, 128 for each Pcache set, each separated by 20(hex) from the previous one.</td>
</tr>
<tr>
<td>Pcache Data Parity</td>
<td></td>
<td>01C00000..01C01FF81</td>
<td>1024 Pcache data parity IPRs, 512 for each Pcache set, each separated by 8(hex) from the previous one.</td>
</tr>
</tbody>
</table>

1Unused fields in the IPR addresses for these groups should be zero. Neither hardware nor microcode detects and faults on an address in which these bits are nonzero. Although noncontiguous address ranges are shown for these groups, the entire IPR address space maps into one of these groups. If these fields are nonzero, the operation of the CPU is UNDEFINED.

2The mnemonic is for the first IPR in the block.

Processor registers in all groups except the normal group are processed entirely by the NVAX CPU chip and will never appear on the NDAL. This is also true for a number of the IPRs in the normal group. IPRs in the normal group that are not processed by the NVAX CPU chip are converted into I/O space references and passed to the system environment via a read or write command on the NDAL.

Each of the 256 possible IPRs in the normal group are of longword length, so a 1-KB block of I/O space is required to convert each possible IPR to a unique I/O space longword. This block starts at address E1000000 (hex). Conversion of an IPR address to an I/O space address in this block is done by shifting the IPR address left into bits <9:2>, filling bits <1:0> with zeros, and merging in the base address of the block. This can be expressed by the equation:

\[
\text{I/O ADDRESS} = \text{E1000000} + (\text{IPR NUMBER} \times 4)
\]
B

ROM Partitioning

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95, and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q–bus and DSSI, will appear on the console and/or printouts from time to time.

This section describes ROM partitioning and subroutine entry points that are public and are guaranteed to be compatible over future versions of the firmware. An entry point is the address at which any subroutine or subprogram will start execution.

B.1 Firmware EPROM Layout

The KA50/51/55/56 has 512 Kbytes of FEPROM. Unlike previous Q22–bus based processors, there is no duplicate decoding of the FEPROM into halt-protected and halt-unprotected spaces. The entire FEPROM is halt-protected. See Figure B–1 for the KA50/51/55/56 FEPROM layout.
The first instruction executed on halts is a branch around the System ID Extension (SIE) and the callback entry points. This allows these public data structures to reside in fixed locations in the FEPROM.

The callback area entry points provide a simple interface to the currently defined console for VMB and secondary bootstraps. This is documented further in the next section.

The fixed area checksum is the sum of longwords from 20040000 to the checksum, inclusive. This checksum is distinct from the checksum that the rest of the console uses.

The console, diagnostic and boot code constitute the bulk of the firmware. This code is field upgradable. The console checksum is from 20044000 to the checksum, inclusive.

The memory between the console checksum and the user area at the end of the FEPROM is reserved for Digital for future expansion of the firmware. The contents of this area is set to FF.

The last 4096 bytes of FEPROM are reserved for customer use and are not included in the console checksum. During a PROM bootstrap with PRB0 as the selected boot device, this block is tested for a PROM "signature block". 
B.1.1 System Identification Registers

The firmware and operating system software reference two registers to determine the processor on which they are running. The first, the System Identification register (SID), is an NVAX internal processor register. The second, the System Identification Extension register (SIE), is a firmware register located in the FEPROM.

B.1.1.1 PR$_S$ SID (IPR 62)

The SID longword can be read from IPR 62 using the MFPR instruction. This longword value is processor specific, however, the layout of this register is shown in Figure B–2. A description of each field is provided in Table B–1.

Figure B–2 SID : System Identification Register

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>RW</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>CPU_TYPE</td>
<td>ro</td>
<td>CPU type is the processor specific identification code.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0A : CVAX</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0B : RIGEL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>13 : NVAX</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>14 : SOC</td>
</tr>
<tr>
<td>24:8</td>
<td>Reserved</td>
<td>ro</td>
<td>Reserved for future use.</td>
</tr>
<tr>
<td>7:0</td>
<td>VERSION</td>
<td>ro</td>
<td>Version of the microcode.</td>
</tr>
</tbody>
</table>

B.1.2 SIE (20040004)

The System Identification Extension register is an extension of the SID and is used to further differentiate between hardware configurations. The SID identifies which CPU and microcode are executing, and the SIE identifies which module and firmware revision are present. Note, the fields in this register are dependent on SID<31:24>(CPU_TYPE).
ROM Partitioning
B.1 Firmware EPROM Layout

By convention, all MicroVAX 3100 systems implement a longword at physical location 20040004 in the firmware FEPROM for the SIE. The layout of the SIE is shown in Figure B–3. A description of each field is provided in Table B–2.

Figure B–3 SIE: System Identification Extension (20040004)

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>RW</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>SYS_TYPE</td>
<td>ro</td>
<td>This field identifies the type of system for a specific processor.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>03 : Bounded system.</td>
</tr>
<tr>
<td>23:16</td>
<td>VERSION</td>
<td>ro</td>
<td>This field identifies the resident version of the firmware encoded as two hexadecimal digits. For example, if the banner displays V5.0, then this field is 50 (hex).</td>
</tr>
<tr>
<td>15:8</td>
<td>SYS_SUB_TYPE</td>
<td>ro</td>
<td>This field identifies the particular system subtype.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>08 : KA50/KA55</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>09 : KA51/KA56</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0A : KA62</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0B : KA53</td>
</tr>
<tr>
<td>7:0</td>
<td>VARIANT</td>
<td>ro</td>
<td>This field identifies the particular system variant.</td>
</tr>
</tbody>
</table>

B.1.2 Call-Back Entry Points

The firmware provides several entry points that facilitate I/O to the designated console device. Users of these entry points do not need to be aware of the console device type, be it a video terminal or workstation.

The primary intent of these routines is to provide a simple console device to VMB and secondary bootstraps, before operating systems load their own terminal drivers.

These are JSB (subroutine as opposed to procedure) entry points located in fixed locations in the firmware. These locations branch to code that in turn calls the appropriate routines.
All of the entry points are designed to run at IPL 31 on the interrupt stack in physical mode. Virtual mode is not supported. Due to internal firmware architectural restrictions, users are encouraged to only call into the halt-protected entry points. These entry points are listed in Table B-3.

<table>
<thead>
<tr>
<th>Call-Back Entry Points</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP$GET_CHAR_R4</td>
</tr>
<tr>
<td>CP$MSG_OUT_NOLF_R4</td>
</tr>
<tr>
<td>CP$READ_WTH_</td>
</tr>
<tr>
<td>PRMPT_R4</td>
</tr>
</tbody>
</table>

### B.1.2.1 CP$GETCHAR_R4

This routine returns the next character entered by the operator in R0. A timeout interval can be specified. If the timeout interval is zero, no timeout is generated. If a timeout is specified and if timeout occurs, a value of 18 (CAN) is returned instead of normal input.

Registers R0, R1, R2, R3 and R4 are modified by this routine, all others are preserved.

```assembly
; Usage with timeout:
movl #timeout_in_tenths_of_second, r0 ; Specify timeout.
jsb @@CP$GET_CHAR_R4                 ; Call routine.
cmpb r0, #x18                        ; Check for timeout.
bpl timeout_handler                 ; Branch if timeout.
; Input is in R0.

; Usage without timeout:
clr r0                               ; Specify no timeout.
jsb @@CP$GET_CHAR_R4                 ; Call routine.
; Input is in R0.
```

```
B.1.2.2 CP$MSG_OUT_NOLF_R4

This routine outputs a message to the console. The message is specified either by a message code or a string descriptor. The routine distinguishes between message codes and descriptors by requiring that any descriptor be located outside of the first page of memory. Hence, message codes are restricted to values between 0 and 511.

Registers R0,R1,R2,R3 and R4 are modified by this routine, all others are preserved.

```
movzbl  #console_message_code,r0          ; Specify message code.
jsb    @@CP$MSG_OUT_NOLF_R4             ; Call routine.

movaq  5$,r0                             ; Specify address of desc.
jsb    @@CP$MSG_OUT_NOLF_R4             ; Call routine.

5$: .ascid /This is a message/       ; Message with descriptor.

pushab 5$                                ; Generate message desc.
pushl  $105-5$                          ; on stack.
movl   sp,r0                             ; Pass desc. addr. in R0.
jsb    @@CP$MSG_OUT_NOLF_R4             ; Call routine.
clrq   (sp)+                             ; Purge desc. from stack.

5$: .ascii /This is a message/        ; Message.
10$: ;
```

B.1.2.3 CP$READ_WTH_PRMPT_R4

This routine outputs a prompt message and then inputs a character string from the console. When the input is accepted, DELETE, CONTROL-U and CONTROL-R functions are supported.

As with CP$MSG_OUT_NOLF_R4, either a message code or the address of a string descriptor is passed in R0 to specify the prompt string. A value of zero results in no prompt. A time-out value in 10-millisecond ticks may be passed in R1. If R1 is zero, the prompt will not timeout.
A descriptor of the input string is returned in R0 and R1. R0 contains the length of the string and R1 contains the address. This routine inputs the string into the console program string buffer and therefore the caller need not provide an input buffer. Successive calls however destroy the previous contents of the input buffer.

Registers R0 and R1 are modified by this routine, all others are preserved.

```
; Usage with a message descriptor (position independent).
pushab 5$                      ; Generate prompt desc.
pushl $10$-5$                  ; on stack.
movl sp,r0                     ; Pass desc. addr. in R0.
crl r1                          ; Specify no time-out.
jsb @CP$READ_WMTPRMT_R4        ; Call routine.
clrq (sp)+                      ; Purge prompt desc.
                           ; Input desc in R0 and R1.
5$:    .ascii /Prompt> /       ; Prompt string.
10$:
```

B.1.3 Boot Information Pointers

Two longwords located in EEPROM are used as pointers to the default boot device descriptor and the default boot flags (Figure B-4), because the actual location of this data may change in successive versions of the firmware. Any software that uses these pointers should reference them at the addresses in halt-protected space.
The following macro defines the boot device descriptor format.

```plaintext
; Default Boot Device Descriptor

boot_device_descriptor::
    .base = .
    .  = base + dsc$w_length
    .word  nvr$S_boot_device
    .  = base + dsc$B_dtype
    .byte  dsc$k_dtype_z
    .  = base + dsc$B_class
    .byte  dsc$k_class_z
    .  = base + dsc$A Pointer
    .long  nvr_base + nvr$B_boot_device
    .  = base + dsc$S_dscdef1
```

---

ROM Partitioning
B.1 Firmware EPROM Layout
Data Structures and Memory Layout

This appendix contains definitions of the key global data structures used by the CPU firmware.

---

**Note**

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95 and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q-bus and DSSI, will appear on the console and/or printouts from time to time.

---

### C.1 Halt Dispatch State Machine

The CPU halt dispatcher determines what actions the firmware will take on halt entry based on the machine state. The dispatcher is implemented as a state machine, which uses a single bitmap control word and the transition (see Table C-1) to process all halts. The transition table is sequentially searched for matches with the current state and control word. If there is a match, a transition occurs to the next state.

The control word comprises the following information:

- **Halt Type**, used for resolving external halts. Valid only if Halt Code is 00.

  - 000: power-up state
  - 001: halt in progress
  - 010: negation of Q22-bus DCOK
  - 011: console BREAK condition detected
  - 100: Q22-bus BHALT
  - 101: SGEC BOOT_L asserted (trigger boot)
Data Structures and Memory Layout
C.1 Halt Dispatch State Machine

  
  00 : RESTART_CODE = 2, external halt
  01 : RESTART_CODE = 3, power-up/reset
  10 : RESTART_CODE = 6, halt instruction
  11 : RESTART_CODE = any other, error halts

- **Mailbox Action**, passed by an operating system in CPMBX<1:0>(HALT_ACTION).
  
  00 : restart, boot, halt
  01 : restart, halt
  10 : boot, halt
  11 : halt

- **User Action**, specified with the SET HALT console command.
  
  000 : default
  001 : restart, halt
  010 : boot, halt
  011 : halt
  100 : restart, boot, halt

- **HEN**, Break (halt) Enable/Disable switch, BDR<07>
- **ERR**, error status
- **TIP**, trace in progress
- **DIP**, diagnostics in progress
- **BIP**, bootstrap in progress CPMBX<2>
- **RIP**, restart in progress CPMBX<3>

A transition to a "next state" occurs if a match is found between the control word and a "current state" entry in the table. The firmware does a linear search through the table for a match. Therefore, the order of the entries in the transition table is important. The control longword is reassembled before each transition from the current machine state. The state machine transitions are shown in Table C.-1.
## Data Structures and Memory Layout

### C.1 Halt Dispatch State Machine

#### Table C-1 Firmware State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Halt Type</th>
<th>Halt Code</th>
<th>Mailbox Action</th>
<th>User Action</th>
<th>HEN-ERR-TIP-DIP-BIP-RIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENTRY</td>
<td>-&gt;RESET INIT</td>
<td>xxx</td>
<td>01</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>ENTRY</td>
<td>-&gt;BREAK INIT</td>
<td></td>
<td>011</td>
<td>00</td>
<td>xx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>ENTRY</td>
<td>-&gt;TRACE INIT</td>
<td></td>
<td>xxx</td>
<td>10</td>
<td>xx</td>
<td>x - 0 - 1 - x - x - x</td>
</tr>
<tr>
<td>ENTRY</td>
<td>-&gt;OTHER INIT</td>
<td></td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>x - x - x - x - x - x</td>
</tr>
</tbody>
</table>

### Perform conditional initialization

| RESET INIT   | ->INIT       | xxx       | xx        | xx             | xxx         | x - x - x - x - x - x |
| BREAK INIT   | ->INIT       | xxx       | xx        | xx             | xxx         | x - x - x - x - x - x |
| TRACE INIT   | ->INIT       | xxx       | xx        | xx             | xxx         | x - x - x - x - x - x |
| OTHER INIT   | ->INIT       | xxx       | xx        | xx             | xxx         | x - x - x - x - x - x |

### Perform common initialization

### Check for external halts

<table>
<thead>
<tr>
<th>INIT</th>
<th>-&gt;BOOTSTRAP</th>
<th>101</th>
<th>00</th>
<th>xx</th>
<th>xxx</th>
<th>x - x - x - x - x - x</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>-&gt;HALT</td>
<td></td>
<td>00</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
</tbody>
</table>

### Check for pending (NEXT) trace

| INIT          | ->TRACE      | xxx       | 10        | xx             | xxx         | x - x - 1 - x - x - x |

---

1. Perform a unique initialization routine on entry. In particular, power-ups, BREAKs, and TRACEs require special initialization. Any other halt entry performs a default initialization.

2. After performing conditional initialization, complete common initialization.

3. Halt on all external halts, except:
   - if DCOK (unlikely) and halts are disabled, boot-strap
   - if SGEC remote trigger, bootstrap

4. Unconditionally enter the TRACE state, if the TIP flag is set and the halt was due to a HALT instruction. From the TRACE state the firmware exits, if TIP is set and ERR is clear; otherwise it halts.

(continued on next page)
### Data Structures and Memory Layout

#### C.1 Halt Dispatch State Machine

Table C–1 (Cont.)  Firmware State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Halt Type</th>
<th>Halt Code</th>
<th>Mailbox Action</th>
<th>User Action</th>
<th>HEN-ERR-TIP-DIP-BIP-RIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRACE</td>
<td>EXIT</td>
<td>xxx</td>
<td>10</td>
<td>xx</td>
<td>xxx</td>
<td>x - 0 - 1 - x - x - x</td>
</tr>
<tr>
<td>TRACE</td>
<td>HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
</tbody>
</table>

Check for pending (NEXT) trace

| INIT           | BOOTSTRAP  | xxx | 01 | xx | xxx | 0 - 0 - 0 - 0 - 0 - 0 |
| INIT           | BOOTSTRAP  | xxx | 01 | xx | 010 | 1 - 0 - 0 - 0 - 0 - 0 |
| INIT           | BOOTSTRAP  | xxx | 01 | xx | 100 | 1 - 0 - 0 - 0 - 0 - 0 |
| INIT           | BOOTSTRAP  | xxx | 1x | 10 | xxx | x - 0 - 0 - 0 - 0 - 0 |
| INIT           | BOOTSTRAP  | xxx | 1x | 00 | 010 | x - 0 - 0 - 0 - 0 - 0 |
| INIT           | BOOTSTRAP  | xxx | 1x | 00 | 100 | x - 0 - 0 - 0 - 0 - 1 |
| INIT           | BOOTSTRAP  | xxx | 1x | 00 | 100 | x - 1 - 0 - 0 - 0 - x |
| INIT           | BOOTSTRAP  | xxx | 1x | 00 | 000 | 0 - 0 - 0 - 0 - 0 - 1 |
| RESTART        | BOOTSTRAP  | xxx | 1x | 00 | 000 | 0 - 1 - 0 - 0 - 0 - x |

Check for bootstrap conditions

Check for restart conditions

---

4 Unconditionally enter the TRACE state, if the TIP flag is set and the halt was due to a HALT instruction. From the TRACE state the firmware exits, if TIP is set and ERR is clear; otherwise it halts.

5 Bootstrap,

   if power-up and halts are disabled.
   if power-up and halts are enabled and user action is 2 or 4.
   if not power-up and mailbox is 2.
   if not power-up and mailbox is 0 and user action is 2.
   if not power-up and restart failed and mailbox is 0 and user action is 0 or 4.

6 Restart the operating system if not power-up and

   if mailbox is 1.
   if mailbox is 0 and user action is 1 or 4.
   if mailbox is 0 and user action is 0 and halts are disabled.

(continued on next page)
### Table C-1 (Cont.) Firmware State Transition Table

<table>
<thead>
<tr>
<th>Current State</th>
<th>Next State</th>
<th>Halt Type</th>
<th>Halt Code</th>
<th>Mailbox Action</th>
<th>User Action</th>
<th>HEN-ERR-TIP-DIP-BIP-RIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>INIT</td>
<td>-&gt;RESTART</td>
<td>xxx</td>
<td>1x</td>
<td>00</td>
<td>000</td>
<td>0 - 0 - 0 - 0 - 0 - 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Check for restart conditions 6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Perform common exit processing, if no errors 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BOOTSTRAP</td>
<td>-&gt;EXIT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - 0 - x - x - x - x</td>
</tr>
<tr>
<td>RESTART</td>
<td>-&gt;EXIT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - 0 - x - x - x - x</td>
</tr>
<tr>
<td>HALT</td>
<td>-&gt;EXIT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - 0 - x - x - x - x</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Exception transitions, just halt 8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INIT</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>BOOT</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>REST</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>HALT</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>TRACE</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
<tr>
<td>EXIT</td>
<td>-&gt;HALT</td>
<td>xxx</td>
<td>xx</td>
<td>xx</td>
<td>xxx</td>
<td>x - x - x - x - x - x</td>
</tr>
</tbody>
</table>

6 Restart the operating system if not power-up and
   if mailbox is 1.
   if mailbox is 0 and user action is 1 or 4.
   if mailbox is 0 and user action is 0 and halts are disabled.

7 Exit after halts, bootstrap or restart. The exit state transitions to program I/O mode.

8 Guard block that catches all exception conditions. In all cases, just halt.

### C.2 Restart Parameter Block

VMB typically utilizes the low portion of memory unless there are bad pages in the first 128K bytes. The first page in its block is used for the Restart Parameter Block (RPB), through which it communicates to the operating system. Usually, this is page 0.
VMB will initialize the Restart Parameter Block (RPB) as shown in Table C-2.

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPB$L_BASE</td>
<td>Physical address of base of RPB.</td>
</tr>
<tr>
<td>RPB$L_RESTART</td>
<td>Cleared.</td>
</tr>
<tr>
<td>RPB$L_CHKSUM</td>
<td>-1</td>
</tr>
<tr>
<td>RPB$L_RSTRTFLG</td>
<td>Cleared.</td>
</tr>
<tr>
<td>RPB$L_HALTPC</td>
<td>R10 on entry to VMB (HALT PC).</td>
</tr>
<tr>
<td>PR$_SAVPSL</td>
<td>PR$_SAVPSL on entry to VMB (HALT PSL).</td>
</tr>
<tr>
<td>RPB$L_HALTCODE</td>
<td>AP on entry to VMB (HALT CODE).</td>
</tr>
<tr>
<td>RPB$L_BOOTR0</td>
<td>R0 on entry to VMB.</td>
</tr>
</tbody>
</table>

**Note**

The field RPB$W_R0UBVEC, which overlaps the high-order word of RPB$L_BOOTR0, is set by the boot device drivers to the SCB offset (in the second page of the SCB) of the interrupt vector for the boot device.

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPB$L_BOOTR1</td>
<td>VMB version number. The high-order word of the version is the major ID and the low-order word is the minor ID.</td>
</tr>
<tr>
<td>RPB$L_BOOTR2</td>
<td>R2 on entry to VMB.</td>
</tr>
<tr>
<td>RPB$L_BOOTR3</td>
<td>R3 on entry to VMB.</td>
</tr>
<tr>
<td>RPB$L_BOOTR4</td>
<td>R4 on entry to VMB.</td>
</tr>
</tbody>
</table>

**Note**

The 48-bit booting node address is stored in RPB$L_BOOTR3 and RPB$L_BOOTR4 for compatibility with ELN VX.X. (This field is only initialized this way when performing a network boot.)

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPB$L_BOOTR5</td>
<td>R5 on entry to VMB.</td>
</tr>
<tr>
<td>RPB$L_IOVEC</td>
<td>Physical address of boot driver's I/O vector of transfer addresses.</td>
</tr>
</tbody>
</table>

(continued on next page)
Data Structures and Memory Layout
C.2 Restart Parameter Block

<table>
<thead>
<tr>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPB$L_IOVECSZ</td>
<td>Size of BOOT QIO routine.</td>
</tr>
<tr>
<td>RPB$L_FILLBN</td>
<td>LBN of secondary bootstrap image.</td>
</tr>
<tr>
<td>RPB$L_FILSIZ</td>
<td>Size of secondary bootstrap image in blocks.</td>
</tr>
<tr>
<td>RPB$Q_PFNMAP</td>
<td>The PFN bitmap is an array of bits, where each bit has the value &quot;1&quot; if the corresponding page of memory is valid, or has the value &quot;0&quot; if the corresponding page of memory contains a memory error. Through use of the PFNMAP, the operating system can avoid memory errors by avoiding known bad pages altogether. The memory bitmap is always page-aligned, and describes all the pages of memory from physical page #0 to the high end of memory, but excluding the PFN bitmap itself and the Q-bus map registers. If the high byte of the bitmap spans some pages available to the operating system and some pages of the PFN bitmap itself, the pages corresponding to the bitmap itself will be marked as bad pages. The first longword of the PFNMAP descriptor contains the number of bytes in the PFNMAP; the second longword contains the physical address of the bitmap.</td>
</tr>
<tr>
<td>RPB$L_PFNCNT</td>
<td>Count of &quot;good&quot; pages of physical memory, but not including the pages allocated to the Q22-bus scatter/gather map, the console scratch area, and the PFN bitmap at the top of memory.</td>
</tr>
<tr>
<td>RPB$L_SVASPT</td>
<td>0.</td>
</tr>
<tr>
<td>RPB$L_CSRPHY</td>
<td>Physical address of CSR for boot device.</td>
</tr>
<tr>
<td>RPB$L_CSRVIR</td>
<td>0.</td>
</tr>
<tr>
<td>RPB$L_ADPPHY</td>
<td>Physical address of ADP (really the address of QMRs - ^x800 to look like a UBA adapter).</td>
</tr>
<tr>
<td>RPB$L_ADPVIR</td>
<td>0.</td>
</tr>
<tr>
<td>RPB$W_UNIT</td>
<td>Unit number of boot device.</td>
</tr>
<tr>
<td>RPB$B_DEVTYP</td>
<td>Device type code of boot device.</td>
</tr>
<tr>
<td>RPB$B_SLAVE</td>
<td>Slave number of boot device.</td>
</tr>
</tbody>
</table>

(continued on next page)
### Data Structures and Memory Layout

#### C.2 Restart Parameter Block

<table>
<thead>
<tr>
<th>(R11)+</th>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>68:</td>
<td>RPB$_FILE</td>
<td>Name of secondary bootstrap image (defaults to [SYS0.SYSEXE][SYSBOOT.EXE]). This field (up to 40 bytes) is overwritten with the input string on a “solicit” boot.</td>
</tr>
</tbody>
</table>

**Note**

1. For VAX/OpenVMS, the RPB$\_FILE must contain the root directory string “SYSn.” on a non-network bootstrap. This string is parsed by SYSBOOT (SYSBOOT does not use the high nibble of BOOTR5).
2. The RPB$\_FILE is overwritten to contain the boot node name for compatibility with ELN VX.X (this field is only initialized this way when performing a network boot).

<table>
<thead>
<tr>
<th>90:</th>
<th>RPB$_B_CONFREG</th>
<th>Array (16 bytes) of adapter types (NDT$_UB0 - UNIBUS).</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0:</td>
<td>RPB$_B_HDRPGCNT</td>
<td>Count of header pages.</td>
</tr>
<tr>
<td>A1:</td>
<td>RPB$_W_BOOTNDT</td>
<td>Boot adapter nexus device type. Used by SYSBOOT and INIADP (OF SYSLOA) to configure the adapter of the boot device (changed from a byte to a word field in Version 12 of VMB).</td>
</tr>
<tr>
<td>B0:</td>
<td>RPB$_L_SCBB</td>
<td>Physical address of SCB.</td>
</tr>
<tr>
<td>BC:</td>
<td>RPB$_L_MEMDSC</td>
<td>Count of pages in physical memory including both good and bad pages. The high 8 bits of this longword contain the TR #, which is always 0 for KA52.</td>
</tr>
<tr>
<td>C0:</td>
<td>RPB$_L_MEMDSC+4</td>
<td>PFN of the first page of memory. This field is always 0 for KA50/51/55/56, even if page #0 is a bad page.</td>
</tr>
</tbody>
</table>

**Note**

No other memory descriptors are used.

| 104:   | RPB$\_L_BADPGS | Count of “bad” pages of physical memory. |

(continued on next page)
Table C–2 (Cont.) Restart Parameter Block Fields

<table>
<thead>
<tr>
<th>(R11)+</th>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>108:</td>
<td>RPB$B_CTRLLLTR</td>
<td>Boot device controller number biased by 1. In VAX/OpenVMS, this field is used by INIT (in SYS) to construct the boot device’s controller letter. A 0 implies this field has not been initialized, else if initialized, A=1, B=2, etc. (this field was added in Version 13 of VMB).</td>
</tr>
<tr>
<td>nn:</td>
<td></td>
<td>The rest of the RPB is zeroed.</td>
</tr>
</tbody>
</table>

C.3 VMB Argument List

The VMB code will also initialize an argument list as shown in Table C–3 (the address of the argument list is passed in the AP).

Table C–3 VMB Argument List

<table>
<thead>
<tr>
<th>(AP)+</th>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04:</td>
<td>VMB$L_FILECPCHE</td>
<td>Quadword filename.</td>
</tr>
<tr>
<td>0C:</td>
<td>VMB$L_LO_PFN</td>
<td>PFN of first page of physical memory (always 0, regardless of where 128 Kbytes of &quot;good&quot; memory starts).</td>
</tr>
<tr>
<td>10:</td>
<td>VMB$L_HI_PFN</td>
<td>PFN of last page of physical memory.</td>
</tr>
<tr>
<td>14:</td>
<td>VMB$Q_PFNMAP</td>
<td>Descriptor of PFN bitmap. First longword contains count of bytes in bitmap. Second longword contains physical address of bitmap. (Same rules as for RPB$Q_PFNMAP listed above.)</td>
</tr>
<tr>
<td>1C:</td>
<td>VMB$Q_UCODE</td>
<td>Quadword.</td>
</tr>
<tr>
<td>24:</td>
<td>VMB$B_SYSTEMID</td>
<td>48-bit (actually a quadword is allocated) booting node address which is initialized when performing a network boot. This field is copied from the Target System Address parameter of the parameters message. (The DECnet HIORD value is added if the field was two bytes.)</td>
</tr>
<tr>
<td>2C:</td>
<td>VMB$L_FLAGS</td>
<td>Set as needed.</td>
</tr>
<tr>
<td>30:</td>
<td>VMB$L_CI_HIPFN</td>
<td>Cluster interface high PFN.</td>
</tr>
</tbody>
</table>

(continued on next page)
### Table C–3 (Cont.) VMB Argument List

<table>
<thead>
<tr>
<th>(AP)+</th>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>34:</td>
<td>VMB$Q_NODENAME</td>
<td>Boot node name which is initialized when performing a network boot. This field is copied from the Target System Name parameter of the parameters message.</td>
</tr>
<tr>
<td>3C:</td>
<td>VMB$Q_HOSTADDR</td>
<td>Host node address (this value is only initialized when booting over the network). This field is copied from the Host System Address parameter of the parameters message.</td>
</tr>
<tr>
<td>44:</td>
<td>VMB$Q_HOSTNAME</td>
<td>Host node name (this value is only initialized when performing a network boot). This field is copied from the Host System Name parameter of the parameters message.</td>
</tr>
<tr>
<td>4C:</td>
<td>VMB$Q_TOD</td>
<td>Time of day (this value is only initialized when performing a network boot). The time of day is copied from the first eight bytes of the Host System Time parameter of the parameters message. (The time differential values are NOT copied.)</td>
</tr>
<tr>
<td>54:</td>
<td>VMB$L XPARAM</td>
<td>Pointer to data retrieved from request of the parameter file.</td>
</tr>
<tr>
<td>58:</td>
<td></td>
<td>The rest of the argument list is zeroed.</td>
</tr>
</tbody>
</table>
Configurable Machine State

The KA50/51/55/56 CFU modules have many control registers that need to be configured for proper operation of the module. The following list shows the normal state of all configurable bits in the CPU module as they are left after the successful completion of power-up ROM diagnostics.

---

**Note**

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95 and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q-bus and DSSI, will appear on the console and/or printouts from time to time.

---

Configuration Register Bit Settings (* = reset state)

NCA:

NCA_CSR1:

15:14: CP2 MT Timer Prescaler
    11 = 144000 cycles* - needed for CQBIT 10ms No Grant timeout

13:12: CP1 MT Timer Prescaler
    00 = 144 cycles - minimum for passive releases, no cycle should take longer than this.

11:10: NDAL Timeout Prescaler
    00 = 3200 cycles* - this is longer than both NCA and NMC transactions timeouts, preserves timeout order.

9:  CQBIT mode
    0 = CQBIT not present* - this is to avoid the Qbus_TRANS deadlock.
Configurable Machine State

8: IO2 ID enable
   1 = enabled

7: Force wrong CP2 bus parity - off - diagnostic use only
6: Force wrong CP1 bus parity - off - diagnostic use only
5: Force wrong NDAL master parity - off - diagnostic use only
4: Force wrong NDAL slave parity - off - diagnostic use only
3: Enable prefetch
   1 = enable CP bus prefetch on DMA reads
2: Force write buffer hit - off - diagnostic use only
1: Force CP2 bus owner - diagnostic use only
   0 = disabled
0: Force CP1 bus owner - diagnostic use only
   0 = disabled

ICCS: Interval Clock Control and Status Register (2100 0060)
NOTE: OpenVMS sets ICCS, NICR to proper values.

6: Interrupt enable
   0 = disabled*
5: Single step - off
4: Transfer
   0 = disabled*
0: Run - increment every lusec - off

NICR: Next Interval Count Register (2100 0064)
31:0 Initial count value for ICR (FFFFFFF0* (10ms))

NMC: Memory Configuration Registers (2101 8000 thru 2101 801C)
NOTE: Diagnostics set these registers based on available memory

31: Base Address Valid
    0 = not valid*
    1 = valid
28:24: Base Address (0 on reset)
    1MB RAM - all address bits used
    4MB RAM - only <28:26> used
2:1 RAM size
    01 = 1MB RAM
    10 = 4MB RAM
    11 = non-existent bank
0: Mode
    1 = 64-bit mode

NMC_CSR18: Mode Control and Diagnostic Status Register (2101 8048)
31: Fast Diagnostic Mode (FDM)
    0 = disabled* - diagnostic use only
30: FDM Second pass
    0 = disabled* - diagnostic use only
Configurable Machine State

29: Diagnostic Checkbit mode
   0 = disabled* - diagnostic use only

28: QBus on IO1
   0 = QBus on IO2*

27: Enable soft error log (NDAL & memory related)
   0 = disabled* - OpenVMS enables this

26: Flush BCache
   0 = don’t flush*

24:17: Memory diagnostic check bits (0*) - may not be read
      as 0

8:7: NDAL Timeout Scaler
     00 = 2600 cycles* - maximum to preserve timeout order

6: Disable memory error
   0 = memory errors detected and corrected*

5: Refresh interval timer select
   0 = 328 cycles*

4:2: Force wrong parity on NDAL transactions - off
     - diagnostic use only

1: Disable memory refresh
   0 = memory refreshed*

0: Force refresh
   0 = normal refresh*

NMC_CSR19: 0-bit Address and Mode Register (2101 804C)
16: Ignore 0-bit mode
    0 = 0-bits checked*

15: Disable 0-bit error
    0 = 0-bit errors detected*

14:6: 0-bit segment address (0*) - not used in normal
      operation

5:3: 0-bit mask (0*) - not used in normal operation

2:0: 0-bit operation mode
     X00 = reconstruction mode* - not used in normal
     operation

NMC_OSCR: 0-bit Data Registers (2101 0000 thru 2101 7FFF)
23:12: 0-bit field 1 (0 at reset)
11:0: 0-bit field 0 (0 at reset)

NVAX: ----- CPUID: CPU ID Register (IPR E)
7:0: CPU identification = 0 (for single processor config.)

SID: System Identification Register (IPR 3E)
     NOTE: this register may only be written by microcode
Configurable Machine State

31:24: CPU type - 13hex (NVAX code)
13:8: Patch revision
7:0: Microcode revision

ICSR: IBox Control and Status Register (IPR D3)
0: VIC enable
   1 = enabled

ECR: EBox Control Register (IPR 7D)
13: FBox test enable
   0 = disable* - diagnostic use only
7: Interval time mode
   1 = full CPU implemented interval timer
5: S3 stall timeout
   0 = counts cycles w/ timeout_enable asserted (~3 sec)*
3: FBox stage 4 bypass
   1 = enabled - improves FBox latency
2: S3 external time base timeout
   0 = disabled* - use internal time base
1: FBox enable
   1 = enabled
0: Vector present
   0 = no* - no vector option available at this time

MMAPEN: Memory Map Enable Register (IPR E6)
0: Memory map enable
   0 = disabled* - OpenVMS enables this

PAMODE: Physical Address Mode Register (IPR E7)
0: Physical address mode
   0 = 30-bit physical address space*

PCCTL: PCache Control Register (IPR F8)
8: PCache Electrical disable
   0 = PCache enabled*
7:5 MBcc:: performance monitor mode (0*) - diagnostic use only
4: PCache error enable
   1 = enables PCache error detection
3: Bank select during force hit mode
   0 = left bank selected if force hit mode enabled* - diagnostic use only
2: Force hit
   0 = disabled* - diagnostic use only
1: I enable
   1 = enable PCache for IREAD, INVAL, I_CF commands
Configurable Machine State

0:   D_enable
     1 = enable PCache for INVAL, D-stream read/write/fill

CCTL: CBox Control Register (IPR A0)
30:   Software ETM
      0 = disabled* - diagnostic use only
16:   Force NDAL parity error - off - diagnostic use only
15:11: Performance monitoring bits (0*) - diagnostic use only
10:   Disable CBox write packer
      0 = write packer enabled* - improves write latency
9:    Read timeout time base
      0 = external time base
8:    Software ECC
      0 = use correct ECC*
7:    Disable BCache errors
      0 = BCache errors detected*
6:    Force Hit
      0 = disabled* - diagnostic use only
5:4:  BCache size
      00 = 128 KB* (KA50/52/55)
      10 = 512 KB (KA51/53/54/56)
3:2:  Data store speed
      00 = 2 cycle read, 3 cycle write* (KA51/53/54/56)
      01 = 3 cycle read, 4 cycle write (KA50/52)
      10 = 4 cycle read, 5 cycle write (KA55)
1:    Tag store speed
      0 = 3 cycle read, 3 cycle write* (KA51/53/54/56)
      1 = 4 cycle read, 4 cycle write (KA50/52/55)
0:    Enable BCache
      1 = enabled

CQBIC: -----

SCR:   System Configuration Register (2008 0000)
14:    Halt enable
      1 = BHALT to CQBIC HALTIN pin to cause halts
12:    Page prefetch disable
      1 = map prefetch disabled - historical latency reasons
7:     Restart enable
      0 = QBus restart causes ARB power-up reset*
3:1:   ICR offset address select bits
      0 = (AUX mode not supported)*
Configurable Machine State

ICR: Interprocessor Communication Register (2000 1F40)
8: AUX Halt
   0 = no halt - AUX mode not supported
6: ICR interrupt enable
   0 = interprocessor interrupts disabled - only uniprocessor config. allowed
5: Local memory external access enable
   0 = external access disabled* - OpenVMS configures map

QMBR: Q-Bus Map Base Address Register (2008 0010)
28:15: address where 8K QBus mapping register are located
(undefined at reset)

SHAC:
-----
NOTE: all SHAC registers are set up by OpenVMS driver

PQBBR: Port Queue Block Base Register (2000 4248)
20:0: upper bits of physical address of base of Port Queue block. Contains HW version, FW version, shared host memory version and CI port maintenance ID at power-up.

PPR: Port Parameter Register (2000 4258)
31:29: Cluster size. For SHAC value = 0.
28:16: Internal buffer length = 0* (For SHAC value = 1010 hex)
7:0: Port number. Same as SHAC’s DSSI ID.

PMCSR: Port Maintenance Control and Status Register (2000 425C)
2: Interrupt enable
   0 = disabled*
1: Maintenance timer disable
   0 = enabled*

SGEC:
-----
NOTE: all SGEC registers are set up by OpenVMS driver

MICSRO: Vector Address, IPL, Synch/Asynch Register (2000 8000)
31:30: Interrupt priority
   00 = 14*
29: Synch/Asynch bus master operating mode
   0 = asynchronous*
15:0: Interrupt vector = 0003hex*
### Configurable Machine State

**NICSR6:** Command and Mode Register (2000 8018)

- 30: Interrupt enable
  - 0 = disabled*

- 28:25: Burst limit mode
  - maximum number of longwords transferred in a single DMA burst. 1*, 2, 4, 8 when NICSR<19> is clear; 1*, 4 when set.

- 20: Boot message enable mode
  - 0 = disabled*

- 19: Single cycle enable mode
  - 0 = disabled*

- 11: Start/Stop transmission command
  - 0 = SGEC transmission process in stopped state*

- 10: Start/Stop reception command
  - 0 = SGEC reception process in stopped state*

- 9:8: Operating mode
  - 00 = normal mode*

- 7: Disable data chaining mode
  - 0 = frames too long for current receive buffer will be transferred to the next buffer(s) in receive list*

- 6: Force collision mode (internal loopback mode only)
  - 0 = no collision*

- 3: Pass bad frames mode
  - 0 = bad frames discarded*

- 2:1: Address filtering mode
  - 00 = normal mode*

**NICSR7:** System Base Register (2000 801C)

- 29:0: System base address - physical starting address of the VAX system page table (unpredictable after reset)

**NICSR9:** Watchdog Timers Register (2000 8024)

- 31:16: Receive watchdog timeout
  - 0 = never timeout*
  - default = 1250 = 2 ms
  - range = 72 µs (45) to 100 ms

- 15:0: Transmit watchdog timeout
  - 0 = never timeout*
  - default = 1250 = 2 ms
  - range = 72 µs (45) to 100 ms

**SSC:**

---

**SSCBAR:** SSC Base Address Register (2014 0000)

- 29:0: Base Address (reset value = 20140000)

**SSCCR:** SSC Configuration Register (2014 0010)

- 27: Interrupt vector disable
  - 0 = interrupt vector enabled*
Configurable Machine State

25:24: IPL Level
   00 = 14*

23: ROM access time
   0 = 350 ns*

22:20: ROM size
   110 = 512KB

18:16: Halt protected space
   110 = 20040000 - 200BFFFF (historical)

15: n/a

14:12: n/a

6: Programmable address strobe 1 ready enable (for BDR)
   1 = ready asserted after address strobe

5:4: Programmable address strobe 1 enable (for BDR)
   11 = read enabled, write enabled

2: Programmable address strobe 0 ready enable
   0 = no ready after address strobe*
   Used for EEPROM programming

1:0: Programmable address strobe 0 enable
    00 = read disabled, write disabled*
    Used for EEPROM programming

SSCBT: SSC Bus Time Out Register (2014 0020)
   23:0: Bus timeout interval = 4000hex (16.384 ms)
       range = 1 to FFFFFFF (1 μs to 16.77 sec)

ADS0MAT: Programmable Address Strobe 0 Match Register (2014 0130)
   29:2: Match address
       0 = disabled*

ADS0MAS: Programmable Address Strobe 0 Mask Register (2014 0134)
   29:2: Mask address bits

ADS1MAT: Programmable Address Strobe 1 Match Register (2014 0140)
   29:2: Match address = 20084000 (for BDR)

ADS1MAS: Programmable Address Strobe 1 Mask Register (2014 0144)
   29:2: Mask address bits = 7C (for BDR)

TICR: Programmable Timer 0 Control Register (2014 0100)
   6: Interrupt enable
       0 = disabled*

2: STP
   0 = run after overflow*

0: RUN
   0 = counter not running* (historical)
Configurable Machine State

TlCR: Programmable Timer 1 Control Register (2014 0110)
  6:  Interrupt enable
      0 = disabled*
  2:  STP
      0 = run after overflow*
  0:  RUN
      1 = counter incrementing every microsecond (historical)

TNIR: Programmable Timer Next Interval Registers (2014 0108, 2014 0118)
  31:0:  Timer next interval count (use 2’s complement)
         range = 0* to 1.2 hours

T0IV: Programmable Timer 0 Interrupt Vector Register (2014 010C)
  9:2:  Timer interrupt vector = 78hex

T1IV: Programmable Timer 1 Interrupt Vector Registers (2014 011C)
  9:2:  Timer interrupt vector = 7Chex

TOY: Time of Year Register (2014 006C)
  31:0:  Number of 10 ms intervals since written

DLED: Diagnostic LED Register (2014 0030)
  3:0:  Display bits
        0 = LEDs on*  (historical)
This appendix describes how the CPU firmware partitions the SSC 1 KB battery-backed-up (BBU) RAM.

Note

The firmware and diagnostics for MicroVAX 3100 Models 85, 90, 95 and 96 were written to support other systems as well. References to features and functions not available on these models, such as Q–bus and DSSI, will appear on the console and/or printouts from time to time.

E.1 SSC RAM Layout

The KA50/51/55/56 firmware uses the 1K byte of NVRAM on the SSC (see Figure E–1), for storage of firmware specific data structures and other information that must be preserved across power cycles. This NVRAM resides in the SSC chip starting at address 20140400. The NVRAM should not be used by the operating systems except as documented below. This NVRAM is not reflected in the bitmap built by the firmware.
E.1 SSC RAM Layout

Figure E–1 KA50/51/55/56 SSC NVRAM Layout

20140400
Public Data Structures (CPMBX, etc.)
Service Vectors
Firmware Stack
Diagnostic State
201407FC
Resvd for Customer Use

E.1.1 Public Data Structures

Public data structures consist of three bytes, NVR0, NVR1, and NVR2. Their functions are described in Table E–1, Table E–2, and Table E–3.

E.1.1.1 Console Program MailBox (CPMBX)

The Console Program MailBox (CPMBX) comprised of NVR0, is a software data structure located at the beginning of NVRAM (20140400). The CPMBX is used to pass information between the CPU firmware and diagnostics, VMB, or an operating system.

Figure E–2 NVR0 (20140400) : Console Program MailBox (CPMBX)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LANGUAGE</td>
<td>RIP</td>
<td>BIP</td>
<td>HLT_ACT</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table E–1 Bit Functions for NVR0

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:4</td>
<td>LANGUAGE</td>
<td>This field specifies the current selected language for displaying halt and error messages on terminals which support MCS.</td>
</tr>
<tr>
<td>3</td>
<td>RIP</td>
<td>If set, a restart attempt is in progress. This flag must be cleared by the operating system, if the restart succeeds.</td>
</tr>
</tbody>
</table>

(continued on next page)
Table E–1 (Cont.) Bit Functions for NVR0

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>BIP</td>
<td>If set, a bootstrap attempt is in progress. This flag must be cleared by the operating system if the bootstrap succeeds.</td>
</tr>
<tr>
<td>1:0</td>
<td>HLT_ACT</td>
<td>Processor halt action - this field in conjunction with the conditions specified for system halts is used to control the automatic restart/bootstrap procedure. HLT_ACT is normally written by the operating system.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7 : Restart; if that fails, reboot; if that fails, halt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 : Restart; if that fails, halt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 : Reboot; if that fails, halt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 : Halt.</td>
</tr>
</tbody>
</table>

E.1.1.2 Terminal Status

Figure E–3 NVR1 (20140401)

Table E–2 Bit Functions for NVR1

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>MCS</td>
<td>If set, indicates that the attached terminal supports Multinational Character Set. If clear, MCS is not supported.</td>
</tr>
<tr>
<td>1</td>
<td>CRT</td>
<td>If set, indicates that the attached terminal is a CRT. If clear, indicates that the terminal is hardcopy.</td>
</tr>
</tbody>
</table>

E.1.1.3 Keyboard Status

Figure E–4 NVR2 (20140402)
NVRAM Partitioning
E.1 SSC RAM Layout

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>KEYBOARD</td>
<td>This field indicates the national keyboard variant in use.</td>
</tr>
</tbody>
</table>

E.1.2 Service Vectors

Service vectors point to the routines for the reading or writing of characters by the console.

E.1.3 Firmware Stack

This section contains the stack that is used by all of the firmware, with the exception of VMB, which has its own built-in stack.

E.1.4 Diagnostic State

This area is used by the firmware resident diagnostics. It serves as the primary communications mechanism between the diagnostics and the console program.

E.1.5 USER Area

The KA50/51/55/56 console reserves the last longword (address 201407FC) of the NVRAM for customer use. This location is not tested by the console firmware. Its value is undefined.
MOP Counters

The following counters are kept for the Ethernet boot channel. All counters are unsigned integers. V4 counters rollover on overflow. All V3 counters "latch" at their maximum value to indicate overflow. Unless otherwise stated, all counters include both normal and multicast traffic. Furthermore, they include information for all protocol types. Frames received and bytes received counters do not include frames received with errors. Table F–1 displays the byte lengths and ordering of all the counters in both MOP Versions 3.0 and 4.0.

Table F–1 MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>V3 Off Len</th>
<th>V4 Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIME_SINCE_CREATION</td>
<td>00 2</td>
<td>00 16</td>
<td><strong>Time since last zeroed.</strong> The time which has elapsed, since the counters were last zeroed. Provides a frame of reference for the other counters by indicating the amount of time they cover. For MOP V3, this time is the number of seconds. MOP V4 uses the UTC Binary Relative Time format.</td>
</tr>
</tbody>
</table>

(continued on next page)
## MOP Counters

### Table F-1 (Cont.) MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>Off Len</th>
<th>Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rx_BYTES</td>
<td>02 4</td>
<td>10 8</td>
<td><strong>Bytes received.</strong> The total number of user data bytes successfully received. This does not include Ethernet data link headers. This number is the number of bytes in the Ethernet data field, which includes any padding or length fields when they are enabled. These are bytes from frames that passed hardware filtering. When the number of frames received is used to calculate protocol overhead, the overhead plus bytes received provides a measurement of the amount of Ethernet bandwidth (over time) consumed by frames addressed to the local system.</td>
</tr>
<tr>
<td>Tx_BYTES</td>
<td>06 4</td>
<td>18 8</td>
<td><strong>Bytes sent.</strong> The total number of user data bytes successfully transmitted. This does not include Ethernet data link headers or data link generated retransmissions. This number is the number of bytes in the Ethernet data field, which includes any padding or length fields when they are enabled. When the number of frames sent is used to calculate protocol overhead, the overhead plus bytes sent provides a measurement of the amount of Ethernet bandwidth (over time) consumed by frames sent by the local system.</td>
</tr>
</tbody>
</table>

(continued on next page)
### MOP Counters

#### Table F–1 (Cont.) MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>V3 Off Len</th>
<th>V4 Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rx_FRAMES</td>
<td>0A 4</td>
<td>20 8</td>
<td><strong>Frames received.</strong> The total number of frames successfully received. These are frames that passed hardware filtering. Provides a gross measurement of incoming Ethernet usage by the local system. Provides information used to determine the ratio of the error counters to successful transmits.</td>
</tr>
<tr>
<td>Tx_FRAMES</td>
<td>0E 4</td>
<td>28 8</td>
<td><strong>Frames sent.</strong> The total number of frames successfully transmitted. This does not include data link generated retransmissions. Provides a gross measurement of outgoing Ethernet usage by the local system. Provides information used to determine the ratio of the error counters to successful transmits.</td>
</tr>
<tr>
<td>Rx_MCAST_BYTES</td>
<td>12 4</td>
<td>30 8</td>
<td><strong>Multicast bytes received.</strong> The total number of multicast data bytes successfully received. This does not include Ethernet data link headers. This number is the number of bytes in the Ethernet data field. In conjunction with total bytes received, provides a measurement of the percentage of this system's receive bandwidth (over time) that was consumed by multicast frames addressed to the local system.</td>
</tr>
<tr>
<td>Rx_MCAST_FRAMES</td>
<td>16 4</td>
<td>38 8</td>
<td><strong>Multicast frames received.</strong> The total number of multicast frames successfully received. In conjunction with total frames received, provides a gross percentage of the Ethernet usage for multicast frames addressed to this system.</td>
</tr>
</tbody>
</table>

(continued on next page)
# MOP Counters

## Table F-1 (Cont.) MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>V3 Off Len</th>
<th>V4 Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx_INIT_DEFERRED</td>
<td>1A 4</td>
<td>40 8</td>
<td><strong>Frames sent(^1), initially deferred.</strong> The total number of times that a frame transmission was deferred on its first transmission attempt. In conjunction with total frames sent, measures Ethernet contention with no collisions.</td>
</tr>
<tr>
<td>Tx_ONE_COLLISION</td>
<td>1E 4</td>
<td>48 8</td>
<td><strong>Frames sent(^1), single collision.</strong> The total number of times that a frame was successfully transmitted on the second attempt after a normal collision on the first attempt. In conjunction with total frames sent, measures Ethernet contention at a level where there are collisions but the backoff algorithm still operates efficiently.</td>
</tr>
<tr>
<td>Tx_MULTI_COLLISION</td>
<td>22 4</td>
<td>50 8</td>
<td><strong>Frames sent(^1), multiple collisions.</strong> The total number of times that a frame was successfully transmitted on the third or later attempt after normal collisions on previous attempts. In conjunction with total frames sent, measures Ethernet contention at a level where there are collisions and the backoff algorithm no longer operates efficiently. <strong>NO SINGLE FRAME IS COUNTED IN MORE THAN ONE OF THE ABOVE THREE COUNTERS.</strong></td>
</tr>
</tbody>
</table>

\(^1\)Only one of these three counters will be incremented for a given frame.

(continued on next page)
### MOP Counters

#### Table F-1 (Cont.) MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>V3 Off Len</th>
<th>V4 Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TxFAIL_COUNT</td>
<td>26 2</td>
<td>-</td>
<td><strong>Send failure count</strong>. The total number of times a transmit attempt failed. Each time the counter is incremented, a type of failure is recorded. When Read-counter function reads the counter, the list of failures is also read. When the counter is set to zero, the list of failures is cleared. In conjunction with total frames sent, provides a measure of significant transmit problems. TxFAIL_BITMAP contains the possible reasons.</td>
</tr>
<tr>
<td>TxFAIL_BITMAP</td>
<td>2C 2</td>
<td>-</td>
<td><strong>Send failure reason bitmap</strong>. This bitmap lists the types of transmit failures that occurred as summarized below:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 - Excessive collisions</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 - Carrier detect failed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2 - Short circuit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3 - Open circuit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4 - Frame too long</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5 - Remote failure to defer</td>
</tr>
<tr>
<td>TxFAIL_EXCESS_COLLS</td>
<td>-</td>
<td>58 8</td>
<td><strong>Send failure—Excessive collisions</strong>. Exceeded the maximum number of retransmissions due to collisions. Indicates an overload condition on the Ethernet.</td>
</tr>
</tbody>
</table>

\(^{2}\)V3 send/receive failures are collapsed into one counter with bitmap indicating which failures occurred.

(continued on next page)
## Table F–1 (Cont.) MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>V3 Off Len</th>
<th>V4 Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TxFAIL_CARIER_CHECK</td>
<td>-</td>
<td>60 8</td>
<td><strong>Send failure—Carrier check failed.</strong> The data link did not sense the receive signal that is required to accompany the transmission of a frame. Indicates a failure in either the transmitting or receiving hardware. Could be caused by either transceiver, transceiver cable, or a babbling controller that has been cut off.</td>
</tr>
<tr>
<td>TxFAIL_SHRT_CIRCUIT</td>
<td>-</td>
<td>68 8</td>
<td><strong>Send failure—Short circuit</strong>. There is a short somewhere in the local area network coaxial cable or the transceiver or controller/transceiver cable has failed. This indicates a problem either in local hardware or global network. The two can be distinguished by checking to see if other systems are reporting the same problem.</td>
</tr>
<tr>
<td>TxFAIL_OPEN_CIRCUIT</td>
<td>-</td>
<td>70 8</td>
<td><strong>Send failure—Open circuit</strong>. There is a break somewhere in the local area network coaxial cable. This indicates a problem either in local hardware or global network. The two can be distinguished by checking to see if other systems are reporting the same problem.</td>
</tr>
<tr>
<td>TxFAIL_LONG_FRAME</td>
<td>-</td>
<td>78 8</td>
<td><strong>Send failure—Frame too long</strong>. The controller or transceiver cut off transmission at the maximum size. This indicates a problem with the local system. Either it tried to send a frame that was too long or the hardware cutoff transmission too soon.</td>
</tr>
</tbody>
</table>

3Always zero.

(continued on next page)
## MOP Counters

### Table F-1 (Cont.) MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>Off</th>
<th>Len</th>
<th>Off</th>
<th>Len</th>
<th>Description</th>
</tr>
</thead>
</table>
| TxFAIL_REMOTE_DEFER         | -   | -   | 80  | 8   | **Send failure—Remote failure to defer**

A remote system began transmitting after the allowed window for collisions. This indicates either a problem with some other system's carrier sense or a weak transmitter.

<table>
<thead>
<tr>
<th>Name</th>
<th>Off</th>
<th>Len</th>
<th>Off</th>
<th>Len</th>
<th>Description</th>
</tr>
</thead>
</table>
| RxFAIL_COUNT                | 2A  | 2   | -   | -   | **Receive failure count**

The total number of frames received with some data error. Includes only data frames that passed either physical or multicast address comparison. This counter includes failure reasons in the same way as the send failure counter. In conjunction with total frames received, provides a measure of data related receive problems. RxFAIL_BITMAP contains the possible reasons.

<table>
<thead>
<tr>
<th>Name</th>
<th>Off</th>
<th>Len</th>
<th>Off</th>
<th>Len</th>
<th>Description</th>
</tr>
</thead>
</table>
| RxFAIL_BITMAP               | 2C  | 2   | -   | -   | **Receive failure reason bitmap**

This bitmap lists the types of receive failures that occurred as summarized below:

- 0 : Block check failure
- 1 : Framing error
- 2 : Frame too long

<table>
<thead>
<tr>
<th>Name</th>
<th>Off</th>
<th>Len</th>
<th>Off</th>
<th>Len</th>
<th>Description</th>
</tr>
</thead>
</table>
| RxFAIL_BLOCK_CHECK          | -   | -   | 88  | 8   | **Receive failure—Block check error**

A frame failed the CRC check. This indicates several possible failures, such as EMI, late collisions, or improperly set hardware parameters.

---

2V3 send/receive failures are collapsed into one counter with bitmap indicating which failures occurred.

3Always zero.

(continued on next page)
## MOP Counters

<table>
<thead>
<tr>
<th>Name</th>
<th>V3 Off Len</th>
<th>V4 Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RxFAIL_FRAMING_ERR</td>
<td>-</td>
<td>90 8</td>
<td>Receive failure—Framing error. The frame did not contain an integral number of 8 bit bytes. This indicates several possible failures, such as EMI, late collisions, or improperly set hardware parameters.</td>
</tr>
<tr>
<td>RxFAIL_LONG_FRAME</td>
<td>-</td>
<td>98 8</td>
<td>Receive failure—Frame too long. The frame was discarded because it was outside the Ethernet maximum length and could not be received. This indicates that a remote system is sending invalid length frames.</td>
</tr>
<tr>
<td>UNKNOWN_DESTINATION</td>
<td>2E 2</td>
<td>A0 8</td>
<td>Unrecognized frame destination. The number of times a frame was discarded because there was no portal with the protocol type or multicast address enabled. This includes frames received for the physical address, the broadcast address, or a multicast address.</td>
</tr>
<tr>
<td>DATA_OVERRUN</td>
<td>30 2</td>
<td>A8 8</td>
<td>Data overrun. The total number of times the hardware lost an incoming frame because it was unable to keep up with the data rate. In conjunction with total frames received, provides a measure of hardware resource failures. The problem reflected in this counter is also captured as an event.</td>
</tr>
</tbody>
</table>

3Always zero.

(continued on next page)
# MOP Counters

## Table F–1 (Cont.)  MOP Counter Block

<table>
<thead>
<tr>
<th>Name</th>
<th>Off Len</th>
<th>Off Len</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO_SYSTEM_BUFFER</td>
<td>32 2</td>
<td>B0 8</td>
<td><strong>System buffer unavailable</strong>. The total number of times no system buffer was available for an incoming frame. In conjunction with total frames received, provides a measure of system buffer related receive problems. The problem reflected in this counter is also captured as an event. This can be any buffer between the hardware and the user buffers (those supplied on Receive requests). Further information as to potential different buffer pools is implementation specific.</td>
</tr>
<tr>
<td>NO_USER_BUFFER</td>
<td>34 2</td>
<td>B8 8</td>
<td><strong>User buffer unavailable</strong>. The total number of times no user buffer was available for an incoming frame that passed all filtering. These are the buffers supplied by users on Receive requests. In conjunction with total frames received, provides a measure of user buffer related receive problems. The problem reflected in this counter is also captured as an event.</td>
</tr>
<tr>
<td>FAIL_COLLIS_DETECT</td>
<td>-</td>
<td>C0 8</td>
<td><strong>Collision detect check failure.</strong> The approximate number of times that collision detect was not sensed after a transmission. If this counter contains a number roughly equal to the number of frames sent, either the collision detect circuitry is not working correctly or the test signal is not implemented.</td>
</tr>
</tbody>
</table>

\(^3\)Always zero.
The error messages issued by the KA50/51/55/56 firmware fall into three categories: halt code messages, VMB error messages, and console messages.

G.1 Machine Check Register Dump

Some error conditions, such as machine check, generate an error summary register dump preceding the error message. For example, examining a nonexistent memory location results in the following display:

>>e/p 1 20000000
MCSR=00006000 MEAR=0B5006010 MMCDSR=01111110 MDAMR=00000000
CESR=80000200 CMCDSR=00000010 CSEAR1=00000000 CSEAR2=00000000
CIOEAR1=00000000 CIOEAR2=00000000 CNEAR=00000000
PCSTS=FFFFFF00 PCADR=FFFFFFF8 TBSTS=C0000000 TBADR=F5755754
NESTS=00000000 NEAOADR=ED14060C NEOCMD=8000F005 NEICMD=00000FF
NEDATHL=00000000 NEDATLO=FF79FF00 CEFSTS=0001920A CEFADR=ED000000
BCETSTS=00000000 BCETIDX=FFFFFF10 BCETAG=FF00F000 BCEDSTS=00000FF00
BCEID1X=0001FF00 BCEIDCC=00000000 BCSCR=00000000 BCER=0000008A
QBEAR=00000000 DEAR=00000000 IPCRD=00000000
SCSICSR4=00 SCSICSR6=00 SCSICSR5=00
?7D MACHINE CHECK 80000000 00000000 20048C68 20048C59 20048C55 40110080

G.2 Halt Code Messages

Except on power-up, which is not treated as an error condition, the following halt messages are issued by the firmware whenever the processor halts (Table G–1).

For example, if the processor encounters a .HALT instruction while in kernel mode, the processor halts and the firmware displays the following before entering console I/O mode:

?06 HLT INST
PC = 800050D3
Error Messages
G.2 Halt Code Messages

The number preceding the halt message is the "halt code." This number is obtained from SAVPSL<13:8>(RESTART_CODE), IPR 43, which is saved on any processor restart operation.

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?02</td>
<td>EXT HLT</td>
<td>External halt, caused by either console BREAK condition, Q22-bus BHALT_L, or DBR&lt;AUX_HLT&gt; bit was set while enabled.</td>
</tr>
<tr>
<td>_03</td>
<td>—</td>
<td>Power-up, no halt message is displayed. However, the presence of the firmware banner and diagnostic countdown indicates this halt reason.</td>
</tr>
<tr>
<td>?04</td>
<td>ISP ERR</td>
<td>In attempting to push state onto the interrupt stack during an interrupt or exception, the processor discovered that the interrupt stack was mapped NO ACCESS or NOT VALID.</td>
</tr>
<tr>
<td>?05</td>
<td>DBL ERR</td>
<td>The processor attempted to report a machine check to the operating system, and a second machine check occurred.</td>
</tr>
<tr>
<td>?06</td>
<td>HLT INST</td>
<td>The processor executed a HALT instruction in kernel mode.</td>
</tr>
<tr>
<td>?07</td>
<td>SCB ERR3</td>
<td>The SCB vector had bits &lt;1:0&gt; equal to 3.</td>
</tr>
<tr>
<td>?08</td>
<td>SCB ERR2</td>
<td>The SCB vector had bits &lt;1:0&gt; equal to 2.</td>
</tr>
<tr>
<td>?0A</td>
<td>CHM FR ISTK</td>
<td>A change mode instruction was executed when PSL&lt;IS&gt; was set.</td>
</tr>
<tr>
<td>?0B</td>
<td>CHM TO ISTK</td>
<td>The SCB vector for a change mode had bit &lt;0&gt; set.</td>
</tr>
<tr>
<td>?0C</td>
<td>SCB RD ERR</td>
<td>A hard memory error occurred while the processor was trying to read an exception or interrupt vector.</td>
</tr>
<tr>
<td>?10</td>
<td>MCHK AV</td>
<td>An access violation or an invalid translation occurred during machine check exception processing.</td>
</tr>
<tr>
<td>?11</td>
<td>KSP AV</td>
<td>An access violation or translation not valid occurred during processing of a kernel stack not valid exception.</td>
</tr>
<tr>
<td>?12</td>
<td>DBL ERR2</td>
<td>Double machine check error. A machine check occurred while trying to service a machine check.</td>
</tr>
<tr>
<td>?13</td>
<td>DBL ERR3</td>
<td>Double machine check error. A machine check occurred while trying to service a kernel stack not valid exception.</td>
</tr>
<tr>
<td>?19</td>
<td>PSL EXCS^1</td>
<td>PSL&lt;26:24&gt; = 5 on interrupt or exception.</td>
</tr>
</tbody>
</table>

^1For the last six cases, the VAX architecture does not allow execution on the interrupt stack while in a mode other than kernel. In the first three cases, an interrupt is attempting to run on the interrupt stack while not in kernel mode. In the last three cases, an REI instruction is attempting to return to a mode other than kernel and still run on the interrupt stack.

(continued on next page)
## Error Messages

### G.2 Halt Code Messages

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?1A</td>
<td>PSL EXC6(^1)</td>
<td>PSL&lt;26:24&gt; = 6 on interrupt or exception.</td>
</tr>
<tr>
<td>?1B</td>
<td>PSL EXC7(^1)</td>
<td>PSL&lt;26:24&gt; = 7 on interrupt or exception.</td>
</tr>
<tr>
<td>?1D</td>
<td>PSL REI5(^1)</td>
<td>PSL&lt;26:24&gt; = 5 on an REI instruction</td>
</tr>
<tr>
<td>?1E</td>
<td>PSL REI6(^1)</td>
<td>PSL&lt;26:24&gt; = 6 on an REI instruction.</td>
</tr>
<tr>
<td>?1F</td>
<td>PSL REI7(^1)</td>
<td>PSL&lt;26:24&gt; = 7 on an REI instruction.</td>
</tr>
<tr>
<td>?3F</td>
<td>MICROVERIFY FAILURE</td>
<td>Microcode power-up self-test failed.</td>
</tr>
</tbody>
</table>

\(^1\)For the last six cases, the VAX architecture does not allow execution on the interrupt stack while in a mode other than kernel. In the first three cases, an interrupt is attempting to run on the interrupt stack while not in kernel mode. In the last three cases, an REI instruction is attempting to return to a mode other than kernel and still run on the interrupt stack.

### G.3 VMB Error Messages

VMB issues the errors listed in Table G–2.

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?40</td>
<td>NOSUCHDEV</td>
<td>No bootable devices found.</td>
</tr>
<tr>
<td>?41</td>
<td>DEVASSIGN</td>
<td>Device is not present.</td>
</tr>
<tr>
<td>?42</td>
<td>NOSUCHFILE</td>
<td>Program image not found.</td>
</tr>
<tr>
<td>?43</td>
<td>FILESTRUCT</td>
<td>Invalid boot device file structure.</td>
</tr>
<tr>
<td>?44</td>
<td>BADCHKSUM</td>
<td>Bad checksum on header file.</td>
</tr>
<tr>
<td>?45</td>
<td>BADFILEHDR</td>
<td>Bad file header.</td>
</tr>
<tr>
<td>?46</td>
<td>BADDIRECTORY</td>
<td>Bad directory file.</td>
</tr>
<tr>
<td>?47</td>
<td>FILNOTCNTG</td>
<td>Invalid program image format.</td>
</tr>
<tr>
<td>?48</td>
<td>ENDOFFILE</td>
<td>Premature end of file encountered.</td>
</tr>
<tr>
<td>?49</td>
<td>BADFILENAME</td>
<td>Bad filename given.</td>
</tr>
<tr>
<td>?4A</td>
<td>BUFFEROVF</td>
<td>Program image does not fit in available memory.</td>
</tr>
<tr>
<td>?4B</td>
<td>CTRLERR</td>
<td>Boot device I/O error.</td>
</tr>
</tbody>
</table>

(continued on next page)
Error Messages
G.3 VMB Error Messages

Table G–2 (Cont.) VMB Error Messages

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?4C</td>
<td>DEVINACT</td>
<td>Failed to initialize boot device.</td>
</tr>
<tr>
<td>?4D</td>
<td>DEVOFFLINE</td>
<td>Device is offline.</td>
</tr>
<tr>
<td>?4E</td>
<td>MEMERR</td>
<td>Memory initialization error.</td>
</tr>
<tr>
<td>?4F</td>
<td>SCBINTE</td>
<td>Unexpected SCB exception or machine check.</td>
</tr>
<tr>
<td>?50</td>
<td>SCB2NDINT</td>
<td>Unexpected exception after starting program image.</td>
</tr>
<tr>
<td>?51</td>
<td>NOROM</td>
<td>No valid ROM image found.</td>
</tr>
<tr>
<td>?52</td>
<td>NOSUCHNODE</td>
<td>No response from load server.</td>
</tr>
<tr>
<td>?53</td>
<td>INSFMAPREG</td>
<td>The Q22–bus map initialization failed.</td>
</tr>
<tr>
<td>?54</td>
<td>RETRY</td>
<td>No devices bootable, retrying.</td>
</tr>
<tr>
<td>?55</td>
<td>IVDEVNAM</td>
<td>Invalid device name.</td>
</tr>
<tr>
<td>?56</td>
<td>DRVERR</td>
<td>Drive error.</td>
</tr>
</tbody>
</table>

G.4 Console Error Messages

The error messages listed in Table G–3 are issued in response to a console command that has error(s).

Table G–3 Console Error Messages

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?61</td>
<td>CORRUPTION</td>
<td>The console program database has been corrupted.</td>
</tr>
<tr>
<td>?62</td>
<td>ILLEGAL REFERENCE</td>
<td>Illegal reference. The requested reference would violate virtual memory protection, the address is not mapped, the reference is invalid in the specified address space, or the value is invalid in the specified destination.</td>
</tr>
<tr>
<td>?63</td>
<td>ILLEGAL COMMAND</td>
<td>The command string cannot be parsed.</td>
</tr>
<tr>
<td>?64</td>
<td>INVALID DIGIT</td>
<td>A number has an invalid digit.</td>
</tr>
<tr>
<td>?65</td>
<td>LINE TOO LONG</td>
<td>The command was too large for the console to buffer. The message is issued only after receipt of the terminating carriage return.</td>
</tr>
<tr>
<td>?66</td>
<td>ILLEGAL ADDRESS</td>
<td>The address specified falls outside the limits of the address space.</td>
</tr>
</tbody>
</table>

(continued on next page)
### Error Messages

#### G.4 Console Error Messages

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?67</td>
<td>VALUE TOO LARGE</td>
<td>The value specified does not fit in the destination.</td>
</tr>
<tr>
<td>?68</td>
<td>QUALIFIER CONFLICT</td>
<td>Qualifier conflict; for example, two different data sizes are specified for an EXAMINE command.</td>
</tr>
<tr>
<td>?69</td>
<td>UNKNOWN QUALIFIER</td>
<td>The switch is unrecognized.</td>
</tr>
<tr>
<td>?6A</td>
<td>UNKNOWN SYMBOL</td>
<td>The symbolic address in an EXAMINE or DEPOSIT command is unrecognized.</td>
</tr>
<tr>
<td>?6B</td>
<td>CHECKSUM</td>
<td>The command or data checksum of an X command is incorrect. If the data checksum is incorrect, this message is issued, and is not abbreviated to &quot;Illegal command&quot;.</td>
</tr>
<tr>
<td>?6C</td>
<td>HALTED</td>
<td>The operator entered a HALT command.</td>
</tr>
<tr>
<td>?6D</td>
<td>FIND ERROR</td>
<td>A FIND command failed either to find the RPB or 128 KB of good memory.</td>
</tr>
<tr>
<td>?6E</td>
<td>TIME OUT</td>
<td>During an X command, data failed to arrive in the time expected (60 seconds).</td>
</tr>
<tr>
<td>?6F</td>
<td>MEMORY ERROR</td>
<td>A machine check occurred with a code indicating a read or write memory error.</td>
</tr>
<tr>
<td>?70</td>
<td>UNIMPLEMENTED</td>
<td>Unimplemented function.</td>
</tr>
<tr>
<td>?71</td>
<td>NO VALUE QUALIFIER</td>
<td>Qualifier does not take a value.</td>
</tr>
<tr>
<td>?72</td>
<td>AMBIGUOUS QUALIFIER</td>
<td>There were not enough unique characters to determine the qualifier.</td>
</tr>
<tr>
<td>?73</td>
<td>VALUE QUALIFIER</td>
<td>Qualifier requires a value.</td>
</tr>
<tr>
<td>?74</td>
<td>TOO MANY QUALIFIERS</td>
<td>Too many qualifiers supplied for this command.</td>
</tr>
<tr>
<td>?75</td>
<td>TOO MANY ARGUMENTS</td>
<td>Too many arguments supplied for this command.</td>
</tr>
<tr>
<td>?76</td>
<td>AMBIGUOUS COMMAND</td>
<td>There were not enough unique characters to determine the command.</td>
</tr>
<tr>
<td>?77</td>
<td>TOO FEW ARGUMENTS</td>
<td>Insufficient arguments supplied for this command.</td>
</tr>
<tr>
<td>?78</td>
<td>TYPEAHEAD OVERFLOW</td>
<td>The typeahead buffer overflowed.</td>
</tr>
<tr>
<td>?79</td>
<td>FRAMING ERROR</td>
<td>A framing error was detected on the console serial line.</td>
</tr>
<tr>
<td>?7A</td>
<td>OVERRUN ERROR</td>
<td>An overrun error was detected on the console serial line.</td>
</tr>
<tr>
<td>?7B</td>
<td>SOFT ERROR</td>
<td>A soft error occurred.</td>
</tr>
<tr>
<td>?7C</td>
<td>HARD ERROR</td>
<td>A hard error occurred.</td>
</tr>
<tr>
<td>?7D</td>
<td>MACHINE CHECK</td>
<td>A machine check occurred.</td>
</tr>
</tbody>
</table>

(continued on next page)
### Error Messages

#### G.4 Console Error Messages

<table>
<thead>
<tr>
<th>Code</th>
<th>Message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7E</td>
<td>CONSOLE STACK OVERRUN</td>
<td>SSC RAM stack overflowed into NVR.</td>
</tr>
<tr>
<td>7F</td>
<td>COMMAND NOT SUPPORTED</td>
<td>Command on similar modules not supported on this product.</td>
</tr>
<tr>
<td>80</td>
<td>ILLEGAL PASSWORD</td>
<td>Password is not 16 characters in length.</td>
</tr>
<tr>
<td>81</td>
<td>INCORRECT PASSWORD</td>
<td>Password entered does not match previously entered password.</td>
</tr>
<tr>
<td>82</td>
<td>PASSWORD FACILITY NOT ENABLED</td>
<td>A password has not been set.</td>
</tr>
</tbody>
</table>
Related Documents

The following documents contain information relating to the maintenance of systems that use the KA50/51/55/56 CPU modules.

<table>
<thead>
<tr>
<th>Title</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Guide to BA42B-Based MicroVAX 3100 Systems Service Information Kit</td>
<td>EK-M3100-IN</td>
</tr>
<tr>
<td>MicroVAX 3100 Models 30, 40, 80, 85, 90, 95, 96 System Illustrated Parts Breakdown</td>
<td>EK-MV310-IP</td>
</tr>
<tr>
<td>MicroVAX 3100 BA42B Enclosure Maintenance</td>
<td>EK-M3100-MG</td>
</tr>
<tr>
<td>MicroVAX 3100 BA42B Enclosure System Options</td>
<td>EK-M3100-OP</td>
</tr>
<tr>
<td>OpenVMS Factory Installed Software User Guide</td>
<td>EK-A0377-UG</td>
</tr>
</tbody>
</table>

1* = current revision, which is always shipped.
Glossary

ASCll
American standard code for information interchange.

BFLAG
Boot FLAG is the longword supplied in the SET BFLAG and BOOT /R5: commands that qualify the bootstrap operation. SHOW BFLAG displays the current value.

BHALT
Q22–bus Halt signal is usually tied to the front panel Halt switch.

BIP
Boot In Progress flag in CPMBX<2>

Bootstrap
A link between console mode (the system firmware) and programming mode (the operating system).

Bugcheck
Software or hardware error fatal to OpenVMS processor or system.

Cache memory
A small, high-speed memory placed between slower main memory and the processor. A cache increases effective memory transfer rates and processor speed.

CMOS
Complementary metal oxide semiconductor.
CPMBX
Console Program Mailbox is used to pass information between operating systems and the firmware.

CRC
Character code recognition. The use of pattern recognition techniques to identify characters by automatic means.

CQMIC
CVAX to Q22–bus interface chip.

CSR
Control status register. A register used to control the operation of a device and record the status of an operation or both.

CPU
Central processing unit. The main unit of a computer containing the circuits that control the interpretation and execution of instructions. The CPU holds the main storage, arithmetic unit, and special registers.

DCOK
Q22–bus signal indicating dc power is stable. This signal is tied to the Restart switch on the System Control Panel.

DE
Diagnostic Executive is a component of the ROM-based diagnostics responsible for set-up, execution, and clean-up of component diagnostic tests.

DMA
Direct memory access. A method of accessing a device's memory without interacting with the device's CPU.

DNA
Digital Network Architecture.

EPROM
Erasable programmable read-only memory. EPROM is a type of read-only memory that can be erased by using ultraviolet light, returning the device to a blank state.
ECC
Error Correction Code. Code that carries out automatic error correction by performing an exclusive "or" operation on the transferred data and applying a correction mask.

Factory Installed Software (FIS)
Operating system software loaded into a system disk during manufacture. On site, the FIS is bootstrapped in the system, prompting a predefined menu of questions on the final configuration.

FEPROM
Flash Erasable Programmable Read-Only Memory (FEPROM). FEPROMs use electrical (bulk) erasure rather than ultraviolet erasure.

FIFO
First-in/first-out. A method used for processing or recovering data in which the oldest item is processed or recovered first.

Firmware
Functionally it consists of diagnostics, bootstraps, console, and halt entry/exit code.

FPU
Floating-point unit. A unit that handles the automatic positioning of the decimal point during arithmetic operations.

FRU
Field replaceable unit.

GPR
General Purpose Registers. On the KA52/53, they are the sixteen standard VAX longword registers R0 through R15. The last four registers, R12 through R15, are also known by their unique mnemonics: AP (Argument Pointer), FP (Frame Pointer), SP (Stack Pointer), and PC (Program Counter), respectively.

Initialization
The sequence of steps that prepare the system to start. Initialization occurs after a system has been powered up.

IPL
Interrupt Priority Level ranges from 0 to 31 (0 to 1F hex).
**IPR**
Internal Processor Registers implemented by the processor chip set. These longword registers are only accessible with the instructions MTPR (Move To Processor Register) and MFPR (Move From Processor Register) and require kernel mode privileges. This document uses the prefix "PR$" when referencing these registers.

**ISE**

**IT**
Interval timer.

**LED**
Light emitting diode.

**Machine check**
An operating system action triggered by certain system errors that can be fatal to system operation. Once triggered, machine check handler software analyzes the error, comparing it to predetermined failure scenarios. Three outcomes are possible: the system continues to run, the software program is halted, or the system crashes.

**μs**
Microsecond (10e-6 seconds)

**MMJ**
Modified modular jack.

**MOP**

**ms**
Millisecond (10e-3 seconds)

**MSCP**
Mass Storage Control Protocol is used in Digital disks and tapes.
NVR
Nonvolatile random access memory. A memory device that retains information in the absence of power.

NVRAM
Nonvolatile RAM. On the KA52/53, this is 1 Kb of battery backed-up RAM on the SSC.

PC
Program Counter or R15.

PCB
Process Control Block is a data structure pointed to by the PR$PCBB register and contains the current process' hardware context.

PFN
Page Frame Number is an index of a page (512 bytes) of local memory. A PFN is derived from the bit field $<23:09>$ of a physical address.

PR$ICC
Interval Clock Control and Status, IPR 24.

PR$IPL$
Interrupt Priority Level, IPR 18.

PR$MAPEN$
Memory Management Mapping Enable, IPR 56.

PR$PCBB$
Process Control Block Base register, IPR 16.

PR$RXCS$
R(X)ceive Console Status, IPR 32.

PR$RXDB$
R(X)ceive Data Buffer, IPR 33.

PR$SAVIP$S
SAVed Interrupt Stack Pointer, IPR 41.
PR$_SAVPC
SAVed Program Counter, IPR 42.

PR$_SAVPDL
SAVed Program Status Longword, IPR 43.

PR$_SCBB
System Control Block Base register, IPR 17.

PR$_SISR
Software Interrupt Summary Register, IPR 21.

PR$_TODR
Time Of Day Register, IPR 27, is commonly referred to as the Time Of Year register or TOY clock.

PR$_TXCS
T(X)ransmit Console Status, IPR 34.

PR$_TXDB
T(X)ransmit Data Buffer, IPR 35.

PROM
Programmable read-only memory. A read-only memory device that can be programmed.

PSL, PSW
Processor Status Longword is the VAX extension of the PSW (Processor Status Word). The PSW (lower word) contains instruction condition codes and is accessible by nonprivileged users; however, the upper word contains system status information and is accessible by privileged users.

QBMB
Q22–bus Map Base Register found in the CQBIC determines the base address in local memory for the scatter/gather registers.

QDSS
Q22–bus video controller for workstations.

QMR
Q22–bus Map Register.
QNA
Q22–bus Ethernet controller module.

RAM
Random access memory. A read/write memory device.

RAP
Register address port.

RIP
Restart In Progress flag in CPMBX<3>.

ROM
Read-only memory. A memory device that cannot be altered during the normal use of the computer.

rPB
Restart parameter block.

SCB
System Control Block. A data structure pointed to by PR$_{SCBB}$. It contains a list of longword exception and interrupt vectors.

SCSI
Small computer system interface. An interface designed for connecting disks and other peripheral devices to computer systems. SCSI is defined by an American National Standards Institute (ANSI) standard.

SDD
Symptom-Directed Diagnosis. Online analysis of nonfatal system errors in order to locate potential system fatal errors before they occur.

SGEC
Second Generation Ethernet Chip.

SHAC
Single Host Adapter Chip.
SP
Stack pointer. An address location that contains the address of the processor-defined stack. The processor-defined stack is an area of memory set aside for temporary storage or for procedure and interrupt service linkages.

SRM
Standard Reference Manual, as in *VAX SRM*.

SSC
System Support Chip.

TOY
Time of year.

**VAXcluster configuration**
A highly integrated organization of OpenVMS systems that communicate over a high-speed communications path. VAXcluster configurations have all the functions of single-node systems, plus the ability to share CPU resources, queues, and disk storage. Like a single-node system, the VAXcluster configuration provides a single security and management environment. Member nodes can share the same operating environment or serve specialized needs.

**VMB**
Virtual machine bootstrap. The VMB program loads and runs the operating system.

**OpenVMS**
Virtual memory system. The operating system for a VAX computer.
Index

A

Acceptance testing, 4-13 to 4-14
Algorithm
to find a valid RPB, 4-32
to restart operating system, 4-31
ANALYZE/ERROR, 5-14
interpreting CPU errors using, 5-15
interpreting DMA to host transaction faults using, 5-28
interpreting memory errors using, 5-18
interpreting system bus faults using, 5-26
ANALYZE/SYSTEM, 5-21
Asynchronous communications interfaces support for, 2-4
Asynchronous communications options list of, 2-4

B

Binary load and unload (X command), 3-35
Bits
  RPBSV_DIAG, 4-24
  RPBSV_SOLICT, 4-24
Block diagram, 1-3
Boot Block Format, 4-23
BOOT command, 3-13
Boot Flags
  RPBSV_BBLOCK, 4-23
Bootstrap
  conditions, 4-17
  definition of, 4-17
  disk and tape, 4-23
Bootstrap (cont’d)
  failure, 4-18
  initialization, 4-18
  memory layout, 4-19
  memory layout after successful bootstrap, 4-21
  network, 4-24
  preparing for, 4-18
  primary, 4-20
  secondary, 4-20

C

Comment command (!), 3-38
! (comment command), 3-38
Communications devices, 2-4
Communications options, 2-4
Configuration
  memory, 1-9
Connectors
  function of, 1-6
  identification of, 1-5
Console command
  LOGIN, 3-21
Console commands
  address space control qualifiers, 3-9
  address specifiers, 3-3
  binary load and unload (X), 3-35
  BOOT, 3-13
  ! (comment), 3-38
  CONTINUE, 3-15
  data control qualifiers, 3-9
  DEPOSIT, 3-15
  EXAMINE, 3-16
  FIND, 3-17
Console commands (cont'd)
   HALT, 3–18
   HELP, 3–18
   INITIALIZE, 3–20
   keywords, 3–10
   list of, 3–11
   MOVE, 3–22
   NEXT, 3–23
   qualifier and argument conventions, 3–3
   qualifiers, 3–9
   REPEAT, 3–24
   SEARCH, 3–25
   SET, 3–27
   SHOW, 3–28
   START, 3–31
   symbolic addresses, 3–4
   syntax, 3–3
   TEST, 3–31
   UNJAM, 3–35
   X (binary load and unload), 3–35

Console error messages
   sample of, 5–41

Console I/O mode
   special characters, 3–2

Console port, testing, 5–58

Console security feature
   values, 3–28

CONTINUE command, 3–15

Controls
   function of, 1–6
   identification of, 1–5

DNA Maintenance Operations Protocol
   (MOP), 4–24

Documents
   related, H–1

E
   Entry Point
      definition of, B–1
   Error during UETP, 5–57
      diagnosing, 5–56
   Error Log Utility
      relationship to UETP, 5–56
   Error messages
      console, sample of, 5–41
   EXAMINE command, 3–16
   External mass storage devices, 2–2

F
   FE utility, 5–47
   Files-11 lookup, 4–23
   FIND command, 3–17
   Firmware
      power-up sequence, 4–1
      updating, 6–1
   Flags
      restart in progress, 4–31

G
   General purpose registers (GPRs)
      symbolic addresses for, 3–4

H
   H3103 loopback connector, 5–58
   H8572 loopback connector, 5–58
   Halt
      dispatch, C–1
   HALT command, 3–18
   Halt protection, override, 5–48
   HELP command, 3–18
Indicators
  function of, 1–6
  identification of, 1–5
INIT, 4–18
Initialization
  following a processor halt, 4–31
  prior to bootstrap, 4–18
INITIALIZE command, 3–20
Initial power-up test
  See IPR
Internal mass storage devices
  list of, 2–2
IPL_31, 4–19
iSYS$TEST logical name, 5–56

KA50/51/55/56 CPU module
  block diagram of, 1–3
KA50/51/55/56 system
  communications options, 2–4
  configurations of, 2–1
  mass storage device configurations, 2–1
  memory configurations, 2–1
KA50 CPU module
  features of, 1–1
KA50 system
  configurations of, 1–1
KA51 CPU module
  features of, 1–1
KA51 system
  configurations of, 1–1
KA55 CPU module
  features of, 1–1
KA55 system
  configurations of, 1–1

Language selection menu
  messages, list of, 4–2
Local Memory Partitioning, 4–19
Log file generated by UETP
  OLDUETP.LOG, 5–57
LOGIN command, 3–21
Loopback connectors
  H3103, 5–58
  H8572, 5–58
  list of, 5–59
Loopback tests, 5–58
  console port, 5–58
  Ethernet, 5–58

Mass storage devices, 2–1
  external, 2–2
  internal, 2–2
  SCSI ID assignments, 2–4
Memory
  acceptance testing of, 4–13
  configurations, 1–10
  expansion connector identification, 1–9
  expansion of, 1–9
  isolating FRU, 4–14, 5–48
  rules for adding, 1–9
  testing, 5–48
Memory configuration
  KA50/51/55/56 system, 2–1
Memory modules, 1–9
Memory option
  installation of, 1–11
Memory test, 1–13
MEM test, 1–13
MicroVAX data types
  support of, 1–4
MicroVAX instructions
  support of, 1–5
MOM$LOAD, 4–25
MOP, functions, 5–53
MOP functions, 4–26
MOP program load sequence, 4–25
MOVE command, 3–22
MS44 memory modules, 1–9

N
Network listening, 4–30
NEXT command, 3–23
NVRAM
  CPMBX, E–2
  partitioning, E–1

O
OLDUETPLOG file, 5–56
Onboard memory
  location of, 1–9
OpenVMS
  error handling, 5–4
  event record translation, 5–14
Operating System
  bootstrap, 4–17
  restarting a halted, 4–31
Operating System Restart
  definition of, 4–31

P
Parameters
  for diagnostic tests, 4–9
  in error display, 5–42
Patchable Control Store
  Error messages, 6–8
PFN bitmap, 4–18
Ports
  function of, 1–6
  identification of, 1–5
POST
  See Power-on self-tests
Power-on self-tests
  description, 4–2
  errors handled by, 4–5
  kernel, 4–3

Power-on self-tests (cont’d)
  mass storage, 4–5
power-up
  machine state, 4–14
  memory layout, 4–15
Power-up sequence, 4–1
Power-up tests, 4–1
Primary Bootstrap, 4–20

R
Registers
  initializing the general purpose, 4–18
Related documents, H–1
REPEAT command, 3–24
REQ_PROGRAM, 4–30
Restart, 4–31
Restart Parameter Block (RPB)
  RIP flag, 4–31
ROM-based diagnostics, 4–6 to 4–10
  console displays during, 5–41
  isolating failures with, 5–43
  list of, 4–6
  parameters, 4–7
  utilities, 4–6
RPB
  initialization, C–5
  locating, 4–32
RPB Signature Format, 4–32
RZ-series ISE
  diagnostics, 4–5

S
Scripts, 4–11
  list of, 4–12
SCSI ID assignments
  recommendations for, 2–4
SEARCH command, 3–25
Secondary Bootstrap, 4–20
SET command, 3–27
SET HOST/DUP command, 3–27
SHOW command, 3–28
SICL messages, 5–34
  converting appended MEL files, 5–37
START command, 3–31
Symbolic addresses, 3–4
  for any address space, 3–7
  for GPRs, 3–4
Synchronous communications options
  list of, 2–5
Synchronous communications standards
  support for, 2–5
System hang, 5–58

T
TEST command, 3–31
Tests, diagnostic
  list of, 4–6
  parameters for, 4–9
Troubleshooting
  procedures, general, 5–2
  UETP, 5–57

U
UETINIT01.EXE image, 5–57
UETP
  interpreting OpenVMS failures with, 5–56
UETP.LOG file, 5–56
UNJAM, 4–18
UNJAM command, 3–35
User Environment Test Package (UETP)
  interpreting output of, 5–56
  running multiple passes of, 5–56
  typical failures reported by, 5–57
Utilities, diagnostic, 4–6

V
VAXELN
  and VMB, 4–20
VAXsimPLUS, 5–3, 5–32
  customizing, 5–39
  enabling SICL, 5–40
  installing, 5–38

Virtual Memory Boot (VMB), 4–21
  definition of, 4–20
  primary bootstrap, 4–20
  secondary bootstrap, 4–23

W
Warmstart, 4–31

X
X command (binary load and unload), 3–35