EMULEX

ENGINEERING CHANGE ORDER

NO. 4861 DATE 14 Jun 88

PAGE 1 OF 1

EQUIPMENT AFFECTED:

DCP-286 Module

- [x] CORRECTIVE
- [ ] MAINTAINABILITY
- [ ] RECORD CHANGE
- [ ] DEVIATION
- [ ] RELEASE
- [ ]

EFFECTIVITY:

All units in house

YES	NO	
[ ]	[x]	FCO REQUIRED
[ ]	[x]	SOFTWARE AFFECTED
[ ]	[x]	PUBLICATIONS AFFECTED

REASON FOR CHANGE:

Rev E documents the change from Rev C to D of PT1010247-xx for the removal of +5V from DB25 connectors for safety reasons.

DISPOSITION:
1. USE AS IS
2. REWORK
3. CHANGE PROMS
4. NOT APPLICABLE
5. INCORPORATE
6. SCRAP
7. SEE NOTE ON PAGE ___

DOCUMENT NUMBER	REV FROM	REV TO	TITLE/DESCRIPTION	NEXT ORDER	ON ORDER AT VENDOR	RECEIVING & INSPECTION	IN STOCK	IN PROCESS	SPARES	
PT1051029-00	D	E	DCP Module Installation							
			and Technical Reference	5	5	5	5	5	5	

Instructions:

Use PT1051029-00 Rev E with PT1010247-xx Rev D
Replace cover
Replace page 2-11
Reproduced in house

DISPOSITION NOTE:

ORIGINATOR	DESIGN SERVICES	PROJECT ENGINEER	MANUFACTURING
L. Bridges	E	Craig M. [illegible]	
QUALITY CONTROL	**FIELD SERVICE**	**TEST ENGINEERING**	**CERTIFICATION**

NO. 4861

PUBLICATION CHANGE NOTICE

EMULEX

NO. 1342 | DATE 23 FEB 88

PAGE 1 OF 1

SYSTEM AFFECTED: DCP-286

PUBLICATION NUMBER	PUBLICATION TITLE	REV FRM	REV TO	EFFECTIVE DATE
PT1051029-00	DCP-286 Module Installation and Technical Reference Guide	C	D	23 FEB 88

DISPOSITION

TYPE	ACTION	TYPE	ACTION
IN STOCK	See Instructions	DISTRIBUTED, HOUSE	See Instructions
ON ORDER	See Instructions	DISTRIBUTED, FIELD	See Instructions

REASON:

To revise FCC classification from Class B to Class A.

INSTRUCTIONS:

Print and distribute the following pages:

Cover
Inventory Checklist
iv, 3-8, 3-10
4-24, 4-25

NO.	ORIGINATOR	ENGINEERING SERVICES	ENGINEERING	MANUFACTURING
	L.L. Karanja			
	QUALITY CONTROL	FIELD SERVICE	PUBLICATIONS	MARKETING
	Susi Wray			

EF035(R6/85)

EMULEX

PUBLICATION CHANGE NOTICE

NO. 1322 DATE 19 JAN 88

PAGE 1 OF 1

SYSTEM AFFECTED

DCP-286

PUBLICATION NUMBER	PUBLICATION TITLE	REV FRM	REV TO	EFFECTIVE DATE
PT1051029-00	DCP-286 Module Installation and Technical Reference Guide	B	C	19 JAN 88

DISPOSITION

TYPE	ACTION	TYPE	ACTION
IN STOCK	See Instructions	DISTRIBUTED, HOUSE	See Instructions
ON ORDER	See Instructions	DISTRIBUTED, FIELD	See Instructions

REASON:

1) Add new time constant in Table 4-11.
2) Update information on initialization of the 8529 interrupt controller (subsection 4.7.1).
3) Remove +12 v from user interface (figures 4-11, 4-12, and 4-13).
4) Delete Addendum AD0053 because the 6 mHz version is no longer necessary.

INSTRUCTIONS:

Print and distribute.
No longer include the AD0053.

	ORIGINATOR	ENGINEERING SERVICES	ENGINEERING	MANUFACTURING
	H. Goldman	B. Lipkin	C.R. McElheny	K.M.
NO.	QUALITY CONTROL	FIELD SERVICE	PUBLICATIONS	MARKETING
	Susi Wray			

EF035(R6/85)

EMULEX

PUBLICATION CHANGE NOTICE

NO. 1281 | DATE 22 SEP 87

PAGE 1 OF 1

SYSTEM AFFECTED

DCP-286

PUBLICATION NUMBER	PUBLICATION TITLE	REV FRM	REV TO	EFFECTIVE DATE
PT1051029-00	DCP-286 Module Installation	A	B	22 SEP 87
	and Technical Reference Guide			

DISPOSITION

TYPE	ACTION	TYPE	ACTION
IN STOCK	Discard	DISTRIBUTED, HOUSE	Discard
ON ORDER	Use Rev B	DISTRIBUTED, FIELD	Discard

REASON:

To delete references to 6 MHz and convert to 8 MHz operation.

INSTRUCTIONS:

Print and distribute.

NO.	ORIGINATOR H. Goldman H. Goldman	ENGINEERING SERVICES	ENGINEERING	MANUFACTURING
	QUALITY CONTROL Susi Wray	FIELD SERVICE	PUBLICATIONS	MARKETING

EF035(R6/85)

DCP-286 MODULE INSTALLATION AND TECHNICAL REFERENCE GUIDE

EMULEX
3545 Harbor Boulevard
Costa Mesa, California 92626
(714) 662-5600 TWX 910-595-2521

PT1051029-00 Rev E
May, 1988

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Cliffhanger	DCP-286
DCP-88	DCP-EXEC

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WARNING

This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

First Printed: January, 1987

EMULEX

PUBLICATION ADDENDUM

NO. AD00053 DATE: 11-03-87

PUBLICATION NUMBER	PUBLICATION TITLE	REV	EFFECTIVE DATE
PT1051029-00	DCP-286 MODULE INSTALLATION	B	Immediately
	AND TECHNICAL REFERENCE GUIDE		

REASON

READ THIS FIRST

Please check your DCP-286. Refer to the product identification tag to ascertain the top assembly number of the board. If your DCP-286 has the top assembly number PT1010229, please note the following changes in this manual:

1. On p. 2-2, the jumper should be between E7 and E8 rather than between E6 and E7.

2. On pages 4-27 and 4-28, please use the column for 3.6864 MHz time constants from the following tables:

Table 4-10. Synchronous Time Constants

Baud Rate	Time Constant (in hex)	
	7.3728 MHz*	3.6864 MHz**
64 K	0038	001B
56 K	0040	001F
38.4 K	005E	002E
19.2 K	00BE	005E
9600	017E	00BE
7200	01FE	00FE
4800	02FE	017E
3600	03FE	01FE
2400	05FE	02FE
2000	0732	0398
1800	07FE	03FE
1200	0BFE	05FE
600	17FE	0BFE
300	2FFE	17FE
150	6002	3000
134.5	6B0E	3586
110	82E6	4172
75	BFFE	5FFE

* Top Assembly Number PT1010247 (8 MHz)
** Top Assembly Number PT1010229 (6 MHz)

ORIGINATOR	ENGINEERING SERVICES	ENGINEERING	PUBLICATIONS
Craig McElhaney		Craig McElhaney	

Table 4-11. Asynchronous Time Constants
(Divided by 16)

Baud Rate	Time Constant (in hex)	
	7.3728 MHz*	3.6864 MHz**
38.4 K	0004	0001
19.2 K	000A	0004
9600	0016	000A
7200	001E	000E
4800	002E	0016
3600	003E	001E
2400	005E	002E
2000	0072	0038
1800	007E	003E
1200	00BE	005E
600	017E	00BE
300	02FE	017E
150	05FE	02FE
134.5	06B0	0357
110	082C	0415
75	0BFE	05FE
50	11FE	08FE

* Top Assembly Number PT1010247 (8 MHz)
** Top Assembly Number PT1010229 (6 MHz)

INVENTORY CHECKLIST

Your Emulex(r) DCP-286 carton contains the following:

- DCP-286 Module
- Card Guide
- Cliffhanger Assembly
  - Single Cliffhanger (connects second serial line to board)
  - Double Cliffhanger (connects serial lines 3 and 4 to board)
- Diagnostic Diskette (including the Diagnostic Manual as a text file)
- DCP-286 Module Installation and Technical Reference Guide
- Limited Warranty (Printed on Back of Inventory Checklist)

If any items are missing or damaged, consult your place of purchase for the procedure to follow in order to correct the problem.

Insert this documentation into the Guide to Operations (in the section reserved for add-on options) that you received with your IBM Personal Computer.

LIMITED WARRANTY

Emulex Corporation warrants this Personal Computer compatible product to be in good working order for a period of two years from the date of purchase from Emulex Corporation or an authorized Emulex dealer. Should this product fail to be in good working order at any time during this two year warranty period, Emulex Corporation will, at its option, repair or replace this product at no additional charge except as set forth below. Repair parts and replacement products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of Emulex Corporation. This limited warranty does not include service to repair damage to the product resulting from accident, disaster, misuse, abuse or non-Emulex modification of the product including product expansion through plug-in additions except as provided by Emulex Corporation.

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Section 1
INTRODUCTION

1.1 Overview

This guide explains how to install and use the Emulex DCP-286 Module, a high performance, multiprotocol communications processor card designed to provide parallel processing capability for the IBM PC, PC-XT, PC-AT, and IBM-compatibles. This guide includes technical reference information about the hardware and software to aid you in programming and using the module for custom applications.

The flexible architecture of the DCP-286 coupled with the power of the on-board 80286 microprocessor provide powerful co-processing capabilities. They elevate the PC to a general-purpose "work horse," regardless of the application or industry, as follows:

- from multitasking, multiprocessing applications where the PC acts as a work station
- to sophisticated communications networking where you need to build a "PC within a PC"

By using such state-of-the-art technology as the Intel iAPX 286 microprocessor system, surface mount components, and CMOS and AS/ALS Schottky devices, DCP-286 design emphasizes power, performance, and flexibility. The goal is to provide an efficient environment, so that users, original equipment manufacturers (OEMs), systems developers, and systems integrators can get the most from the PC.

1.1.1 How To Use This Guide

This guide contains information for setting up and installing the DCP-286 Module as follows:

- Section One (Introduction) introduces the DCP-286. The unique features and capabilities of the module in relation to specific uses are explored. Performance factors and compatibility with other Emulex DCP-88 products are also included.
- Section Two (DCP-286 Module Setup) describes how to set the switches and jumpers on the DCP-286.
- Section Three (DCP-286 Module Installation) describes how to physically install the board in your PC.
- Section Four explores the technicalities of the DCP-286 hardware.
- Section Five explains how to use the sample DMA program supplied on the diskette as an example to guide you in programming for the DCP-286.
- Appendix A is a summary of the switch and jumper settings.

1.1.2 Related Documentation

Although this guide includes technical information about the operation and programming of the DCP-286, it does not describe the instruction set or give technical details about the Intel iAPX 286 microprocessor system, 8530 Serial Communications Controller device, 8259 Interrupt Controller, or the 8254 Counter/Timer device. This manual does not include specific information about the IBM family of PCs.

For additional information in these areas, refer to the following documents:

- *Technical Reference Personal Computer PC*
  IBM Corporation # 1502234, April 1983.
- *Technical Reference Personal Computer AT*
  IBM Corporation # 1502494, March 1984.
- *DCP/VM Module for the IBM PC*
  Emulex/Emulex User's Manual # 16-00445-00 Rev D, 1985.
- *Microsystem Components Handbook*, Vols I and II
  Intel Corporation # 230843-002, 1985.
- *Memory Components Handbook Supplement*
  Intel Corporation # 210830-004, 1985.
- *Technical Manual, Z8030/Z8530 SCC Serial Communications Controller*
  Zilog, Inc. # 00-2057-02, 1983.

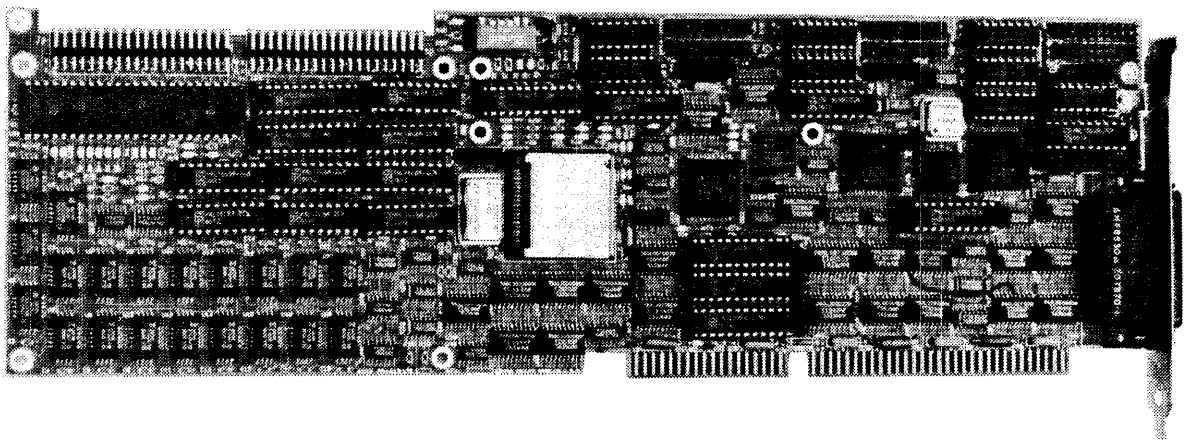
1.2 General Description

The Emulex DCP-286 Module (Figure 1-1) is a high-performance, multiprotocol communications processor with on-board "intelligence" that fits in a full-size expansion slot. It is ideal as a front-end communications processor to offload the overhead associated with handling communications. architecturally, the DCP-286 hardware is flexible and powerful enough for creating "a computer within a computer" by writing software to handle your co-processing needs.

As an "intelligent" controller, the DCP-286 provides four multiprotocol communications lines (RS-232) with four DMA channels that are software configurable from full-duplex to four half-duplex lines.

Memory is fixed at 512 KB. The DCP-286 can share memory with the PC through a user-selectable 16/32/64 KB window that is enabled/disabled under software control.

A communications piggyback adapter can be provided as a means for converting all four communications lines to RS-422/485.



PT1029-0173

Figure 1-1. The Emulex DCP-286 Module

1.3 Hardware and Software Requirements

An IBM PC, PC-XT, PC-AT, or IBM-compatible with a minimum of 256 KB of RAM and one floppy disk drive is required to support the DCP-286.

The DCP-286 is not dependent on any particular operating system -- rather, user-written software drivers and applications tailor the DCP-286 functionality to fit the specific needs.

1.4 Compatibility with the DCP-88 Module

The Emulex DCP-88/VM Module (herein referred to as the DCP-88) is the predecessor to the DCP-286 Module. A multiprotocol, communications processor board with an on-board 8088 microprocessor, the DCP-88 is generally compatible with the DCP-286. However, some areas of functional differences must be considered between the two modules. These areas are outlined in the following subsections.

1.4.1 Control Registers

Although the DCP-286 has three control registers to the one control register on the DCP-88, the control and status bits for the DCP-286 are virtually the same as the DCP-88 except for some default values in the second and third control registers.

Control Register 1: In a write operation, bits 0 through 7 of this register are identical between the two modules. No differences in the control functions of the register exist between the DCP-286 and the DCP-88.

A read operation of this register produces identical results for the two modules except for bit 4.

In the DCP-88, bits 4 and 5 are the memory size status bits. When a 0 is read from bit 4, two banks of memory are installed. In the DCP-286, memory size is fixed at 512 KB; therefore, bits 4 and 5 are returned as 0,0.

Control Register 2: Two bits in Control Register 2 must be set on the DCP-286 to ensure compatibility with the DCP-88. Bit 7 must be set to a 1 to enable interrupts to the PC, and bit 6 must be set to a 1 to enable shared memory.

Bits 6 and 7 are cleared to a 0 after a power-on reset.

Control Register 3: Unlike the DCP-88, the PC's base address for shared memory is programmable in the DCP-286. After a power-on reset, this base address is 00000 and the window size is 64 KB. Before shared memory can be used, the base address must be defined by Control Register 3. (See Section 4.3.1.3.)

1.4.2 Shared Memory

Unlike the DCP-88, shared memory on the DCP-286 can be initialized and verified without going into transparent mode. Parity checking is enabled after a power-on reset and is not affected by a programmed reset.

1.4.3 Interrupts

Unlike the DCP-88, which has certain interrupts fixed by hardware, the DCP-286 interrupts are tri-stateable and must be enabled by setting bit 7 of Control Register 2 to a 1. The interrupt vectors for the timers and the maskable interrupt from the PC are under program control and are no longer fixed. These interrupts are also maskable through the 8259 Interrupt Controller. (See Section 4.7.)

Transparent interrupts for the DCP-286 are on the same level as the programmable interrupt request to the PC.

1.4.4 Timers

An Intel 8254 timer on the DCP-286 provides three timer counters. The DCP-88 time interval of 17.8 milliseconds (ms) can be realized by any of these three counters. (See Section 4.8.)

1.5 Performance

Using DMA, the DCP-286 is capable of supporting high speed data transfers. The general performance of the 80286 microprocessor as compared to the 8088 4.77 MHz microprocessor is assumed to be twice as high with a 20% improvement because of the 16-bit memory structure.

The rates shown in Table 1-1 are the limits of the DCP-286 as defined by DMA hardware and the Serial Communications Controllers (SCCs). Background processing has not been considered in these figures.

Table 1-1. Maximum Transfer Rates
(Background Processing not Considered*)

Module Configuration	Bits/sec Per Line	Bits/sec Aggregate
8 MHz	1.5 M	1.830 M

* In determining actual performance with a typical application, background processing becomes a factor.

Background processing is the amount of time it takes to process each character after it has been received into memory from the 8530 SCCs. The time required to transfer the character from the SCC to memory is considered foreground processing time.

1.6 Configuration Options

The DCP-286 is set up to support an optional RS-422/485 piggyback board interface. RS-232 drivers and receivers (U48, U49, U64, U65, U85, U86, U87, and U92) are in sockets. These drivers/receivers may be replaced with 14-pin shunts to provide TTL levels to the headers for each communication line. Provision is made to support the RS-422/485 piggyback adaptor approximately one inch by eight inches for protocol conversion.

CAUTION

Do not use 16-pin shunts to replace RS-232 drivers/receivers, as this will short -12 V to ground, and blow fuse F1.

1.7 Features

The main features of the DCP-286 module are as follows:

- 80286 microprocessor -- 8 MHz; 0 wait states; interleaved memory.
- Four, multiprotocol communications lines:
  - DTE/DCE configurable
  - Software configurable DMA support: 4 half-duplex lines; 2 full-duplex lines; or 2 half-duplex lines and 1 full-duplex line.
- Three timer counters with maskable interrupts.
- 16/32/64 KB shared memory window sizes

BLANK

Section 2
DCP-286 MODULE SETUP

2.1 Overview

This section describes the various selectable configuration options on the DCP-286. You should choose the setup for your needs and make the selections before you install the module in your PC.

Setting up the DCP-286 module consists of setting switches on the SW1 switch bank and installing or removing jumpers at various locations on the module. Section 2.2 shows the factory configuration. If you choose the factory configuration, you should check to be sure the switch positions and jumper placements remained intact during shipping.

If you need to make other selections, Sections 2.3 and 2.4, respectively, describe the switch options and the jumper selections.

2.2 Checking the Factory Configuration

Figure 2-1 is a layout of the DCP-286 for your reference in locating switch and jumper positions on the board and making connections. It also shows the factory configuration. Figure 2-2 shows the switch settings for alternate base I/O addresses for the DCP-286 control registers.

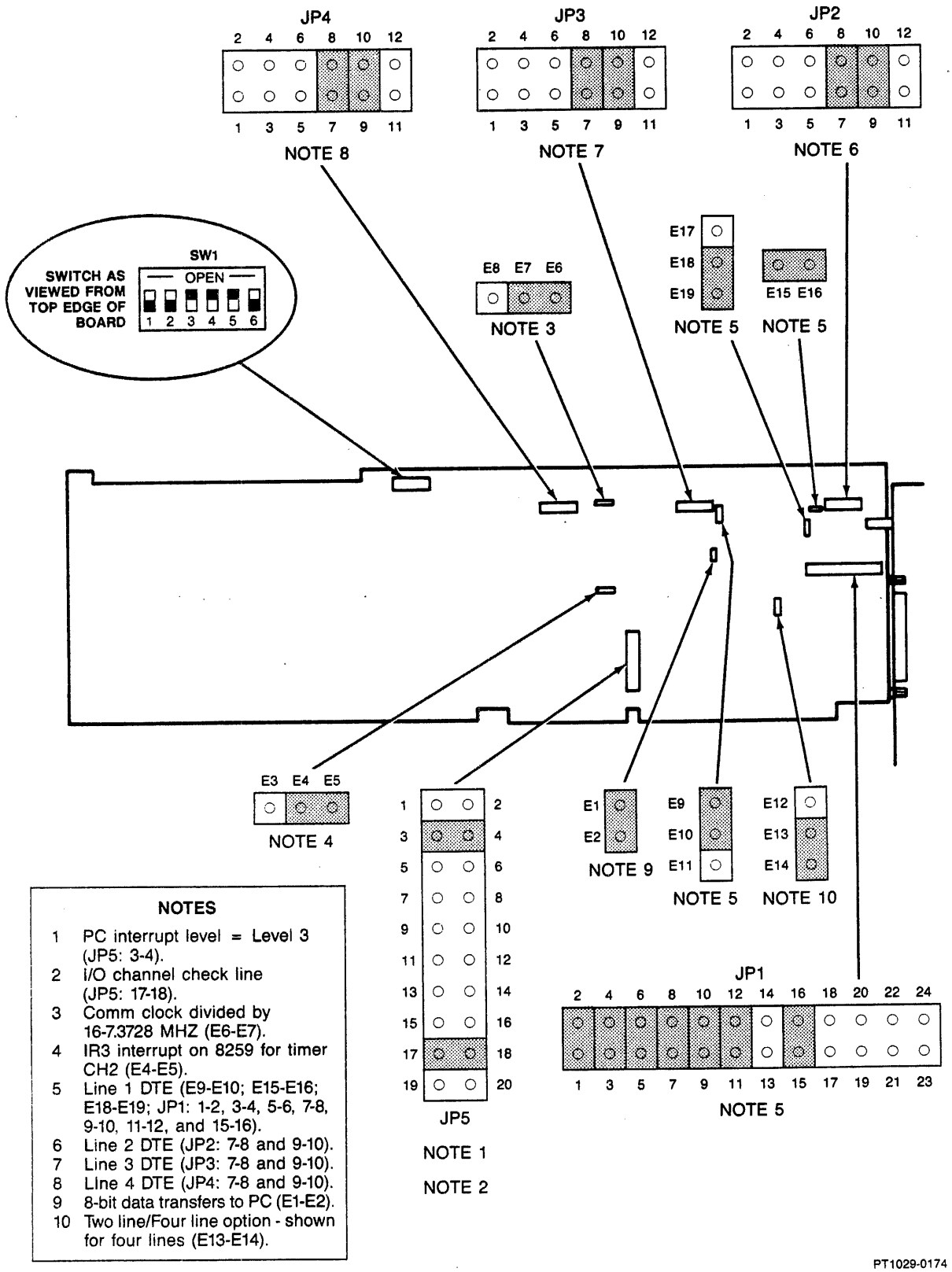


Figure 2-1. Layout Drawing of the DCP-286: Factory Jumper and Switch Configurations

2.3 Option Switches

Switch bank SW1 (see Figure 2-1) allows you to select the following:

- The I/O base address that the PC sees.
- AT bus configuration with two I/O connectors or PC bus configuration with one connector.

2.3.1 Base I/O Address to PC

The PC sees four Control Register addresses for the DCP-286. You must select the base address for these four Control Registers using switches 1 through 4 on SW1. Figure 2-2 illustrates the various settings.

2.3.2 DCP-286 Memory

Switch 6 on SW1 is configured ON at the factory. In this position, all accesses to DCP-286 memory are "wrapped around" on a 512-KB boundary. The power-on reset address is supported at the top of the 512 KB of DCP-286 memory (7000:FFF0). Switch 6 must remain in the ON position. Otherwise DCP-286 memory will not "wrap around," and the power-on reset address will not be supported.

2.3.3 AT Bus Configuration

Switch 5 on SW1 is configured OFF (OPEN) at the factory. In this position, the DCP-286 is configured for a PC-type bus, and must be configured for 8-bit data transfer (see Section 2.4.7). The DCP-286, in this configuration, may be operated in an AT-type bus with two connectors. The data transfers are, however, limited to 8 bits.

The DCP-286 may be configured for 16-bit data transfer by placing switch 5 on SW1 in the ON (CLOSED) position. In this position, the DCP-286 must be plugged into a PC/AT-type bus with two connectors. This placement allows the DCP-286 to be addressed above the 1M boundary in PC/AT memory. In this configuration, the user **must** configure the DCP-286 for 16-bit data transfer (see Section 2.4.7).

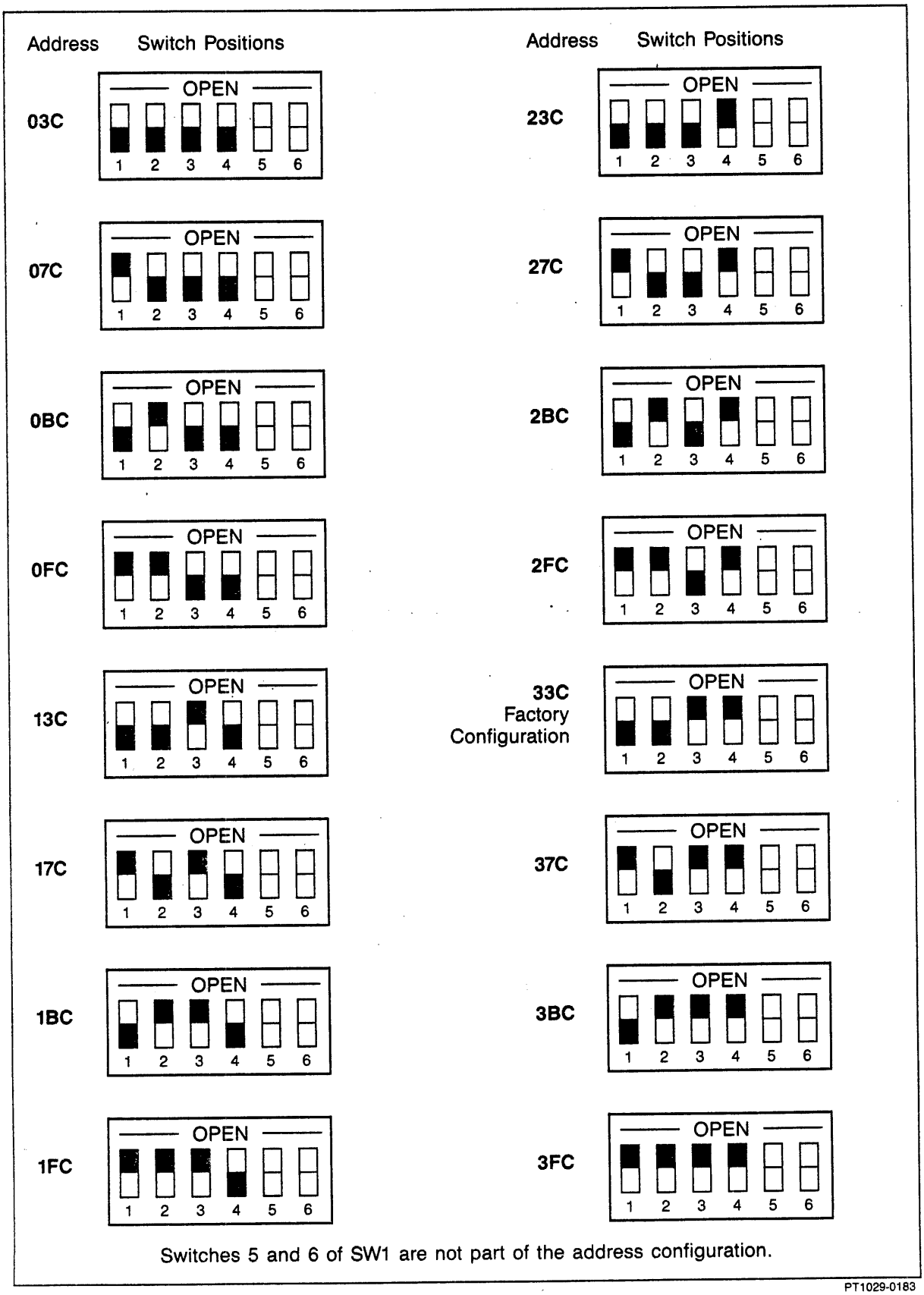


Figure 2-2. Base I/O Address Switch Settings

2.4 Jumper Selectable Options

Several configuration options for the DCP-286 are made by installing or removing jumpers at specific positions. These options are explained in the following subsections. Refer to Figure 2-1 for the locations on the board.

2.4.1 Selection of Timer Input Clock Rate

The input clock rate to the three timer channels on the 8254 is jumper selectable between the communications clock divided by 8 or 16. The factory setting is for a communications clock of 7.3728 MHz. It provides a time interval from 4.34 microseconds to 142 milliseconds.

Moving the jumper to E7-E8 allows for halving the range of the time interval, which was 4.34 microseconds - 142 milliseconds, to a range of 2.17 microseconds - 71 milliseconds.

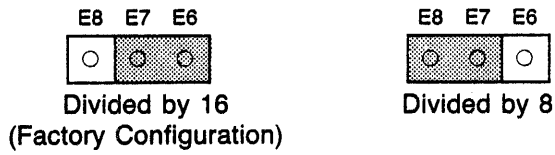


Figure 2-3. Options for Timer Input Clock Rate

2.4.2 PC Interrupt Level

Four interrupt levels are available in the IBM PC as shown in Figure 2-4.

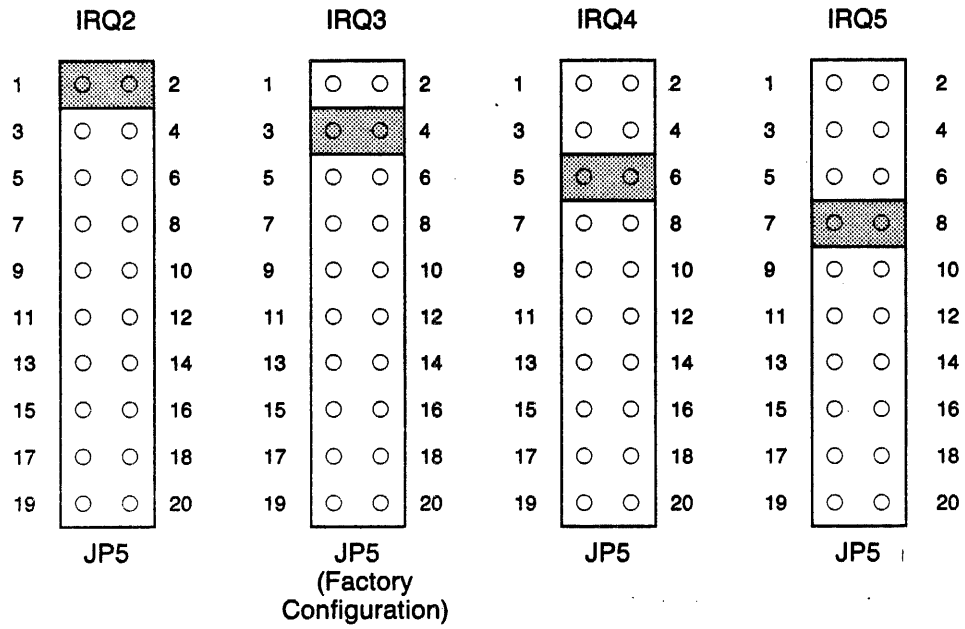


Figure 2-4. Interrupt Level Choices -- IBM PC

Four additional interrupt levels are available for PC-AT as shown in Figure 2-5.

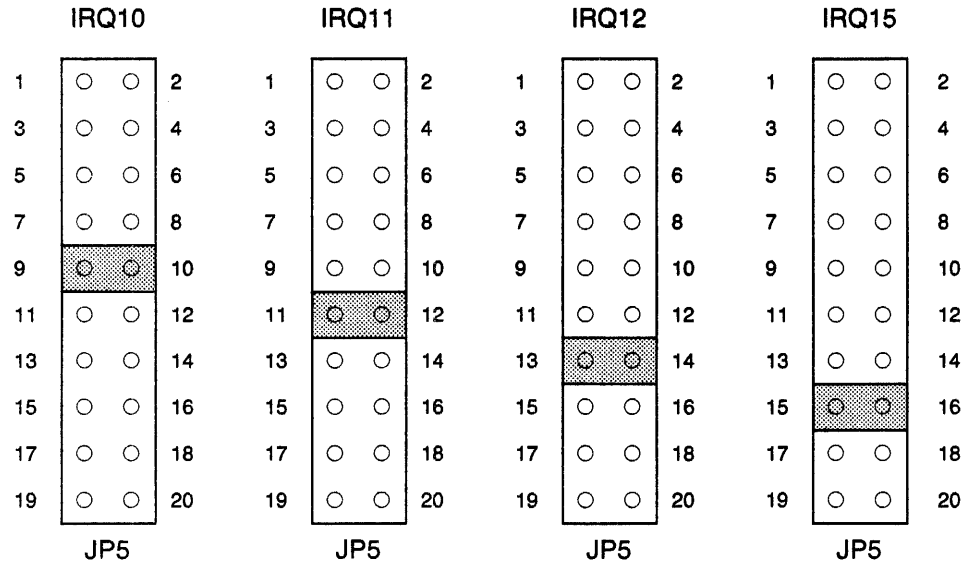


Figure 2-5. Interrupt Level Choices -- PC-AT

2.4.3 Local Interrupt Level

The level 3 interrupt (IR3) on the 8259 Interrupt Controller on the DCP-286 is selectable between timer CH2 and an unused interrupt (EIRQ0-). The jumper positions for these two interrupts are shown in Figure 2-6.

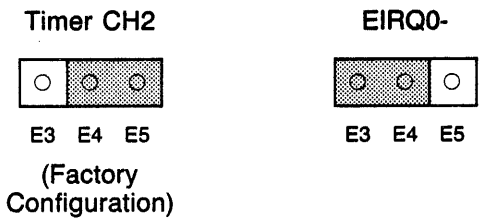


Figure 2-6. IR3 Interrupt Selections

2.4.4 PC I/O Channel Check Disable

The factory configuration of the DCP-286 provides an interrupt line to the PC for parity errors. For debugging purposes, that line may be "open circuited" by removing the jumper at JP5: 17-18

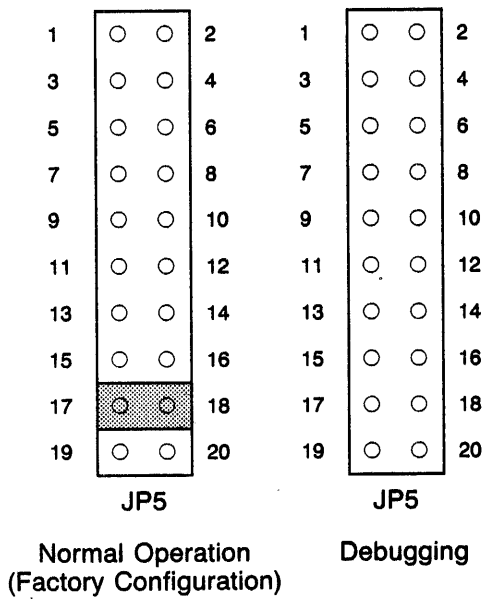


Figure 2-7. PC I/O Channel Check Disable

2.4.5 DTE/DCE Configurations

You must set up each communications line as Data Terminal Equipment (DTE) or Data Communications Equipment (DCE). The DTE and DCE jumper positions for each line are shown in Figures 2-8 through 2-12.

Choose DTE or DCE for each line and place the jumpers as shown for each line.

Communications line 1 requires extensive jumper placements on JP1 as well as some E#s. All positions not shown as shadowed must be OPEN (OFF). Figure 2-8 shows the DTE configuration, which is the factory configuration. Figure 2-9 shows the DCE configuration.

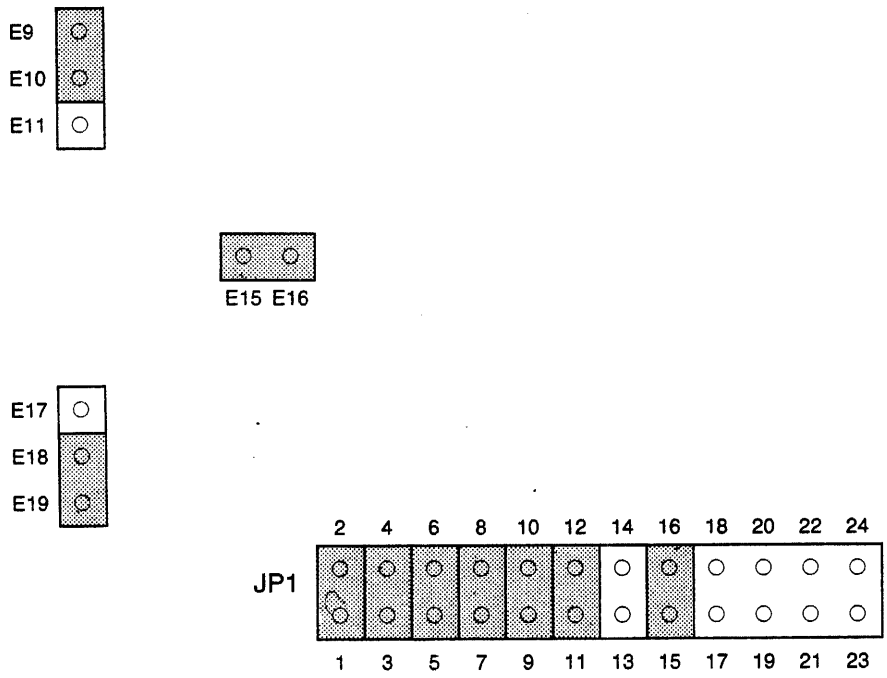


Figure 2-8. Line 1 as DTE

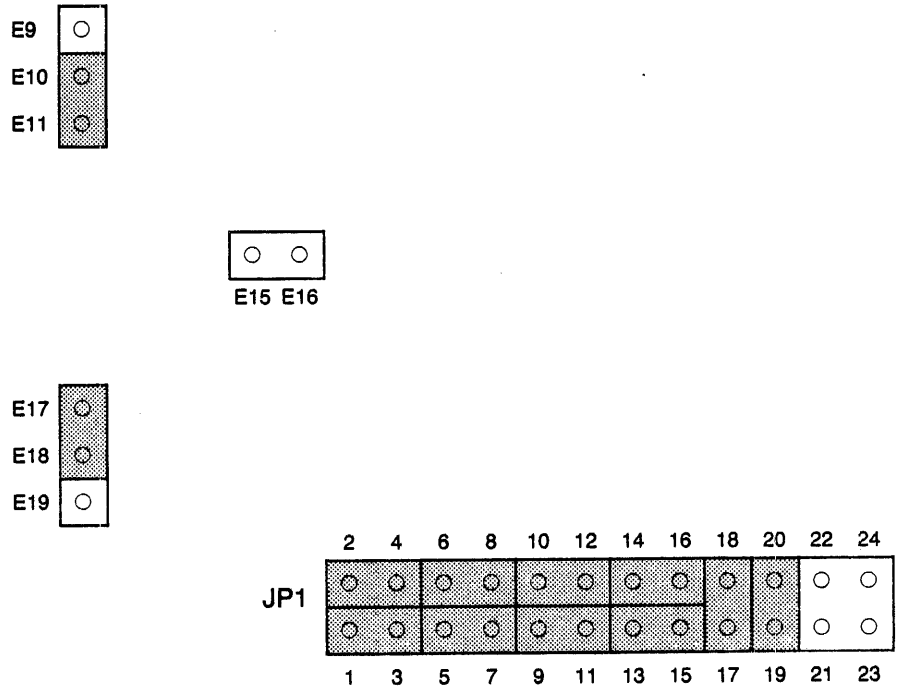


Figure 2-9. Line 1 as DCE

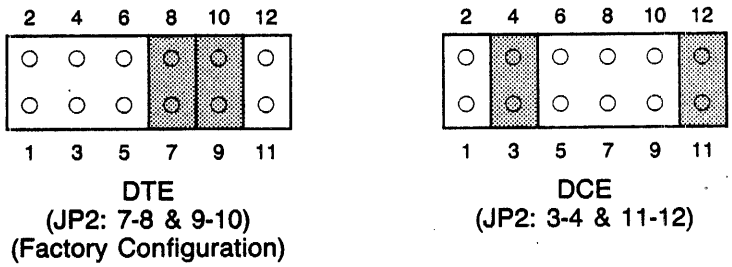


Figure 2-10. Line 2 -- DTE and DCE Positions

Figure 2-11. Line 3 -- DTE and DCE Positions

Figure 2-12. Line 4 -- DTE and DCE Positions

2.4.6 RS-422 System Voltage

To set up the voltage required (+5 volts) for an RS-422 communications piggyback adapter, install jumpers as shown in Figure 2-13. (This option is not available on Rev. C boards or later.)

NOTE

Line 1 is not used in this configuration.

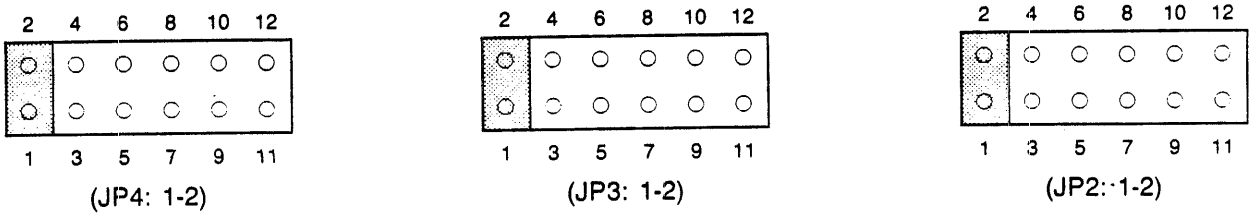


Figure 2-13. RS-422 Voltage Setup

2.4.7 8/16-Bit Data Transfers

When operating in a PC/AT bus or equivalent, the DCP-286 must be configured for 16-bit data transfers to and from the AT. It is also a requirement that the shared memory window for the DCP-286 be addressed above one megabyte in the AT's memory and that the window size be one megabyte. If the window size cannot be one megabyte, the DCP-286 should be configured for 8-bit transfers and switch position 5 on SW1 should be placed in the OPEN (OFF) position.

The DCP-286 is configured for 16-bit transfers by removing the jumper between E1 and E2 and placing it between 19 and 20 on JP5. Figure 2-14 shows this jumper placement. To configure the DCP-286 for 8-bit data transfers, remove the jumper between 19 and 20 on JP5 and place it between E1 and E2.

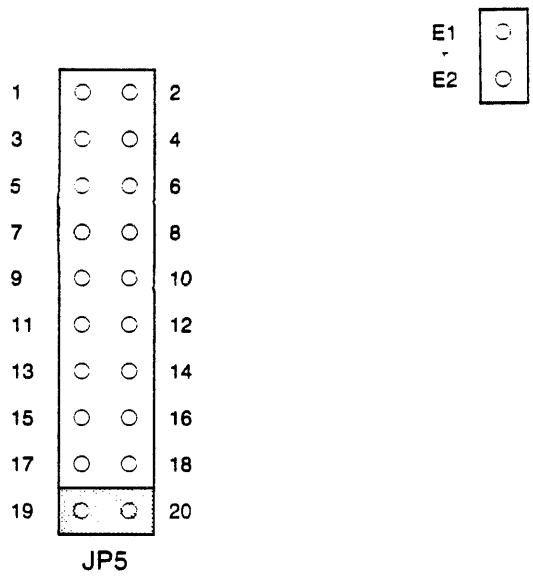


Figure 2-14. Jumper for 16-Bit Data Transfers

2.4.8 2/4 Communication Lines Option

When the DCP-286 is configured for only two communications lines, the jumper between E12 and E13 should be installed (see Figure 2-15). For four line operation, the jumper must be placed between E13 and E14.

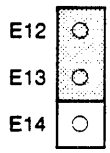


Figure 2-15. Jumper for Operation with Two Communication Lines

Section 3
INSTALLATION

3.1 Overview

This section describes the steps that must be taken to prepare the PC and to physically install the DCP-286 Module in the PC motherboard. Instructions are given for IBM machines only; you should consult your reference manual if you are installing the DCP-286 in an IBM compatible machine.

3.1.1 Tool Requirements

The only tool you need to install the DCP-286 is a flat-blade screwdriver.

3.2 Removing the System Unit Cover

In order to gain access to the expansion slots on the motherboard, you must disconnect the system unit from the other system components and remove the unit cover. The following steps explain how to prepare your IBM unit for the DCP-286 installation (for non-IBM units, refer to the appropriate installation manual for instructions on removing the system cover):

1. Turn off the system unit power switch. Turn off the power switches on all peripheral equipment (printer, monitor, and so forth). Unplug the system unit and other optional equipment from the wall outlet.

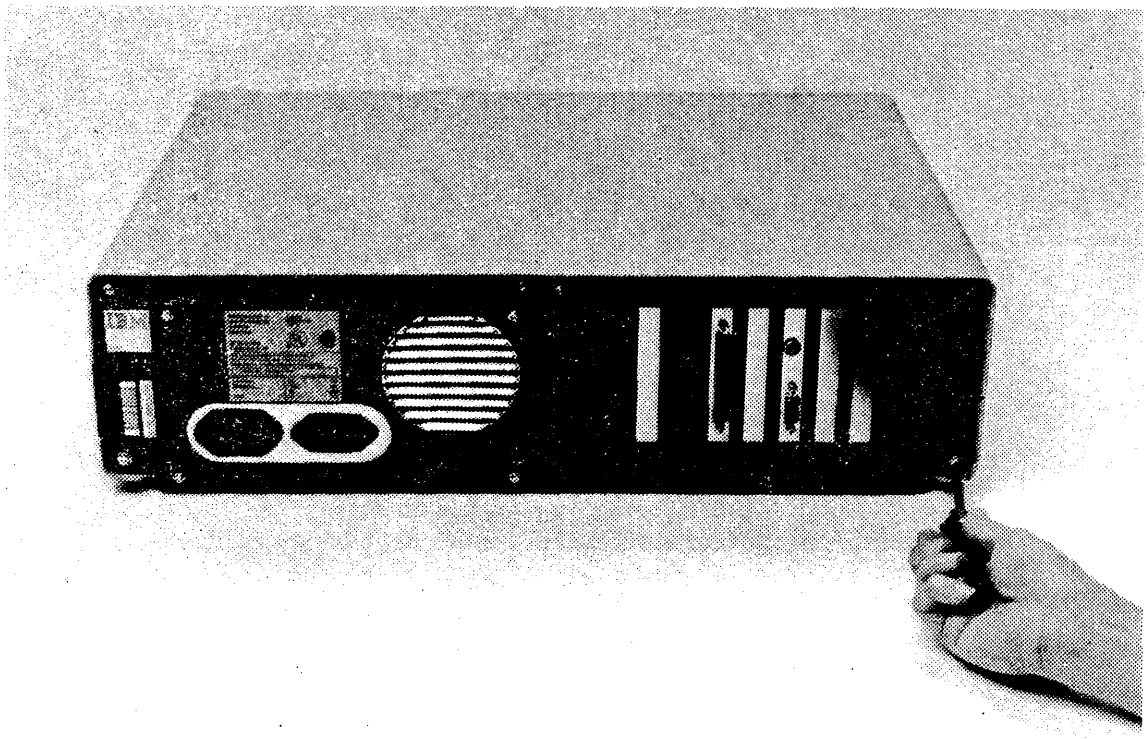
2. Disconnect all peripheral cables (including the keyboard cable) from the rear panel of the system unit. Remove all peripherals from the work area.

3. Turn the system unit around so you have easy access to the rear panel.

   Remove the cover mounting screws located on the rear panel, using a flat blade screwdriver, as shown in Figure 3-1. (If you have a PC-AT, you must first remove the back panel, which is attached to the rear of the unit with Velcro strips.)

The number of screws depends on the model of your PC. Newer PCs, PC-XTs, and PC-ATs have five screws; older PCs have two screws. The screws are located in the upper and lower left and right corners and the upper center of the back panel.

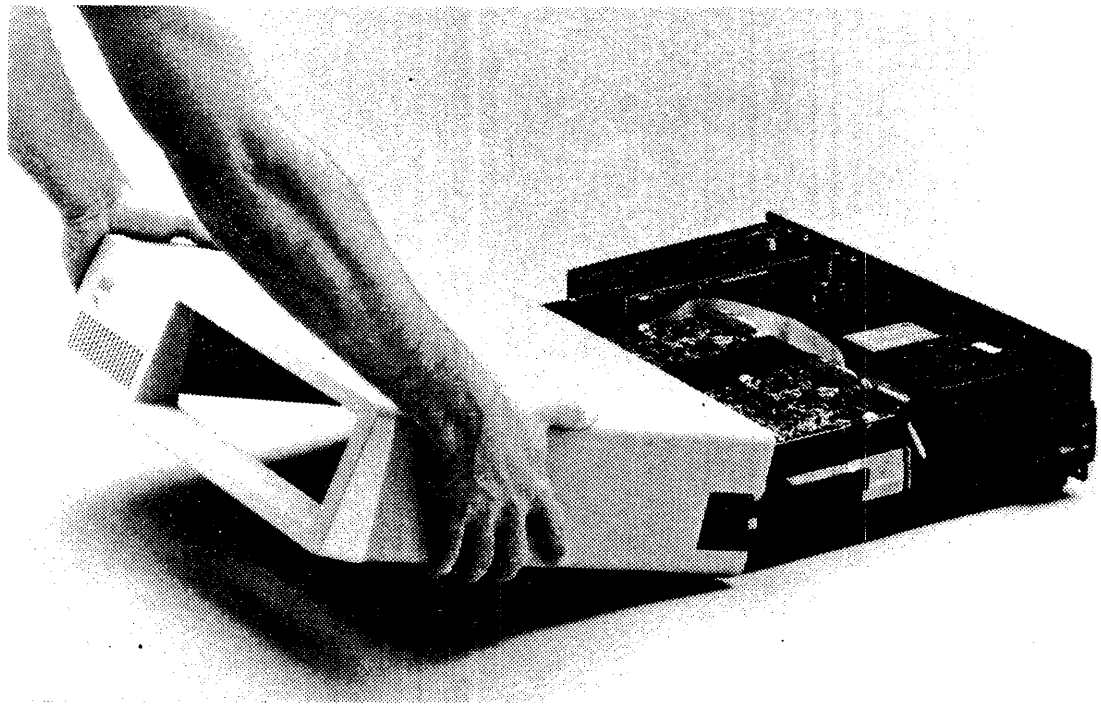
Turn the screws counterclockwise; after removing the screws, place them in a safe location.



PT1029-0014

Figure 3-1. Removing the Cover Mounting Screws

4. Carefully slide the system unit cover forward from the rear as shown in Figure 3-2. When the cover will go no farther, tilt the cover up and remove it from the base. Set the cover aside in a safe place.



PT1029-0015

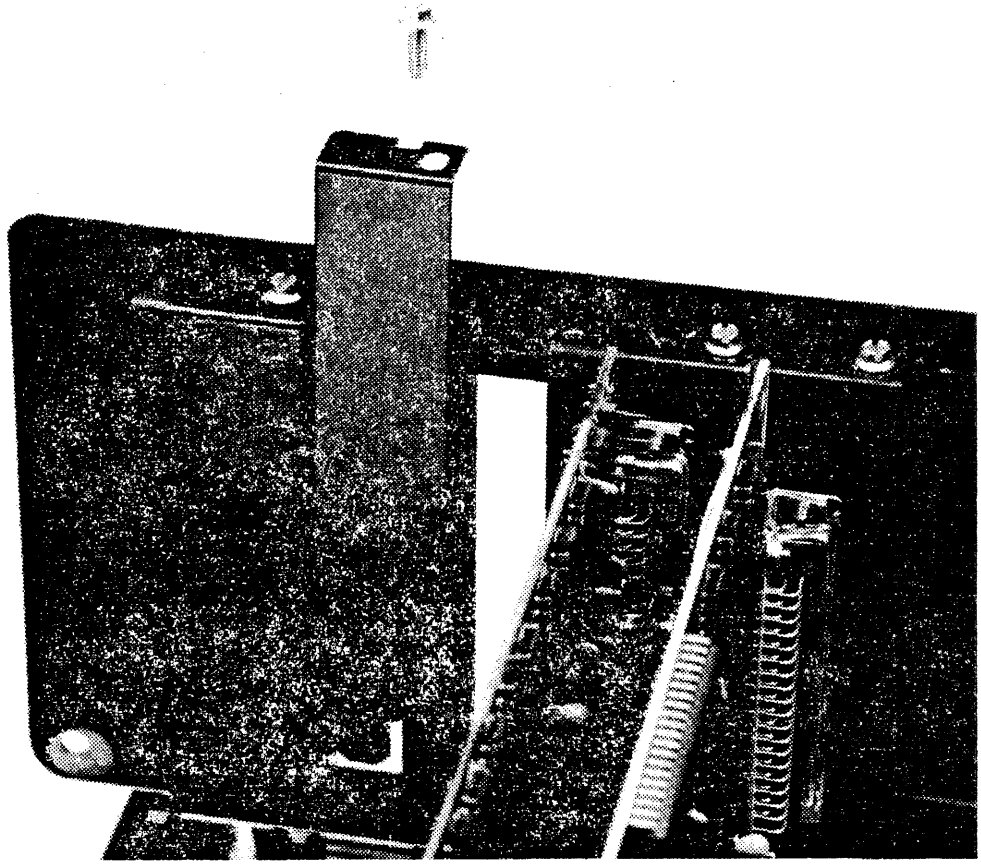
Figure 3-2. Removing the System Unit Cover

3.3 Installing the DCP-286

The following steps explain how to install your Emulex DCP-286 Module.

1. Facing the disk drives, look at the inside left rear of your system unit. Several expansion slots are available for additional cards; you can install your DCP-286 in any one of the unused slots.

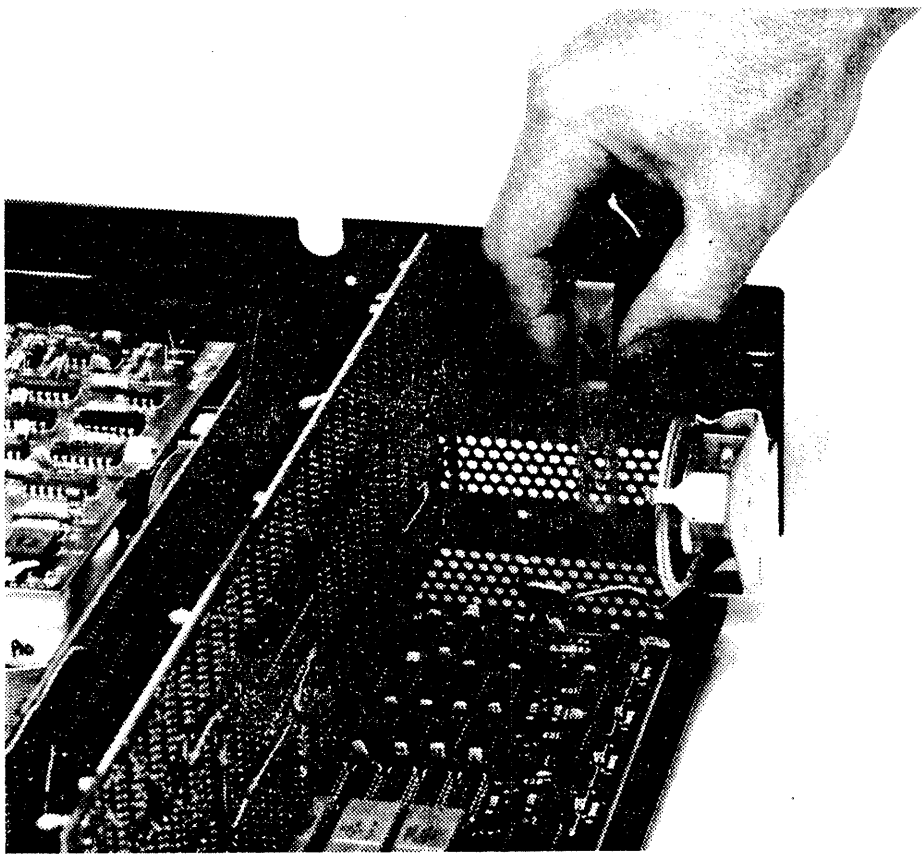
2. Using a flat blade screwdriver, remove the screw that holds the system expansion slot cover in place (see Figure 3-3).



PT1029-0020

Figure 3-3. Removing the System Expansion Slot Cover

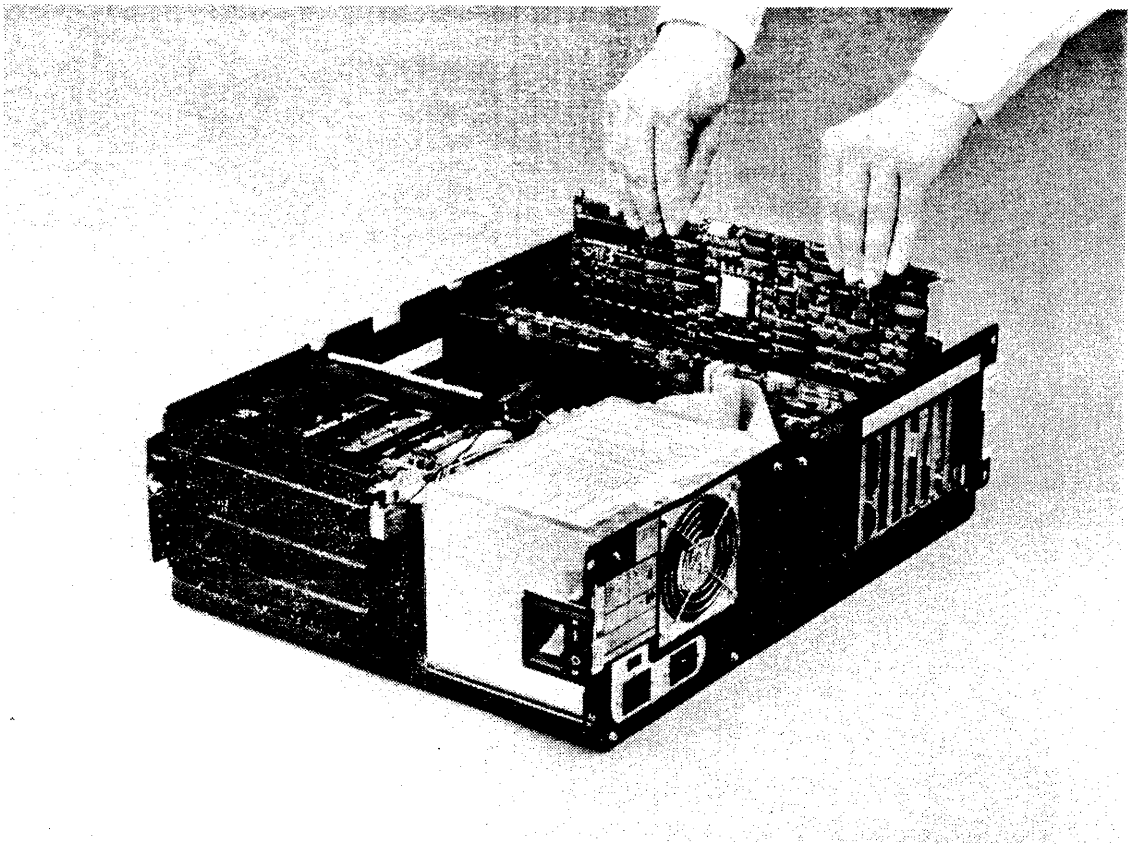
3. Install the card guide that was supplied with the DCP-286, using the holes that are aligned with the slot you are planning to use for the adapter (see Figure 3-4). Card guides are built into the PC-AT, so this step is not necessary if you are installing the adapter in a PC-AT.



PT1029-0021

Figure 3-4. Installing the Forward Card Guide

4. Insert the DCP-286 into the IBM motherboard connector, fitting the connector on the DCP-286 through the rear panel of the system unit. Once the edge connector is aligned into the motherboard, seat the board by pressing down on the top edge of the board with the heel of your hand (see Figure 3-5).



PT1029-0175

Figure 3-5. Seating the Adapter in the IBM Motherboard

5. Attach the Cliffhangers to the DCP-286 board.

   - Line 2 comes out on a single, male DB-25 Cliffhanger.
   - Lines 3 and 4 come out on a double, male DB-25 Cliffhanger.

   The ribbon cables of each Cliffhanger must be attached to the appropriate connector on the DCP-286 Module. These connectors are located along the top edge of the board (see Figure 3-6 for the exact locations.)

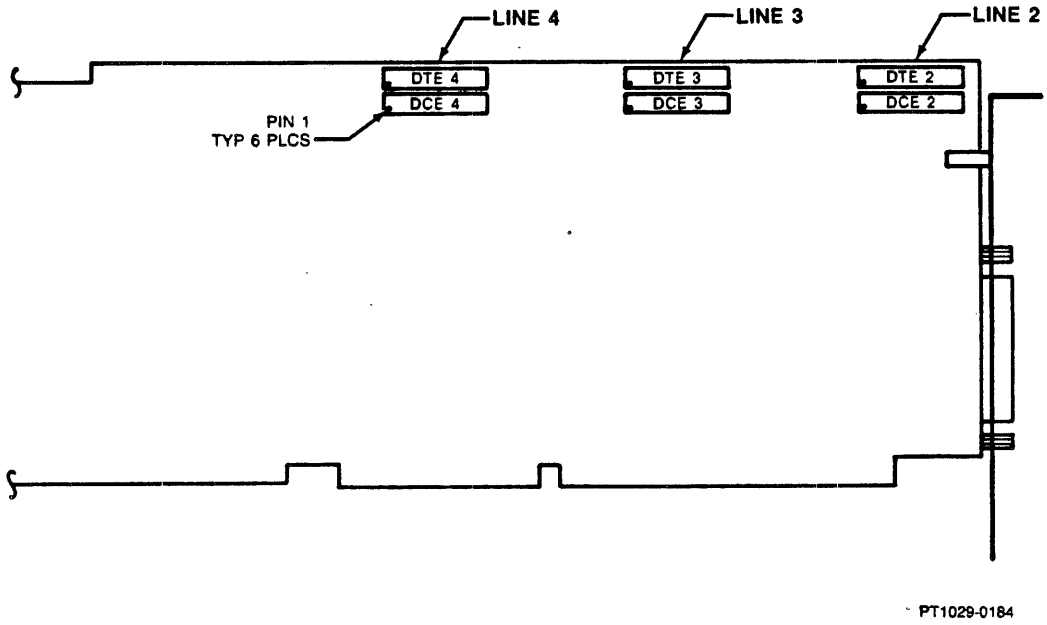


Figure 3-6. Location of Connectors for Ribbon Cables

Which connector you attach the Cliffhanger connector to depends on the line number and on the configuration of the line -- either DTE or DCE. The connectors for these lines are labeled "DTE2" or "DCE2", and so forth.

Orient each ribbon cable so that the colored stripe on the cable is at the pin 1 end of the connector. Pin 1 on the connector is the end away from the rear panel.

6. Once the ribbon cable connectors are mated with the DCP-286 board connectors, position the Cliffhanger assembly over the top edge of the rear panel of the system unit so that one of the screwholes on each Cliffhanger is placed over one of the screws on the rear panel. See Figure 3-6.

   Remove the appropriate screws, put the Cliffhangers in place, and reattach the screws. If you are installing the DCP-286 in a PC-XT or PC-AT, follow the additional instructions included with the Cliffhanger.

   Be sure that the DCP-286 board is securely screwed down. A loose connection may cause the DCP-286 to fail.

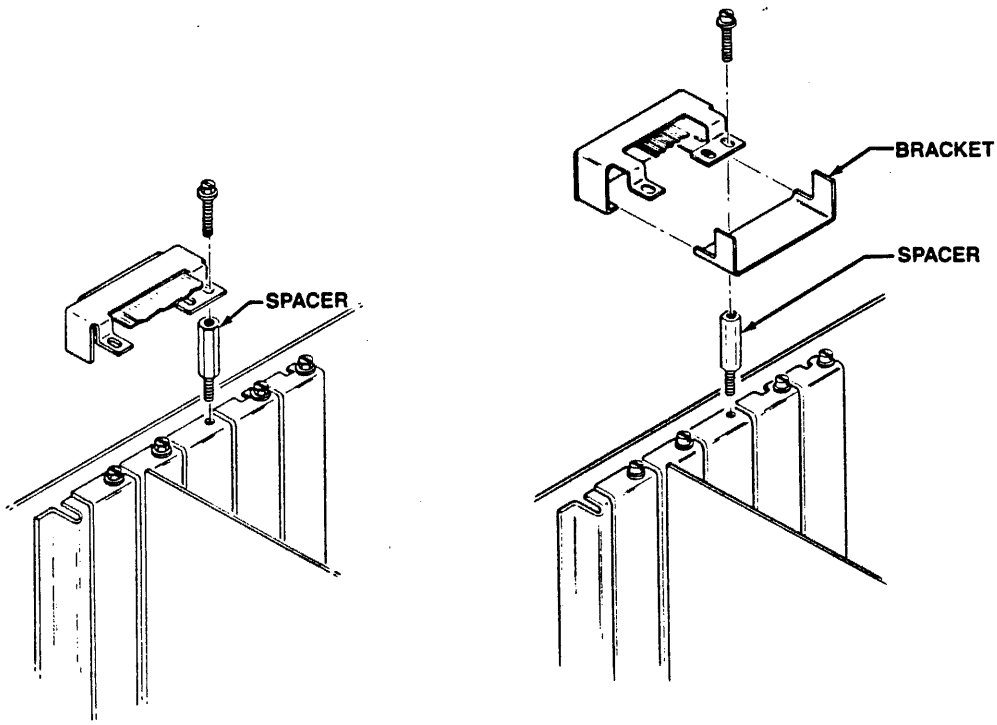


Figure 3-7. Attaching the Cliffhangers

7. Replace the system unit cover and reassemble the system. (Perform the steps listed in Subsection 3.2 in the reverse order.)

3.4 Connecting External Equipment to the DCP-286

One RS-232 connector now protrudes through the rear panel of the system unit. This connector is line 1. Additional RS-232connectors for lines 2, 3, and 4 are now available on the Cliffhanger assemblies. Connection to a modem or other serial device is made through these male DB-25 connectors with standard RS-232 cables.

NOTE

Be sure to use an 11-wire cable for synchronous applications. Many asynchronous cables are only nine pins and do not work correctly. Synchronous applications require at least the following pins: 1, 2, 3, 4, 5, 6, 7, 8, 15, 17 and 20.

If you have nonstandard cabling requirements, see Section 4.11 for the pin/signal information.

All connections made to the DCP-286 Module should be made using a shielded cable to reduce radio-frequency interference. (See also Subsection 3.6.1.)

3.5 Running the DCP-286 Diagnostic

The diagnostic diskette included with your DCP-286 performs a complete functional checkout of the DCP-286 Module. You should run these tests once the module is installed to be sure that it is functioning properly. The instructions for running the diagnostics are included with the diskette. The file name is DCP286.USR. It can be either copied to a printer (COPY DCP286.USR LPT1:) or sent to the screen (DCP286.USR CON:).

3.6 Problems after Installation

The hardware installation of the DCP-286 is now complete. However, you will not know if the board is operating correctly until you bring up the software for the module.

Because the software for the DCP-286 Module is user-written specifically for the application, diagnosing problems may be difficult. Ensure the highest level of quality assurance in debugging your software. For example, build in checkpoints wherever possible in an effort to be able to isolate problems in software and thus, help determine if a problem is software or hardware related.

If, however, you experience a problem immediately after the installation of the DCP-286, check the following potential causes of problems (these points are related to the module itself and do not include software):

- Are any connections to other boards loose?
- Are the cable connections made properly? Are these connections loose?
- Are the configuration jumpers set correctly?
- Are the configuration switches set correctly?
- Are the external equipment connections made properly and is the equipment powered on?

If your answers to the above questions are the appropriate ones and the problem remains, try running the diagnostic. If the diagnostic fails, note down the error codes and then contact Emulex technical support at the following address:

Emulex Technical Support
3545 Harbor Blvd.
Costa Mesa, CA 92626
714-662-5600 800-854-7112 outside California

If the diagnostic provides no useful information, go back to the beginning of the installation procedure, follow the instructions, and remove the DCP-286. Then try your system to determine whether or not it operates correctly. If your system operates correctly, possibly the DCP-286 Module that you received is defective. Refer to the Limited Warranty at the beginning of this document for the procedure to follow.

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If your system does not operate normally, the problem may be in your system.

3.6.1 Minimizing Radio-Frequency Interference

Computer equipment such as the DCP-286 Module generates and uses radio-frequency energy in its operation. This energy can be radiated into the atmosphere and received by television sets, FM stereos, and other radio receivers. It is noticed as a whining, buzzing, or hissing sound on radios, and as "snow" or a peculiar pattern on television screens.

The DCP-286 Module meets the Federal Communication Commission (FCC) limitation for the radiation of radio-frequency energy (Subpart J of Part 15, FCC Rules - Class A). If the DCP-286 is installed in accordance with the instructions given in this manual, interference with radio receivers is unlikely.

Because of environmental differences, Emulex cannot guarantee that interference will not occur in any installation. If interference is suspected, verify that the DCP-286 Module is the source by turning the computer off and on. If the board is causing the interference, try to correct the problem with one or more of the following actions:

- Reorient the receiving antenna.
- Relocate the computer with respect to the receiver.
- Move the computer away from the receiver.
- Plug the computer into a different outlet so that the computer and receiver are on different branch circuits.

If necessary, consult your dealer service representative or an experienced radio or television technician for additional suggestions. You may also find the following booklet prepared by the FCC helpful:

Title:	*How to Identify and Resolve Radio-TV Interference Problems*
Publication Number:	004-00345-4
Publisher:	Government Printing Office Washington, D.C. 20402

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Section 4
HARDWARE TECHNICAL INFORMATION

4.1 Overview

This section gives a detailed explanation of the operation of the DCP-286 Module. It is intended for systems developers who require technical information in order to write custom software for the module. The level of discussion assumes a knowledge of hardware implementation and of the IBM Macro Assembler as well as a knowledge of data communications in general.

For detailed information about the Intel iAPX 286 microprocessor, the 8237 DMA Controller, or the 8259 Interrupt Controller, refer to the *Microsystems Components Handbook*, Vols I and II, Intel Corporation, #230843-002, 1985. For detailed information on the 8530 Serial Communications Controller (SCC), refer to Zilog's *Technical Manual Z8030/8530 SCC Serial Communications Controller*, #00-2057-02, 1983.

Used in conjunction with Section Five, Programming, this information will greatly aid systems developers and integrators in creating custom applications for the DCP-286.

To give an understanding of the overall architecture of the DCP-286, Section 4.2 describes its operation in general terms. The subsections that follow Section 4.2 focus on the details of specific areas on the module.

4.2 Hardware Overview

This introductory overview is to give you an idea of how the entire DCP-286 module works, which makes it easier to understand the more detailed descriptions that follow. Reading the overview first and then moving to the sections that follow is a good strategy. As you read, refer to the DCP-286 block diagram in Figure 4-1.

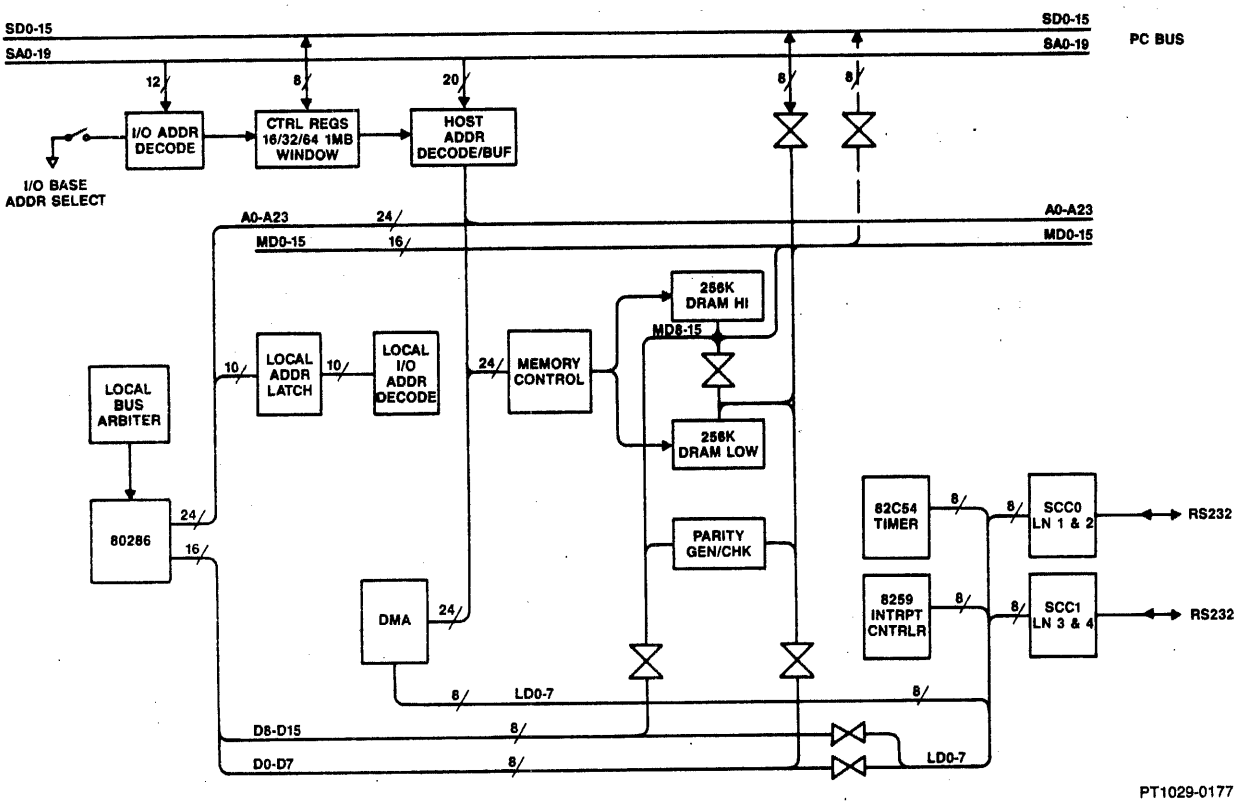


Figure 4-1. DCP-286 Block Diagram

The DCP-286 Module is a high speed, front-end, communications co-processor. As such, it runs independently of the PC processor and relieves it of most communications chores. It is particularly useful in multitasking, multiuser situations in that its flexible architecture allows independent processing of various kinds -- under software control.

In large part, the power and flexibility of the module results from the Intel iAPX 286 microprocessor -- the same microprocessor used in the PC-AT. The 80286 clock rate is 8 MHz.

Throughout this manual the on-board 80286 microprocessor is referred to as the local processor. Generally, local is used in this guide to describe devices or operations that are on the DCP-286 module.

Applications software developed for the DCP-286 runs in the dual-ported memory on the module. This 512 kilobytes (KB) of dynamic random access memory (DRAM) holds applications software and acts as a buffer to pass data to and from the PC. This memory can be accessed by both the local processor and the PC processor. The PC can access the DCP-286 memory through a window that may be 16 KB, 32 KB, 64 KB, or 1 megabyte (MB). (The 1-MB window requires an IBM PC-AT or equivalent as the PC.) The starting address for shared memory is under software control.

When the PC processor needs to initialize and control the DCP-286, it does so through the Control Registers. The base for these three Control Registers is switch-selectable using switches 1 through 4 on SW1. The PC can start, reset, and interrupt the local processor through these Control Registers. Control Register 1 is a general purpose register; Control Register 2 selects the block of DCP-286 memory that is shared with the PC via the window. Control Register 3 selects the starting address (base address) for the window in the PC memory map.

The DCP-286 Module contains four RS-232 serial ports or lines. These serial lines are implemented by the 8530 SCC. The 8530 SCC is an intelligent communications device that provides either asynchronous or synchronous protocols (for example, Bisync, HDLC, and SDLC). Each SCC device provides two serial I/O channels. Also, each port (or line) can be set up as Data Terminal Equipment (DTE) for communications to a modem, or Data Communications Equipment (DCE) for direct communications with another DTE (null modem operation). Each port supports the modem signals necessary for full- or half-duplex synchronous or asynchronous operation.

RS-422/485 operation is achieved with a communications piggyback adapter, approximately 1″ x 8″. Each line is individually configurable to either RS-232 or RS-422/485.

Four DMA channels are available to execute data transfers directly between the SCC devices and DCP-286 memory. Up to one MB of DCP-286 memory may be accessed by the DMA, even though the board has only 512 KB. Lines 1 and 2 can be operated in full-duplex mode.

Software development on the DCP-286 is made easy through the use of the transparent mode. In this mode, the 80286 is disabled, and control of the DCP-286 peripherals is turned over to the PC processor. All I/O ports are available to the PC so that software can be written and tested on the PC as if it were running on the DCP-286 Module.

4.3 PC Interface

The interface between the DCP-286 Module and the PC is controlled entirely by the PC. The DCP-286 requires the PC to move data in and out of shared memory and to initialize and control it via the Control Registers. The DCP-286 does not have the ability to transfer data to and from the PC memory.

When used with an IBM PC or PC-XT, all I/O and memory data transfers are made on a byte basis. The DCP-286 hardware automatically converts the 16-bit memory on the module to 8 bits for the data transfer. When used with PC-ATs, the DCP-286 is configurable for either 8- or 16-bit data transfers. See Sections 2.3.3 and 2.4.7 for the switch setting and jumper selections regarding 8-/16-bit data transfers.

The PC must have a base address for the three Control Registers in order to access the DCP-286. This I/O base address is selected through the first four switch positions on SW1. Sixteen base addresses from 03C to 3FC are available; the factory setting is 33C. See Figure 2-2 for the switch settings of these 16 addresses.

4.3.1 Control Registers

In normal operation (local mode), the DCP-286 is controlled by its local processor and operates completely independent of the PC processor. When the PC processor needs to access the module -- to start, reset, or interrupt the module -- it does so through the three Control Registers. The Control Registers also provide the means for software control of various operations.

Control Register 1 allows for general control functions and operation. Control Register 2 primarily sets up the memory segment address scheme for the DCP-286, enables or disables PC access to DCP-286 memory and interrupts to the PC. Control Register 3 determines the base address of the shared memory window as seen from the PC.

The following subsections provide bit definitions of the Control Registers.

4.3.1.1 Control Register 1

Figure 4-2 shows a layout of Control Register 1. Each bit is explained following the figure.

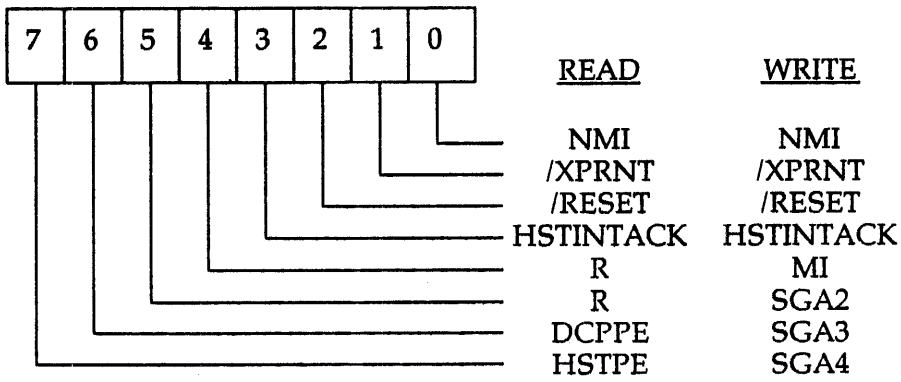


Figure 4-2. Layout of Control Register 1

BIT 0 (NMI -- READ/WRITE)

Bit 0 is the Nonmaskable Interrupt bit. Setting this bit to 1 causes a nonmaskable interrupt to the local processor. The low-to-high transition is latched by the local processor. This bit must be cleared by the PC. However, no timing restriction on clearing the NMI bit exists. This bit is cleared after power-up.

BIT 1 (/XPRNT -- READ/WRITE)

Bit 1 is the Transparent Mode bit. When this bit is reset to 0 and bit 2 is set to a 1, the local processor is placed in the hold mode, and the DCP-286 peripherals are accessible by the PC processor. This state is the transparent mode and is useful during software development.

This bit is reset to 0 after power up, which prevents uncontrolled execution by the local processor before a program is loaded. To start or restart the local processor, this bit must be set to 1. Except for starting and restarting operations, Control Register 1 should not be accessed unless this bit is set to 1. (See section 4.3.2.)

BIT 2 (/RESET -- READ/WRITE)

Bit 2 is the Programmed Reset Bit. A 0 in this bit location causes a general reset to the DCP-286. In this state, the local processor cannot execute code; it is held in this state until the bit is set to 1 by the PC processor. Both /RESET and /XPRNT must be set to 1 to start the local processor.

NOTE

The SCCs are not affected by this bit.

The local processor requires a minimum reset pulse width of 16 system clock cycles. The minimum time for a Programmed Reset to the DCP-286 is 1.5 microseconds.

BIT 3 (HSINTACK -- READ/WRITE)

Bit 3 is the Host Interrupt Acknowledge Bit. This bit is used during Transparent Mode only and, when set to 1, places the SCCs in the interrupt acknowledge cycle. The PC is then allowed only one I/O read to capture the interrupt vector from the SCCs. When set to 1, any I/O read is treated as an interrupt acknowledge read. This bit is cleared after power-up.

BIT 4 (MI -- WRITE)

Writing a 1 to bit 4, the Maskable Interrupt Bit, causes a maskable interrupt on level 2 to the 8259 Interrupt Controller. This bit is latched in the 8259 device and not in the Control Register. Therefore, this bit does not need to be cleared to complete a maskable interrupt.

BIT 4 (RESERVED -- READ)

BITS 5-7 (SGA2-SGA4 -- WRITE)

When the shared memory window size is less than 1 MB, these bits serve as the seventeenth (SGA2), eighteenth (SGA3), and nineteenth (SGA4) address bits to the DCP-286 memory. The Segment Address bits (SGA2-SGA4) are used by the PC to select a 64 KB segment within the DCP-286 memory (these bits function in the same way on the DCP-88).

In addition, Control Register 2 provides six segment address bits that allow the PC to access DCP-286 memory in 16, 32, or 64 KB segments. If Control Register 2 is used for segment addressing, the SGA bits in Control Register 1 (bits 5-7) must remain 0. Bits 5-7 are cleared to 0 after power up. If the shared memory window size is 1 MB, the PC accesses the DCP-286 memory directly and the SGA bits are ineffective.

BIT 5 (RESERVED -- READ)

BIT 6 (DCPPE -- READ)

Bit 6, the DCP Parity Error Bit, is set only by the local processor itself. A 1 is returned when a memory access read occurred with even parity. When set, this bit activates the IOCHCK line to the PC, and holds it active low until cleared. This bit is cleared by any write to Control Register 1 and after power-up. This bit is not cleared by a Programmed Reset (bit 2 = 0).

NOTE

Not clearing this bit by a Programmed Reset (bit 2 = 0) is a variance from DCP-88 operation.

BIT 7 (HSTPE -- READ)

Bit 7, the Host Parity Error Bit, can only be set by a PC access read from DCP-286 memory with even parity. When set, this bit returns a 1 and IOCHCK- is held active low to the PC.

This bit is cleared by any write to Control Register 1 and after power-up. This bit is not cleared by a Programmed Reset (bit 2 = 0). Thus, the PC can verify memory integrity when bit 2 is 0 without requiring the DCP-286 to be in the transparent mode. However, memory must be enabled by setting bit 6 in Control Register 2.

NOTE

Not clearing this bit by a Programmed Reset (bit 2 = 0) is a variance from DCP-88 operation.

4.3.1.2 Control Register 2

Figure 4-3 shows the layout of Control Register 2. Bit definitions follow the figure.

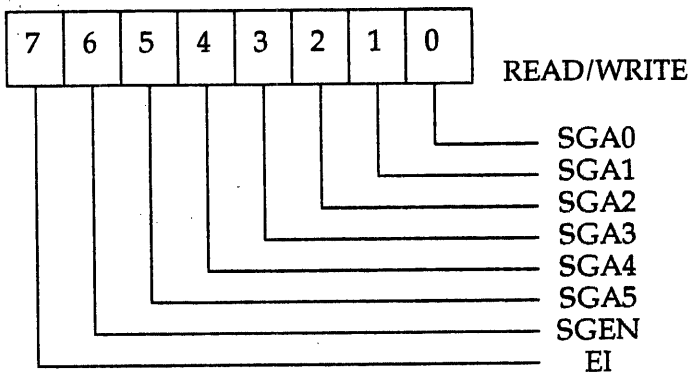


Figure 4-3. Layout of Control Register 2

BITS 0-5 (SGA0-SGA5 -- READ/WRITE)

Table 4-1 lists the relationship of Segment Address Bits 0-5 and the DCP-286 memory address bits.

Table 4-1. SGA0-SGA5 Bit Relationships

Segment Bit	DCP-286 Memory Address Bit	Segment Size
SGA5	A19 (20th)	
SGA4	A18 (19th)	
SGA3	A17 (18th)	
SGA2	A16 (17th)	64 KB
SGA1	A15 (16th)	32 KB
SGA0	A14 (15th)	16 KB

These bits are cleared to 0 after power-up, and they have no effect when the shared memory window size is 1 MB. Likewise, SGA0 has no effect when the window size is 32 KB; SGA1 has no effect for a window size of 64 KB.

Segment Address Bits SGA2 - SGA4 must be 0 if Control Register 1 is used to implement segment addressing. Table 4-2 shows 16-KB memory segment addressing.

BIT 6 (SGEN -- READ/WRITE)

Bit 6, the Segment Enable Bit, must be set to 1 before the PC can access DCP-286 memory. This bit is 0 after power-up. Regardless of the shared memory window size, the PC can not access DCP-286 memory when this bit is zero.

BIT 7 (EI -- READ/WRITE)

When Bit 7, the Enable Interrupts Bit, is set to a 1, interrupts to the PC are enabled. When this bit is 0, interrupts to the PC are disabled (tri-stated). After power-up, this bit is cleared to 0.

Table 4-2. 16-KB Memory Segment Addressing

16 KB Segment (From)	(To)	Bit Positions and Names					
		5 SGA5	4 SGA4	3 SGA3	2 SGA2	1 SGA1	0 SGA0
0	16,383	0	0	0	0	0	0
16,384	32,767	0	0	0	0	0	1
32,768	49,151	0	0	0	0	1	0
49,152	65,535	0	0	0	0	1	1
65,536	81,919	0	0	0	1	0	0
81,920	98,303	0	0	0	1	0	1
98,304	114,687	0	0	0	1	1	0
114,688	131,071	0	0	0	1	1	1
131,072	147,455	0	0	1	0	0	0
147,456	163,839	0	0	1	0	0	1
163,840	180,223	0	0	1	0	1	0
180,224	184,319	0	0	1	0	1	1
184,320	212,991	0	0	1	1	0	0
212,992	229,375	0	0	1	1	0	1
229,376	245,759	0	0	1	1	1	0
245,760	262,143	0	0	1	1	1	1
262,144	278,527	0	1	0	0	0	0
278,527	294,911	0	1	0	0	0	1
294,912	311,295	0	1	0	0	1	0
311,296	327,679	0	1	0	0	1	1
327,680	344,063	0	1	0	1	0	0
344,064	360,447	0	1	0	1	0	1
360,448	376,831	0	1	0	1	1	0
376,832	393,215	0	1	0	1	1	1
393,216	409,599	0	1	1	0	0	0
409,600	425,983	0	1	1	0	0	1
425,984	442,367	0	1	1	0	1	0
442,368	458,751	0	1	1	0	1	1
458,752	475,135	0	1	1	1	0	0
475,136	491,519	0	1	1	1	0	1
491,520	507,903	0	1	1	1	1	0
507,904	524,287	1	1	1	1	1	1

4.3.1.3 Control Register 3

The PC's base address (starting address) for shared DCP-286 memory is under software control. Control Register 3 contains six bits, the Segment Starting Address Bits, which are used to select this base address.

When the window size is 32 KB or less, the PC must access DCP-286 memory indirectly through the six Segment Address Bits in Control Register 2. When the window size is 64 KB, the PC can access shared memory through either Control Registers 1 or 2.

Figure 4-4 shows the layout of Control Register 3. Bit definitions follow the figure.

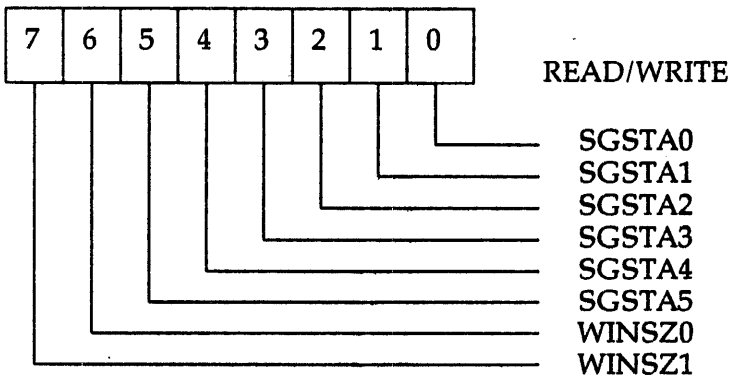


Figure 4-4. Layout of Control Register 3

BITS 0-5 (SGSTA0-SGSTA5 -- READ/WRITE)

Bits 0-5, the Segment Starting Address Bits, determine the base address for shared memory as seen from the PC. These bits serve two address ranges based on the shared memory window size selected by bits 6 and 7. After power-up, these bits are 0.

Table 4-3 lists the relationship of Segment Starting Address Bits 0-5 and the PC memory address bits.

Table 4-3. SGSTA0-SGSTA5 Bit Relationship

Segment Bit	DCP-286 Memory Address Bit
Window Sizes Less Than 1 MB:	
SGSTA5	A19 (20th)
SGSTA4	A18 (19th)
SGSTA3	A17 (18th)
SGSTA2	A16 (17th)
SGSTA1	A15 (16th)
SGSTA0	A14 (15th)
Window Size of 1 MB:	
SGSTA5	A23 (24th)
SGSTA4	A22 (23rd)
SGSTA3	A21 (22nd)
SGSTA2	A20 (21st)
SGSTA1	X
SGSTA0	X

BITS 6-7 (WINSZ0-WINSZ1 -- READ/WRITE)

Bits 6 and 7, the Window Size 0-1 Bits, determine the window size of shared memory as seen from the PC. The default is a 64 KB window at power-up. Table 4-4 shows the bit configurations for window sizes.

Table 4-4. Window Size Bit Configurations

WINSZ1	WINS0	Window Size
0	0	64 KB
0	1	32 KB
1	0	16 KB
1	1	1 MB

Examples of Starting Addresses

The configuration of the Window Size Bits 0 and 1 (bits 6 and 7) determine the effectivity of the Segment Starting Address Bits. The possible window sizes are 16 KB, 32 KB, 64 KB, and 1 MB.

When the window size is less than 1MB, all six segment Starting Address Bits are used, and the base address is selectable on a 16-KB boundary anywhere within the first 1 MB of PC memory. Table 4-5 gives examples of starting addresses of a window size of less than 1 MB.

Table 4-5. 16-KB Starting Addresses - Window Less than 1 MB

16 KB Starting Address	Bit Positions and Names					
	5 SGSTA5	4 SGSTA4	3 SGSTA3	2 SGSTA2	1 SGSTA1	0 SGSTA0
0A0000	1	0	1	0	0	0
0A4000	1	0	1	0	0	1
0A8000	1	0	1	0	1	0
0AC000	1	0	1	0	1	1
0B0000	1	0	1	1	0	0
0B4000	1	0	1	1	0	1
0B8000	1	0	1	1	1	0
0BC000	1	0	1	1	1	1
0C0000	1	1	0	0	0	0
0C4000	1	1	0	0	0	1
0C8000	1	1	0	0	1	0
0CC000	1	1	0	0	1	1
0D0000	1	1	0	1	0	0
0D4000	1	1	0	1	0	1
0D8000	1	1	0	1	1	0
0DC000	1	1	0	1	1	1
0E0000	1	1	1	0	0	0
0E4000	1	1	1	0	0	1
0E8000	1	1	1	0	1	0
0EC000	1	1	1	0	1	1

When the window size is 1 MB, only the top four Segment Starting Address Bits are used, and the base address is selectable on a 1-MB boundary anywhere in the upper 15 MB of PC memory. A 1-MB window size requires an IBM PC-AT or equivalent.

Table 4-6 gives examples of starting address for a window size of 1 MB.

Table 4-6. Starting Addresses - Window of 1 MB

1 MB Starting Address	Bit Positions and Names					
	5 SGSTA5	4 SGSTA4	3 SGSTA3	2 SGSTA2	1 SGSTA1	0 SGSTA0
100000	0	0	0	1	X	X
200000	0	0	1	0	X	X
400000	0	1	0	0	X	X
800000	1	0	0	0	X	X
D00000	1	1	0	1	X	X
E00000	1	1	1	0	X	X
F00000	1	1	1	1	X	X

4.3.1.4 Example of Shared Memory Setup

The PC can access any portion of the DCP-286 512 KB of RAM through a window of shared memory. The size of the window is set up through Control Register 3. The Segment Address Bits in Control Register 2 determine where the base address of the window will be in the DCP-286 memory. The Segment Starting Address Bits in Control Register 3 determine where the base address of the window will be in the PC's memory.

A representative example of this scheme is shown in Figure 4-5 This example assumes that the base address at which the PC sees the 64-KB window is 0D0000. The bit configuration is 1-1-0-1-0-0 (SGSTA5-SGSTA0) for 34 hex in Control Register 3. To select a 64-KB window, bits 6 and 7 of that register are 0.

The base address on the DCP-286 side for the window is at the top of the 512 KB--that is, it begins at 448 KB. The bit configuration is 0-1-1-1-0-0 (SGA5-SGA0) or DC hex in Control Register 2. This example also assumes that bits 6 (Segment Enable) and 7 (Enable Interrupts) in Control Register 2 are set.

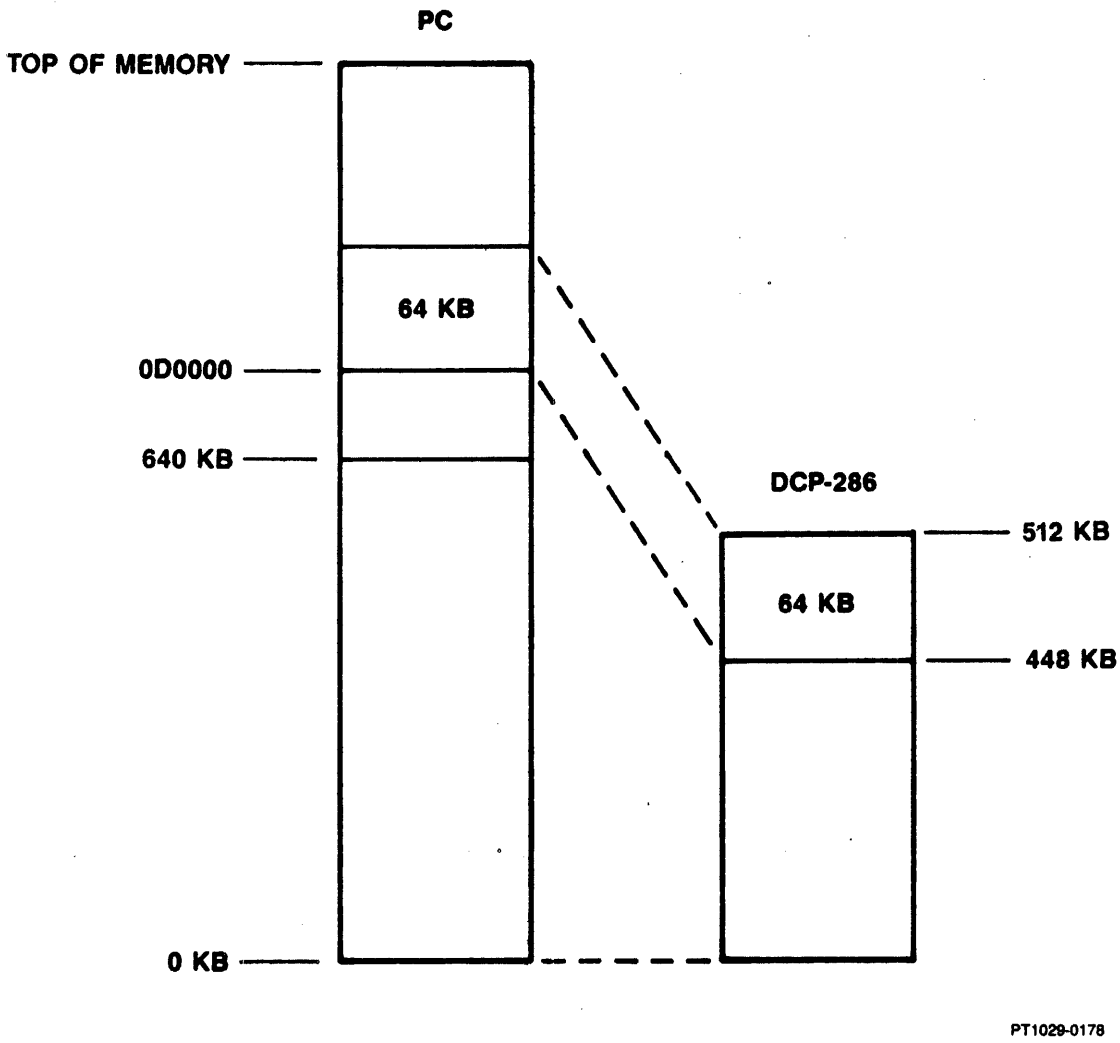


Figure 4-5. Example of Shared Memory Window

4.3.2 Local vs Transparent Mode

The DCP-286 can operate in either of the following two modes:

- Local mode -- This is the normal operating mode. The local processor controls all I/O ports and performs co-processing. The PC processor cannot access the DCP-286 except through the Control Registers and shared memory.

- Transparent mode -- In this mode, the local processor is disabled, and the PC processor can access all DCP-286 I/O ports. This mode also disables the co-processing function of the DCP-286 (the local processor cannot execute code). This mode is useful for software development so that software can be written and tested on the PC and then run on the DCP-286 after it is fully debugged.

The DCP-286 is placed in transparent mode by writing a 0 to bit 1 and a 1 to bit 2 of Control Register 1, which sets the Transparent Mode Bit and clears the Programmed Reset Bit. In this mode, the PC processor has access to all peripherals on the DCP-286. All I/O addresses and interrupt vector addresses are at their normal locations. The DMA controller is accessible in transparent mode but cannot be used to transfer data because it cannot acquire the local bus.

4.3.3 Interrupts

The PC can interrupt the local processor on the DCP-286 in two ways: a maskable interrupt through bit 4 of Control Register 1 or a nonmaskable interrupt through bit 0 of Control Register 1 (see Section 4.3.1.1.).

The DCP-286 can interrupt the PC only on a single level. Interrupts to the PC can be enabled/disabled through bit 7 of Control Register 2 (Section 4.3.1.2).

The interrupt level is set by jumpers for one of the available interrupt levels. In the PC or PC-XT, four interrupt levels are available: IRQ2, IRQ3, IRQ4, or IRQ5. The factory configuration selects IRQ3 (see Figure 2-4 for the jumper options).

For the PC-AT, eight interrupt levels are available: IRQ2, IRQ3, IRQ4, IRQ5, IRQ10, IRQ11, IRQ12, and IRQ15. The factory configuration selects IRQ3 (see Figure 2-5 for the jumper options).

The DCP-286 generates a maskable interrupt (programmed interrupt) to the PC by issuing an I/O read or write to address 3DC hex.

NOTE

Interrupts during transparent mode occur on the same level as a programmed interrupt from the local processor to the PC. This implementation is a variance between the DCP-88 and the DCP-286.

The DCP-286 can also generate a nonmaskable interrupt to the PC; this interrupt occurs when a DCP-286 memory parity error generates an IOCHCK. You may disable this interrupt by removing the jumper at JP5: 17-18. This "open-circuited" operation may be useful in debugging.

4.4 Local I/O Addresses

All I/O operations to peripherals on the DCP-286 are 8 bits wide. However, no programming restriction exists because the DCP-286 hardware multiplexes and demultiplexes the local processor 16-bit data bus to the 8-bit data bus for the peripherals. The I/O addresses for peripherals on the DCP-286 are given in hex in Table 4-7. The I/O address space is limited by hardware to modulo 1024 bytes.

Table 4-7. I/O Addresses

Address	Description
300	DMA BASE ADDR -CH0
301	DMA BASE WORD COUNT -CH0
302	DMA BASE ADDR -CH1
303	DMA BASE WORD COUNT -CH1
304	DMA BASE ADDR -CH2
305	DMA BASE WORD COUNT -CH2
306	DMA BASE ADDR -CH3
307	DMA BASE WORD COUN -CH3
308	DMA COMMAND/STATUS REG
309	DMA SOFTWARE REQUEST REG
30A	DMA MASK REG
30B	DMA MODE REG
30C	DMA CLEAR BYTE PTR
30D	DMA TEMP REG
30E	DMA CLEAR MASK REG
30F	DMA SET MASK REG
310	DMA CH0 PAGE REG
311	DMA CH1 PAGE REG
312	DMA CH2 PAGE REG
313	DMA CH3 PAGE REG
314	RESERVED
315	RESERVED
316	RESERVED
317	RESERVED
318	8259 INITIALIZATION COMMAND REG
319	8259 OPERATION COMMAND REG
31A-31F	RESERVED
280-283	RESERVED
284	TIMER COUNTER 0
285	TIMER COUNTER 1
286	TIMER COUNTER 2
287	TIMER CONTROL REG
3D8-3DB	RESERVED
3DC	MASKABLE INTERRUPT TO PC
3DD-3DF	RESERVED
3E0	COMMAND/STATUS CHB - LN 2
3E1	DATA REG CHB - LN 2
3E2	COMMAND/STATUS CHA - LN 1
3E3	DATA REG CHA - LN 1
3E4	COMMAND/STATUS CHB - LN 4
3E5	DATA REG CHB - LN 4
3E6	COMMAND/STATUS CHA - LN 3
3E7	DATA REG CHA - LN 3
3E8-3E9	RESERVED
3EA	CONTROL REG (WR)
3EA	STATUS REG (RD)
3EB-3EF	RESERVED

4.5 Local Control Register

The Local Control Register (at address 3EA) provides several control functions for the DCP-286. This write-only register is used to set up Lines 1 and 2 for full-duplex DMA, to select the uppermost megabyte of memory, and to provide a general purpose test point.

Figure 4-6 shows the layout of the register. The bits are explained following the figure.

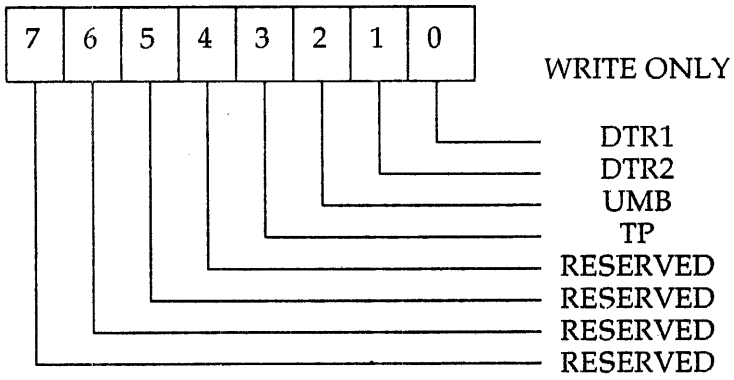


Figure 4-6. Layout of Control Register

BIT 0 (DTR 1 -- WRITE)

Setting the Data Terminal Ready Line 1 Bit selects the full- duplex mode for communication line 1 using DMA. For any other set up, DTR is controlled by the SCC for line 1, and bit 0 must remain a 0. A 1 in this bit location activates DTR1. Bit 0 is cleared to 0 after a power-up.

BIT 1 (DTR 2 -- WRITE)

Setting the Data Terminal Ready Line 2 Bit selects the full- duplex mode for communication line 2 using DMA. For any other set up, DTR is controlled by the SCC for line 2, and bit 0 must remain a 0. A 1 in this bit location activates DTR2. Bit 1 is cleared to 0 after a power-up.

BIT 2 (UMB -- WRITE)

Setting the Upper Megabyte Bit to 1 (active) forces all memory accesses by either the PC or the DMA to occur in the uppermost 1 MB of DCP-286 memory. The window size still applies when this bit is active. This bit is cleared to 0 after power-up. Given that the DCP-286 is limited to 512 KB, this bit should always be set to 0.

BIT 3 (TP -- WRITE)

The Test Point Bit is attached to a hardware test point at the top of the board. It may be used as a debug tool for trigger points or timing measurements or as an error indicator. Bit 3 is cleared to 0 after power-up.

BITS 4-7 (RESERVED)

4.6 Local Status Register

The Local Status Register (at address 3EA) allows software to determine certain pieces of information regarding the state of the DCP-286. This read-only register indicates: (1) the status of DTR1 and DTR2; (2) the selection of the uppermost MB of memory; and (3) the modem status for the four communication lines.

Figure 4-7 shows the layout of the Local Status Register. Explanations of the bits follow the figure.

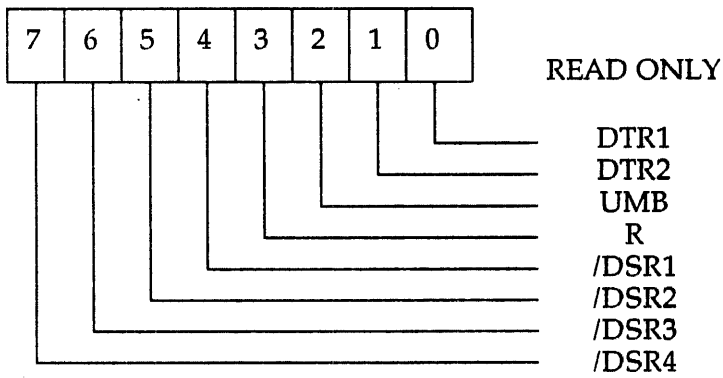


Figure 4-7. Layout of Local Status Register

BIT 0 (DTR1 -- READ)

The DTR1 Bit shows the status of the Data Terminal Ready Line 1. This bit is a 1 when full-duplex DMA is used for Line 1 and DTR is active.

BIT 1 (DTR2 -- READ)

The DTR2 Bit shows the status of the Data Terminal Ready Line 2. This bit is a 1 when full-duplex DMA is used for Line 2 and DTR is active.

BIT 2 (UMB -- READ)

This bit is a 1 when PC and DMA accesses to memory are in the uppermost MB of DCP-286 memory. Given that the DCP-286 is limited to 512 KB, this bit should be 0.

BIT 3 (RESERVED -- READ)

BITS 4-7 (/DSR1-4 -- READ)

These bits provide the modem status for Data Set Ready from each of the communications lines. A 0 in any bit location indicates that DATA SET IS READY.

4.7 Local Interrupts

The interrupts to the local processor on the DCP-286 are classified in two categories: those generated by the SCCs and those generated by the 8259 Interrupt Controller. The SCCs generate their own interrupt vectors and priority is established by an Interrupt Enable Line that is daisy-chained from device to device.

The 8259 Interrupt Controller processes all remaining interrupts. It generates vectors and manages interrupt priorities under software control. This device functions as an overall manager by archiving the requests, determining the relative importance of the interrupt, and issuing the interrupt based on that priority. Interrupts generated by the SCCs take priority over interrupts generated by the 8259.

4.7.1 Initialization of the 8259 Interrupt Controller

Before interrupts can be processed, the 8259 Interrupt Controller must be properly initialized. No hardware reset exists for the 8259. For information about programming the 8259, refer to the list of documents in Section 1.1.2. Initialization of the 8259 Interrupt Controller will require four control words (bytes). The first control word must specify the following:

a. Control word 4 is required.
b. Cascade mode.
c. Call interval of 8.
d. Edge-triggered mode.

The remaining bits are zero. The first initialization control word is written to address 318 (hex), with bit 4 equal to a "1". Initialization control words two, three, and four are written to address 319 (hex). Control word two specifies all eight bits of the interrupt number. Refer to Table 4-8 for the suggested interrupt number and corresponding vector addresses. Control word three must be zeroed out to specify no slave 8259 controllers attached. Control word three is not required. Control word four must specify 8086 mode (bit 0 = "1") and the non-buffered mode (bit 3 = "0"). Automatic End of Interrupt (AEOI) and the Special Fully Nested Mode are optional.

4.7.2 Priority

The priority within the 8259 can be either fixed or rotating. Fixed priority among the eight levels of the 8259 is under software control. Table 4-8 lists all possible interrupts with the default priorities. Priority is listed from highest to lowest. The suggested interrupt numbers and the corresponding vector addresses are listed for compatibility with the Emulex DCP EXEC software.

Table 4-8. Interrupt Priority and Vector Addresses

IRPT Level	Description		IRPT No.	Vector Addr (H)
N/A	Receive Character Rdy	Ln 1	4C	130
N/A	Transmit Buffer Empty	Ln 1	48	120
N/A	External Status Change	Ln 1	4A	128
N/A	Special Receive Condition	Ln 1	4E	138
N/A	Receive Character Rdy	Ln 2	44	110
N/A	Transmit Buffer Empty	Ln 2	40	100
N/A	External Status Change	Ln 2	42	108
N/A	Special Receive Condition	Ln 2	46	118
N/A	Receive Character Rdy	Ln 3	4D	134
N/A	Transmit Buffer Empty	Ln 3	49	124
N/A	External Status Change	Ln 3	4B	12C
N/A	Special Receive Condition	Ln 3	4F	13C
N/A	Receive Character Rdy	Ln 4	45	114
N/A	Transmit Buffer Empty	Ln 4	41	104
N/A	External Status Change	Ln 4	43	10C
N/A	Special Receive Condition	Ln 4	47	11C
IR0	Parity Error		C0	300
IR1	End of DMA Process		C1	304
IR2	Maskable Interrupt from PC		C2	308
IR3	Timer CH2		C3	30C
IR6	Timer CH0		C6	318
IR7	Timer CH1		C7	31C

Interrupt numbers '40 - '40F' (hex) for the SCC devices are realized by programming write register 2 in the SCC for ports 1 and 2 to '40' and a '41' (hex) in the SCC for ports 3 and 4. Interrupt numbers 'C0' - 'C7' (hex) are realized by programming the Initialization Control Word 2 (ICW2) of the 8259 to a 'C0' (hex).

4.8 Timers

Three separate timers are provided through the Intel 8254 Programmable Interval Timer on the DCP-286. Each timer can operate in four of the six possible operating modes. Modes 1 and 5 are not used by the hardware. Modes 0 and 4 can be used in a similar manner to generate a software triggered interrupt.

However, mode 2 is the preferred mode for operation as a timer. The time interval when using interrupts is n times the input count interval where n equals the initial count loaded into the counter. Mode 3 can also be used as a timer where its time interval is (n divided by 2) times the input count interval. For information on programming the 8254 device, refer to the manufacturer's manual listed in Section 1.1.2.

The input count interval (period of the input clock) to all three timers is jumper selectable. The option is between dividing the communications Baud rate clock by 8 or 16. The factory setting is the communications clock divided by 16 (see Figure 2-3 for the jumper options).

With the communications clock divided by sixteen, the period of the input clock to timer channels 0, 1, and 2 is 2.17 microseconds. Timer CH2 can be used without interrupts to count at this rate. If interrupts are used, they should be used with timer channels 0 and 1 and the available range would be 4.34 microseconds to 142 milliseconds.

4.9 Direct Memory Access (DMA)

The Intel 8237 DMA Controller on the DCP-286 provides four channels of DMA. This controller runs off the processor clock divided by two (4 MHz for the 8 MHz DCP- 286). It provides only one line to indicate that the last character in a block of data has been transferred. This line is used to generate the DMA interrupt for all four channels at interrupt level 1 on the 8259 Interrupt Controller.

The 8237 DMA Controller is second in priority for acquiring the local bus for access to DCP-286 memory. The PC has first priority. The priority for accessing DCP-286 memory is implemented in a hardware programmable device; therefore, reassignments are possible, if required.

NOTE

There is a programming restriction associated with the 8237 DMA controller. Successive I/Os to it cannot occur within 500 nanoseconds of each other. This requirement is met by inserting a JUMP $+2 instruction between successive I/Os.

4.9.1 Page Addressing

The DMA channels are limited to transfers of 65,536 bytes or less. The DMA Page Register supplies the upper four bits of the 20-bit DMA address for each channel.

NOTE

In order to avoid "wrap-around," take precautions with respect to block size and starting addresses.

The 8237 DMA Controller can access memory anywhere within a 1-MB memory space. A layout of the DMA Page Register for one channel is shown in Figure 4-8. All four DMA channels are the same so this figure is representative of all four. Bit locations 0-3 are "don't cares."

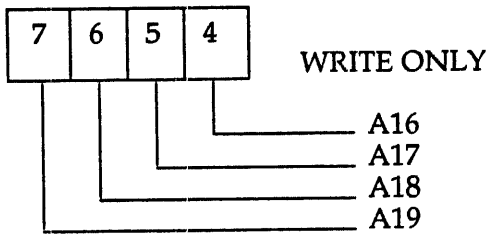


Figure 4-8. Layout of Representative DMA Page Register

The DMA page registers are write only and supply the four most significant address bits during a DMA cycle. Each page register defines a 64-KB page for each DMA channel. These registers are undefined after a power-up, and are not cleared by a Programmed Reset.

4.9.2 Line Configurations

The default configuration for the DMA Controller is four half-duplex lines with DMA channels 0, 1, 2, and 3 dedicated to communication lines 1, 2, 3, and 4, respectively. Communcation lines 1 and 2 are separately configurable to full-duplex DMA. When configured as a full-duplex line, the DTR line cannot be controlled through the SCC device. Auxiliary control for DTR on lines 1 and 2 is available in the Local Control Register (Section 4.5).

Whenever communication line 1 is configured for full-duplex DMA, CH2 of the DMA Controller is dedicated to the transmit function and CH0 must be used for the receive function. In this case, communication line 3 loses its DMA capability. Do NOT enable DMA on communication line 3 when communication line 1 is configured for full-duplex DMA.

Whenever communication line 2 is configured for full-duplex DMA, CH3 of the DMA Controller is dedicated to the transmit function and CH1 must be used for the receive function. In this case, communication line 4 loses its DMA capability. Do NOT enable DMA on communication line 4 when communication line 2 is configured for full-duplex DMA.

4.9.3 Initializing the 8237 DMA Controller

The 8237 DMA controller should be initialized via the Command Register (address 308) for the following conditions:

1. Memory-to-memory disabled
2. Channel 0 address hold disabled
3. Controller enabled
4. Normal timing
5. Fixed priority
6. Extended write
7. DREQ active low
8. DACK active low

This results in '60' hex being written to the Command Register (address 308).

4.9.4 DMA Transfer Mode

The normal operating mode for the 8237 DMA controller is the Single Transfer Mode. In this mode the DMA controller must gain access to the local 286 CPU bus for each character transferred, and then relinquish the bus.

The 8237 DMA controller can also operate in the Demand Transfer Mode. This mode takes advantage of queued receive characters in the SCC devices, and it transfers multiple characters for one access to the local 286 CPU bus. The Block Transfer Mode for the 8237 DMA controller is reserved for memory-to-memory applications only. It cannot be used with the SCC devices, since data transfers are not synchronized. The cascade mode cannot be used with the 8237 DMA controller.

4.10 8530 Serial I/O Operation

The Zilog 8530 SCC, or equivalent, is used for all four serial communications lines on the DCP-286. This device supports asynchronous, byte-synchronous and bit-synchronous SDLC and HDLC protocols. NRZI data encoding is also supported by the SCCs.

Channel assignment is as follows:

- First SCC -- CHA assigned to communication line 1 CHB assigned to communication line 2
- Second SCC -- CHA assigned to communication line 3 CHB assigned to communication line 4

4.10.1 Programming Restrictions

INTERRUPT ACKNOWLEDGE CYCLE

During any interrupt acknowledge cycle to the SCC, only one I/O read is allowed. In the transparent mode, the software must allow only one I/O read during the PC interrupt acknowledge cycle.

USING DMA WITH SCCs

When using DMA with the SCCs, always enable the DMA Controller after enabling the SCCs. When reset, the SCC can cause a DMA request to transmit the first character before the SCC is ready in either full-duplex or half-duplex.

4.10.2 Modem Control

All four communications lines are capable of operating in full synchronous mode with five modem control lines. Ring Indicator Status is not supported on any of the lines.

Each port is configurable between DTE and DCE. This eliminates the need for a modem in those applications where the line length remains within the RS-232C or RS-422/485 specifications. RS-422/485 is achieved through a communications piggyback adapter. Table 4-9 lists the supported modem control signals.

Table 4-9. Supported Modem Control Signals

Signal Name	RS232 Pin No. (25-Pin Connector)	Signal Definition
DTR	20	Data Terminal Ready
RTS	4	Request to Send
CTS	5	Clear to Send
DSR	6	Data Set Ready
DCD	8	Data Carrier Detected

4.10.3 Baud Rate Generator

The formula for calculating the time constant required for the SCC Baud rate generator in synchronous mode is as follows:

$$\text{Time Constant} = \left[\frac{7.3728\ \text{MHz}}{2(\text{Baud Rate})}\right] - 2$$

The Baud rate is in bits/second; the frequency is in Hz. The resulting time constant is the decimal count that is written to write registers 12 and 13 in the SCC. Register 12 contains the least significant byte.

For asynchronous applications, the Baud rate clock must be either 16, 32, or 64 times the desired Baud rate. The resulting time constant must be divided accordingly.

Table 4-10 lists the required time constants, in hex, for synchronous applications. Table 4-11 lists the required time constants, in hex, for an asynchronous application where the clock is divided by 16.

Table 4-10. Synchronous Time Constants (7.3728 MHz)

Baud Rate	Time Constant (in Hex)
64 K	0038
56 K	0040
38.4 K	005E
19.2 K	00BE
9600	017E
7200	01FE
4800	02FE
3600	03FE
2400	05FE
2000	0732
1800	07FE
1200	0BFE
600	17FE
300	2FFE
150	6002
134.5	6B0E
110	82E6
75	BFFE

Table 4-11. Asynchronous Time Constants (7.3728 MHz) (Divided by 16)

Baud Rate	Time Constant (in Hex)
76.8 K	0001
38.4 K	0004
19.2 K	000A
9600	0016
7200	001E
4800	002E
3600	003E
2400	005E
2000	0072
1800	007E
1200	00BE
600	017E
300	02FE
150	05FE
134.5	06B0
110	082C
75	0BFE
50	11FE

4.11 RS-232 Serial Interfaces

The physical connection of the serial interface is made through a 25-pin type D male connector that requires a cable with a mating female connector. The connector for line 1 is brought out the rear panel of the system unit. It is attached to the DCP-286 module. The connectors for lines 2, 3, and 4 are brought out on a single (line 2) and a double (lines 3 and 4) Cliffhanger assembly.

The standard serial interface consists of a synchronous DTE connection. Figure 4-9 shows the cabling signals for the RS-232 interface.

The serial ports can also be configured as DCE by changing the jumper settings. See Figures 2-9 through 2-12 for the jumper options.

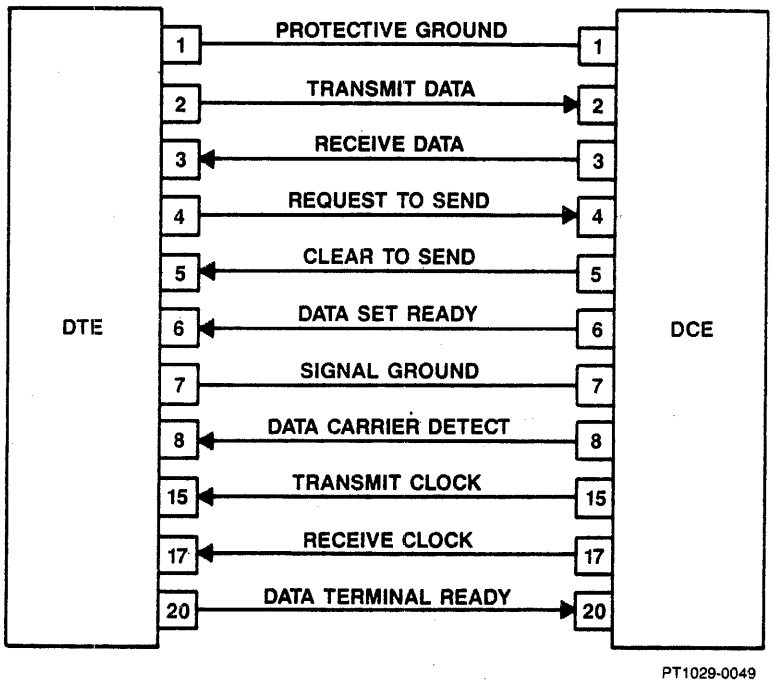


Figure 4-9. Cabling Signals for RS-232 Interfaces

Figures 4-10 through 4-13 show simplified schematics of the four serial ports. Use these schematics if you need more detailed information on the serial port pin/signal assignments.

Cabling signals and pin assignments for the RS-422/485 serial interface are described in a separate manual about the piggyback adapter required for RS-422/485 communications.

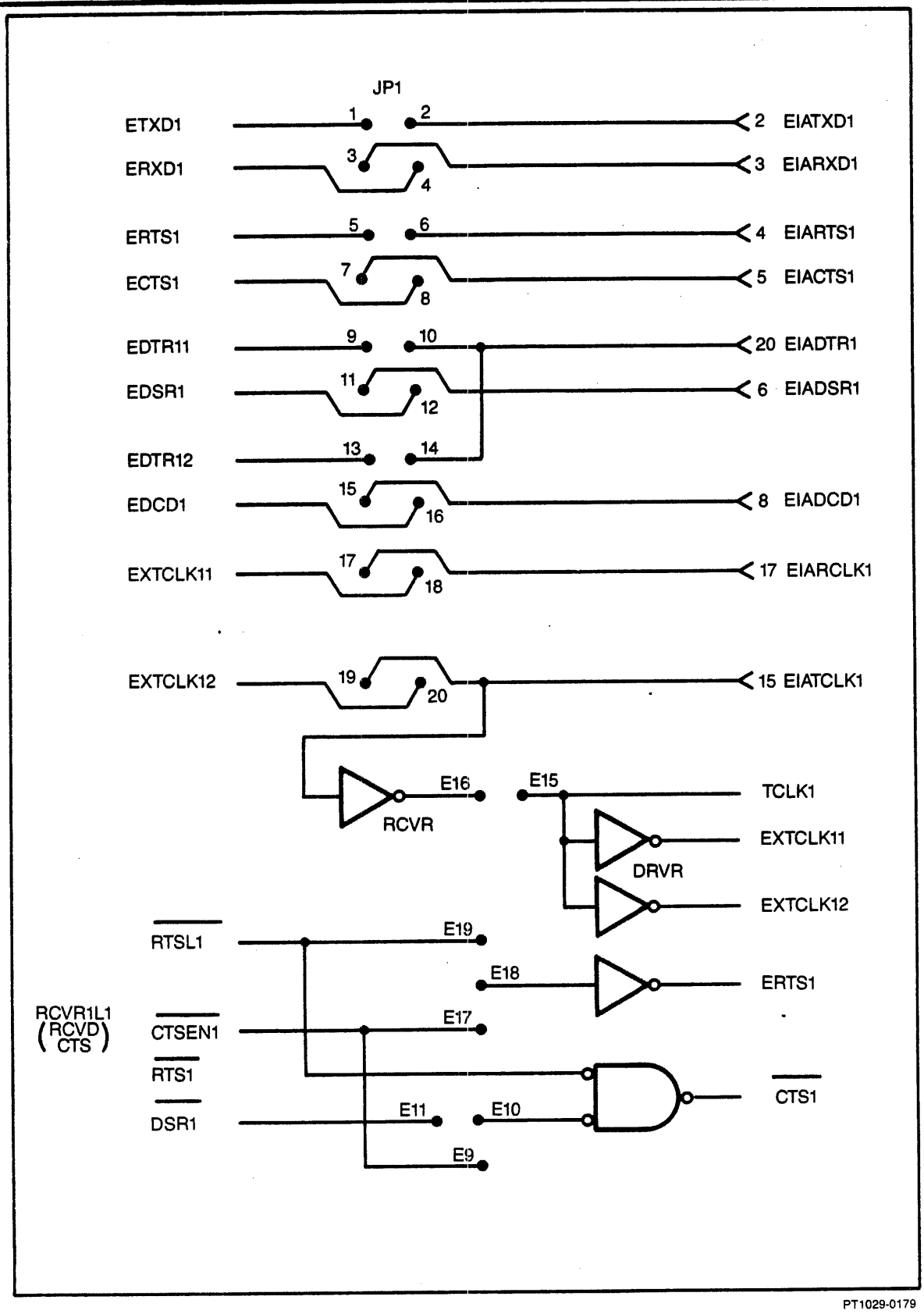
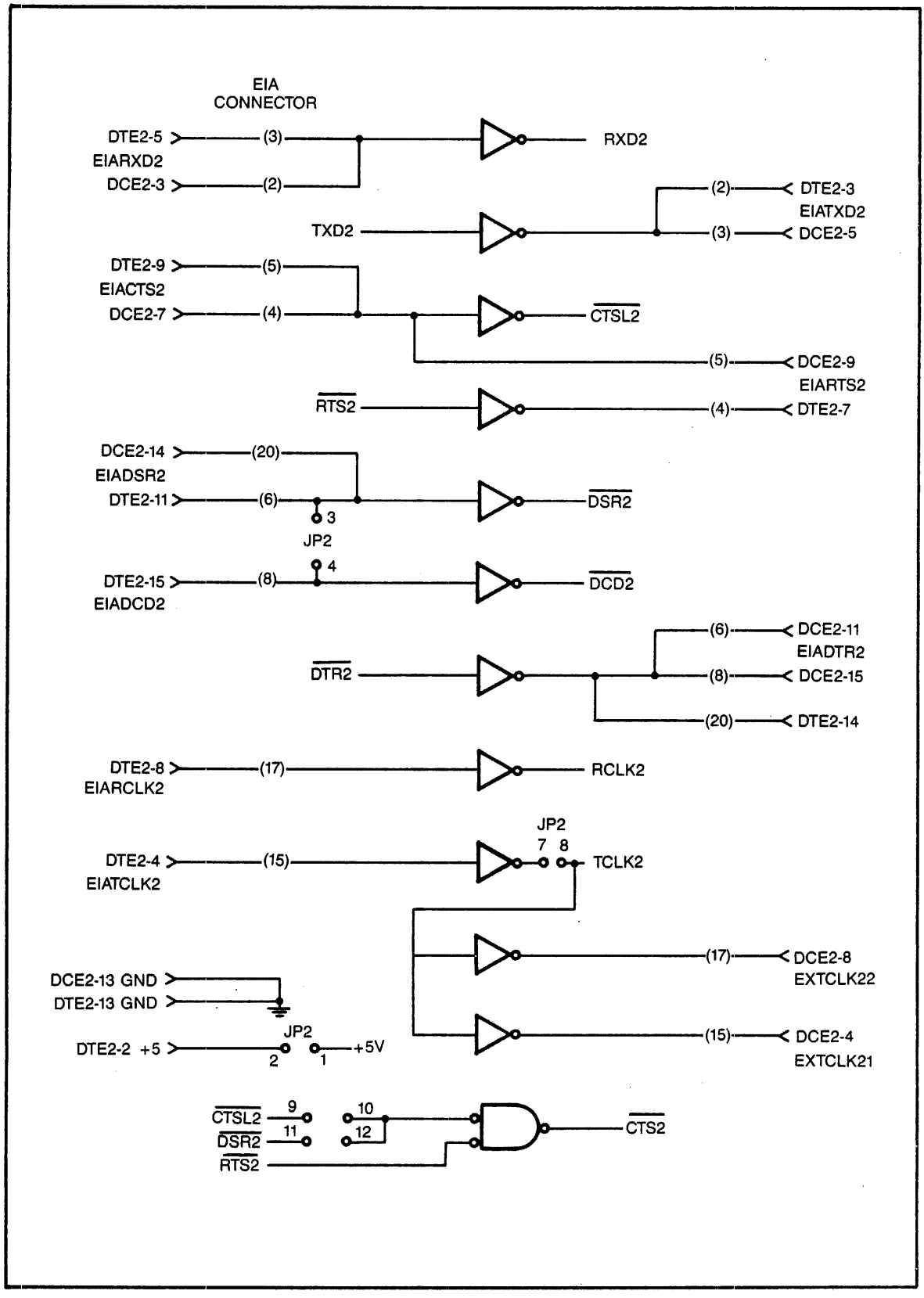


Figure 4-10. Simplified Schematic of Serial Port 1



PT1029-0180

Figure 4-11. Simplified Schematic of Serial Port 2

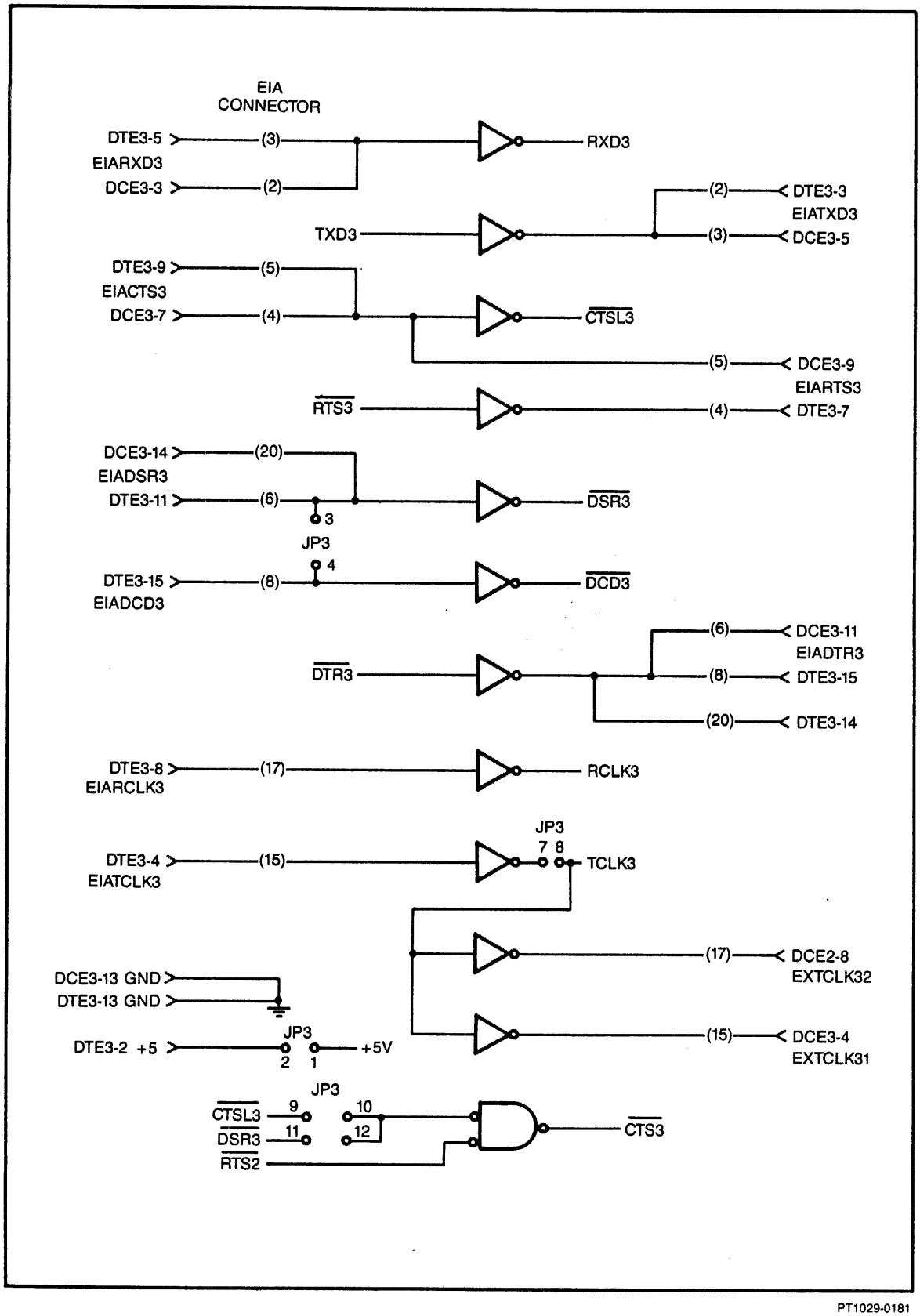
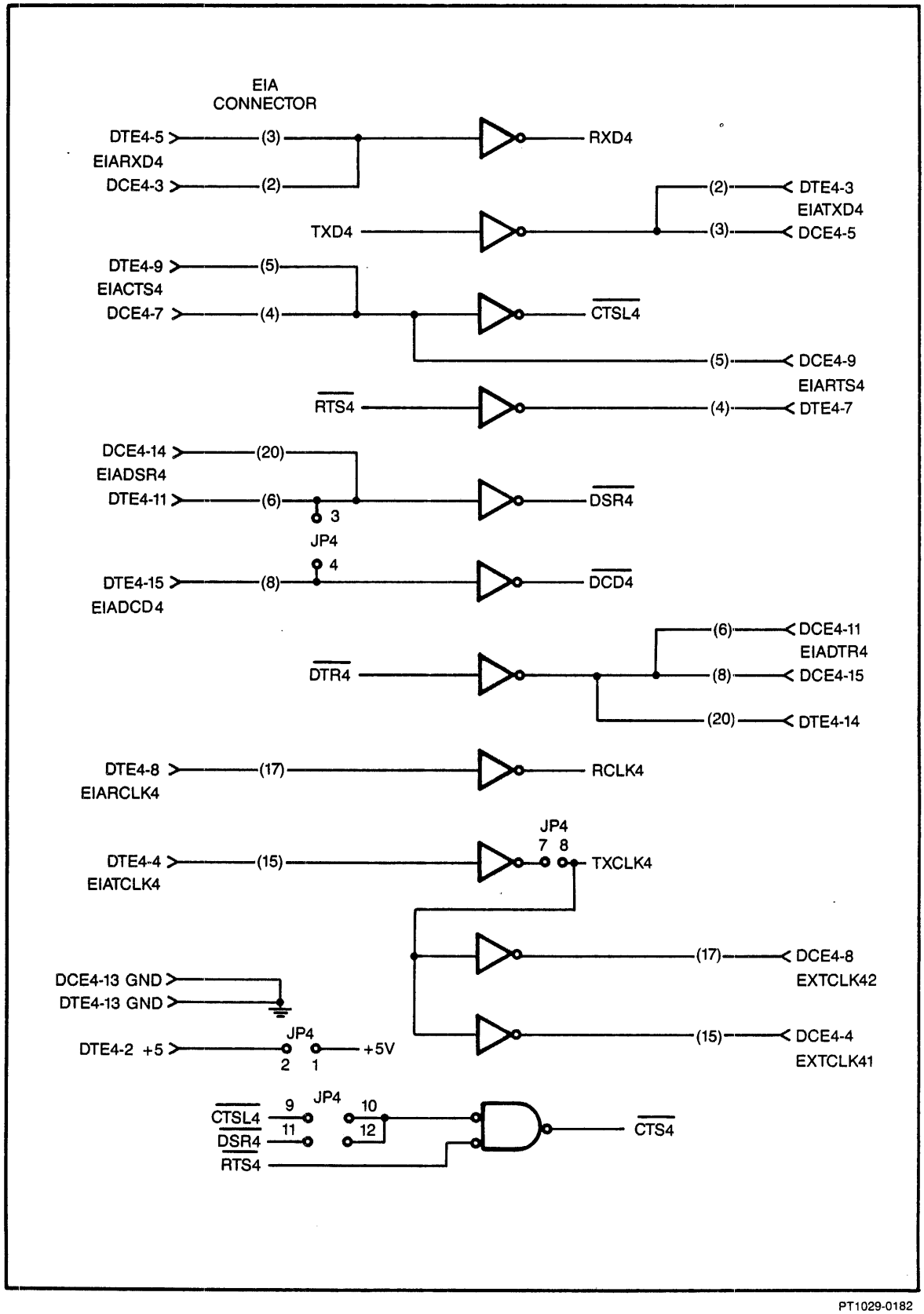


Figure 4-12. Simplified Schematic of Serial Port 3



PT1029-0182

Figure 4-13. Simplified Schematic of Serial Port 4

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5.1 DMA Test Program

This section provides programming information through an example program, DMA Test Program. The source code for this program is contained on the Diagnostic Diskette included with your DCP-286. This source code allows the independent software vendor, OEM, or user to understand the programming of various functions necessary for developing application programs involving the DCP-286.

The DMA Test Program is made up of two modules -- DMAPC.ASM and DMADCP.ASM. Each module is briefly described in the following subsections. The code itself is extensively documented with comments explaining the action being performed. Headings are included to separate major functional areas within each module.

Basically, one module executes on the PC to initialize the DCP-286 and download the program. The other module runs on the DCP-286 to manipulate various devices and set up the tests.

To execute the program, type the following in response to the DOS prompt (version 2.0 or above) on an IBM PC/XT/AT or compatible:

C>DMATEST.EXE<Enter>

5.2 DMAPC Module

The DMAPC module executes on an IBM PC/XT/AT or compatible and performs the following functions:

- Initialize the DCP-286 Control Registers.
- Set the DCP-286 Power-On Reset Vector.
- Download the DCP-286 module and verify.
- Prompt the user to input the test parameters.
- Initialize the values of the test parameters.
- Start execution of the DCP-286 DMA test program.
- Monitor the values of the DMA test program error variables.
- Display messages on the PC to report error conditions.

These functions are described in the following subsections.

5.2.1 Initialize DCP-286 Control Registers

The first function performed by the DMAPC module is to initialize the DCP-286 Control Registers (1 - 3) with specific configuration information.

Control Register 1: First, this register is set up so that (1) the DCP-286 is in transparent mode; and (2) program reset is active. To implement this setup, 0 hex is written to Control Register 1.

Control Register 3: This register is initialized next so that the DC-286 shares RAM with the PC in its address space at the starting address of D0000 hex. The shared RAM window size is set to 64 KB. To implement this setup, 34 hex is written to Control Register 3.

Control Register 2: This register is initialized (1) for enabled interrupts; (2) for segment enable to be active; and (3) for the starting address of shared RAM in the local processor (80286 on the DCP-286) to be F0000 hex. To implement this setup, an FF, FE, or FC hex is written to Control Register 2.

NOTE

For a window size of 64 KB, bits 0 and 1 in this register are "don't care".

5.2.2 Set DCP-286 Power-On Reset Vector

The Power-On Reset Vector for the local processor (80286) must be at F000:FFF0 hex in the address space of the local processor. Because the shared RAM window at the D000 hex segment in the PC address space maps into the F000 hex segment in the local processor address space, the reset vector is written at D000:FFF0 hex of the PC address space.

5.2.3 Download DCP-286 Program and Verify

In order to load the DMA Test Program into segment 0000 hex of the local processor address space, the shared RAM at the D000 hex segment of the PC address space must be mapped into segment 0000 hex of the local processor.

This mapping is performed by writing a C0 hex in Control Register 2. Downloading code into the DCP-286 then becomes simply an exercise in moving code from one area to another in the PC address space. To verify a successful download, the contents of RAM in two separate areas addressable by the PC processor are compared.

NOTE

Programs larger than 64 KB can only be downloaded in chunks with a maximum size of 64 KB.

5.2.4 Prompt User Input of Test Parameters and Initialize Values

For the testing, the user is prompted to enter test parameter values. The keyboard inputs are then passed to the DMA Test Program that runs on the DCP-286.

The test parameters input for the DCP-286 DMA Test Program must be passed to the DCP-286 through the shared memory window and then initialized. This function is completed by the program executing on the PC.

5.2.5 Start Execution of DCP-286 DMA Test Program

Execution of the DCP-286 DMA Test Program is started by forcing a program reset to the DCP-286 and disabling the transparent mode. To cause these actions, the programmed reset and transparent mode bits -- bits 2 and 1, respectively -- in Control Register 1 are set to 1.

5.2.6 Monitor Values of DMA Test Program Error Variables

The PC program continually reads the values of the error variables defined for the DMA Test Program, in order to report messages on errors. The testing of error variables is accomplished through the shared RAM window to the DCP-286 memory.

5.2.7 Display Messages for Error Conditions

When a DMA Test Program error variable contains a meaningful error code, the appropriate message is fetched and displayed.

5.3 DMADCP Module

The DMADCP module contains code to manipulate the various devices (for example, to reset and initialize the SCCs, DMA Controller, and so forth) and routines that complete various actions in specific sequences that comprise the tests.

The following DMA tests are performed:

- Half-Duplex Receive Test.
- Half-Duplex Transmit Test.
- Full-Duplex Test.

The program allows the user to select the specific lines to be tested and the specific tests to be run. The Half-Duplex Receive and Half-Duplex Transmit Tests can be done either on one selected line or on all four lines. The Full-Duplex Test can be done only on line 1 or line 2.

Before starting the test, the user selects whether or not the test should stop or continue if an error occurs. When an error is detected, a trigger pulse is provided on the test point by first setting and then clearing the test-point output bit in the Local Control Register. This pulse output on the DCP-286 test point can be used as a trigger source for diagnostic purposes.

The following subsections outline the test sequences.

5.3.1 Half-Duplex Receive Test

The code for this test performs the following functions in the order listed:

1. The DMA and SCC devices on the DCP-286 are reset.
2. The SCC device is set up for receive using DMA.
3. The DMA channel is set up for receive.
4. The receive buffer is cleared.
5. The transmit buffer is initialized.
6. The SCC transmit is enabled.
7. The SCC receive is enabled.
8. The DMA channel is enabled.
9. Receive data is compared, byte-by-byte, as it is received with the transmit data. The DMA channel word count is continually polled in order to determine whether or not it has been decremented.

When the word count is decremented, it marks the arrival of a new receive character. The receive character is compared with the transmit character. If no error occurs, the test continues until a predetermined count of characters is received, and then the test is terminated successfully.

5.3.2 Half-Duplex Transmit Test

The code for this test performs the following functions in the order listed:

1. The DMA and SCC devices on the DCP-286 are reset.
2. The SCC device is set up for transmit using DMA.
3. The DMA channel is set up for transmit.
4. The receive buffer is cleared.
5. The transmit buffer is initialized.
6. The SCC transmit is enabled.
7. The SCC receive is enabled.
8. The DMA channel is enabled.
9. Receive data is compared, byte-by-byte, as it is received with the transmit data. The DMA channel word count is continually polled in order to determine whether or not it has been decremented.

When the word count is decremented, it marks the arrival of a new receive character. The receive character is compared with the transmit character. If no error occurs, the test continues until a predetermined count of characters is received, and then the test is terminated successfully.

5.3.3 Full-Duplex Test

The code for this test performs the following functions in the order listed:

1. The DMA and SCC devices on the DCP-286 are reset.
2. The SCC device is set up for full duplex using DMA.
3. The DMA channel for receive is set up.
4. The DMA channel for transmit is set up.
5. The receive buffer is cleared.
6. The transmit buffer is initialized.
7. Data Terminal Ready (DTR) is enabled through the Local Control Register.
8. The SCC receive and transmit are enabled.
9. The DMA Channel for receive is enabled.
10. The DMA channel for transmit is enabled.
11. Receive data is compared, byte-by-byte, as it is received with the transmit data. The DMA channel word count is continually polled in order to determine whether or not it has been decremented.

When the word count is decremented, it marks the arrival of a new receive character. The receive character is compared with the transmit character. If no error occurs, the rest continues until a predetermined number of characters are received, and then the test is terminated successfully.

Appendix A
JUMPER AND SWITCH SUMMARY

A summary of the factory switch and jumper settings appears in Table A-1. Table A-2 lists the configuration options.

Table A-1. Factory Configuration Summary.

Switch/Jumper	Meaning
SW1 = CLOSED SW2 = CLOSED SW3 = OPEN SW4 = OPEN	SW1 - SW4 sets Control Register Base address; factory setting to 33C.
SW5 = OPEN SW6 = CLOSED	PC Bus Configuration (one connector) 512 KB Memory
JP5:3-4	IR3 for PC
JP5:17-18	I/O Channel Check Line
E6-E7	Comm Clock of 7.3728 MHz
E4-E5	IR3 on 8259 = Timer CH2
E9-E10,E15-E16, E18-E19 and JP1: 1-2,3-4,5-6,7-8, 9-10,11-12, 15-16	Line 1 as DTE
JP2:7-8 and 9-10	Line 2 as DTE
JP3:7-8 and 9-10	Line 3 as DTE
JP4:7-8 and 9-10	Line 4 as DTE
E1-E2	8-Bit Data Transfers

Table A-2. Configuration Options (Sheet 1)

Switch/Jumper	Meaning
SW1 - SW4	SW1 - SW4 sets Control Register Base address. See Figure 2-2 for table of addresses.
SW5 = CLOSED = OPEN*	AT Bus Configuration PC/XT Bus Configuration
SW6 = CLOSED* = OPEN	512 KB Memory Illegal Setting
JP5:1-2 JP5:3-4* JP5:5-6 JP5:7-8	IRQ2 for PC IRQ3 for PC IRQ4 for PC IRQ5 for PC
JP5:9-10 JP5:11-12 JP5:13-14 JP5:15-16	IRQ10 for PC/AT IRQ11 for PC/AT IRQ12 for PC/AT IRQ15 for PC/AT
JP5:17-18* Removed	I/O Channel Check Line Do not interrupt PC for parity
E7-E8* E6-E7	Comm Clock of 3.6864 MHz Comm Clock of 7.3728 MHz
E4-E5* E3-E4 E12-E13 E13-E14	IR3 on 8259 = Timer CH2 IR3 on 8259 = EIRQ0 Two-Line Configuration Four-Line Configuration
E9-E10,E15-E16, E18-E19 and JP1: 1-2,3-4,5-6,7-8, 9-10,11-12, 15-16	Line 1 as DTE*
E10-E11,E17-E18, JP1:2-4,1-3,6-8,5-7, 10-12,9-11,14-16, 13-15,17-18, and 19-20	Line 1 as DCE
*Factory Setting	

Table A-2. Configuration Options (Sheet 2)

Switch/Jumper	Meaning
JP2:7-8 and 9-10* JP2:3-4 and 11-12	Line 2 as DTE Line 2 as DCE
JP3:7-8 and 9-10* JP3:3-4 and 11-12	Line 3 as DTE Line 3 as DCE
JP4:7-8 and 9-10* JP4:3-4 and 11-12	Line 4 as DTE Line 4 as DCE
JP5:19-20 E1-E2*	16-Bit Data Transfers 8-Bit Data Transfers
*Factory Setting	

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