PRELIMINARY
DSH32 Synchronous/Asynchronous Serial Line Option

VAXstation 2000 and MicroVAX 2000 Technical Manual Addendum:

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1 Introduction

The DSH32 is a synchronous/asynchronous serial line option that provides the MicroVAX 2000 system with one port for one synchronous communications at data rates up to 19.2 K baud, and one port for eight data-only asynchronous lines supporting a variety of protocols. The ports are full-duplexed with bit or character-oriented protocol.

The DSH32 option consists of: a controller module (PN 54-18905-01), an asynchronous (DSH32-A) driver/receiver module (PN 54-17231-01), a synchronous (DSH32-S) driver/receiver module (PN 54-17230-01), and a 68-pin Y-type ribbon cable (PN 17-02290-01).

2 Physical Description

This section describes the DSH32 controller module and the two driver/receiver modules.

2.1 DSH32 Controller Module

The DSH32 controller module is a four-layer printed circuit board that measures 26.42 centimeters (10.4 inches) by 19.31 centimeters (7.6 inches), and weighs 425.25 grams (15.0 ounces). It connects to the MicroVAX 2000 system module by two 40-pin connectors (J1 and J2 on the DSH32 controller module connect to J8 and J11, respectively, on the system module). All power, ground, and data/address lines come through these connectors.

In addition, there is one 68-pin connector which connects to the two driver/receiver modules. Each driver/receiver module receives its power and data lines through this connector, so the system module is actually supplying the power for the entire DSH32 option subsystem through connectors J8 and J11 on the DSH32 controller module.

2.2 DSH32 Driver/Receiver Modules

Each driver/receiver module is a four-layer printed circuit board that measures 8.13 centimeters (3.20 inches) by 13.21 centimeters (5.20 inches), and weighs 99.23 grams (3.5 ounces). The two driver/receiver modules are both mounted in the expansion adapter, and connected to the DSH32 controller module using a 68-pin Y-type ribbon cable. Connector J1 on the driver/receiver module is used for the connection of an adapter cable which is connected to a modem or a host computer system. Table 1 lists the electrical standards and cable part numbers for the DSH32-A (asynchronous) and DSH32-S (synchronous) driver/receiver modules.

Table 1 Electrical Standard Cables

Electrical Standard	Cable Part Numbers
DSH32-A	
—DEC423	17-01174-02
DSH32-S	
—RS-422/V.36	17-01871-01
—RS-232/V.24	17-01872-01
—RS-423/V.10	17-01873-01

2.3 Electrical Characteristics

The power for both the logic module and the driver/receiver module is supplied by the MicroVAX 2000 system module through connectors J3 and J4 on the controller module. The modules power requirements are as follows:

- +12 V at 494.00 mA maximum
- –12 V at 240.00 mA maximum
- +5 V at 3.44 A maximum

2.4 Environmental Specifications

The DSH32 synchronous/asynchronous communication option environmental specifications are listed in Tables 1 through 3. Refer to Table 2 for storage conditions, Table 3 for operating conditions, and Table 4 for nonoperating conditions.

Table 2 Storage Conditions

Parameter	Range
Temperature range	5° C (41° F) to 50° C (122° F)
Relative humidity	10% to 95% (noncondensing)
Maximum wet bulb temperature	32° C (90° F)
Maximum dew point	2° C (36° F)
Altitude	2400 m (8000 ft) at 36° C (97° F)

Table 3 Operating Conditions

Parameter	Range
Temperature range	10° C (50° F) to 40° C (104° F)
Temperature change rate	11° C (52° F) degree/hour maximum
Relative humidity	10% to 90% (noncondensing, no diskette)
	20% to 80% (diskette in use)
Maximum wet bulb temperature	28° C (82° F)
Minimum dew point	2° C (36° F)
Altitude	2400 m (8000 feet) at 36° C (97° F)
Heat dissipation	17.4 watts maximum

Table 4 Nonoperating Conditions

Parameter	Range
Temperature range	-40° C (-40° F) to 66° C (151° F)
Relative humidity	95% at 66° C (151° F) (may condense)
Maximum wet bulb temperature	28° C (82° F)
Minimum dew point	2° C (36° F)
Altitude	4900 m (16,000 feet)

3 DSH32 Controller Module Input/Output Connectors

The DSH32 controller module connects to the MicroVAX 2000 system module by two 40-pin connectors (J1 and J2). The module uses a 68-pin connector (J3) for connection to the two driver/receiver modules.

Connectors J1 and J2 on the controller module share data/address lines, control lines, and several power and ground lines with connectors J8 and J11, respectively, on the system module. The signals on connectors J1 and J2 are listed in Table 5.

Connector J3 on the controller module connects the controller module, channels 0 through 7, to the driver/receiver module.

Table 5 Controller Module Connectors J1 and J2

Pin	Signal	Pin	Signal
J1-1	GND	J2-1	+5
J1-2	GND	J2-2	+5
J1-3	BDAL31	J2-3	+12
J1-4	BDAL30	J2-4	-12
J1-5	BDAL29	J2-5	GND
J1-6	BDAL28	J2-6	CLK0 H
J1-7	BDAL27	J2-7	BRESET L
J1-8	BDAL26	J2-8	VAS L
J1-9	BDAL25	J2-9	VDS L
J1-10	BDAL24	J2-10	WR L
J1-11	BDAL23	J2-11	DBE L
J1-12	BDAL22	J2-12	N/C
J1-13	GND	J2-13	GND
J1-14	GND	J2-14	GND
J1-15	BDAL21	J2-15	CAS03 L
J1-16	BDAL20	J2-16	CAS02 L
J1-17	BDAL19	J2-17	CAS01 L
J1-18	BDAL18	J2-18	CAS00 L

Table 5 (Cont.) Controller Module Connectors J1 and J2

Pin	Signal	Pin	Signal
J1-19	BDAL17	J2-19	N/C
J1-20	BDAL16	J2-20	OPTIRQ2
J1-21	BDAL15	J2-21	N/C
J1-22	BDAL14	J2-22	N/C
J1-23	BDAL13	J2-23	OPTROMENA L
J1-24	BDAL12	J2-24	OPTVIDENA L
J1-25	BDAL11	J2-25	VIDIRQ L
J1-26	BDAL10	J2-26	VIDEOF L
J1-27	GND	J2-27	GND
J1-28	GND	J2-28	GND
J1-29	BDAL09	J2-29	INTENA L
J1-30	BDAL08	J2-30	SCYC/IAD2 H
J1-31	BDAL07	J2-31	DCYC/IAD1 H
J1-32	BDAL06	J2-32	STFH/IADD H
J1-33	BDAL05	J2-33	N/C
J1-34	BDAL04	J2-34	N/C
J1-35	BDAL03	J2-35	N/C
J1-36	BDAL02	J2-36	N/C
J1-37	BDAL01	J2-37	N/C
J1-38	BDAL00	J2-38	N/C
J1-39	GND	J2-39	N/C
J1-40	GND	J2-40	+5 V

The DSH32 controller module layout is shown in Figure 1.

MA-X0970-88

Figure 1 DSH32 Controller Module Layout

4 Functional Description

The DSH32 module is functionally divided into three subsystems.

- **Interface subsystem**—Interfaces the asynchronous communication subsystem (DSH32-A), the synchronous communication subsystems (DSH32-S), and the diagnostic ROM to the central processing unit (CPU).
- **Asynchronous communication subsystem**—The major features of this subsystem are:

  – Eight data lead only serial lines at independent baud rates up to 38,400 bits per second.

– Two hundred and fifty-six character input FIFO buffer with programmable hold-off timer.
– Sixty-four character per line output FIFO buffer.

The major differences between the DSH32-A controller module (DHU implemetation) and the other DHU-like products are:

– The module has 8 versus 16 serial lines.
– The module has no output direct memory access (DMA) support.
– The module has no modem control.

- **Synchronous communication subsystem**—This subsystem uses two dual universal synchronous communication controller (DUSCC) to provide two independent, multiprotocol, full duplex receiver/transmitter channels. Each DUSCC supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls. This subsystem also contains 32 Kbytes of RAM space, which is used as a buffer between the synchronous lines and the CPU.

NOTE

Addresses and diagnostic codes have been reserved for possible future expansion to a second synchronous line, and are presented in the document for the sake of completeness.

All hardware associated with synchronous port 1 or a second DUSCC (DUSCC II), is not supported, and any diagnostic codes associated with this port or DUSCC should not normally occur.

Figure 2 shows a block diagram of the DSH32 option.

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Figure 2 DSH32 Option Block Diagram

4.1 Interface Subsystem

The interface subsystems allows the two communication subsystems and the diagnostic ROM to interface to the CPU through the connector(s) on the module. The control signals present at this connector are similar to the standard control signals of the MicroVAX bus, but the relative timing between them is slightly different.

The MicroDMA in the synchronous subsystem was designed to interface directly to the CPU, while the DC7045 in the asynchronous subsystem was designed to be used in a Q-bus system. The interface subsystem uses three field programmable logic sequencers (FPLSs) to translate from the control signals at the connector to the appropriate control signals for the device that is selected.

The diagnostic ROM subsystem includes a 64 Kbyte, 8-bit wide ROM which contains the diagnostic code and identification information for the system. This ROM resides from address 2014.0000 to 2017.FFFF and is directly addressable through longword reads by the CPU. However, only the least significant byte of each longword will contain useful data.

This subsystem also includes a programmable array logic (PAL) chip to decode which region of the address space is being accessed, and which device is selected.

The DSH32 controller module is accessible in the memory address ranges of 2014.0000 - 2017.FFFF, 3800.0000 - 3800.000E, and 3900.0000 - 3900.FFFF (hexadecimal). See Table 6 for a general address map of the controller module.

Table 6 DSH32 Controller Module General Address Map

Address Range (Hexadecimal)	Contents
2014.0000 - 2017.FFFF	Self-diagnostic ROM
3800.0000 - 3800.000E	DC7045 registers
3900.0000 - 3900.01FF	MicroDMA registers
3900.0200 - 3900.023F	Port-A DUSCC registers
3900.0210	Port-0 Transmitter FIFO
3900.0214	Port-0 Receiver FIFO
3900.0240 - 3900.027F	Port-I DUSCC registers
3900.0250	Port-I Transmitter FIFO
3900.0254	Port-I Receiver FIFO
3900.0280	Cable code input register
3900.02C0	Modem control output register
3900.8000 - 3900.FFFF	I/O buffer static RAM

4.2 Asynchronous Communication Subsystem

The asynchronous communication subsystem uses a DC7044 octal asynchronous receiver/transmitter (OCTART) and a DC7045 OCTART controller to transmit and receive data on each of the 8 data-only (no modem control) lines.
The controller maintains a 64-character output FIFO buffer for each of the 8 lines, as well as a 256 character input FIFO buffer that services all of the lines. When characters are received on a line, the data is stored in the input FIFO buffer and an interrupt signal is sent to the CPU. The CPU reads the data from the FIFO buffer and process it accordingly. Similarly, when a FIFO buffer becomes empty, an interrupt is sent telling the CPU that the line is ready to transmit more data.

Two interrupts are used for programming control of the asynchronous subsystem. Table 7 lists their vectors and source.

Table 7 Asynchronous Subsystem Interrupts

Vector	Interrupt Mask Bit	Source
244h	VF	Receive FIFO not empty
248h	VS	Transmit FIFO empty

The receiver interrupt must be enabled by setting bit 0 in the video select register (2008.000E). This bit selects the interrupt source for vector 244h as the communication option port. The other bits must always be written to zero. The receiver interrupt is qualified on the DSH32 option by any value that was programmed into the hold-off timer for receive interrupts that is explained later in this document.

All functions of the asynchronous subsystem are controlled by reading and writing the registers in the DC7045. These registers are word addressable and should never be addressed as longwords. Table 8 briefly describes the registers.

Table 8 Registers

Register	CSR Address (hexadecimal)	Type
Control and status (SLU_CSR)	3800.0000	r/w[1]
Receive buffer (SLU_RBUF)	3800.0002	ro[1]
Receive timer (SLU_RTIM) [2] [3]	3800.0002	wo[1]
Line parameter (SLU_LPR) [4]	3800.0004	r/w
Transmit FIFO data (SLU_DATA) [4]	3800.0006	wo
Transmit FIFO size (SLU_DATA) [3] [4]	3800.0006	wo
Line status (SLU_STAT) [3] [4]	3800.0007	ro
Line control (SLU_CNTL) [4]	3800.0008	r/w
Not used [4] [5]	3800.000A	r/w

[1]Read/write = r/w; write only = wo; read only = ro

[2]Available only when SLU_CSR [0:3] equal 0.

[3]Able to be read/written as a single byte only or as part of the word it is in.

[4]A separate register is available for each line based on the value of SLU_CSR [0:3].

[5]Not used on this module. These registers are normally used to implement DMA output transfers and are listed here only because they appear in the address space.

Table 8 (Cont.) Registers

Register	CSR Address (hexadecimal)	Type
Transmit enable [4]	3800.000C	r/w
Not used [4] [5]	3800.000E	r/w

[4]A separate register is available for each line based on the value of SLU_CSR [0:3].

[5]Not used on this module. These registers are normally used to implement DMA output transfers and are listed here only because they appear in the address space.

Registers are accessed by instructions which use the register address as a source or destination. However, before multiple registers are accessed, the channel number should be written to the CSR address (3800.0000). For example the following I/O commands would be executed to read the line status register of channel number 3:

```
MOVB   #CHAN,@#CSR      ;WRITE CHANNEL NUMBER TO CSR
MOV    @#CSR+6,R0       ;READ THE LINE STATUS REGISTER
```

Example:

```
CHAN = 0er00011(b)

where
        e = the R.IE bit
        r = the RESET bit
  0011(b) = channel number 3
```

CSR + 6 addresses a block of 16 line status registers, only 8 of which are used. The DHT32-A hardware indexes this address by three, thereby selecting line status register of channel number 3.

4.2.1 Control And Status Register

Figure 3 shows the bits in the control and status register (SLU_CSR).

Figure 3 Control And Status Register

Data Bit	Definition
<15> (RO)	Transmitter ready (T.RDY). Set this bit when a transmit FIFO becomes empty. This bit is cleared by reading the register or setting the RESET bit.
<14> (RW)	Transmit interrupt enable (T.IE). When this bit is set, an interrupt is generated to the system at vector address 248h whenever the T.RDY bit becomes set. Clear by writing to 0. Setting the RESET bit has no effect on this bit.
<13> (RO)	Diagnostic failure (D.FAIL). When this bit is set and the RESET bit is clear, a failure has been detected by internal module diagnostics. The bit is set if the RESET bit is set and cleared after internal diagnostics have run successfully.
<12> (RO)	Not used. This bit is not used on the serial option card and should be ignored by system software.
<11:8> (RO)	Transmit line number (T.LINE). These bits hold the line number that caused the T.RDY bit to set. The bits are only valid while T.RDY is set. Clear by setting the RESET bit.
<7> (RO)	Receiver done (R.DON). This bit is set when receive FIFO data is available. This bit is set by setting the RESET bit since diagnostic information is left in the receive FIFO. This bit is only cleared when the FIFO is empty.
<6> (RW)	Receiver interrupt enable (R.IE). Setting this bit enables a receive interrupt to the system at vector address 244h. An interrupt occurs under the following conditions: • R.IE is set and a character is placed into an empty FIFO.[1] • R.IE is changed from a 0 to a 1 while the FIFO is not empty.[1]
<5> (RW)	Reset (RESET). Setting this bit causes the module to reset itself and run the internal diagnostics. The bit stays set while the diagnostics are running. This bit should not be written to a 1 when it is already set. Clear by completion of diagnostics.
<4> (RW)	Diagnostic skip (D.SKP). When this bit is set at the same time as the RESET bit, the reset and diagnostic time is shortened. This allows fast resetting of the module.

[1]Both of the previous conditions are subject to the delay specified in the hold-off timer in register SLU_RTIM. The enable is cleared bywriting to 0. Setting the RESET bit does not affect this bit.

Data Bit	Definition
<3:0> (RW)	Line select number (L.SEL). This field is used to select which line the SLU_LPR, SLU_DATA, SLU_SIZE, SLU_STAT, and SLU_CNTL registers represent. Additionally, when these bits are all 0, the SLU_RTIM value may be set. Only lines zero through seven are valid on the serial option card. Any data written to registers outside that range cause unpredictable results.

NOTES

To enable receive interrupts from the serial option card, bit 0 of the video select register (VDCSEL) should be set to 1.

Since the state of the transmit ready bit is cleared on any read of the register, the software must use only word or byte write instructions and not read-modify-write instructions (BISW, INCB) when accessing the register.

4.2.2 Receive Buffer Register

Figure 4 shows the bits in the receive buffer register (SLU_RBUF).

Figure 4 Receive Buffer Register

Data Bit	Definition
<15> (RO)	Data valid (D. VAL). This bit is set whenever the receive FIFO is not empty. The bit is set by RESET since diagnostic information is left in the FIFO.
<14> (RO)	Overrun error (O.ERR). This bit is set if a character is received on the indicated line (R.LINE) and the FIFO for that line if full or an error occured while receiving a character. If this bit is set along with F.ERR and P.ERR then the R.DATA field contains diagnostic information.
<13> (RO)	Framing error (F.ERR). This bit is set if there was a framing error (no stop) on receiving the character. If this bit is set along with O.ERR and P.ERR then the R.DATA field contains diagnostic information. A break detected on the indicated line appears as a framing error with a null (all 0) data field.
<12> (RO)	Parity error (P.ERR). This bit is set if parity is enabled for the line and the parity of the character received is incorrect. If this bit is set along with O.ERR and F.ERR then the R.DATA field contains diagnostic information.
<11:8> (RO)	Receive line (R.LINE). These bits form the binary value of the line number for which the data in the word is valid. (Even though there is room for 16 lines, only lines 0 through 7 are considered valid.)

Data Bit	Definition
<7:0> (RO)	Received data (R.DATA). These bits contain the data received for the indicated line. If the error bits (O.ERR, P.ERR and F.ERR) are all clear, then the data is valid. If any one of the bits are set, then the data is invalid due to the condition specified by that bit (with the exception of F.ERR; see that bit's documentation). If all the error bits are set, then the word contains diagnostic information in the R.DATA field.

4.2.3 Receive Timer Register

Figure 5 shows the bits in the receive timer register (SLU_RTIM).

Figure 5 Receive Timer Register

Data Bit	Definition
<7:0> (WO)	Receiver time delay (R.TIME). When the L.SEL bits in SLU_CSR are all 0, a byte written to this address sets the value of an interrupt holdoff timer for receive character interrupts. The following table shows the various programmed values and the response of the option card.

The value is set to 1 by setting the RESET bit.

Value	Interrupt Requested
0	The receive FIFO becomes three quarters (48 characters) full. This could take an infinite amount of time.
1	Immediate interrupt. The interrupt is requested as soon as the FIFO is not empty.
2 to 255	An interrupt is requested after the first character is received and the number of milliseconds equal to the value written have passed.

4.2.4 Line Parameter Register

The line parameter register (SLU_LPR) is used to program the characteristics for each of the eight asynchronous lines of the DSH32-A subsystem. The line parameter register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register. Figure 6 shows the bits in the line parameter register.

Figure 6 Line Parameter Register

Data Bit	Definition
<15:12> (RW)	Transmit speed (T.SPEED). These bits are used to set the transmit speed of the selected line. See Table 9 for the baud rates that correspond to the values for the field. The field is set to 1101 (9600 baud) by setting the RESET bit.
<11:8> (RW)	Receive speed (R.SPEED). These bits are used to set the receive speed of the selected line. See Table 9 for the baud rates that correspond to the values for the field. The field is set to 1101 (9600 baud) by setting the RESET bit.
<7> (RW)	Stop code (S.CODE). This bit defines the length of the transmitted stop bit. If S.CODE is set to 0, then one stop bit is always sent. If S.CODE is set to 1, the two stop bits are sent for 6-, 7-, and 8-bit characters and one and one-half stop bits for 5-bit characters. Setting the RESET bit sets S.CODE to 0.
<6> (RW)	Even parity select (E.PAR). This bit selects the sense of the character parity (if enabled by P.ENA). If set to 1, then even parity is expected. If set to 0, then odd parity is expected. Setting the RESET bit sets E.PAR to 0.

Data Bit	Definition
<5> (RW)	Parity enable (P.ENA). This bit enables the detection and transmission of character parity. If set to 1, then parity is enabled for the line. If set to 0, parity is disabled for the line. Setting the RESET bit clears this bit.
<4:3> (RW)	Character length (C.LEN). These bits define the number of bits that make up each character. The bits do not include the start, stop or parity bits. The following information shows the character length for each of the field settings.

Value	Bits Per Character
00	5
01	6
10	7
11	8

Setting the RESET bit causes this field to be set to 11 (8 bits per character).

Data Bit	Definition
<2:1> (RW)	Diagnostic control (DIAG). These bits control the state of the internal diagnostics on the option. If both bits are set to 0, then the background diagnostics only reports the status when an error is detected. If the bits are set to 01, then the background program runs and reports the status whether or not an error is detected. Once these bits are set to 01, no other bits should be changed in this register until that code is cleared to 0.
<0> (RW)	Disable XON and XOFF reporting (D.XRPT). This bit is used to control whether or not XON and XOFF characters are saved in the receive FIFO. If this bit is 0, then XON and XOFF characters are saved. If this bit is 1 and the transmit auto flow control (T.AUTO) bit in the line control register (SLU_CNTL) is set, then XON and XOFF characters are not saved in the FIFO. Setting the RESET bit clears this bit.

Table 9 defines the binary codes used to select the transmit and receive data rates for the controller module.

Table 9 Binary Codes Used to Select Baud Rates

Value	Baud Rate
0000	50
0001	75
0010	110
0011	134.5
0100	150
0101	300
0110	600
0111	1200
1000	1800
1001	2000
1010	2400
1011	4800
1100	7200
1101	9600
1110	19,200
1111	38,400

4.2.5 Transmit FIFO Data Register

The transmit FIFO data register (SLU_DATA) sends characters out to the desired line. The transmit FIFO data register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register. Figure 7 shows the bits in the transmit FIFO data register.

Figure 7 Transmit FIFO Data Register

Data Bit	Definition
<15:0> (WO)	Transmit data (T.DATA). The transmit data field programs the data to be sent out to the selected line. If a byte write is performed to the register, only the data in the low byte is placed in the transmit FIFO. If a word write is performed to the register, then two characters are placed in the FIFO. First the low byte is placed in the FIFO, then the high byte. Setting the RESET bit clears this register.

4.2.6 Transmit FIFO Size Register

The transmit FIFO size register (SLU_SIZE) is used to determine the amount of available space in the transmit FIFO for the selected line. The transmit FIFO size register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register (SLU_CSR). Figure 8 shows the bits in the transmit FIFO size register.

Figure 8 Transmit FIFO Size Register

Data Bit	Definition
<7:0> (RO)	FIFO space available (F.SIZE). This field is used to indicate the number of entries left in the transmit FIFO for the selected line. The available size ranges from 0 to 64 characters. Setting the RESET bit sets this field to 40h (64 entries are available).

4.2.7 Line Status Register

The line status register (SLU_STAT) is used to read the status of the modem control signals on the module. While modem control is not used, the status bits are set to indicate to DHU compatible software that no modem control exists. This register must be read (as a word) along with the FIFO size register. It is documented here at its byte position.

The line status register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register (SLU_CSR). Figure 9 shows the bits in the line status register.

Figure 9 Line Status Register

Data Bit	Definition
<7> (R0)	Data set ready (DSR) bit. Not implemented. Always read as 0.
<6> (R0)	Not implemented. Always read as 0.
<5> (R0)	Ring indicator (RI) bit. Not implemented. Always read as 0.
<4> (R0)	Data carrier detect (DCD) bit. Not implemented. Always read as 0.
<3> (R0)	Clear to send (CTS) bit. Not implemented. Always read as 0.
<2> (R0)	Not implemented. Always read as 0.
<1> (R0)	Modem status (M.STAT) bit. This bit is used to indicate if modem support is available for the selected line. No modem support is available at all on the option so this bit will always read as 1.
<0> (R0)	Not implemented. Always read as 1.

4.2.8 Line Control Register

The line control register (SLU_CNTL) is used to control miscellaneous line interface functions. The line control register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register. Figure 10 shows the bits in the line control register.

Figure 10 Line Control Register

Data Bit	Definition
<15> (RO)	Not implemented. Always read as 0.
<14> (RO)	Not implemented. Always read as 0.
<13> (RO)	Not implemented. Always read as 0.
<12> (RW)	Request to send (RTS) bit. Not used on module. Setting or clearing this bit has no effect.
<11> (RO)	Not implemented. Always read as 0.
<10> (RO)	Not implemented. Always read as 0.
<9> (RW)	Data terminal ready (DTR) bit. Not used on module. Setting or clearing this bit has no effect.
<8> (RW)	Link type (L.TYPE). This bit is used to inform the controller module of a modem attached to the selected line. Since modem control is not supported on the DSH32 option, this bit should always be left cleared. Setting the bit should have no effect on the controller function.

Data Bit	Definition
<7:6> (RW)	Maintainance mode (MAINT). These bits are used to control the maintainance features incorporated into the module. A 2-bit value is used to place the module in one of four operating states. The values and the corresponding states are listed in the following table.

Value	Operating State
00	Normal operating state.
01	Automatic echo mode. The data received on the selected line is sent back out to the corresponding transmit line (even if T.ENA is cleared). The normal internal receive/transmit path is used and the characters are saved in the receive FIFO. The receive line must be enabled and no data placed into the FIFO by the user is transmitted. The baud rate selected for the receiver is used for both transmit and receive.
10	Local loopback. The data sent out the transmit channel is looped back to the receive channel even if the receiver enable is clear. The transmitter enable must be set (T.ENA), any data received at this time is ignored, and the output line is held in the mark condition. The baud rate selected for the transmitter is used for both transmit and receive.
11	Remote loopback. The data received is retransmitted at the receiving baud rate. The data is not saved in the FIFO and the transmit enable is ignored. The receive enable must be set.

Setting the RESET bit causes these bits to be set to 00 (normal operating mode).

Data Bit	Definition
<5> (RW)	Force transmit XOFF (F.XOFF). This bit is used to send an XOFF before any other character in the FIFO. If this bit stays set, an XOFF is sent after every other character received on that line. When the bit is cleared (after being set), an XON character is sent unless the receiver auto flow control (R.AUTO) is enabled and the FIFO is three-quarters full.
<4> (RW)	Transmitter auto flow control (T.AUTO). This bit is used to control the controller module's response to valid flow control characters received on a line. When the bit is set, a received XOFF character causes the transmisson to stop until an XON character is received. The T.ENA bit is actually cleared and set by this action so host software can override this action. To completely disable a channel both this bit and the T.ENA bit must be cleared. Setting the RESET bit causes this bit to clear.
<3> (RW)	Transmit break (BREAK). This bit is used to assert a break condition on the selected channel. The condition is held until the bit is cleared. Setting the RESET bit causes this bit to clear.
<2> (RW)	Receive line enable (R.ENA). This bit is used to enable and disable the receiving of data on the selected line. This bit is set to enable a line. Setting the RESET bit clears this bit.
<1> (RW)	Receiver auto flow control (R.AUTO). This bit is used to control the flow of characters into the receive FIFO. An XOFF character is sent to any line that has this bit set when the receive FIFO become three-quarters full. An XON character is then sent when the FIFO becomes less than half full. Setting the RESET bit clears this bit.
<0> (RW)	Transmit abort (T.ABT). This bit is used to flush all characters from the transmit FIFO for a line. A few characters may be sent after the bit is set. When the FIFO is cleared, the T.RDY bit is set and, if enabled, an interrupt is requested. Setting the RESET bit clears this bit.

4.2.9 Transmit Enable Register

The transmit enable register (SLU_TXA) is used to enable data transmission on the selected line. Extreme care must be taken when setting the enable bit in this register. While the other bits in the register are not used, setting certain bits could hang up the controller module. Only the most significant bit of this register should ever be changed.

The transmit enable register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register. Figure 11 shows the bits in the transmit enable register.

Figure 11 Transmit Enable Register

Data Bit	Definition
<15> (RW)	Transmitter enable (T.ENA). This bit is used to enable and disable the transmission of characters on the selected line. When this bit is set, the controller asynchronous subsystem will transmit all characters placed in the FIFO. When cleared, the DSH32 controller transmits flow control characters that are generated by the controller module (if enabled by the user). To completely stop character transmission on a line, both the T.AUTO bit and the T.ENA bit should be cleared. Setting the RESET bit sets this bit.
<14:8> (RO)	Not implemented. Always read as 0.
<7> (RW)	Do not set. Setting this bit hangs up the controller module. Setting the RESET bit clears the bit.
<6> (RO)	Not implemented. Always read as 0.
<5:0> (RO)	Not used. Always set to 0.

4.3 Synchronous Communication Subsystem

The synchronous communication subsystem uses one DUSCC to provide the one full-duplex synchronous communication port with bit- or character-oriented protocol. These chips reside on the subsystem's 32-bit I/O bus, with 32 Kbytes (8K x 32-bits) of static RAM (SRAM) and two 8-bit registers.

A MicroVAX 78532 DMA controller chip (MicroDMA) is used to provide DMA transfers between the DUSCC and the SRAM, and to interface the 32-bit system bus to the 32-bit DSH32 I/O bus. The DSH32 does not do DMA transfers with the MicroVAX 2000 main memory.

In addition, a PAL is used to control data flow on the I/O bus. The synchronous subsystem is accessible in the memory address range of 39000000-3900FFFF, and divided into four subranges:

MicroDMA registers	3900.0000 - 3900.01FF
DUSCC registers	3900.0200 - 3900.027F
8-bit registers	
– cable code register	3900.0200
– modem control register	3900.02C0
SRAM	3900.8000 - 3900.FFFF

The synchronous subsystem includes a driver/receiver module (PN 54-17230-01) which contains the drives for the electrical standard supported by the DSH32 module. This driver/receiver module mounts in the expansion adapter and is connected to the controller module using a 68-pin "Y" ribbon cable (PN 17-02290-01).

4.3.1 I/O Bus Interface

The main bus on the synchronous subsystem is a 32-bit I/O bus. It is on this bus (address ranges 3900.0200 through 3900.02FF, and 3900.8000 through 3900.FFFF) that the DUSCC, the 8-bit registers, and the RAM reside. This bus is interfaced to the system 32-bit bus through the interface subsystem, and throughthe MicroDMA, which controls all transactions on the I/O bus. When the system software accesses a location corresponding to the synchronous subsystem, theMicroDMA will run a bus separate cycle on the I/O bus to access the device at the specified location. In this way all synchronous subsystem memory locations and registers may be accessed in any combination of bytes, words, or longwords.

This function is completely transparent to the programmer, however the I/O bus width must be set to 4 bytes through the WID field in the MicroDMAs DGCTL register before the RAM, DUSCCs or 8-bit registers can be accessed. A PAL is used to control the flow of data on the I/O bus.

4.3.2 DMA Controller

The synchronous subsystem uses the MicroDMA to provide DMA service between each of the communication ports and the 32 Kbytes of the on-board SRAM, allowing large messages to be transmitted and received with a minimum of CPU intervention. The MicroDMA has four independent DMA channels, numbered 0 to 3. These channels move data between the SRAM and the transmit and receive FIFOs of each of the two communication ports.

The priority of the four channels is fixed, with 0 being the highest and 3 being the lowest. DMA channels 0 and 1 service the port-0 receive and transmit FIFOs, respectively. DMA channel 2 and 3 service the port-1 receive and transmit FIFOs respectively. In this way port-0 always has priority over port-1.

4.3.3 Modes of Operation

The MicroDMA controller is used in two of the four modes. These are I/O DMA mode and I/O access mode. The I/O access mode allows the MicroVAX 2000 system to access the devices on the I/O bus. This mode does not use any of the four DMA channels, and is active at power-up. Before the I/O bus can be accessed, the WID field in the DGCTL register must be written to a value of 11 to configure the I/O bus width to 4 bytes. The behavior of the bus depends upon which subrange in the I/O bus address space is accessed.

NOTE

Addresses and diagnostic codes have been reserved for possible future expansion to a second synchronous line, and are presented in the document for the sake of completeness.

All hardware associated with synchronous port 1 or a second DUSCC (DUSCC II), is not supported, and any diagnostic codes associated with this port or DUSCC should not normally occur.

If the SRAM space is accessed, the bus supports byte, word, and longword operations at any address in the range. If the DUSCC space is accessed, **only byte-wide operations are supported**, although any address in the range can be accessed. If a word or longword operation is attempted to one of the DUSCCs, the results are unpredictable, and the chip may be damaged.

If the 8-bit registers are accessed, the bus supports byte, word, and longword operations to the appropriate address, but **only the least significant byte of the bus is used**. For example, if the software tries to do a longword read from the cable code register, the data from the register will only appear in bits <7:0> of the longword. If the software tries to do a word write to the modem control register, the data to be written must be present on bits <7:0> of the word.

I/O DMA mode is the mode used to transfer data between the SRAM and the two communication ports. In this mode, the I/O bus width is set to 8-bits, so only byte-width transfers are supported.

4.3.4 Interrupts

There are three sources of interrupts in the synchronous subsystem: the MicroDMA and the two communication ports (DUSCCs). All three interrupt lines are NANDed together to the NIIRQ2 of connector J2. The following edge on this signal corresponds to the interrupt vector 254. Refer to the appropriate system module specification for more information about interrupts.

There is only one condition that will cause the MicroDMA to pose an interrupt to the CPU. This condition is when the transfer specified by the MicroDMA's various registers has terminated, and the DMA channel has been configured to interrupt the CPU on termination. The termination of a DMA channel will occur when its byte count register reaches zero, or if the channel is associated with a port receiver, when the DUSCC receives an EOM flag.

When an interrupt occurs in the MicroVAX 2000 system, the CPU responds with an interrupt acknowledge cycle, which reads a vector out of the systems boot ROM. Because of this, the synchronous subsystem has no opportunity to supply a vector to the CPU.

NOTE

It is necessary for the interrupt service routine to determine which device in the synchronous subsystem generated the interrupt. In addition, it is very important that the interrupt handler makes sure that all

interrupting conditions have been cleared before returning control to the main program.
This condition exist because the interrupt line to the MicroVAX 2000 system is edge sensitive, and if all interrupting conditions are not cleared, it is impossible for the subsystem to generate further interrupts.

Because the interrupt line is edge sensitive, the interrupt handler must be written so that at the end of the service routine, it will jump back to the beginning of the polling routine and does not go to the next device. This will ensure that none of the synchronous subsystem interrupts will be missed.

4.3.5 Registers

The DSH32 has two groups of registers: MicroDMA, and communication or port registers. The following sections describe each group:

4.3.5.1 MicroDMA Registers

The 63 internal MicroDMA registers occupy a 512 byte block of the MicroVAX 2000 system address space, located at 3800.0000 - 3800.01FF. These registers are 32-bit wide and are byte addressable. Because the DSH32 controller module does not use all modes of operation of the MicroDMA, only 17 of the 63 registers are used. Before any of the 4 DMA channels can be used, the system software must be configured for several of these registers. Table 10 lists the MicroDMA registers and their addresses.

Table 10 MicroDMA Registers

Register	Address (Hexadecimal)	Access
DMA global control register	3900.0000	R/W
Channel 0 control register	3900.0040	R/W
Channel 1 control register	3900.0080	R/W
Channel 2 control register	3900.00C0	R/W
Channel 3 control register	3900.0100	R/W
Channel 0 I/O source address	3900.004C	R/W
Channel 1 I/O source address	3900.008C	R/W
Channel 2 I/O source address	3900.00CC	R/W
Channel 3 I/O source address	3900.010C	R/W
Channel 0 I/O destination address	3900.0058	R/W
Channel 1 I/O destination address	3900.0098	R/W
Channel 2 I/O destination address	3900.00D8	R/W
Channel 3 I/O destination address	3900.0118	R/W
Channel 0 initial byte count	3900.0050	R/W
Channel 1 initial byte count	3900.0090	R/W
Channel 2 initial byte count	3900.00D0	R/W
Channel 3 initial byte count	3900.0110	R/W
Channel 0 current byte count	3900.0068	R
Channel 1 current byte count	3900.00A8	R
Channel 2 current byte count	3900.00E8	R
Channel 3 current byte count	3900.0128	R

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DMA Global Control Register

The DMA global control register (DGCTL) is used to control, configure, and determine the global status for the MicroDMA controller. Figure 12 shows the bits in the DMA global control register.

Figure 12 DMA Global Control Register

Data Bits	Definition
<31:5>	Unused in the DSH32 option. Read only 0s. Must be written as 0s.
<4:3>	These two read/write bits are used by the MicroDMA to determine the width of the I/O bus. These bits are cleared by reset, and must both be set to 1s before the I/O bus is accessed for the I/O bus to function correctly.
<0>	Reset. Setting this bit has the same effect as asserting the reset pin.

DMA Channel Control Registers

The four channel control registers (DCCTL0 through DCCTL3) are used to control, configure, and determine the status for the four channels. Figure 13 shows the bits in the DMA channel control register.

Refer to Table 10 for the registers addresses.

Figure 13 DMA Channel Control Register

Data Bits	Definition
<31:24>	Not used by the DSH32 option. Returns 0s.
<23>	Done bit. A read/write bit set to indicate that the current channel operation terminated. Cleared during a reset operation or when the Enable bit (bit 0) is set. For diagnostic purposes, this bit may be written to a 1.
<22>	I/O Interrupt bit (IOI). A read-only bit which, when set, indicates that the channel's I/O interrupt request (IIR) input has been asserted. If the terminate on interrupt (TOI) (bit-10) is also set, the current transfer will terminate. In the synchronous subsystem, this bit can only be set on DMA channels 0 and 2, which are connected to port 0 and port 1 receivers,respectively. When set, this bit indicates that the corresponding port's receiver has received an end of message (EOM) flag.
<21:17>	Not used by the DSH32 option.
<16:11>	Must be written to 0s.
<10>	Terminate on interrupt (TOI) bit. A read/write bit set to terminate DMA transfers on a channel upon the assertion of the IIR input for the channel. This bit indicates that the corresponding port's receiver has received an end of message (EOM) flag. This bit can only be set on DMA channels 0 and 2, servicing port receivers 0 and 1, respectively.
<9:8>	Read/write bits that determine whether the source and/or destination addresses will remain the same or be incremented during a DMA transfer on a channel. If bit <8> is set, the source address will be incremented. If cleared, the source address will remain the same. If bit <9> is set, the destination address will be incremented. If cleared, the destination address remains the same.
<7:6>	Read/write bits that specify the data width of the I/O device associated with the channel. Must be written to 0s.
<5:4>	Must be written to 01.
<3>	Not used by the DSH32 option.
<2>	Interrupt enable (IE) bit. A read/write bit set to enable the MicroDMA to generate an interrupt when the done bit (<23>) is set. Cleared by a reset operation.

Data Bits	Definition
<1>	Terminate (TERM) bit. A read/write bit set to force the termination of the current channel operation, but allows data currently in an internal MicroDMA buffer to be written. Cleared during a reset operation or by setting the enable bit (<0>).
<0>	Enable bit. A read/write bit set to enable operations on a channel. If the bit is cleared during an active channel operation, the operation is aborted. This bit is cleared when the channel's operation terminates or by a reset operation.

DMA I/O Source Address Registers

The DMA I/O source address registers (DCIDS0 through DCIDS3) must be loaded with the address of the source of the DMA transfer. This address may be associated with the communication port or the start of a memory buffer in the DSH32 synchronous subsystem on-board SRAM. Because the I/O bus has only a 24-bit address, only the bottom 24 bits of the address are used.

The I/O source address register bits are shown next. Figure 14 shows the bits for the DMA I/O source address registers (DCIDS0 through DCIDS3). Refer to Table 10 for the I/O source address registers addresses.

Figure 14 DMA I/O Source Address Register

DMA I/O Destination Address Registers

The DMA I/O destination address registers (DCIDD0 through DCIDD3) must be loaded with the address that specifies the destination of a DMA transfer. This address may be associated with the communication port or the start of a memory buffer in the DSH32 synchronous subsystem on-board SRAM. Because the I/O bus has only a 24-bit address, only the bottom 24 bits of the address are used. Figure 15 shows the bits for the DMA I/O destination address registers (DCIDD0 through DCIDD3).

Figure 15 DMA I/O Destination Address Register

DMA Initial Byte Count Registers

The DMA initial byte count registers (DCIBC0 through DCIBC3) must be loaded with the initial byte count for a DMA transfer. When the transfer is started, the register information is copied into the channel's current byte count register where it is decremented as the transfer proceeds. Figure 16 shows the bits in the DMA initial byte count register.

Figure 16 DMA Initial Byte Count Register

DMA Current Byte Count Registers

The DMA current byte count registers (DCBC0 through DCBC3) contain the byte count for the transfer currently in progress. The registers specify the number of bytes remaining in the transfer. These registers are read-only. Figure 17 shows the bits in the current byte count register.

Figure 17 DMA Current Byte Count Register

4.3.5.2 Communication Port Registers

The synchronous subsystem provides two DSV11 compatible communication ports (port 0 and port 1) which support bit- and character-oriented synchronous protocols and may operate at data rates up to 19.2 Kbauds.

NOTE

Addresses and diagnostic codes have been reserved for possible future expansion to a second synchronous line, and are presented in the document for the sake of completeness.

All hardware associated with synchronous port 1 is not supported, and any diagnostic codes associated with this port should not normally occur.

Each port consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a bit rate generater, and a parity generater/checker. Each port also includes the full set of RS-449 category-I modem control and a subset of the catagory-II modem controls. The registers for the two ports are all 8-bits wide and occupy addresses in the range 3900.0200 to 3900. 02FF in a MicroVAX 2000 subsytem.

The synchronous subsystem is connected to a separate driver/receiver module for the supported standards. In addition to the data, clock, and modem controls, the subsystem also includes a 4-bit input code which indicates the type of cable that has been connected to the MicroVAX 2000 system, and two outputs to tell the driver module whether to use RS-422 or RS-232 driver and receivers.

The connector code consists of four signals which are selectively pulled low by the cable connected to the MicroVAX 2000 system, indicating the type of cable, and the desired electrical standard. At configuration time, it is necessary for the software to read this four-bit code, determine which electrical standard is desired, and indicate this to the driver module by asserting the appropriate bit in the modem control output register (MCOR).

To provide the data link protocol, each communication port includes a dual universal serial communications controller (DUSCC). In addition to the data lines, the DUSCCs also provide the majority of the modem controls. Those that are not provided by the DUSCCs are implemented in the modem control output register.

Each DUSCC is a single-chip MOS-LSI communications device that provides multiprotocol, full-duplex, receiver/transmitter communication in a single package. Although each DUSCC is capable of providing two full-duplex communications channels, the DSH32 uses a DUSCC for each port,to provide greater versatility and simpler programming.

Each DUSCC has a separate transmitter/receiver DMA service request output which are connected to the MicroDMA's I/O transfer request (ITR) inputs. The DUSCCs are normally configured in full-duplex dual address DMA mode: this mode allows the receiver and tranmitter of each port to request service of the MicroDMA whenever receiver data is available, or new transmit data is needed. In addition, the DUSCCs "DONE" pins are connected to the MicroDMA's I/O interrupt inputs, allowing the receipt of an end of message (EOM) flag service on that DMA channel and generate an interrupt to the CPU.

The following sections describe the communication port registers having a uniquely defined content for the DSH32-S synchronous subsystem. Table 11 lists the communication Port-0 (DUSCC I) registers and their hexadecimal addresses.

Table 11 Communication Port Registers (Port-0 DUSCC I)

Register	Address Port-0 DUSCC I	Access
Channel mode register 1	3900.0200	R/W
A channel mode register 2	3900.0201	R/W
B channel mode register 2	3900.0221	R/W
Syn 1/secondary address 1 register	3900.0202	R/W
Syn 2/secondary address 1 register	3900.0203	R/W
Transmitter parameter register	3900.0204	R/W
A transmitter timing register	3900.0205	R/W
B transmitter timing register	3900.0225	R/W
receiver parameter register	3900.0206	R/W
A receiver timing register	3900.0207	R/W
B receiver timing register	3900.0227	R/W
A counter/timer preset register high	3900.0208	R/W
B counter/timer preset register high	3900.0228	R/W
A counter/timer preset register Low	3900.0209	R/W
B counter/timer preset register Low	3900.0229	R/W
A counter/timer control register	3900.020A	R/W
B counter/timer control register	3900.022A	R/W
A output and miscellaneous register	3900.020B	R/W
B output and miscellaneous register	3900.022B	R/W
A counter/timer high	3900.020C	R
B counter/timer high	3900.022C	R
A counter/timer low	3900.020D	R
B counter/timer low	3900.022D	R

Table 11 (Cont.) Communication Port Registers (Port-0 DUSCC I)

Register	Address Port-0 DUSCC I	Access
A pin configuration register	3900.020E	R/W
B pin configuration register	3900.022E	R/W
A channel command register	3900.020F	R/W
B channel command register	3900.022F	R/W
Transmitter FIFO	3900.0210	W
Receiver FIFO	3900.0214	R
Receiver status register	3900.0218	R/W
Transmitter and receiver status register	3900.0219	R/W
A input and counter timer status register	3900.021A	R/W
B Input and Counter Timer Status Register	3900.023A	R/W
General status register	3900.021B	R/W
A interrupt enable register	3900.021C	R/W
B interrupt enable register	3900.023C	R/W
A interrupt control register	3900.021E	R/W
B interrupt control register	3900.023E	R/W
Modem control output register	3900.02C0	-
Cable code input register	3900.0280	-

The following sections describe the communication port registers having a uniquely defined content for the DSH32 synchronous subsystem. Table 12 lists the communication Port-1 (DUSCC II) registers and their hexadecimal addresses.

NOTE

Communication Port-1 (DUSCC II) as listed in Table 12 is for future expansion and is not supported on the MicroVAX 2000 system.

Table 12 Communication Port Registers (Port-1 DUSCC II)

Register	Address Port-1 DUSCC II	Access
Channel mode register 1	3900.0240	R/W
A channel mode register 2	3900.0241	R/W
B channel mode register 2	3900.0261	R/W
Syn 1/secondary address 1 register	3900.0242	R/W
Syn 2/secondary address 1 register	3900.0243	R/W
Transmitter parameter register	3900.0244	R/W
A transmitter timing register	3900.0245	R/W
B transmitter timing register	3900.0265	R/W
Receiver parameter register	3900.0246	R/W
A receiver timing register	3900.0247	R/W
B receiver timing register	3900.0267	R/W
A counter/timer preset register High	3900.0248	R/W
B counter/timer preset register High	3900.0268	R/W
A counter/timer preset register Low	3900.0249	R/W
B counter/timer preset register Low	3900.0269	R/W
A counter/timer control register	3900.024A	R/W
B counter/timer control register	3900.026A	R/W
A output and miscellaneous register	3900.024B	R/W
B output and miscellaneous register	3900.026B	R/W
A counter/timer high	3900.024C	R
B counter/timer high	3900.026C	R
A counter/timer low	3900.024D	R
B counter/timer low	3900.026D	R

Table 12 (Cont.) Communication Port Registers (Port-1 DUSCC II)

Register	Address Port-1 DUSCC II	Access
A pin configuration register	3900.024E	R/W
B pin configuration register	3900.026E	R/W
A channel command register	3900.024F	R/W
B channel command register	3900.026F	R/W
Transmitter FIFO	3900.0250	W
Receiver FIFO	3900.0254	R
Receiver status register	3900.0258	R/W
Transmitter and receiver status register	3900.0259	R/W
A input and counter timer status register	3900.025A	R/W
B input and counter timer status register	3900.027A	R/W
General status register	3900.025B	R/W
A interrupt enable register	3900.025C	R/W
B interrupt enable register	3900.027C	R/W
A interrupt control register	3900.025E	R/W
B interrupt control register	3900.027E	R/W
Modem control output register	3900.02C0	-
Cable code input register	3900.0280	-

Channel Mode Register

The DUSCC) chip has four registers which are used to configure the mode of operation. These are the channel mode 1 registers and the channel mode 2 registers. No restrictions on the value are placed in the two channel mode 1 registers. However, bits <5:3> of the channel mode 2 registers must have certain values for the DSH32 synchronous subsystem to operate properly. Figure 18 shows the location and contents of the channel mode 2 register.

Figure 18 Channel Mode 2 Register Location and Contents

Figure 19 Port Pin Configuration Register Location and Contents

Port Pin Configuration Registers

The DUSCC has two registers to define the functions of its multifunction pins. These registers must be loaded with a specific value for proper operation of the DSH32 synchronous subsystem. Figure 19 shows the location and contents of the port pin configuration register.

Port Receiver Timing Register

The DUSCC has two registers to define the source and speed of their receive clocks. These registers must be loaded with a specific value for proper operation of the DSH32 synchronous subsystem. Figure 20 shows the address and contents of the port receiver timing register.

Figure 20 Port Receiver Timing Register Address and Contents

NOTE

Bits <3:0> in these registers are used to select the receiver bit rate. The receive clock normally comes from the modem. However, during certain diagnostic modes of operation, it may be useful to generate the receive clock from the DUSCCs internal bit rate generator.

Port Transmitter Timing Registers

The DUSCC has two registers to define the source and speed of their transmit clocks. These registers must be loaded with a specific value for proper operation of the DSH32 synchronous subsystem. Figure 21 shows the address and contents of the port transmitter timing register.

Figure 21 Port Transmitter Timing Register Address and Contents

NOTE

Bits <3:0> in these registers are used to select the transmitter bit rate from the DUSCCs internal bit rate generator. This is only meaningful if the DUSCC is providing its own transmit clock.

Port Output and Miscellaneous Registers

The DUSCC has two port output and miscellaneous registers. These registers are used for configuring miscellaneous modes of operation and controlling various outputs of the DSH32 synchronous subsystem. The registers bits are explained below. Figure 22 and Figure 23 show the format of these registers.

Figure 22 Channel A Output and Miscellaneous Register

Data Bits	Definition
<7:5>	Transmitted residual character length bits - see DUSCC data sheet.
<4>	TxRDY activate mode bit.
<3>	RxRDY activate mode bit.
<2:1>	Not used by the DSH32 synchronous subsystem.
<0>	This bit is the port's request-to-send (RS) output. The bit may be asserted and negated under program control. When set, the port's RS output will be asserted, and when clear, the RS output will be unasserted. The DUSCC may also be configured to negate RS automatically five bit times after the last character in the transmitter FIFO has been set.

Figure 23 Channel B Output and Miscellaneous Register

Data Bits	Definition
<7:5>	Transmitted residual character length bits.
<4>	TxRDT activate mode bit.
<3>	RxRDY activate mode bit.
<2>	Local loopback (LL) bit. This state of the local-loopback output will follow this bit. When set, the local-loopback signal is asserted low.
<1>	Terminal ready (TR) bit. When set, the terminal ready signal is asserted low.
<0>	This bit is the port's request-to-send (RS) output. The bit may be asserted and negated under program control. When set, the port's RS output will be asserted, and when clear the RS output will be unasserted. The DUSCC may also be configured to negate RS automatically five bit times after the last character in the transmitter FIFO has been sent.

Input and Counter/Timer Status Registers

The port has two input and counter/timer status registers, one for each of the two channels in the DUSCC. The port modem control signals are readable at these registers. Figure 24 and Figure 25 show the format of these registers. The register bits are explained in the following table.

Figure 24 Channel A Input and Counter/Timer Status Register

Data Bits	Definition
<7>	Counter/timer running bit.
<6>	Counter/timer zero detect bit.
<5>	Delta receiver ready bit. When set, this bit indicates that a transition has occurred on the receiver-ready (RR) modem control signal. The port can be configured to generate an interrupt on this condition.
<4>	Delta clear-to-send bit. When set, this bit indicates that a transition has occurred on the clear-to-send (CS) modem control signal. The port can be configured to generate an interrupt on this condition.
<3>	Receiver-ready (RR) bit. This bit reflects the status of the RR modem control signal. This bit reads as a 0 when the RR signal is asserted, and as a 1 when the RR signal is negated.
<2>	Clear-to-send (CS) bit. This bit reflects the status of the CS modem control signal. This bit reads as a 0 when the CS signal is asserted, and as a 1 when the CS signal is negated.
<1>	Test mode (TM) bit. This bit reflects the status of the TM modem control signal. This bit reads as a 0 when the TM signal is asserted, and as a 1 when the TM signal is negated.
<0>	Unused, reads as a 1.

Figure 25 Channel B Input and Counter/Timer Status Register

Data Bits	Definition
<7>	Counter/timer running bit.
<6>	Counter/timer 0 detect bit.
<5>	Delta data mode bit. When set, this bit indicates that a transition has occurred on the data mode (DM) modem control signal. The port can be configured to generate an interrupt during this condition.
<4>	Delta incoming call bit. When set, this bit indicates that a transition has occurred on the incoming call (IC) modem control signal. The port can be configured to generate an interrupt during this condition.
<3>	Data mode (DM) bit. This bit reflects the status of the DM modem control signal. This bit reads as a 0 when the DM signal is asserted, and as a 1 when the DM signal is negated.
<2>	Incoming call (IC) bit. This bit reflects the status of the IC modem control signal. This bit reads as a 0 when the IC signal is asserted, and as a 1 when the IC signal is negated.
<1>	Unused, reads as a 1.
<0>	Unused, reads as a 1.

Modem Control Output Register

The modem control output register (MCOR) provides each communication port with the RS-449 signals Select Rate (SR) and Remote Loopback (RL), and two signals which indicate to the driver/receiver module to implement the RS-422 or the RS-232 electrical standard. Figure 26 shows the format of the register. The register bits are explained in the following table.

Figure 26 Modem Control Output Register

Data Bits	Definition
<7>	Not used.
<6>	Not used.
<5>	Port-1 BCONNTEST H bit. When this bit is asserted, the driver/receiver will go to the local loopback mode . This means that some of the RS-232 data which cannot be looped back through the normal operation mode will be looped back in this test mode.
<4>	Port-0 ACONNTEST H bit. When this bit is asserted, it forces the driver/receiver module into the local loopback mode. This means that some of the RS-232 data which cannot be looped back through the normal operation mode will be looped back in this mode.
<3>	Port-1 SR L . Same as bit 1, but for Port-1.
<2>	Port-1 RL L . Same as bit 0, but for Port-1.
<1>	Port-0 SR L bit. This bit controls the port-0 select rate (speed select) output. When this bit is cleared, the select rate output is asserted. When set, the output is negated.
<0>	Port-0 RL L bit. This bit controls the port-0 remote loopback output. When this bit is cleared, the remote loopback output is asserted. When set, the output is negated.

Cable Code Input Register

The cable code input register contains two 4-bit codes that indicate the type of cable connected to the MicroVAX 2000 system box.

Figure 27 shows the format of the register. The register bits are explained in the following table.

Figure 27 Cable Code Input Register

Data Bits	Definition
<7:4>	Port-0 code bits. These bits represent the 4-bit code which indicates the type of cable that is connected to the MicroVAX 2000 system box (port-). The table presented in Figure 28 shows the correspondence between these bits and the type of cable used.
<3:0>	Port-1 code bits. These bits represent the 4-bit code which indicates the type of cable that is connected to the MicroVAX 2000 system box (port-1). The table presented in Figure 28 shows the correspondence between these bits and the type of cable used.

Figure 28 shows the 4-bit code and the corresponding cable type.

Port Interrupt Control Registers

Each DUSCC and each SYNC port has one interrupt control register. Figure 29 shows the format of these registers. The register bits are explained in the followingtable.

Figure 28 4-Bit Code And Cable Type

Figure 29 Port Interrupt Control Registers

Data Bits	Definition
<7:6>	DUSCC channel A/B interrupt priority bits.
<5:4>	Vector mode bits. These bits must be loaded with the value 11 to indicate non-vectored mode. The DSH32 synchronous subsystem does not support the interrupt acknowledge cycles.
<3>	Vector bits to modify.
<2>	Vector includes status bit.
<1>	DUSCC channel A master interrupt enable bit.
<0>	DUSCC channel B master interrupt enable bit.

5 Internal Diagnostics

The DSH32 option has three levels of internal diagnostics: power-up test, self-test, and system exerciser. Each of these is discussed in the following sections. If an error occurs during the internal diagnostic, refer to the *VAXstation 2000 and MicroVAX 2000 Maintenance Guide* (EK-VSTAB-MG) for troubleshooting procedures.

5.1 Power-up Test

Power-up tests are the same for the DSH32 option as they are for the basic system. However, run TEST 4 (T 4) for testing the asynchronous subsystem of the DSH32 option, and run TEST 3 (T 3) for testing the synchronous subsystem of the DSH32 option. The countdown display should not show an underscore following the four or the three.

The power-up test symbols are the same for the DSH32 option as they are for the other tests, and they function the same way.

The power-up test can take up to approximately 6 seconds to complete. It is important that the user not manipulate the option in any way during this time. The results of the power-up test are displayed in the configuration utility.

5.2 Self-Test

The DSH32 option can be self-tested in either Field Service or customer mode. The field service mode self-test tests the entire option, where the customer mode self-test does not test the two driver/receiver modules.

The Field Service mode self-test requires a loopback connector to be attached to the option. No loopback connector is required for the customer mode self-test. The results of the self-test are displayed in the configuration utility.

5.2.1 Power-Up and Self-Test Error Codes

The configuration table contains the results of the self-test and power-up tests. Table 13 and Table 14 list the possible error codes that the configuration table may display for the DSH32-A subsystem of the DSH32 option.

Figure 30 shows the format for reading the error code for the DSH32-A subsystem.

Figure 30 Error Code Format for the DSH32-A

Table 13 Power-Up and Self-Test Error Codes for DSH32-A

Error Code[1]	Definition
0001	Normal SLU module operation; no errors detected.
0010	Control and status register failed read after write test.
0020	Controller is hung; internal hardware self-test never flagged completion by clearing CSR reset bit.
0030	Internal hardware self-test failed; diagnostic fail bit set.
0040	Internal self-test result bytes failed to generate a receiver interrupt.
0050	Receiver done not set following internal hardware self-test.
0060	Receiver done not clear after reading self-test bytes.
0070	Could not find any valid data in receiver FIFO.
00A0	Data valid bit was set when FIFO should have been empty.
00B0	Internal self-test error—low octart error.
00C0	Internal self-test error—high octart error.
00D0	Internal self-test error—RAM error.
00E0	Internal self-test error—undefined status code found.
0101	FIFO size register error; FIFO SB empty, size register indicates FIFO is not.
2000	An illegal transmitter interrupt was detected.
2020	A data compare error was detected while performing alternating bit pattern read after write test of the SLU RAM space.

[1]Low 16-bits of the module information line or the appropriate 16-bits for a particular communication line.

Table 14 Field Service Mode Self-Test Error Codes (with loopback installed) for DSH32-A

Error Code[1]	Definition
0001	Normal operation; no errors detected.
0050	Receiver done not ready following internal auto diagnostics.
0060	Receiver done not clear after reading self-test bytes.
0070	Could not find any valid data in receiver FIFO.
0080	Transmitter failed to generate interrupt on transmit FIFO empty.
011x	Transmitter did not become ready before timer expired following null character transmitted.
0120	Data not received; receiver done did not become ready before timer expired following transmission of an ASCII character.
0131	Null character expected in receiver FIFO, not found.
0141	Transmitted data expected in receiver FIFO, not found.
0161	Transmit FIFO overrun error detected during basic data transmission test.
0171	Framing error occurred during basic data transmission test.
0181	Parity error occurred during basic data transmission test.
0190	FIFO data "receive line" bit field indicates that the data was received on the wrong line.
01A0	Transmitter action bit not clear with data sent on disabled line.
01B1	Receiver not done when data is expected from FIFO.
01D1	Port never became ready to send new data.
2010	Transmit ready bit did not clear with transmitter action FIFOs emptied.

[1]Low 16-bits of the module information line or the appropriate 16-bits for a particular communication line.

Figure 31 shows the format for reading the self-test error code for the DSH32-S subsystem. Table 15 lists the possible self-test error codes that the configuration table may display for the DSH32-S subsystem of the DSH32 option.

Figure 31 Error Code Format for DSH32-S

NOTE
The base system ROM must be version 2.1 or higher.

Table 15 Power-Up and Self-Test Error Codes for DSH32-S Subsystem

Error Codes	Message Description
0001.xxx0	µDMA DAL bus test
0002.xxx0	Static RAM checkerboard test
0003.xxx0	Static RAM SNAIR test
0004.xxx0	I/O register test
0005.xxx0	Check for loopback connector test
0006.xxx0	µDMA static (register) test
0007.xxx0	DUSCC I static (register) test
0008.xxx0	Check for second DUSCC test
0009.xxx0	DUSCC II static (register) test
000A.xxx0	DUSCC I reset circuit test
000B.xxx0	DUSCC I counter/timer test

Table 15 (Cont.) Power-Up and Self-Test Error Codes for DSH32-S Subsystem

Error Codes	Message Description
000C.xxx0	DUSCC II counter/timer test
000D.xxx0	Modem signal test
000E.xxx0	µDMA functional test
000F.xxx0	DUSCC I BOP protocol transmit/receive test
0010.xxx0	DUSCC II BOP protocol transmit/receive test
0011.xxx0	DUSCC I COP/BISYNC protocol test
0012.xxx0	DUSCC II COP/BISYNC protocol test
0013.xxx0	DUSCC I dynamic test
0014.xxx0	DUSCC II dynamic test
0015.xxx0	µDMA interrupt test
0016.xxx0	DUSCC I interrupt test
0017.xxx0	DUSCC II interrupt test

NOTE

Error codes replace the "xxx" in Table 15. If a error code is returning the address of the failing register, this address is only the last three hex digits of the 32-bit address. It should be understood that the prefix "39000" must be added to any address that is returned.

The DSH32-S subsystem is a single-port device for the MicroVAX 2000 system. Errors associated with DUSCC II would not normally occur.

5.3 System Exerciser

Run the exerciser to simulate worst-case operating conditions for the devices in the MicroVAX 2000 system. See Section 2.3.3 of the *VAXstation 2000 and MicroVAX 2000 Maintenance Guide* for a complete explanation of the system exerciser. The results of the system exerciser are displayed as they occur, and are not reported by the configuration utility.

To run the system exerciser in customer mode, install no loopbacks. Type **T 0** at the console prompt.

To run the field service mode system exerciser on the entire MicroVAX 2000 system, including the DSH32 option, do the following steps:

1. Insert a 25-pin loopback in the modem port.
2. Insert H3199 50-pin loopback in port D of the expansion adapter.
3. Insert an H3101 36-pin loopback in port C of the expansion adapter.
4. Insert MMJ loopback connectors in ports 2 and 3 of the DEC 423 converter. If you do not install these loopbacks, the exerciser will drop these two serial lines from the test.
5. Insert and load the special-keyed diskette and TK50 compact tape cartridge from the maintenance kit (if read/write testing of the RX33 and TK50 drives is needed). If the keyed diskette or TK50 cartridge is not inserted, the system tests those devices in customer mode.
6. Run the exerciser by entering TEST 101 (run once) or TEST 102 (run forever). See Table 2.4 in the maintenance guide for a complete explanation of these commands:

To run the system exerciser on the DSH32 option only, do the following steps.

1. Insert the 25-pin loopback in the modem port.
2. Insert the 36-pin loopback in port D of the expansion adapter.
3. Insert the 50-pin loopback in port C of the expansion adapter.
4. Type TEST 80000106 at the console prompt.
5. Type 4 3 at the ? >>> prompt.

NOTE

Typing 4 3 will test both the DSH32-A and DSH32-S subsystems of the DSH32 option. Typing 3 will test only the DSH32-S. Typing 4 will test only the DSH32-A.

This procedure tests only as far as the loopbacks on ports C and D. To include the 36-pin cable in the test, install the 36-pin loopback connector on the end of the cable in place of the cable concentrator for testing the DSH32-S. Install this loopback connector to port D to test the DSH32-A.

To include the 36-pin cable and the cable concentrator in the test, install the DECconnect loopback in the connectors of the cable concentrator in place of terminal cables. Only the lines that have loopbacks installed are tested. Other lines are dropped from the test.

5.3.1 System Exerciser Error Codes

A description of the system exerciser test commands for the DSH32 are listed in Table 16. Table 17 lists the modes.

Table 16 System Exerciser Test Commands for the DSH32

Commands	Descriptions
T 00000000	Customer mode, select all devices, run forever, no loopback required
T 00000101	Field Service mode, one pass, external loopback required
T 00000102	Field Service mode, run forever, external loopback required
T 80000103	Manufacturing mode, run forever, external loopback required
T 80000106	Field Service mode to run only specified options, run forever

Table 17 System Exerciser Test Modes for the DSH32

Test Mode	Loopback Type	Audience
Full functional	Internal loopback	Customer mode
Burst mode	Internal loopback	Customer mode
Full functional	External loopback	Field Service and manufacturing
Burst mode	External loopback	Field Service and manufacturing

5.3.1.1 System Exerciser Error Codes for the DSH32-A

Figure 32 shows an example of the system exerciser display while running the system exerciser for the DSH32-A in field service mode. Customer mode gives the same display, but with a CU in place of the FS on the top of the display.

Figure 32 System Exerciser Display Example (DSH32-A Subsystem Only)

In the previous example a normal status and error message follows the SLU mnemonic. Under that are four lines of messages. The lower order field of four digits of the first line represent the status of line 0 of the DSH32-A subsystem. The higher order field of four digits represent the status of line 1, and so on, for all eight lines. In this example, all the lines have successfully passed the exerciser.

A number 1 in the field indicates that the line is working. Otherwise the exerciser displays some other code that reflects the error condition that caused the line to be dropped. The following example illustrates this:

```
                    007F.0321
status for line 1--> 0001.0001 <--status for line 0
status for line 3--> 0001.0001 <--status for line 2
status for line 5--> 0001.0001 <--status for line 4
status for line 7--> 0321.0001 <--status for line 6
```

In the example, line 7 was dropped because data was lost on that line. The first line, which represents the overall status of the DSH32 option, reflects that line 7 was dropped by displaying 7F. The code 0321 on the first line shows that the error on line 7 was the last error detected. Each of the error fields maintain the error code for that line's failure or success.

Table 18 lists the exerciser error codes for the DSH32-A.

Table 18 Exerciser Error Codes for the DSH32-A

Error Code[1]	Definition
0000	Fatal software error occurred making a call to ELN KERNEL.
0001	Normal SLU module operation; no errors detected.
0010	Control and status register failed read after write test.
0020	Controller is hung, internal hardware self-test never flagged completion by clearing CSR Reset bit.
0030	Internal hardware self-test failed, diagnosic fail bit set.
0050	Receiver done not set following internal auto diagnostics.
0070	Could not find any valid data in receiver FIFO.
00B0	Internal self-test error—low octart error.
00C0	Internal self-test error—high octart error.
00D0	Internal self-test error—RAM error.
00E0	Internal self-test error—undefined status code found.
010x	FIFO size register error; FIFO SB empty but size register indicates FIFO is not.
011x	Transmitter did not become ready before timer expired following ASCII character transmitted; non-fatal error.
0110	Transmitter did not become ready before timer expired following ASCII character transmitted; fatal error.
012x	Receiver done did not become ready before timer expired following ASCII character transmitted.
019x	FIFO data "received line" bit field indicates that the data was received on the wrong port during simultaneous channel data transmission test.
020x	Transmit FIFO overrun error detected during simultaneous channel data transmission test.
021x	Framing error occurred during simultaneous channel data transmission test.

[1]Low 16-bits of the module information line or the appropriate 16-bits for a particular communication line.

Table 18 (Cont.) Exerciser Error Codes for the DSH32-A

Error Code[1]	Definition
022x	Parity error occurred during simultaneous channel data transmission test.
023x	Data error on port; channel 0 dropped from test.
024x	Data error on port; channel 1 dropped from test.
025x	Data error on port; channel 2 dropped from test.
026x	Data error on port; channel 3 dropped from test.
027x	Data error on port; channel 4 dropped from test.
028x	Data error on port; channel 5 dropped from test.
029x	Data error on port; channel 6 dropped from test.
02Ax	Data error on port; channel 7 dropped from test.
02B0	All lines have been dropped—data wrap tests can no longer run.
02C0	Receive FIFO contained more than eight internal selftest result bytes.
02Dx	Parity error detected during multiport data wrap test.
02Ex	Framing error detected during multiport data wrap test.
02Fx	Overrun error detected during multiport data wrap test.
0300	Time-out occurred waiting for transmitter interrupt service routine to flag completion of data packet transmission.
0310	Time-out occurred waiting for receiver interrupts.
032x	Data lost on line.
0330	Receiver done did not clear after emptying receive FIFO.
0340	Data error detected while testing RCVR FIFO.
0350	Status error found while testing RCVR FIFO.
0360	Ran out of usable ports in testing RCVR FIFO; all lines failed.

[1]Low 16-bits of the module information line or the appropriate 16-bits for a particular communication line.

Table 18 (Cont.) Exerciser Error Codes for the DSH32-A

Error Code[1]	Definition
0370	Two hundred fifty six character packet not completely received during FIFO test.
0380	Data valid not clear after emptying receive FIFO.
0390	Failed to force overrun error in receive FIFO test.
0400	Controller is hung; internal hardware skip self-test never flagged completion by setting receiver done bit.
0420	Entire data packet lost during simultaneous transmission test.
043x	Transmit FIFO did not have enough space to transmit entire data packet during receive FIFO test.
0440	SLU requested an interrupt for an unused line; interrupt requests should come from lines 0 through 7 only.
045x	Data packet only partially received from FIFO when timer for receive data expired.
0460	Data was received on an unused line. Data should come from lines 0 through 7 only.
1000	The base system firmware returned a fatal status condition when the exerciser requested a communication port with the system exerciser monitor.
1010	Found background monitor error code (307 octal) during receive FIFO test.
1020	Found background monitor error code (307 octal) during simultaneous channel transmission test.
1030	A read of the CSR register was returned as all 1s. May indicate that the controller board is not firmly plugged into the MicroVAX 2000 system module.
1040	A read of the RBUF register was returned as all 1s. May indicate that the controller board is not firmly plugged into the MicroVAX 2000 system module.

[1]Low 16-bits of the module information line or the appropriate 16-bits for a particular communication line.

5.3.1.2 System Exerciser Error Codes for the DSH32-S

Figure 33 shows an example of the system exerciser displaying 1 port (port 0), without errors while running the system exerciser in field service mode for the DSH32-S. Figure 34 shows an example of the system exerciser displaying 2 ports (port 0 and port 1) without errors while running the system exerciser in field service mode for the subsystem. Customer mode gives the same display, but with a CU in place of the FS on the top of the display. Table 19 lists the system exerciser error codes.

NOTE

Port 1 is not available on MicroVAX 2000 systems.

Figure 33 System Exerciser Display Example of 1 Port (Port 0) with 0 Errors (DSH32-S Subsystem Only)

The information is displayed with two lines following the DSH32-S mnemonic. The first or top line is the common module information line, and its error field is divided into two halves by a decimal point. This information will either reflect the operating status of the synchronous line, or an error code indicating a problem with the main module itself, and not with the synchronous line. The second line displayed reflects the status of the synchronous line port 0. It will either reflect a good operating status of 0000.0001 or an appropriate error message as indicated in Table 19.

If two synchronous lines are supported, than 3 lines are displayed. Again the first or top line is the common module information line, and its error field is divided into two halves by the decimal point. This information will either reflect the operating status of the synchronous lines, or an error code indicating a problem with the main module itself, and not a particular synchronous line. The second and third lines displayed, reflect the status of

Figure 34 System Exerciser Display Example of 2 Ports (Port 0 and Port 1) With 0 Errors (DSH32-S Subsystem Only)

the individual synchronous lines port 0 and port 1 respectively. They will either reflect a good operating status of 0000.0001 or an appropriate error message as indicated in Table 19.

When the left most digit of the common module information line's error field is a 0, then this information reflects the operating status of the synchronous line (port). The four digits to the left of the decimal point represent those synchronous lines which are currently running, and the four digits to the right of the decimal point represent those synchronous lines which have failed. Thus each half of the four digits will be coded as follows:

0000 = No ports
0001 = Only port 0
0010 = Only port 1
0011 = Port 0 and port 1

These codes are to be interpreted by which half or side they are found, as to whether the line(s) is running or not. If the common module information line's left most digit is non-zero, then the information contained in the error field represents an actual error code related to the module, and can be interpreted using the error chart in Table 19.

Figure 35 illustrates an example of a 1 port system which encountered a module error. The "??" to the far left indicates that what ever was found on that display line was dropped from the testing procedure. Thus the module was dropped due to a module error indicated by the left most digit (non-zero) in the error field. This error code can be read directly from the error code chart in Table 19 to identify its meaning. Note that the synchronous port 0 line still indicates that it was successful and that the error was not due to the module error.

Figure 35 System Exerciser Display Example of a Module Error on a System With 1 Port (Port 0) (DSH32-S Subsystem Only)

Figure 36 shows an example of a 2 port system in which one of the synchronous ports (port 0) failed. The common module information line's error field reads "0010.0001" which identifies that only port 1 is running (0010.), and that only port 0 failed (.0001). Note that port 0's display line also contains "??" which further indicates that synchronous line was dropped. The error field contains the error code 3000.000F which identifies the reason for its failure. Port 1 is still running as is indicated by its successful error code of 0000.0001.

Figure 36 System Exerciser Display Example of a 2 Port System (Port 0 and Port 1) With Error on Port 0 (DSH32-S Subsystem Only)

In addition, if all of the available synchronous lines fail, or an error occurs to the common module components, than the module will be dropped from the system exerciser. Once again this is indicated in the display by the "??" that appears to the far left of the common module information line. The reasons for the failures can be identified by the values contained in the error fields.

Table 19 lists the system exerciser error codes.

Table 19 Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
System Errors			
00xx			Basic system module running okay (top most line displayed)
	0001	0000	1 line (port 0) running, no lines failed
	0011	0000	2 lines (port 0 and port 1) running, no lines failed
	0000	0001	No lines running, 1 line (port 0) failed
	0000	0011	No lines running, 2 lines (port 0 and port 1) failed
	0001	0010	1 line (port 0) running, 1 line (port 1) failed
	0010	0001	1 line (port 1) running, 1 line (port 0) failed
0000	0000	0001	Successful running of an individual port line (2nd and/or 3rd lines displayed)
1xxx			Module system errors
	1000	0001	Unable to communicate with VSE monitor
		0002	Unable to communicate with VSE monitor during the delay routine
		0003	Unable to communicate with VSE monitor during the functional test

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
System Errors			
	1100	xxxx	Unable to attach ISR to device reason masks
		7C1C	Bad mode—The procedure was called from a program that was not running in kernal mode
		7C3C	Bad value—The device_variable argument is an array with more than 16 elements
		7C74	Device already connected– The device named in the ker$create_ device call is already connected to a DEVICE value
		7C9C	No access—An argument specified is not accessed to the calling program
		7CF0	No object—No free job object table entries available
		7CE4	No pool—No free system pool is available
		7CFC	No such device—The device name specified in a Ker$create_devices. Call cannot be found in the list of devices
		7D24	No system pages—No free system page table entries are available to map the I/O region
	1200	xxxx	Unable to map interrupt registers to physical memory mask
		7C1C	Bad mode—The physical address argument was specified by a program that was not running in kernal mode

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
System Errors			
		7C3C	Bad value—The virtual_address argument is not the job's address space
		7C9C	No access—An argument specified is not accessible to the calling program
		7CB4	No memory—No free pages of physical memory are available
		7D04	No virtual—No free contiguous virtual address space is available for process
	1300	xxxx	Unable to map tx/rx buffers to physical memory mask
		7C1C	Bad mode—The physical address argument was specified by a program that was not running in kernal mode
		7C3C	Bad value—The virtual_address argument is not in the job's address space
		7C9C	No access—An argument specified is not accessible to the calling program
		7CB4	No memory—No free pages of physical memory are available
		7D04	No virtual—No free contiguous virtual address space is available for the process
	1400	xxxx	Unable to free mapped tx/rx buffers to physical memory mask

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
System Errors			
		7C3C	Bad value—The virtual_address argument is not in the job's address space
	1500	xxxx	Unable to allocate device type memory
		7C1C	Bad mode—The physical address argument was specified by a program that was not running in kernal mode
		7C3C	Bad value—The virtual_address argument is not in the job's address space
		7C9C	No access—An argument specified is not accessible to the calling program
		7CB4	No memory—No free pages of physical memory are available
		7D04	No virtual—No free contiguous virtual address space is available for the process

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
Interrupt Service Routine			
2xxx			Interrupt service routine (Individual port errors)
	2001	0001	(System error) illegal port 1 interroupt
	2002	xxxx	DUSCC I RSRA error bit set xxxx = input register value
	2003	xxxx	DUSCC I transmit error bit set xxxx = input register value
	2004	xxxx	UDMA transmit current byte count error port 0 xxxx = input register value
	2005	xxxx	UDMA receive current byte count error port 0 xxxx = input register value
	2102	xxxx	DUSCC II RSRA error bit set = input register valus
	2103	xxxx	DUSCC I transmit error bit set xxxx = input register value
	2104	xxxx	UDMA transmit current byte count error port 1 xxxx = input register value
	2105	xxxx	UDMA receive current byte count error port 1 xxxx = input register value
	2200	xxxx	(System Error) illegal port number detected in ISR xxxx = port number which will be more than 2

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
Loopback Connector Errors			
3xxx			Loopback connector error (Individual port errors)
	3000	xxxx	Port 0 loopback connector mask
		000F	No cable
		000E	V.35 cable
		000D	RS-423/V.24 cable
		000C	X.21 cable
		000B	V36/RS-422
		0000	Loopback cable
	3100	xxxx	Port 1 loopback connector mask
		000F	No cable
		000E	V.35 cable
		000D	RS-423/V.24 cable
		000C	X.21 cable
		000B	V36/RS-422
		0000	Loopback cable

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
Testing Errors			
4xxx			Individual port errors during burst test
	4000	xxxx	Time-out occurred waiting for the device to set DONE bit indicating operation complete during functional mode test (port 0)

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
Testing Errors			
	4101	xxxx 7C54	Time-out occurred waiting for device to set DONE bit indicating operation complete during functional mode burst test (port 1)
	411Y	xxxx	(System error) kernal error while testing port(s) 0 and/or 1. (Y = test mode: 1 = Customer, 2 = field service, 3 = manufacturing)
		7C04	Bad count—The procedure call specified an incorrect number of arguments
		7C34	Bad type—An argument in the object list is not a type that can be waited for
		7C3C	Bad value—An argument in the object list is invalid or refers to a deleated object
		7C9C	No access—An argument specified is not accessible to the calling program
	412Y	xxxx 7C54	Time-out occurred waiting for the device to set DONE bit indicating operation complete during burst test of port(s) 0 and/or 1. (Y = test mode: 1 = customer, 2 = field service, 3 = manufacturing)

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
Testing Errors			
	413Y	xxxx	(System error) kernal error while testing port 0. (Y = test mode: 1 = customer, 2 = field service, 3 = manufacturing)
		7C04	Bad count—The procedure call specified an incorrect number of arguments

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
Testing Errors			
		7C34	Bad type—An argument in the object list is not a type that can be waited for
		7C3C	Bad value—An argument in the object list is invalid or refers to a deleted object
		7C9C	No access —An argument specified is not accessible to the calling program
	414Y	xxxx 7C54	Time-out occurred waiting for device to set DONE bit indicating operation complete during burst test for port 0. (Y = test mode: 1 = customer, 2 = field service, 3 = manufacturing)
	415Y	xxxx	(System error) kernal error while testing port 1. (Y = test mode: 1 = Customer, 2 = field service, 3 = manufacturing)
		7C04	Bad count—The procedure call specified an incorrect number of arguments
		7C34	Bad type—An argument in the object list is not a type that can be waited for

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
Testing Errors			
		7C3C	Bad value—An argument in the object list is invalid or refers to a deleated object
		7C9C	No access—An argument specified is not accessible to the calling program

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
Testing Errors			
	416Y	xxxx 7C54	Time-out occurred waiting for the device to set DONE bit indicating operation complete during burst test for port 1. (Y = test mode: 1 = customer, 2 = field service, 3 = manufacturing)
	417Y	xxxx	(System error) kernal error while testing port 0 and 1. (Y = test mode: 1 = customer, 2 = field service, 3 = manufacturing)
		7C04	Bad count—The procedure call specified an incorrect number of arguments
		7C34	Bad type—An argument in the object list is not a type that can be waited for
		7C3C	Bad value—An argument in the object list is invalid or refers to a deleted object
		7C9C	No access —An argument specified is not accessible to the calling program
	418Y	xxxx 7C54	Time-out occurred waiting for device to set DONE bit indicating operation complete during burst test for port 0. (Y = test mode: 1 = customer, 2 = field service, 3 = manufacturing)
	419Y	xxxx 7C54	Time-out occurred waiting for device to set DONE bit indicating operation complete during burst test for port 1. (Y = test mode: 1 = customer, 2 = field service, 3 = manufacturing)

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
Memory Errors			
5xxx			Individual port memory errors
	50yy	xxxx	Unable to initialize port 0 tx buffer memory with a 0 at address 3900.xxxx with yy + 1 memory errors encountered
	51yy	xxxx	Unable to initialize port 1 tx buffer memory with a 0 at address 3900.xxxx with yy + 1 memory errors encountered
	52yy	xxxx	Unable to write pattern byte to port 0 tx buffer memory at address 3900.xxxx with yy + 1 memory errors encountered
	53yy	xxxx	Unable to write pattern byte to port 1 tx buffer memory at address 3900.xxxx with yy + 1 memory errors encountered
	54yy	xxxx	Unable to initialize port 0 rx buffer memory with a 0 at address 3900.xxxx with yy + 1 memory errors encountered
	55yy	xxxx	Unable to initialize port 1 rx buffer memory with a 0 at address 3900.xxxx with yy + 1 memory errors encountered
	56yy	xxxx	Comparsion of transmit and receive buffer for port 0 did not match at address 3900.xxxx with yy + 1 differences found
	57yy	xxxx	Comparsion of transmit and receive buffer for port 1 did not match at address 3900.xxxx with yy + 1 differences found

Table 19 (Cont.) Exerciser Error Codes for DSH32-S

Status Group Code	Status Codes	Error Codes	Diagnostic Message Description
Memory Errors			
6xxx			SYNC RAM longword test errors
	6000	xxxx	Unable to allocate memory 32 Kbytes of SYNC RAM space
	6100	xxxx	Unable to free 32 Kbytes of allocated SYNC RAM space
	6200	xxxx	SYNC memory longword compare error detected at address equal to 3900.8000 + offset xxxx

5.4 Option Diagnostic ROM

The option diagnostic ROM for the DSH32 module resides in the addressing range 2014.0000 - 2017.FFFF (hexadecimal). The option diagnostic ROM must be version 1.0 or higher.

5.5 Base System ROM

The base system ROM must be version 1.2 or higher.