DL11
asynchronous
line interface
engineering drawings

digital equipment corporation · maynard, massachusetts

DRAWING DIRECTORY

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

THIS IS PRINT SET

CUSTOMER PRINT SET INDEX

SEQUENCE

PRINT SET #1

DRAWING DIRECTORY	B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE (PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	E-CS-M78ØØ-YA-1
CABLE ASSEMBLY (KL8/E)	D-IA-7008360-Ø-Ø
SOFTWARE LIST	A-SL-DL11-Ø-4
ACCESSORY LIST	A-AL-DL11-Ø-5
INSTALLATION PROCEDURE	A-SP-DL11-Ø-2

PRINT SET #2

DRAWING DIRECTORY	B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE (PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	E-CS-M78ØØ-Ø-1
CABLE, MODEM BCØ5C	D-UA-BCØ5C-Ø-Ø
FILTER NETWORK	B-CS-G8ØØ-Ø-1
MODEM TEST CONN	D-CS-H315-Ø-1
SOFTWARE LIST	A-SL-DL11-Ø-4
ACCESSORY LIST	A-AL-DL11-Ø-5
INSTALLATION PROCEDURE	A-SP-DL11-Ø-2

SEQUENCE

PRINT SET #3

DRAWING DIRECTORY	B-DD-DL11-0
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-0-0
ASYNCHRONOUS LINE INTERFACE (PL)	A-PL-DL11-0-0
ASYNCHRONOUS LINE INTERFACE	E-CS-M7800-0-1
CABLE, MODEM BC05C	D-UA-BC05C-0-0
CABLE ASSEMBLY (KL8/E)	D-IA-7008360-0-0
MODEM TEST CONN.	D-CS-H315-0-1
INSTALLATION PROCEDURE	A-SP-DL11-Ø-2

UNIT VARIATIONS

VARIATION	TITLE	DL11-1	DL11-2
DL11-A	ASYNC LINE INTERFACE, CURRENT LOOP	1	0
DL11-B	ASYNC LINE INTERFACE, EIA	0	1
DL11-C	ASYNC LINE INTERFACE, CURRENT LOOP	1	0
DL11-D	ASYNC LINE INTERFACE, EIA	0	1
DL11-E	ASYNC LINE INTERFACE, DATA SET	0	1

PRINT SET TYPE

REVISIONS

REV	CHG. NO.	
A	DL11-C0001	P. JANSON
B	DL11-00002	P. JANSON
C	DL11-00003	JANSON
D	DL11-00004	JANSON
E	DL11-00005	L. CONDON
F	DL11-00006	CONDON
H	DL11-00007	CONDON

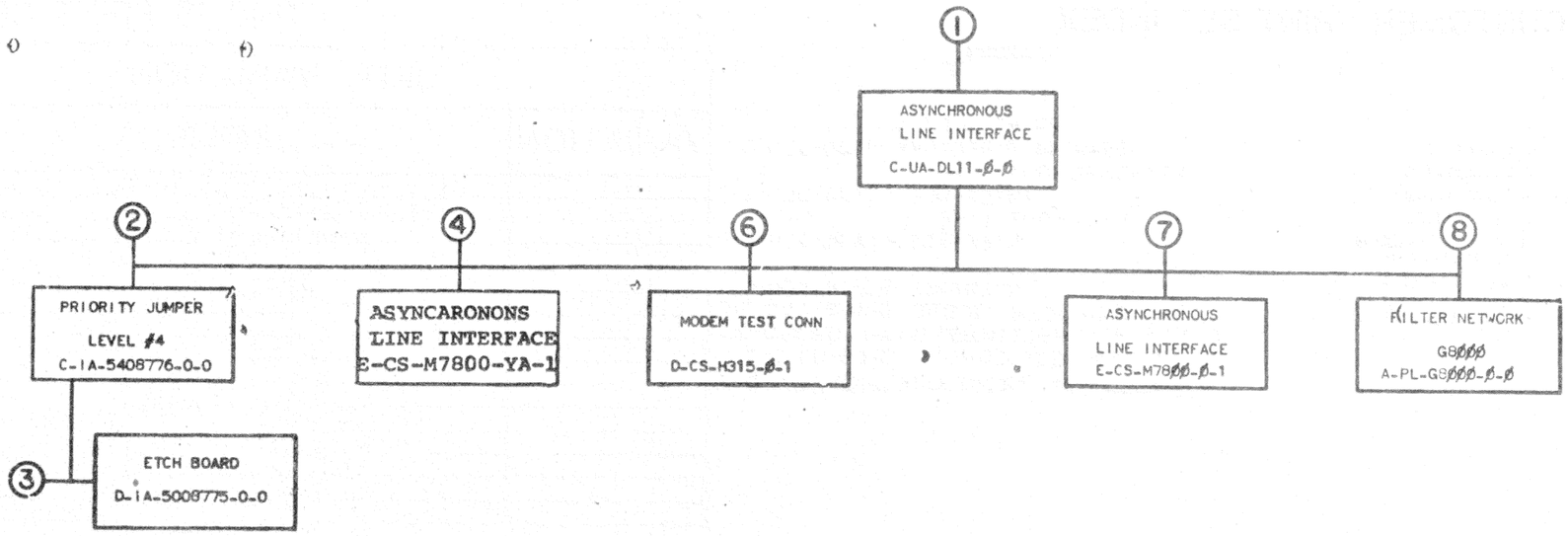
USED ON OPTION/MODEL

DRN.	DATE 4-25-72
CHK'D.	DATE 5/9/72
PROJ. ENG.	DATE 5/11/72
PROD.	DATE 5-15-72
RELEASED	DATE

TITLE: ASYNCHRONOUS LINE INTERFACE

SIZE	CODE	NUMBER	REV
B	DD	DL11-Ø	H

SHEET 1 OF 3 DIST G



TITLE	SHEET	SIZE	CODE	NUMBER	REV
ASYNCHRONOUS LINE INTERFACE	2 OF 3	B	DD	DL11-Ø	H

ELECTRICAL

CUSTOMER PRINT SET DLI1-1	DLI1-2	DLI1-3	DEPOT SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
X	X	X		1.	C-UA-DL11-Ø-Ø	D	1	ASYNCHRONOUS LINE INTERFACE	
X	X	X			A-PL-DL11-Ø-Ø	C	1	ASYNCHRONOUS LINE INTERFACE (PL)	
	X	X			D-UA-BCØ5C-Ø-Ø	#	1	CABEE MODEM BCØ5C	
X		X			D-IA-7008360-0-0	#	1	CABLE, ASSEMBLY (KL8/E)	
					A-SP-DL11-Ø-1	*	11	ENGINEERING SPECIFICATION	
X	X	X			A-SP-DL11-Ø-2	E	9	INSTALLATION PROCEDURE	
					A-SP-DL11-Ø-3	A	7	TEST PRODEDURE	
X	X				A-SL-DL11-Ø-4	*	1	SOFTWARE LIST	
X	X				A-PL-DL11-Ø-5	C	1	ACCESSORY LIST	
				2.	C-IA-5408776-0-0		1	PRIORITY JUMPER LEVEL #4	
					B-CS-5408776-0-1		1	CIRCUIT SCHEMATIC	
					K-CO-5408776-0-4		1	X-Y COORDINATE HOLE LOC	
					B-MH-5408776-0-6		1	MODULE ECO HISTORY	
				3.	C-AH-5408776-0-5		1	ASSY/DRILLING HOLE LAYOUT	
X				4	E-CS-M7800-YA-1	#	6	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M7800-YA-4		1	X-Y COORDINATE HOLE LOCATION	
					D-AH-M7800-YA-5		1	ASSY DRILLING HOLE LAYOUT	
					B-MH-M7800-YA-6		1	MODULE ECO HISTORY	
X	X			6.	D-CS-H315-Ø-1	#	1	MODEM TEST CONN	
					K-CO-H315-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-H315-Ø-5		1	ASSY DRILLING HOLE LAYOUT	
					B-MH-H315-Ø-6		1	MODULE ECO HISTORY	
X	X			7.	E-CS-M78ØØ-Ø-1	-#	7	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M78ØØ-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-M78ØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-M78ØØ-Ø-6		1	MODULE ECO HISTORY	
	X			8.	A-PL-G8ØØØØ-Ø-Ø		1	FILTER NETWORK	
X					B-CS-G8ØØØØ-Ø-1	#	1	CIRCUIT SCHEMATIC	
					K-CO-G8ØØØØ-Ø-4		1	X-Y COORINATE HOLE LOC	
					C-AH-G8ØØØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-G8ØØØØ-Ø-6		1	MODULE ECO HISTORY	

MECHANICAL

CUSTOMER PRINT SET DLI1-1	DLI1-2	DLI1-3	DEPOT SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
				1.	C-UA-DL11-Ø-Ø	D	1	ASYNCHRONOUS LINE INTERFACE	
					A-PL-DL11-Ø-Ø	C	1	ASYNCHRONOUS LINE INTERFACE (PL)	
					D-UA-BCØ5C-Ø-Ø		1	CABLE, MODEM BCØ5C	
					D-IA-7008360-0-0		1	CABLE ASSEMBLY (KL8/E)	
				2.	C-IA-5408776-0-0		1	PRIORITY JUMPER LEVEL #4	
					K-CO-5408776-0-4		1	X-Y COORDINATE HOLE LOC	
					B-MH-5408776-0-6		1	ASSY/DRILLING HOLE LAYOUT	
				3.	D-IA-5008775-0-0		1	ETCH BOARD	
					C-AH-5408776-0-5		1	ASSY/DRILLING HOLE LAYOUT	
				6.	D-CS-H315-Ø-1		1	MODEM TEST CONN	
					K-CO-H315-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-H315-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-H315-Ø-6		1	MODULE ECO HISTORY	
				7.	E-CS-M78ØØ-Ø-1		7	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M78ØØ-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-M78ØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-M78ØØ-Ø-6		1	MODULE ECO HISTORY	
				8.	A-PL-G8ØØØØ-Ø-Ø		1	FILTER NETWORK	
					K-CO-G8ØØØØ-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-G8ØØØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-G8ØØØØ-Ø-6		1	MODULE ECO HISTORY	

TITLE	SHEET	SIZE	CODE	NUMBER	REV
ASYNCHRONOUS LINE INTERFACE	3 OF 3	B	DD	DLII-Ø	H

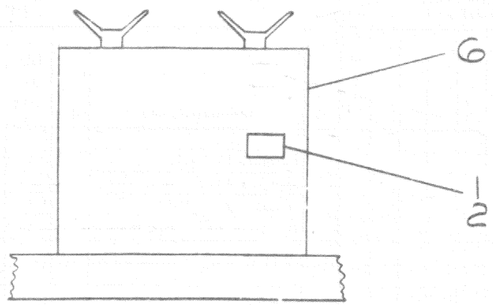
DRB 108

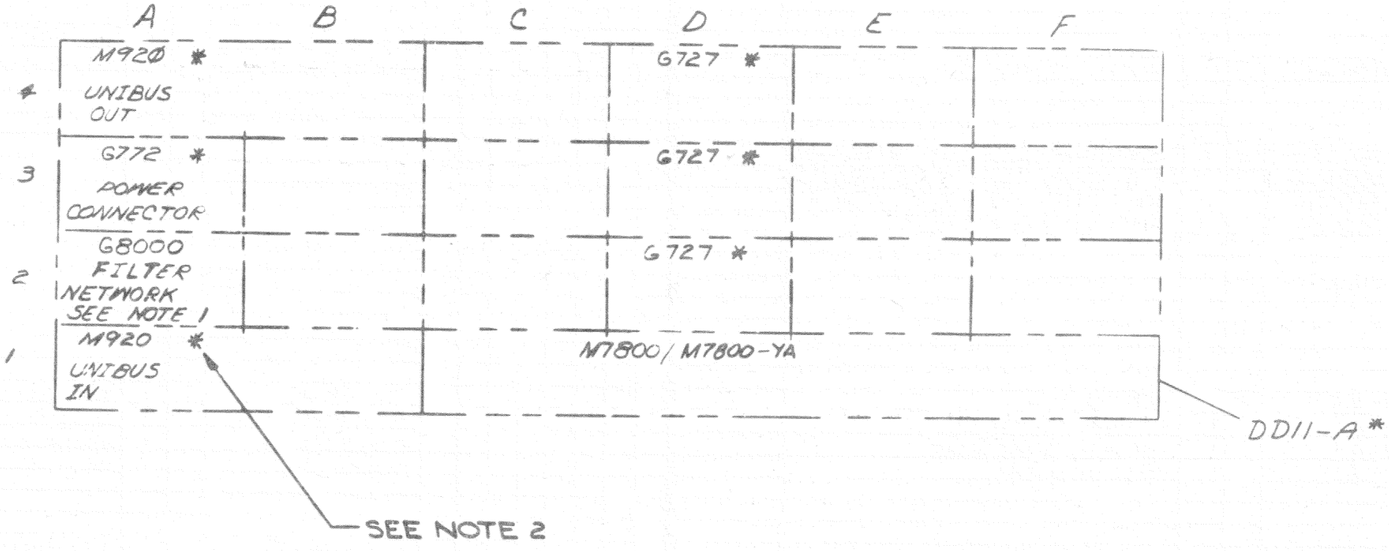
DEC 10-(2SB)-1063-2-4871

G

NOTES:

1. G 8000 IS REQUIRED ONLY IN PDP 11 SYSTEMS WHERE +15V IS NOT AVAILABLE. THE INSTALATION REQUIRES 2 WIRES TO BE ADDED.
   A03V2 - A02V2
   A02N2 - CXXU1
   WHERE (XX) IS THE SLOT NUMBER CONTAINING THE DL11.
2. ITEMS INDICATED WITH ASTERICK (*) ARE SHOWN FOR REFERENCE ONLY AND ARE NOT PART OF THIS UNIT.





REVISIONS											
CHK.	CHANGE NO.	REV.		CHK.	CHANGE NO.	REV.		CHK.	CHANGE NO.	REV.	
[illegible]	DL11-00001	A	[illegible] 2-18-72	[illegible]	DL11-00002	B	[illegible] 7-19-72	[illegible]	DL11-00005	C	[illegible] 10-5-72
[illegible] JANSON				[illegible] JANSON				L. CONDON			[illegible] 7-31-73
[illegible]	DL11-00006	D	[illegible] 4-11-73	CONDON			[illegible] 10-1-73				

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP-11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS: XXX - .005, XX - .02, X - .1; ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRN. [illegible]	DATE 7/10/72	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D [illegible]	DATE [illegible]	
ENG. [illegible]	DATE 5-11-72	TITLE: ASYNCHRONOUS LINE INTERFACE
PROJ. ENG. [illegible]	DATE 5-11-72	
PROD. [illegible]	DATE 5-15-72	
NEXT HIGHER ASSY. B-00-DL11-0		SIZE C, CODE UA, NUMBER DL11-0-0, REV. D
SCALE NONE		
SHEET / OF /		DIST. C

SIZE CODE C UA | NUMBER DL11-0-0 | REV. D

DEC FORM NO. DRC 100-A

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

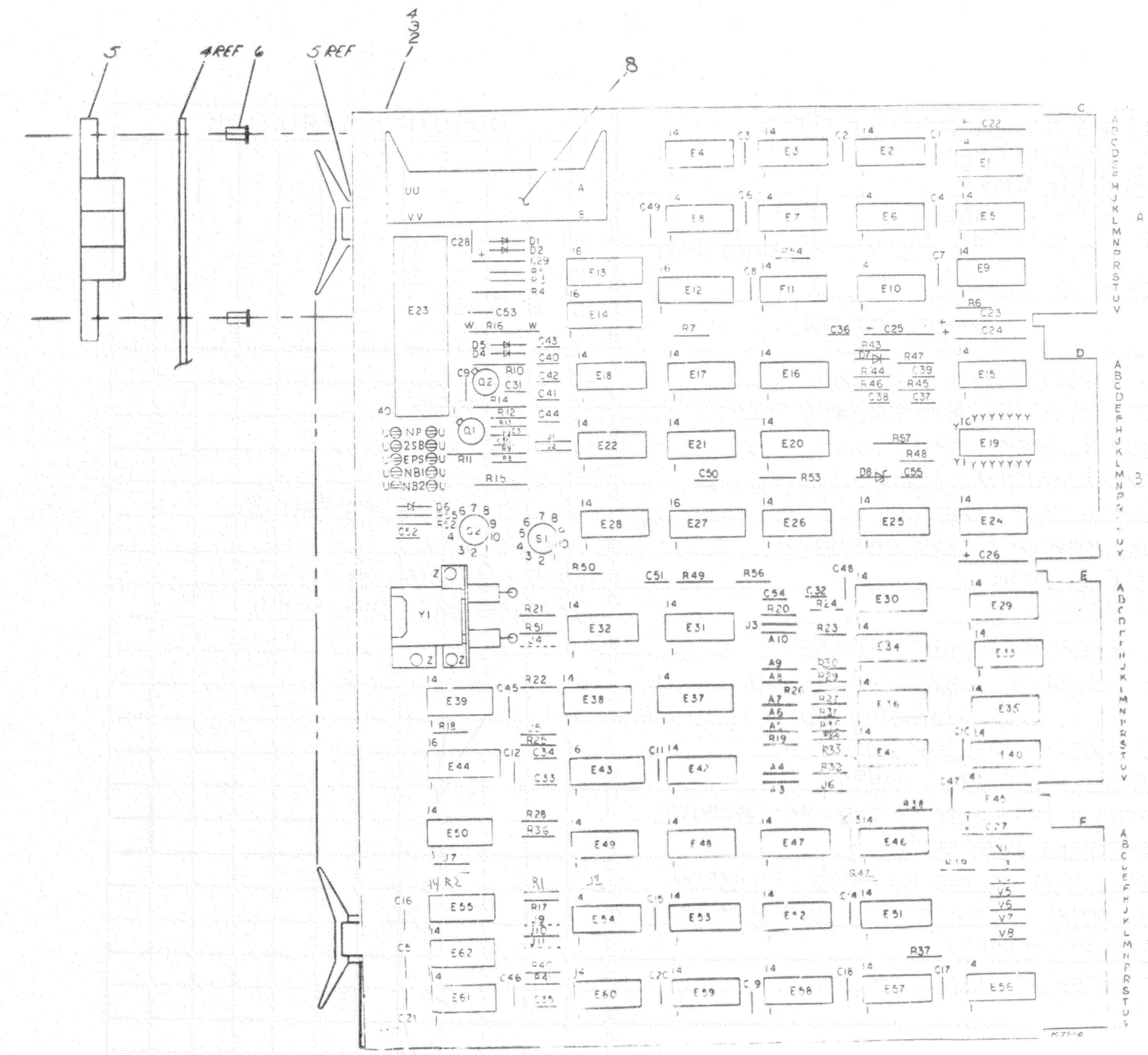
PARTS LIST

MADE BY M. PIERCE	CHECKED J. FERGUSON	SECTION 1
ENG [signature]	PROD [signature]	ISSUED SECT. 1
DATE 5/11/72	DATE 5/15/72	

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	
1	C-IA-5408776-0-0	PRIORITY JUMPER LEVEL #4	1	1	1	1	-	
2	C-IA-5408776-0-0	PRIORITY JUMPER LEVEL #5	-	-	-	-	1	
3	D-UA-BCØ5C-25	CABLE, MODEM BCØ5C	-	1	-	1	1	
4	D-IA-7008360-0-0	CABLE ASSEMBLY (KL8E)	1	-	1	-	-	
5	D-CS-H315-Ø-1	MODEM TEST CONNECTOR	-	-	-	-	A/R	See Note 2
6	E-CS-M7800-Ø-1	ASYNCHRONOUS LINE INTERFACE	-	1	-	1	1	
7	A-PL-G8ØØØ-Ø-Ø	FILTER NETWORK	-	A/R	-	A/R	A/R	See Note 1
8		CRYSTAL	A/R	A/R	A/R	A/R	A/R	See Note 3
9	E-CS-M7800-XA-1	ASYNCHRONOUS LINE INTERFACE	1	-	1	-	-	
	NOTES: 1.	G8000 IS REQUIRED ONLY IN PDP 11 SYSTEMS WHERE +15V IS NOT AVAILABLE. ONE PER DD11-A.						
	2.	ONE H315 PER PDP11 SYSTEM						
	3.	CRYSTAL FREQUENCY DEFINED BY CUSTOMER SPECIFIED BAUD RATE						
	4.	APPLY TAPE TO TOP SURFACES OF CRYSTAL AND MOUNTING BRACKETS TO INSULATE FROM ADJACENT MODULES.						
10	9008269	TRANSPARENT VINYL TAPE	A/R					

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV	ECO NO.
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø	A	PL	DL11-Ø-Ø	-	DTI-C 1005
	SHEET 1 OF 1	DIST	C			

DEC FORM DEC 16-(325)-1031-M870
DRA 110



NOTES:

1.) PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.

2.) JUMPERS TO BE USED AT CONNECTIONS A3-A10, J4-J6, J9-J10, V3-V8, AND [illegible]

3.) LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X).

4.) DEC 8640's WERE PHASED IN AS 380 REPLACEMENTS. ANY 380 FAILURES SHOULD BE REPLACED BY 8640's.

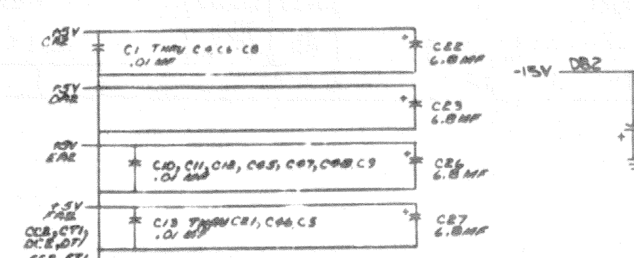
PIN NOMENCLATURE

MODULE	SYSTEM UNIT
A	C
B	D
C	E
D	F

PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	R3	RES 750Ω 1/4W 5%	1301401	67
1	R38	RES 390Ω 1/4W, 5%	1300309	66
1	D6	DIODE 1N746A	1104860	65
2	Q1, Q2	TRANSISTOR G534D	1503409-00	64
1	C53	CAP 100PF 100V 5% DIPPED MICA	1000016	63
1	C54	CAP 560PF 100V 5% DIPPED MICA	1000025	62
2	C50, C51	CAP .047MF CERAMIC	1009678	61
1	E24	IC DEC 74161	1910650	60
2	C34, C35	CAP 330PF 100V 5% DIPPED MICA	1000023	59
1	C32	CAP 470PF 100V 5% DIPPED MICA	1000024	58
1	C31	CAP 1000PF 100V 5% DIPPED MICA	10000[illegible]	57
27	[illegible]	CAP .01UF 100V 20% CERAMIC DISC	1001610	56
1	C49	CAP .47UF 35V 10% TANT	1005965	55
5	C22, C24, C25, C26, C27	CAP 6.8UF 35V 20% TANT	1000067	54
1	C12	CAP 15PF 100V 5% DIPPED MICA	10000[illegible]	53
2	R14, R15	RES 1.5K 1/4W 5%	1300394	52
5	R23, R25, R40, R52, R55	RES 1K 1/4W 5%	1300365	51
1	R41	RES 47Ω 1/4W 5%	1300202	50
1	R13	RES 68Ω 1/2W 10%	1300[illegible]	49
1	R5	RES 82Ω 1/4W 5%	1301477	48
1	R20	RES 100Ω 1/4W 5%	1300229	47
1	R11	RES 150Ω 1/4W 5%	1300230	46
1	R42	RES 180Ω 1/4W 5%	1301322	45
1	E53	RES 220Ω 1/4W 5%	1300271	44
5	D1-D5	DIODE [illegible]	11[illegible]	43
3	R[illegible], R13, R51	RES 270Ω 1/4W 5%	1300316	42
1	R4	RES 360Ω 1/2W 5%	1300338	41
3		NUT HEX #2-56	9006[illegible]	40
1	R16	RES 750Ω 1W 5%	1302385	39
26	R1, R2, R6, R7, R11-R[illegible], R26, R27-R33, R39, R47, R50, R[illegible], R54, R56	RES 10K 1/4W 5%	1300471	38
2	R9, R12	RES 1.5K 1/4W 5%	1300394	37
1	E23	IC DEC UART	[illegible]	36
4	E32, E35, E60, E62	IC DEC 74[illegible]	1905547	35
2	E36, E61	IC DEC 8242	1909712	34
3	E[illegible], E43, E57	IC DEC 7408	1910135	33
3		SCR PHIL HD PAN #2-56X 25[illegible]	9006[illegible]	32
2	E20, E26	IC DEC [illegible]	1909[illegible]	31
11	E1, E2, E3, E7-E9, E11, E30, E47, E54, E56	IC DEC 8881	1909705	30
2		AUGAT 8000 RS-1	1202812	29
1	E49	IC DEC 74123	1910436	28
3	E[illegible], E37, E42	IC DEC 74H74	1909687	27
3	E22, E59, E58	IC DEC 7400	1905575	26
1	E10	IC DEC 7413	1909989	25
2	E50, E53	IC DEC 7402	1909004	24
8	E5, E9, E33, E35, E40, E45, E46, E28	IC DEC 8640	1911464	23
1	E12	IC DEC 74153	1909937	22
1	E60	IC DEC 74H04	1909931	21
1	E25	IC DEC 7492	1909033	20
4	E6, E17, E38, E39	IC DEC 7404	1909686	19
1	E24	IC DEC 7493	1909056	18
1	E34	IC DEC 7410	1905576	17
1	E29	IC DEC 314	1909704	16
1	E31	IC DEC 7442	1910046	15
1	E44	IC DEC 8271	1904215	14
2	E13, E14	IC DEC 74175	1910651	13
1		BRACKET, CRYSTAL HOLDER	5302825	12
1		BRACKET, CRYSTAL HOLDER	5303154	11
1	E19	IC SOCKET	1209838	10
2	S1, S2	SWITCH, SINGLE POLE, 10 POS	1210042-1	9
1		40 PIN CONNECTOR BERG	1209941	8
10		SPLIT LUGS	9006735	7
8		EYELET #G54-7 E.B. STIMPSON	9006732	6
4		HANDLE, FLIP-CHIP, MAGENTA	9008337-06	5
1		ETCHED CIRCUIT BOARD	5009978	4
REF		MODULE ECO HISTORY	[illegible]-M7800-[illegible]	3
REF		ASSY/DRILLING HOLE LAYOUT	[illegible]-AH-M7800-[illegible]-5	2
REF		X-Y COORDINATE HOLE	[illegible]-M7800-[illegible]-4	1

ETCH BOARD REV F



IC PIN LOCATIONS

IC TYPE	GND	+5V	+V	-12V
DEC 74161	8	16	—	—
DEC UART	3	1	—	2
DEC 74175	8	16	—	—
DEC 8271	8	16	—	—
DEC 7442	8	16	—	—
DEC 314	1	8	—	—
DEC 7493	10	5	—	—
DEC 7492	10	5	—	—
DEC 74153	8	16	—	—
DEC 8640	1	8	—	—
DEC 7490	10	5	—	—
DEC 74123	8	16	—	—

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE.

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.
G534D	MPS6653
1N746A	1N4[illegible]A
D664	1N3606

DIGITAL EQUIPMENT CORPORATION

TITLE: ASYNCHRONOUS LINE INTERFACE

E CS M7800-YA-1

DL-2 BINIT H
DL1 BUS INIT L
DL-2 RINIT L

DL-2 BDB7 H
DL-2 BDB6 H
DL-2 BDB5 H
DL-2 BDB4 H
DL-2 BDB3 H
DL-2 BDB2 H
DL-2 BDB1 H
DL-2 BDB0 H

DL-4 RD7 H
DL-4 RD6 H
DL-4 RD5 H
DL-4 RD4 H
DL-4 RD3 H
DL-4 RD2 H
DL-4 RD1 H
DL-4 RD0 H
DL-5 RBUF TO BUS H

DL-4 XMIT READY H
DL-4 XMIT INT ENB (1)H
DL-4 BREAK (1)H
DL-5 XCSR TO BUS H

DL-4 RCVR DONE H
DL-4 RCVR INT ENB (1)H
DL-4 DATASET INT ENB (1)H
DL-4 SEC XMIT (1)H (K)
DL-4 REQ TO SEND (1)H (M)
DL-4 PARITY (1)H
DL-4 DATA TERMINAL READY (1)H (J)

CP2 BUS DB7 L
CV2 BUS DB6 L
CP2 BUS DB5 L
CN2 BUS DB4 L
CT2 BUS DB3 L
CU2 BUS DB2 L
CR2 BUS DB1 L
CS2 BUS DB0 L

+5V
R1 1K
J6
DL-5 RBUF TO BUS L
DL-4 OR ERR H
DL-4 FR ERR H
DL-4 P ERR H

+5V
J7
R2 1K
DL-6 RCSR TO BUS L

ERROR H
DL-6 RCBR TO BUS H
DL-4 RCVR BUSY (1)H

CD2 BUS D15 L
CE2 BUS D14 L
CF2 BUS D13 L
CH2 BUS D12 L
CM1 BUS D11 L
CJ2 BUS D10 L

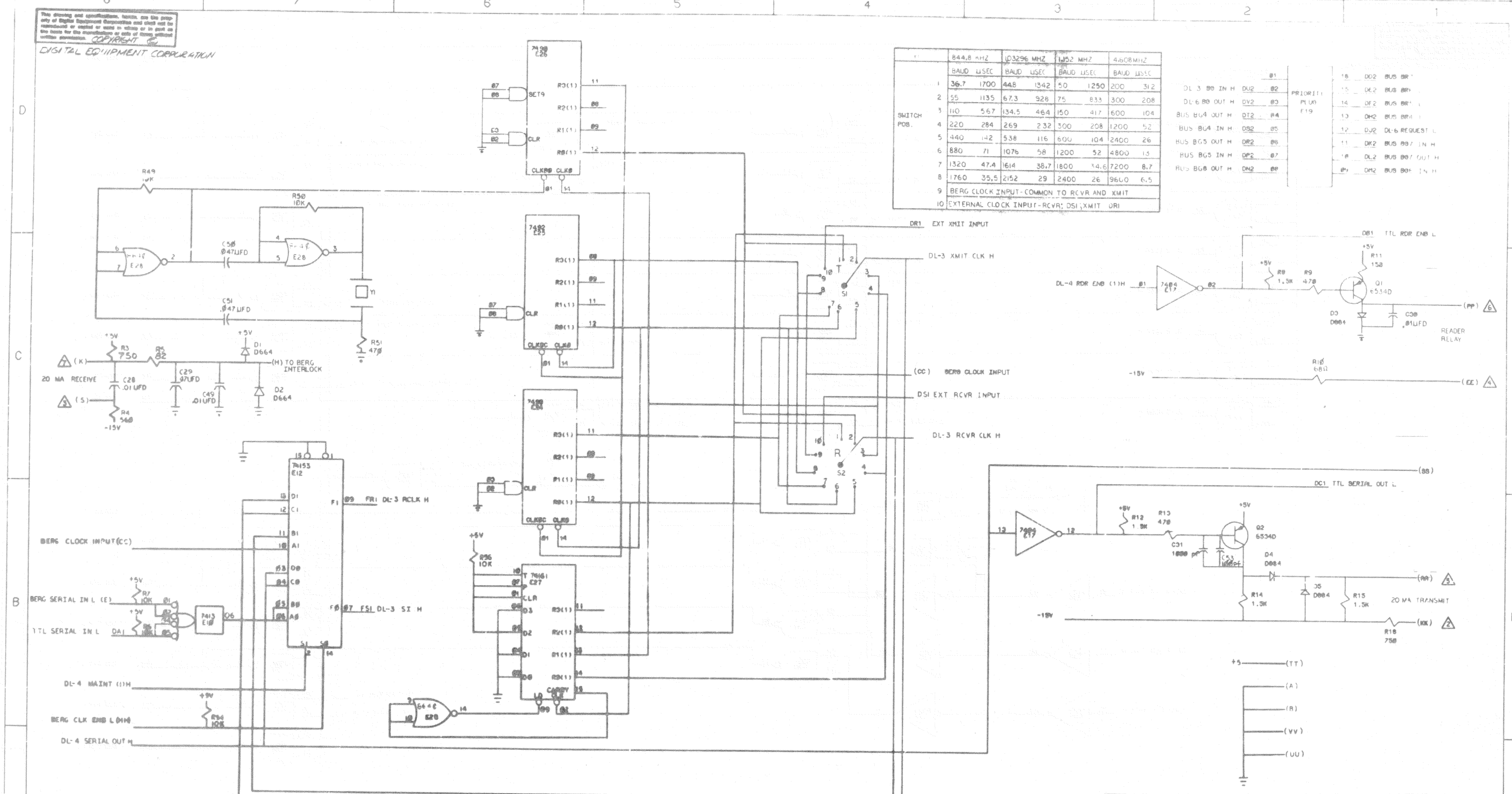
QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

DL11

EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (BUS RECEIVERS & DRIVERS) DL-2

D | CS | M7800-YA-1 | REV. D



	844.8 KHZ		1.03296 MHZ		1.152 MHZ		4.608 MHZ	
SWITCH POS.	BAUD	μSEC	BAUD	μSEC	BAUD	μSEC	BAUD	μSEC
1	36.7	1700	44.8	1342	50	1250	200	312
2	55	1135	67.3	928	75	833	300	208
3	110	567	134.5	464	150	417	600	104
4	220	284	269	232	300	208	1200	52
5	440	142	538	116	600	104	2400	26
6	880	71	1076	58	1200	52	4800	13
7	1320	47.4	1614	38.7	1800	34.6	7200	8.7
8	1760	35.5	2152	29	2400	26	9600	6.5
9	BERG CLOCK INPUT - COMMON TO RCVR AND XMIT							
10	EXTERNAL CLOCK INPUT - RCVR; DSI ; XMIT DRI							

NOTES:
1. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X)
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE [illegible] CABLE. THIS CABLE ALSO CONNECTS BERG PINS H TO E.

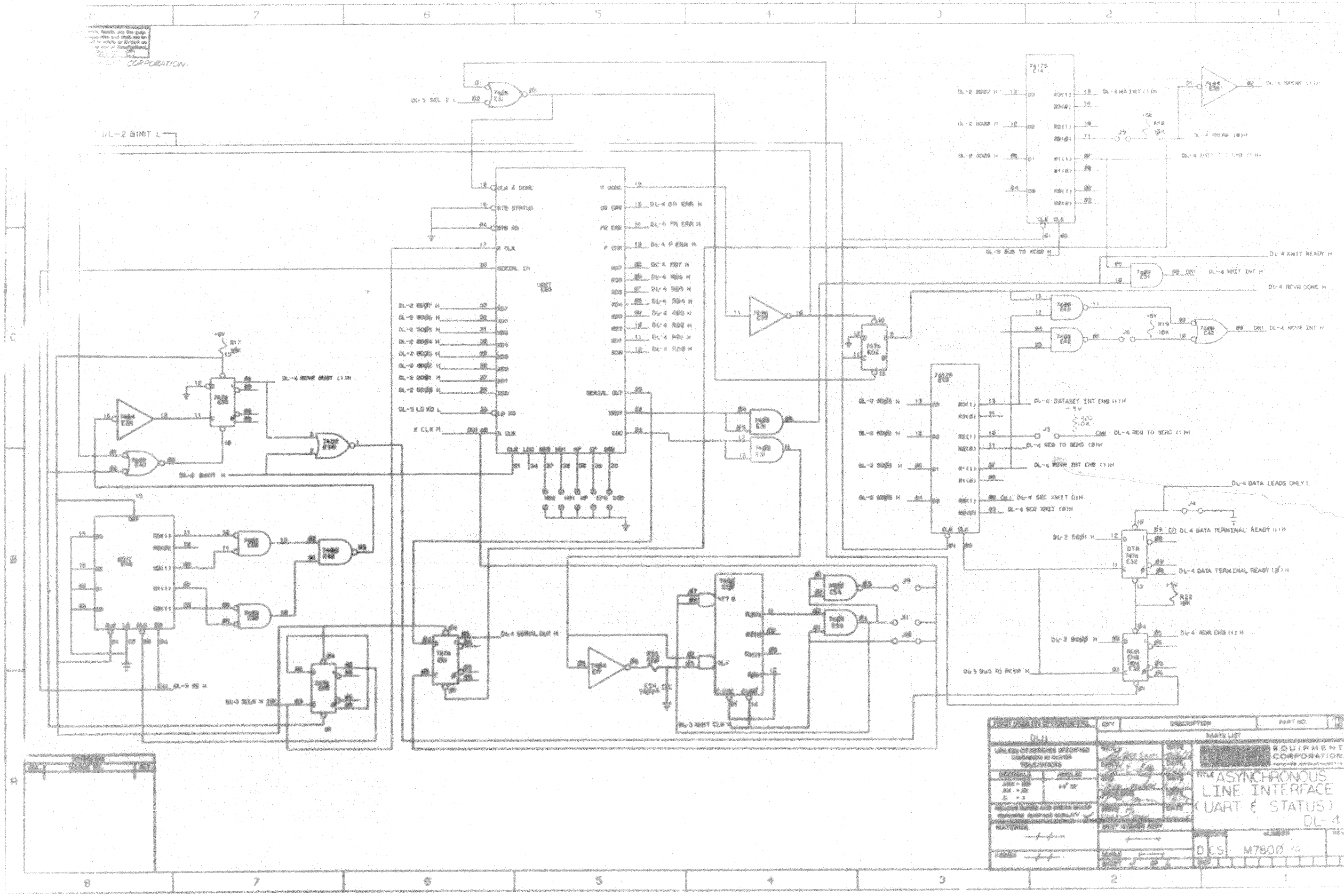
DL11

EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (CLOCK & CURRENT LOOPS) DL-3

D CS M7800-YA-1

SHEET 3 OF 6

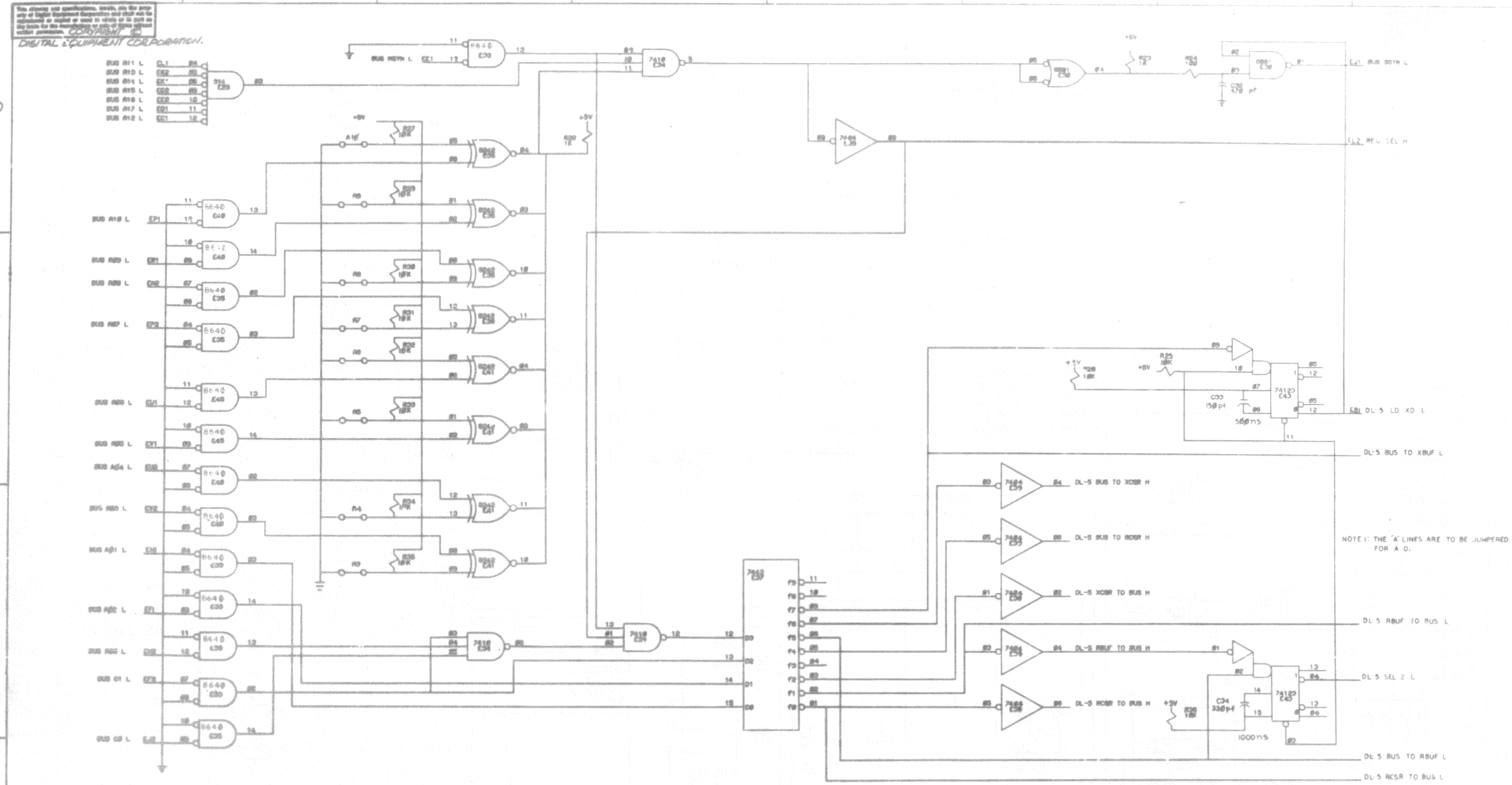


FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DL11		PARTS LIST		

EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (UART & STATUS) DL-4

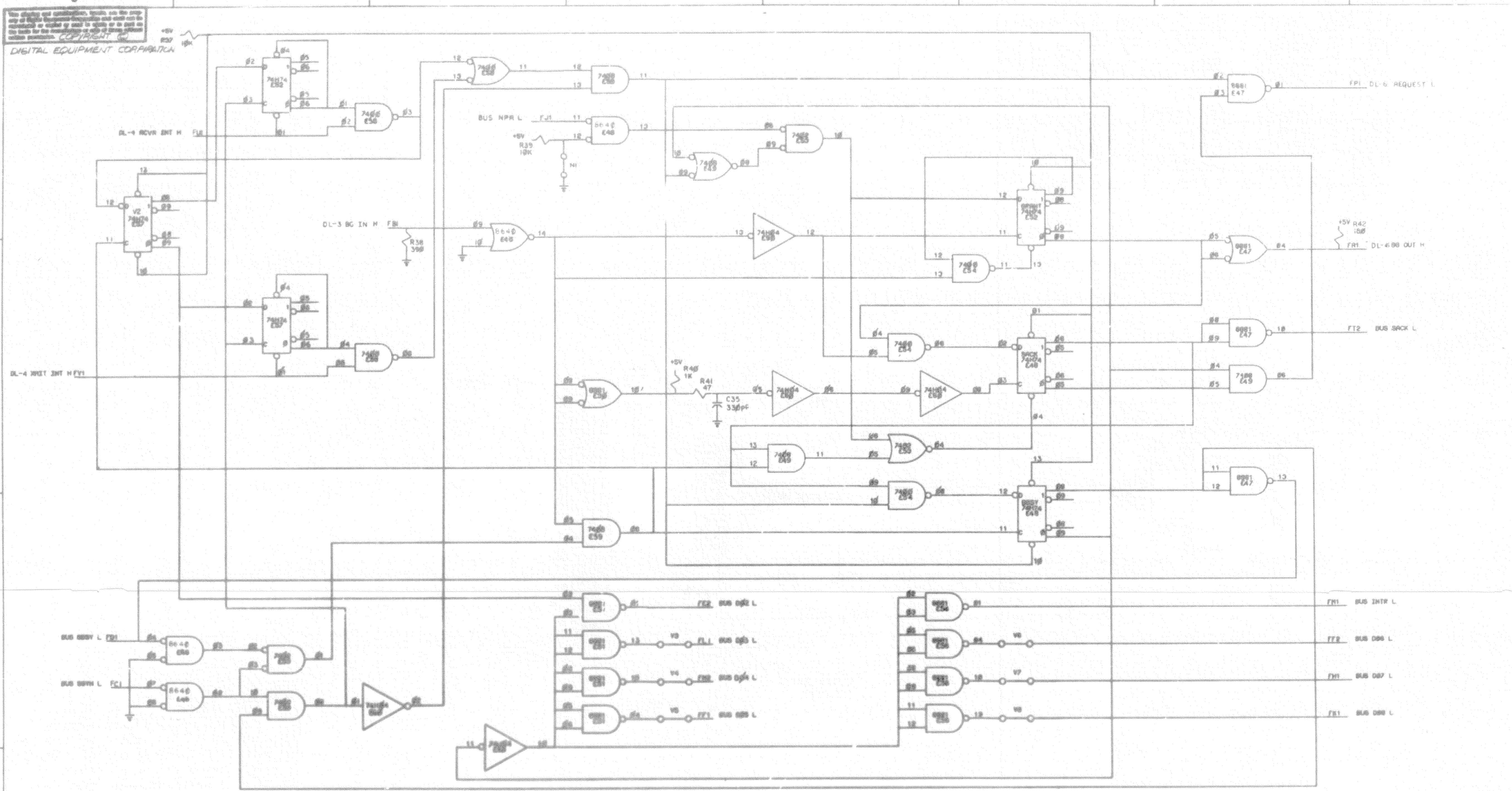
D CS M7800 YA



NOTE 1: THE 'A' LINES ARE TO BE JUMPERED FOR A 0.

FIRST USED ON OPTION/MODEL	DL11
TITLE	ASYNCHRONOUS LINE INTERFACE (ADDRESS SELECTION) DL-5
SIZE	D
CODE	CS
NUMBER	M7800
SHEET	5 OF 6

DIGITAL EQUIPMENT CORPORATION



NOTE: THE "V" LINES ARE TO BE JUMPERED FOR A L

REVISIONS

CHK.	CHANGE NO.	REV

FIRST USED ON OPTION/MODEL	DL11
QTY. / DESCRIPTION / PART NO. / ITEM NO.	PARTS LIST
MATERIAL	—
FINISH	—

DIGITAL EQUIPMENT CORPORATION

TITLE: ASYNCHRONOUS LINE INTERFACE (INTERRUPT CONTROL) DL-6

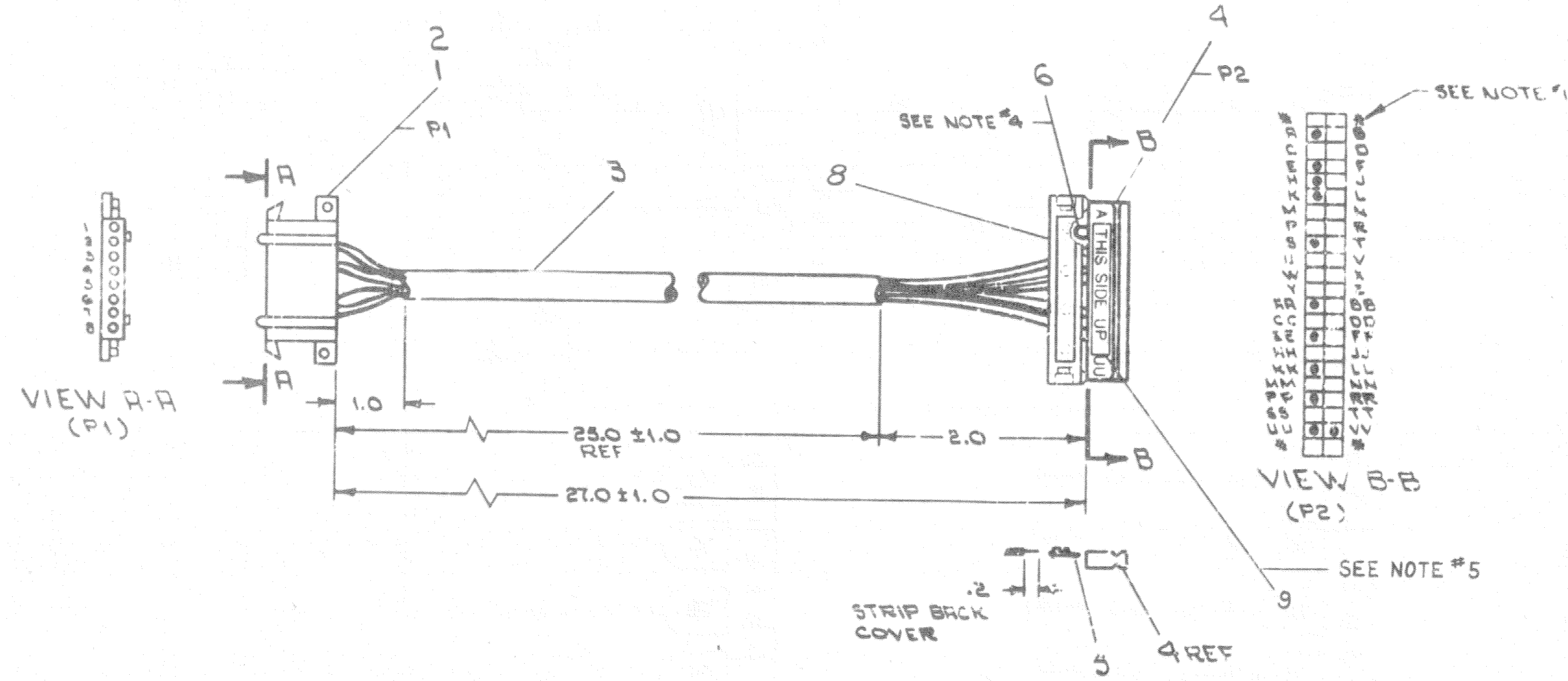
D CS M7800-YA-1

SHEET 6 OF 6

WIRE TABLE

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	PAIR NO.	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH
3	22	BLK	1	P1-2	2	P2-KK	5
3		RED		P1-3	2	P2-S	
3,7		SHIELD		SEE NOTE #2	—	P2-R(NOTE #3)	
3		BLK	2	P1-4	2	P2-EE	
3		WHT		P1-5	2	P2-RR	
3,7		SHIELD		SEE NOTE #2	—	P2-UU(NOTE #3)	
3		BLK	3	P1-6	2	P2-PP	
3		GRN		P1-7	2	P2-K	
3,7		SHIELD		SEE NOTE #2	—	P2-VV(NOTE #3)	
6	22	BLK	—	P2-E	5	P2-H	5

NOTES:
1. ASTERISKS INDICATE CAVITIES NOT USED OR DESIGNATED BY LETTERS.
2. DRAIN WIRES TO BE CUT BACK TO OUTER INSULATION ON P1 END OF CABLE ONLY. SHIELDS TO BE CUT BACK TO OUTER INSULATION ON BOTH ENDS OF CABLES.
3. DRAIN WIRES ON P2 END OF CABLE TO BE EACH ENCLOSED WITH ITEM #7 (TUBING) FROM END OF CABLE JACKET TO POINT WHERE THEY ENTER P2 CONNECTOR.
4. ITEM #6 (WIRE) TO BE APPROXIMATELY ONE (1) INCH LONG.
5. PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #4 (BERG HOUSING) AS SHOWN.



QTY	DESCRIPTION	PART NO	ITEM NO
1	LABEL, THIS SIDE UP	361567	9
1	STRAIN RELIEF	1211166	8
A/R	TUB. #18 TEF. THINWALL NAT	9107278-11	7
A/R	WIRE #22 AWG STRD TEF BLK	9107350-00	6
11	SOCKET, CRIMP #47216	1210089-07	5
1	HOUSING BERG #65043-15	1210918-15	4
A/R	CABLE, BELDEN #8777-3PR SHLD	9107723-0	3
6	CONTACT MATE-N-LOCK (FEMALE)	1209379	2
1	CONN. MATE-N-LOCK (FEMALE)	1209340 00	1

PARTS LIST

FIRST USED ON OPTION/MODEL: PDP 8E

DO NOT SCALE DRAWING. UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES ANGLES ± 0°30'. FINAL SURFACE QUALITY. REMOVE BURRS AND BREAK SHARP CORNERS.

MATERIAL: SEE PARTS LIST

FINISH:

DRN DATE 1APR 71 | CHK'D DATE 4-8-71 | ENG DATE 4-4-71 | PROJ ENG DATE 4-1-71 | PROD DATE

NEXT HIGHER ASSY: A ML KL8 E-0

SCALE: NONE | SHEET OF

digital EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: CABLE ASSEMBLY (KL8E)

SIZE D | CODE IA | NUMBER 7008360-0-0 | REV E

CHANGE HISTORY: KL8E-00006 (REV B) F. CLARK; ECO 7008360-00001 (REV C) B. REGAN 10-29-73; ECO 7008360-00002 (REV D) REGAN; ECO 7008360-(XXX) (REV E)

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

SOFTWARE LIST

MADE BY Pellegrini	CHECKED J. Jonson	SECTION
DATE 8/29/72	DATE 8-31-72	
ENG K. Janson	PROD J. Mitte	ISSUED SECT.
DATE 8/29/72	DATE 8-31-72	

LEGEND
- D DOCUMENT
- DN DOCUMENT CHANGE NOTICE
- PA PAPER TAPE ASCII
- PB PAPER TAPE BINARY
- PM PAPER TAPE READ-IN-MODE

ITEM NO	DWG NO. / PART NO.	DESCRIPTION	QUANTITY VARIATION: DL11-A	DL11-B	DL11-C	DL11-D	DL11-E			KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
1	LIBKIT-11-KL11-04	KL11 MAINDEC	1	1	0	0	0				
2	LIBKIT-11-DL11C-A-K	DL11 MAINDEC	0	0	1	1	0				
3	LIBKIT-11-DL11E-A-K	DL11 MAINDEC	0	0	0	0	1				

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV	FCO NO
DL11 SOFTWARE LIST	SHEET 1 OF 1	A	SL	DL11-0-4		
		DIST.				

DEC FORM NO DEC-16-(327)-1049-X471
DRA 120

DIGITAL EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

ACCESSORY LIST

MADE BY [illegible]	CHECKED [illegible]	SECTION
DATE [illegible]	DATE 8 8 72	
ENG [illegible]	PROD [illegible]	ISSUED SECT.
DATE [illegible]	DATE 7-7-72	

LEGEND

D DOCUMENT
DN DOCUMENT CHANGE NOTICE
PA PAPER TAPE ASCII
PB PAPER TAPE BINARY
PM PAPER TAPE READ-IN-MODE

ITEM NO	DWG NO. / PART NO	DESCRIPTION	QUANTITY / VARIATION							KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
			DL11-A	DL11-B	DL11-C	DL11-D	DL11-E				
1	M7800	SYNCHRONOUS LINE INTERFACE (EIA)	-	1	-	1	1				
2	6P000	FILTER NETWORK	0	A/R	0	A/R	A/R				
3	M7801-YA	ASYNCHRONOUS LINE INTERFACE (CURRENT LOOP)	1	0	1	0	0				
4	54[illegible]770	PRIORITY JUMPER LEVEL #4	1	1	1	1	1				
5	BC05[illegible]25	4 WIRE CABLE	0	1	0	1	1				
6	7[illegible]0836	TTY CABLE	1	0	1	0	0				
7		CRYSTAL	1	1	1	1	1				
8		DL11 ENGINEERING DRAWING	1	1	1	1	1				
9	DEC-11-HDLAA-A-D	DL11 ASYNCHRONOUS LINE INTERFACE MANUAL	1	1	1	1	1				
10	LIBKIT 11 KL11-04	KL11 MAINDEC	1	1	0	0	0				
11	LIBKIT-11-DL11C-A-K	DL11 MAINDEC	0	0	1	1	0				
12	LIBKIT-11 DL11E-A-K	DL11 MAINDEC	0	0	0	0	1				
13	M[illegible]5	MODEM TEST CONNECTOR	0	0	0	0	A/R				

NOTES:
1. 58000 IS REQUIRED ONLY IN PDP-11 SYSTEMS WHERE +18V IS NOT AVAILABLE. ONE PER BD11-A.
2. CRYSTAL FREQUENCY DEFINED BY CUSTOMER SPECIFIED BAUD RATE.
3. ONE M[illegible]5 PER PDP11 SYSTEM
4. INSURE THAT TRANSPARENT VINYL TAPE HAS BEEN APPLIED TO THE TOP SURFACE OF THE CRYSTAL AND MOUNTING BRACKET.

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV	FCO NO
DL11 CHECK LIST	SHEET 1 OF 1	A	AL	DL11-0 5	C	DL11-00005
		DIST				

DEC-11-[illegible]5-NL72 DRAWING

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

DATE 6-21-72

TITLE DL11 INSTALLATION PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	CHANGE PER ECO	DL11-4	JANSON	3/73	P. Janson	4-73
D	CHANGE PER ECO	DL11-5	CONDON	7/73	[illegible]	[illegible]
E	CHANGE PER ECO	DL11-7	CONDON	8/74	[illegible]	[illegible]

ENG	APPD	SIZE	CODE	NUMBER	REV
[illegible]	[illegible]	A	[illegible]	[illegible]	E

DEC FORM NO DRA 107A

SHEET 1 OF 9

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

DL11 INSTALLATION PROCEDURE:

Installation of the M7800 module or its variation as a DL11-A through DL11-E option consists of the following preparations:

1. Jumper insertion/deletion for selection of operation mode (A, B, C, D, or E).
2. Register address assignment.
3. Vector address assignment.
4. Priority assignment.
5. Special NPR jumper insertion/deletion.
6. Selection of data format (data bits, stop bits, parity).
7. Selection of crystal for baud rate.
8. Installation of G8000 in systems where +10v is not available.
9. Filter capacitor selection for high baud rate current-loop.

A. OPERATION MODE

The following describes the jumpers associated with controlling the mode of operation (A,B,C,D, or E):

J1. Ties EIA driver to REQUEST-TO-SEND lead (pin 4) of dataset cable. IN for DL11-B,D, and E; does not affect DL11-A and C. Drawing DL-7.

J2. Ties EIA driver, normally used for the REQUEST-TO-SEND lead, to FORCE BUSY lead (pin 25) for use with Bell 103E. This is a customer option. If not specified, jumper is OUT for all DL11's. Drawing DL-7.

J3. When inserted, allows REQUEST-TO-SEND lead (pin 4) to be controlled by bit 2 of the receiver status register. OUT for DL11-B and D; IN for DL11-E; does not affect DL11-A and C. Drawing DL-4.

J4. When inserted, forces "DATA LEADS ONLY" mode of EIA operation. Turns DATA TERMINAL READY (pin 20) and REQUEST-TO-SEND (pin 4) on. IN for DL11-B and D; OUT for DL11-E; does not affect DL11-A and C. Drawing DL-4.

J5. When inserted, allows the BREAK bit to function. OUT for DL11-A and B; IN for DL11-C, D, and E. Drawing DL-4.

J6. When inserted, allows DSET INT to cause interrupts. OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-4.

J7. When inserted, allows dataset control bits to be read as part of the receiver status register.

SIZE	CODE	NUMBER	REV
A	SP	[illegible]	E

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

SHEET [illegible] OF [illegible]

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

J7. (con't)

OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-2.

J8. When inserted, allows error bits to be read as part of the receiver data register. OUT for DL11-A and B; IN for DL11-C,D and E. Drawing DL-2.

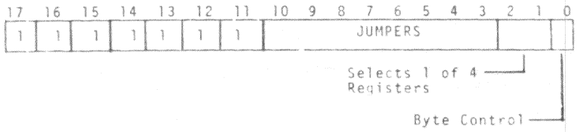
Summary of mode control jumpers:

JUMPER	A	B	C	D	E	DRAWING
J1	*	IN	*	IN	IN	DL-7
J2	OUT	OUT	OUT	OUT	OUT	DL-7
J3	*	OUT	*	OUT	IN	DL-4
J4	*	IN	*	IN	OUT	DL-4
J5	OUT	OUT	IN	IN	IN	DL-4
J6	OUT	OUT	OUT	IN	IN	DL-4
J7	OUT	OUT	OUT	OUT	IN	DL-2
J8	OUT	OUT	IN	IN	IN	DL-2

*= don't care

B. REGISTER ADDRESS ASSIGNMENTS:

The DL11 can respond to addresses with the following format:



Bits 10 through 3 are controlled by jumpers A10 to A3. A jumper inserted indicates a zero.

For the DL11-A and B used as the console device, address 777560 is assigned. For additional units, assign 776XX0, where XX=50 for the first additional unit and XX=67 for the 16th unit.

For the DL11-C,D and E assign address 77XXX0, where XXX=561 for the first line, and XXX=617 for the 31st line. Assign all C's first, then D's, and then E's.

SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	E

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

SHEET 3 OF 9

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

C. VECTOR ADDRESS ASSIGNMENT:

Jumpers V8 through V2 control the interrupt vector. A jumper inserted provides a vector bit of one. Vectors can be produced in the form XX0 and XX4, where XX ranges from 00 to 77.

For the DL11-A and B used as a console device the vector address is 060/064. For additional units, vectors are floating.

For the DL11-C,D, and E vector addresses are floating. Assign all C's first, then D's, then E's.

D. PRIORITY ASSIGNMENT:

Interrupt priority is established by inserting a "priority plug" in the socket at M7800 location E19. For DL11-A,B,C,D and E use level 4.

SUMMARY OF REGISTER, VECTOR AND PRIORITY ASSIGNMENTS:

	ADDRESS	VECTOR	PRIORITY
DL11-A,B CONSOLE	777560 777562 777564 777566	60/64	BR4
DL11-A,B ADDITIONAL UNITS *	776XX0 776XX2 776XX4 776XX6	Floating	BR4

* where XX= 50 for line #1
and XX= 67 for line #16

	ADDRESS	VECTOR	PRIORITY
DL11-C,D,E	77XXX0 77XXX2 77XXX4 77XXX6	Floating	4

where XXX= 561 for line #1
and XXX= 617 for line #31

SIZE	CODE	NUMBER	REV
A	SP	[illegible]	E

DEC FORM NO DEC 16-(381)-1022-N370 DRA 108

SHEET [illegible] OF [illegible]

E. SPECIAL NPR JUMPER:

Jumper N1, shown on drawing DL-6, controls the response of the interrupt circuit to an NPR request. The jumper should normally be IN, except for 11/20 and 11/15 systems without the KH11 option.

F. SELECTION OF DATA FORMAT:

1. Data Bits

Split lug pairs NB2 and NB1 control the number of data bits in the serial character as follows:

NB2	NB1	# OF DATA BITS
OUT	OUT	8
OUT	IN	7
IN	OUT	6
IN	IN	5

2. Parity

Parity is controlled by split lug pairs NP and EPS as follows:

NP	EPS	PARITY
OUT	OUT	OFF
OUT	IN	OFF
IN	OUT	EVEN
IN	IN	ODD

3. Stop Bits

Split lug pair 2SB and jumpers J9, J10 and J11 control the number of stop bits in the serial character as follows:

2SB	J9	J10	J11	# OF STOP BITS
OUT	OUT	IN	OUT	2
IN	OUT	IN	OUT	1
IN	OUT	OUT	IN	1.5 for TI, GI, and SCM UARTS
IN	IN	OUT	OUT	1.5 for WD UARTS

G. CRYSTAL SELECTION:

The clocking scheme of the DL11 consists of a single crystal oscillator feeding a divider network, with two 10-position switches tapping various points to feed into the UART's

G. Con't

transmitter and receiver sections. Thus, for a given crystal frequency, 8 baud rates are independently selectable for transmit and receive. The two addition switch positions select external clocks.

SPEED GROUP		1	2	3	4
		CRYSTAL (HZ)			
POSITION	FACTOR	844.8K	1.03296M	1.152M	4.608M
1*	23040	36.7	44.8	50	200
2	15360	55	67.3	75	300
3	7680	110	134.5	150	600
4	3840	220	269	300	1200
5	1920	440	538	600	2400
6	960	880	1076	1200	4800
7	640	1320	1614	1800	7200
8	480	1760	2152	2400	9600

*Most counter-clock wise position.

To determine a crystal frequency for a non-standard baud rate, pick the position of the closest baud rate in the 1.152MHz column, and then multiply the non standard baud rate by the factor for that position. For example, if the customer specifies 1050 baud. this is closest to 1200 baud, position 6.

1050 X 960 = 10080000 = 1.008MHz.

The crystal frequency should not fall outside the range of the standard crystals.

The part numbers for the standard crystals are as follows:

844.8 KHz	18-10245-1*
1.03296 MHz	18-05501-6
1.152 MHz	18-05501-5
4.608 MHz	18-05501-7

* [illegible] crystals only. Do not use crystals [illegible]

When ordering a special crystal, refer to purchase specification [illegible] for crystal specification.

Insure that transparent vinyl tape (9008269) is applied to the top surfaces of the crystal and mounting brackets to insulate from adjacent modules.

H. G8000 INSTALLATION:

For DL11-B, D, and E a positive voltage is required between 9 and 15 volts to operate the EIA drivers. For PDP-11/20 and PDP-11/15 systems with the H720 power supply, a G8000 module must be installed to provide this voltage. Using a filter network, this module converts the full-wave rectified "+8V" signal to a positive DC voltage.

1. Install G8000 into slot AØ2 of DD11-A.
2. Wire AØ3V2 to AØ2V2.
3. Wire AØ2N2 to CXXU1 where XX is the slot location of the M7800.

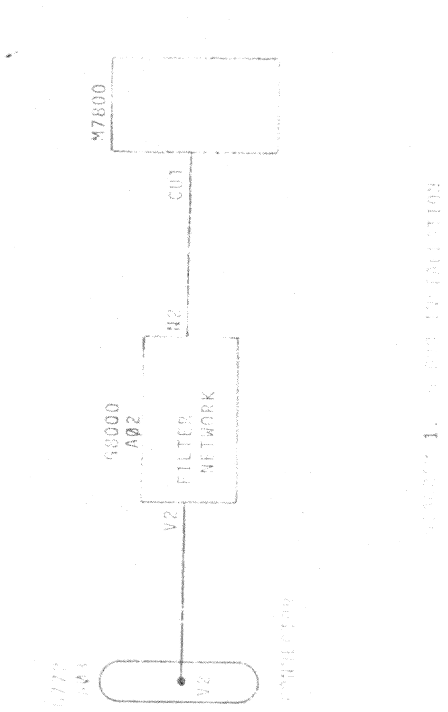
Refer to diagram 1.

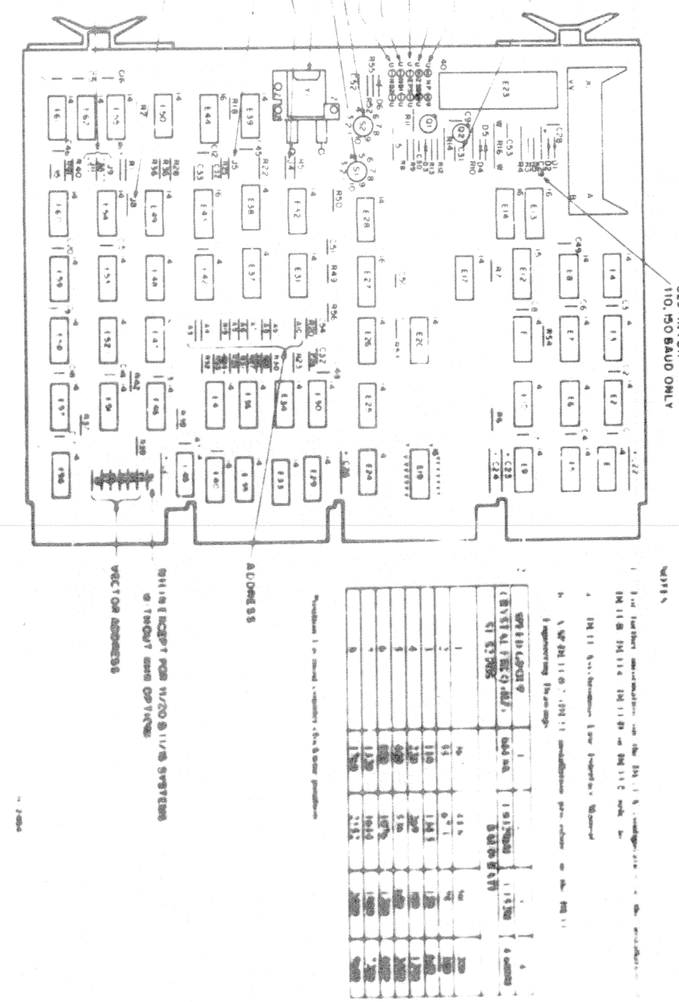
I. FILTER CAPACITOR SELECTION:

For DL11-A's and DL11-C's, which operate with 20ma current loops, capacitors are used to filter the receive line and slow the switching time of the transmit line. To avoid excessive distortion above 150 baud, the capacitance in each of these two circuits must be reduced. This is accomplished by clipping C29 (.47 mfd) and C31 (1000 pf), both shown on drawing DL-3.

J. DL11-B,D,E in Systems with +15V available using DD11-A
There is a special situation of using a DD11-A to mount a DL11-B, D, Or E in systems with +15V available. These systems have +15V available and it appears at pin AØ3V2 of the DD11-A when using power harness such as 7009177, 7008855, or 7008909. In this situation, no G8000 is necessary, and +15V can be wired directly from AØ3V2 to CXXU1, where XX is the slot number of the DL11.
NOTE: this does not apply to DL11-A or C or DD11-B.

K. When using the DL11-B,D,E in an 11/05 processor pin CXXU1 has +15V available on it so no G8000 or no jumpers are required.





SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	F

NOTES:

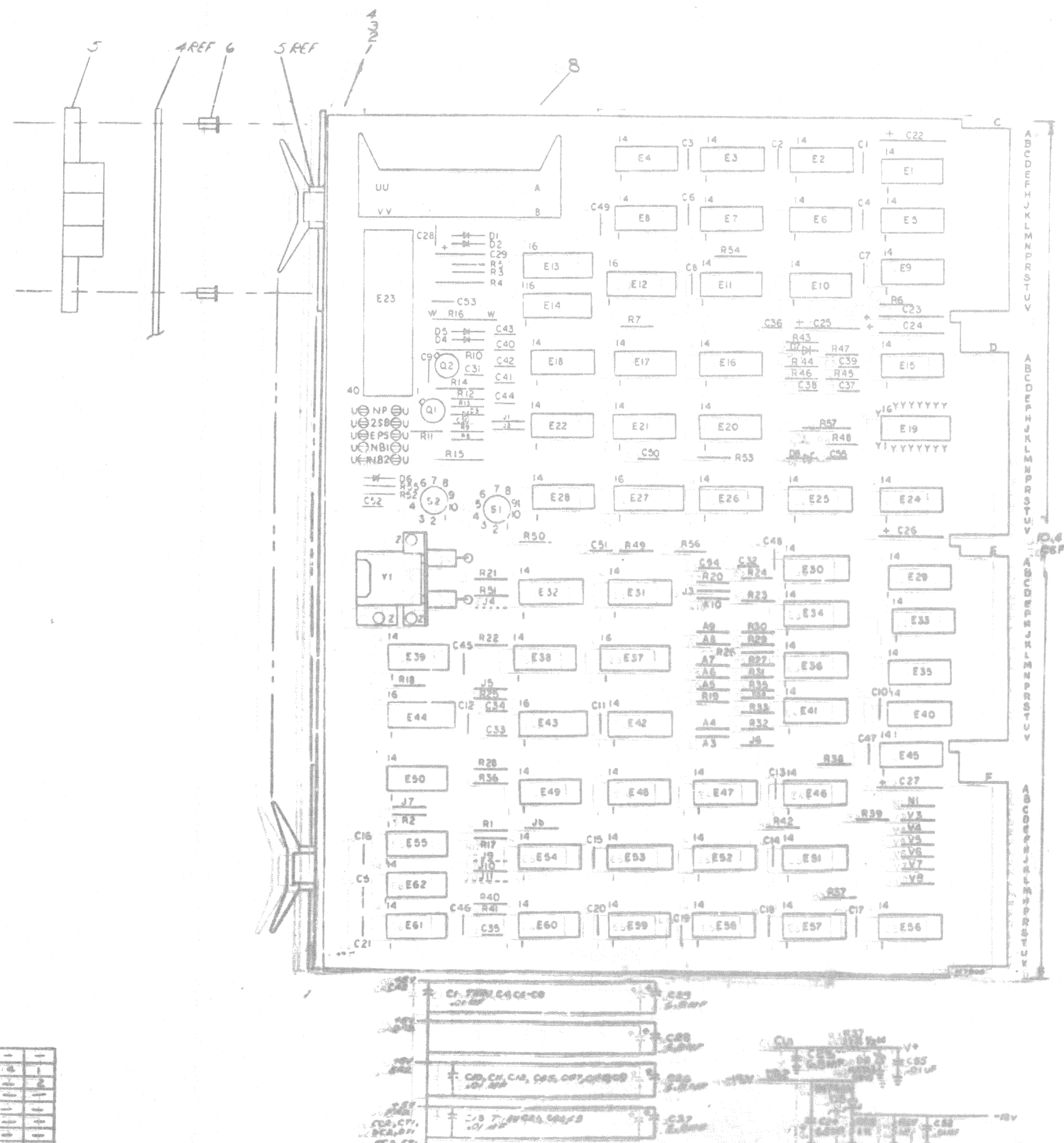
1.) PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.

2.) JUMPERS TO BE USED AT CONNECTIONS A3-A10, J1-J10, V3-V8, AND N1.

3.) LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X).

4. DEC 8640'S [illegible] AS DEC 380 REPLACEMENTS [illegible] SHOULD BE REPLACED BY 8640'S.

5. FOR YC VERSION, C36 VALUE IS 1200 PF.



PIN NOMENCLATURE

MODULE	SYSTEM UNIT
A	C
B	D
C	E
D	F

IC TYPE	GND	+5V	-V	-12V
DEC 74161	8	16	—	—
DEC 1488	7	—	14	1
DEC UART	3	1	—	2
DEC 74175	8	16	—	—
DEC 8271	8	16	—	—
DEC 7442	8	16	—	—
DEC 314	1	8	—	—
DEC 7493	10	5	—	—
DEC 7492	10	5	—	—
DEC 74153	8	16	—	—
DEC 8640	1	8	—	—
DEC 7490	10	5	—	—
DEC 74123	8	16	—	—

GND AND +5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE.

IC PIN LOCATIONS

YC

QTY	QTY	REF DESIGNATION	DESCRIPTION	PART NO.
1	1	R57	RES 39, 1/2W, 5%	13002[illegible]
1	1	D8	DIODE ZENER, 12V 10% [illegible]	11[illegible]
1	1	E47	IC DEC 74161	[illegible]
3	3		NUT KEPS #2	[illegible]
3	3		SCR PHL PAN HD [illegible]	[illegible]
2	2		AUGAT [illegible]	[illegible]
6	6	D1-D5, D7	DIODE 1664 [illegible]	[illegible]
1	1	D6	DIODE 1N742A	1124[illegible]
2	2	Q1, Q2	TRANSISTOR [illegible]	[illegible]
1	1	C53	CAP 100PF 100V 5% DIPPED [illegible]	[illegible]
1	1	C54	CAP 560PF 100V 5% DIPPED [illegible]	[illegible]
2	2	C50, C51	CAP .047MF CERAMIC	[illegible]
[illegible]	[illegible]	C[illegible]	CAP 220PF 100V 5% DIPPED MICA	1000021
[illegible]	[illegible]	[illegible], C35	CAP 330PF 100V 5% DIPPED MICA	1000023
[illegible]	[illegible]	C[illegible], C37-C44	CAP 470PF 100V 5% DIPPED MICA	1000024
1	1	C[illegible]	CAP 1000PF 100V 5% DIPPED MICA	10000[illegible]
30	30	C1-C28, 30, 45-49, 52, 55	CAP .01UF 100V 20% CERAMIC DISC	10016[illegible]
[illegible]	[illegible]	[illegible]	CAP .47UF 35V 10% TANT	10059[illegible]
[illegible]	[illegible]	[illegible]-C27	CAP 6.8UF 35V 20% TANT	100006[illegible]
[illegible]	[illegible]	[illegible]	CAP 150PF 100V 5% DIPPED MICA	1000014
2	2	R14, R15	RES 1.5K 1/2W 5%	1300394
6	6	R[illegible], R40, R48, R52, R[illegible]	RES 1K 1/4W 5%	1300365
[illegible]	[illegible]	[illegible]	RES 47 Ω 1/4W 5%	1300202
[illegible]	[illegible]	[illegible]	RES 68 Ω 1/2W 10%	1300220
[illegible]	[illegible]	[illegible]	RES 82 Ω 1/4W 5%	13[illegible]417
4	4	R[illegible], R45, R46, R47	RES 100 Ω 1/4W 5%	1300229
[illegible]	[illegible]	[illegible]	RES 130 Ω 1/4W 5%	1300250
[illegible]	[illegible]	[illegible]	RES [illegible] Ω 1/4W 5%	1300322
[illegible]	[illegible]	[illegible], R53	RES 220 Ω 1/4W 5%	1300271
[illegible]	[illegible]	R36	RES 390 Ω 1/4W 5%	1300309
[illegible]	[illegible]	R[illegible], R13, R43, R51	RES 470 Ω 1/4W 5%	1300316
[illegible]	[illegible]	R[illegible]	RES 560 Ω 1/2W 5%	1300338
[illegible]	[illegible]	R3	RES 750 Ω 1/4W	1301401
1	1	R16	RES 750 Ω 1W 5%	1302385
21	21	R1, R2, R6, R7, R17-R22, R25, R27-R33, R39, R41, R50, R54, R56	RES 10K 1/4W 5%	1300479
2	2	R5, R6	RES 1.5K 1/4W 5%	1300391
[illegible]	[illegible]	[illegible]	IC DEC UART	[illegible]
[illegible]	[illegible]	[illegible], E55, E61, E62	IC DEC 7474	[illegible]
3	3	[illegible]	IC DEC 8242	1909712
[illegible]	[illegible]	[illegible]	IC DEC 7408	1910155
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	1910323
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	1909037
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	1909705
[illegible]	[illegible]	[illegible]	IC MC1488	19103[illegible]
[illegible]	[illegible]	[illegible]	IC DEC 74123	1910436
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	1909667
[illegible]	[illegible]	[illegible]	IC DEC 7400	1905575
[illegible]	[illegible]	[illegible]	IC DEC 7413	1909989
[illegible]	[illegible]	[illegible]	IC DEC 7402	1909004
[illegible]	[illegible]	[illegible]	IC DEC 8640	1911469
[illegible]	[illegible]	[illegible]	IC DEC 74153	1910437
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	1909937
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	19090[illegible]
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	1909646
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	1909054
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	1905576
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	1909[illegible]
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	1910[illegible]
[illegible]	[illegible]	[illegible]	IC DEC [illegible]	1909[illegible]
[illegible]	[illegible]	[illegible]	IC DEC 7473	1909631
[illegible]	[illegible]	[illegible]	[illegible] CRYSTAL HOLDER	[illegible]
[illegible]	[illegible]	[illegible]	[illegible] CRYSTAL [illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	S1, S2	SWITCH, SINGLE POLE, 10 POS	[illegible]
[illegible]	[illegible]	[illegible]	40 PIN CONNECTOR BERG	1209941
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible] A. G. STEVENSON	[illegible]
[illegible]	[illegible]	[illegible]	[illegible] FLIP-CHIP, MAGENTA	[illegible]
[illegible]	[illegible]	[illegible]	[illegible] CIRCUIT BOARD	5009775
[illegible]	[illegible]	[illegible]	MODULE ECO HISTORY	[illegible]
[illegible]	[illegible]	[illegible]	ASSY/DRILLING HOLE LAYOUT	[illegible]
[illegible]	[illegible]	[illegible]	[illegible] HOLE	[illegible]

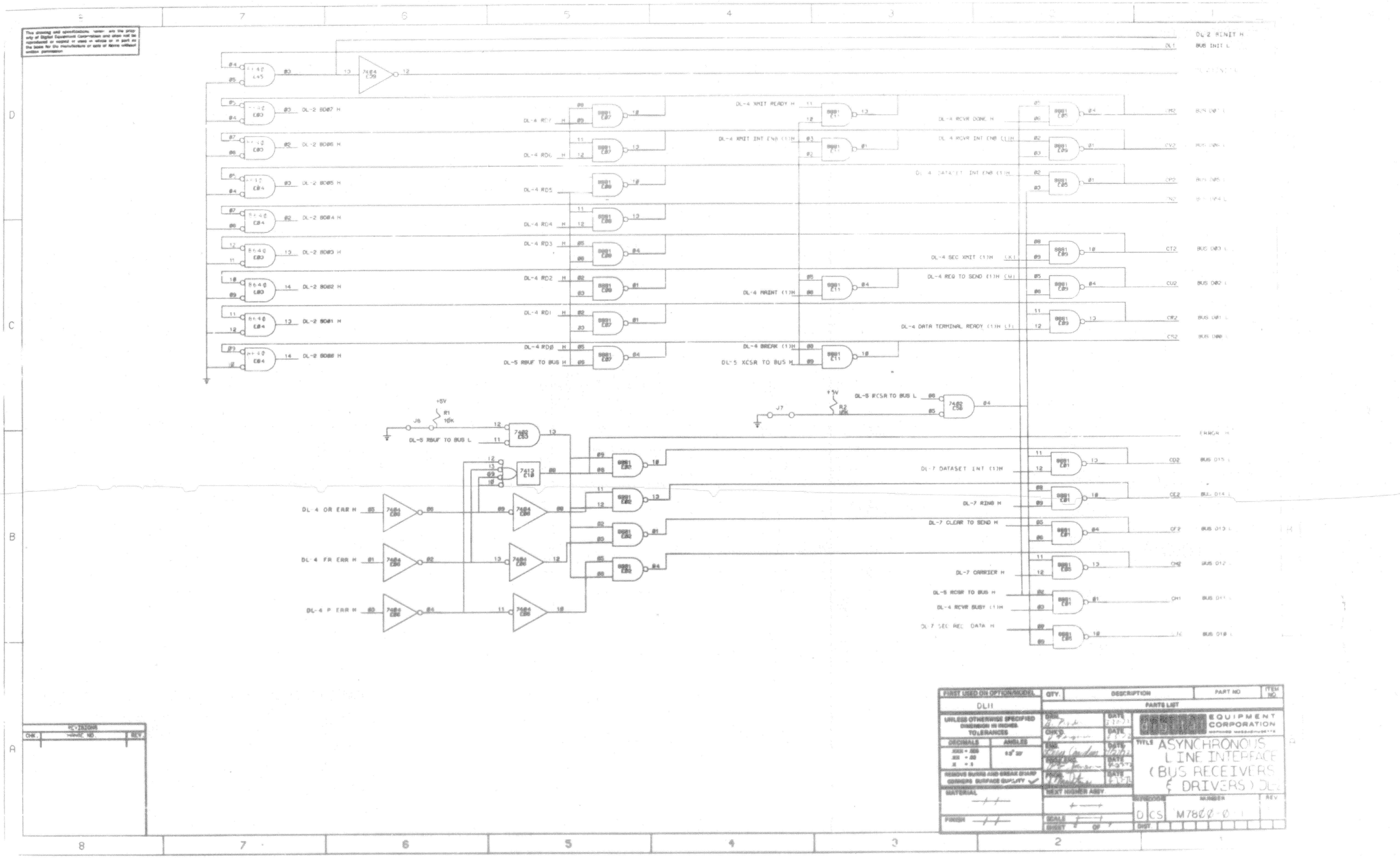
PARTS LIST

SEMICONDUCTOR CONVERSION CHART

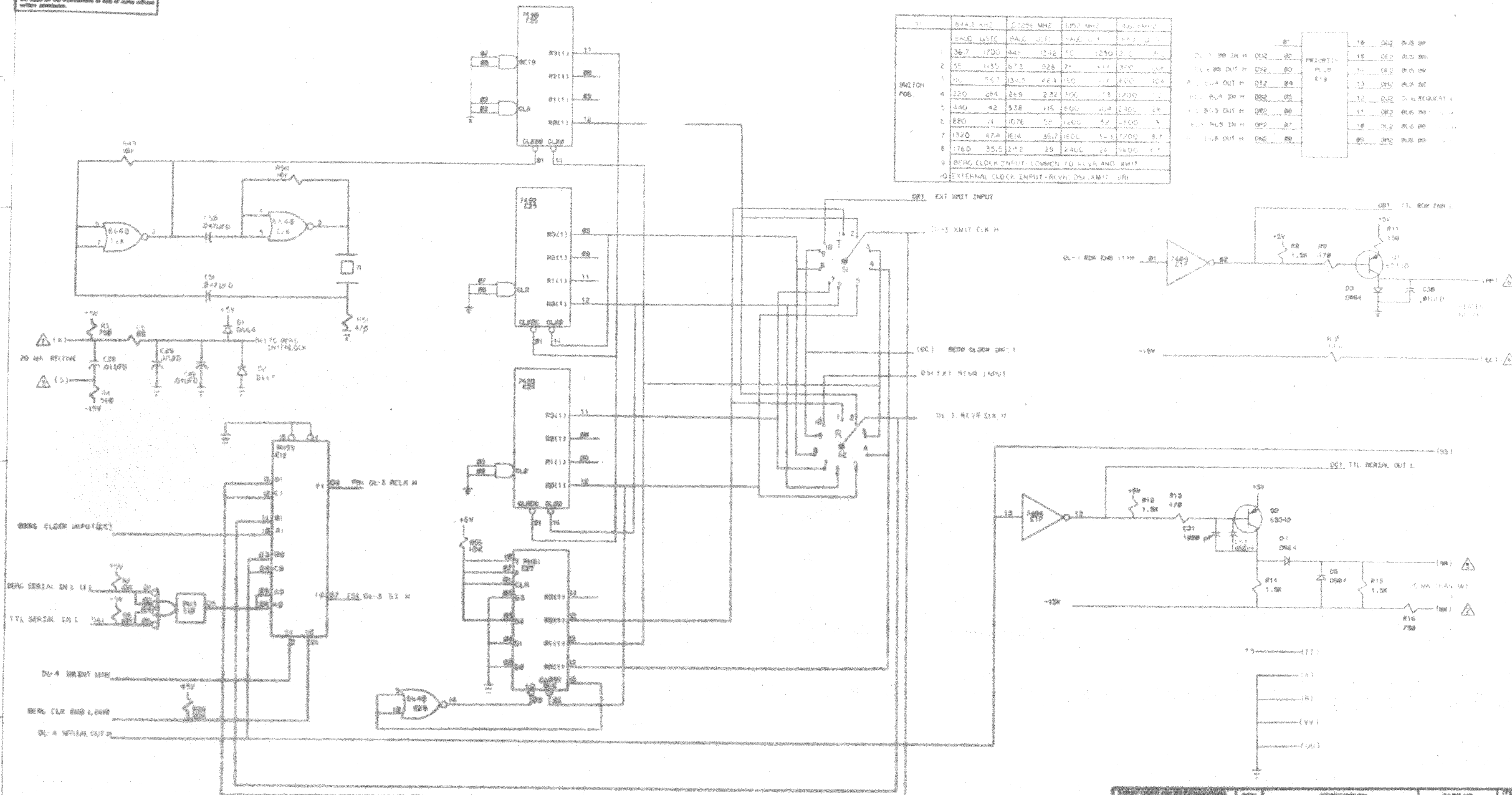
DIGITAL EQUIPMENT CORPORATION

TITLE: ASYNCHRONOUS LINE INTERFACE

CS M7800



DL-2 BINIT H
BUS INIT L
DL-2 BD07 H
DL-2 BD06 H
DL-2 BD05 H
DL-2 BD04 H
DL-2 BD03 H
DL-2 BD02 H
DL-2 BD01 H
DL-2 BD00 H
DL-4 RD7 H
DL-4 RD6 H
DL-4 RD5
DL-4 RD4 H
DL-4 RD3 H
DL-4 RD2 H
DL-4 RD1 H
DL-4 RD0 H
DL-5 RBUF TO BUS H
DL-4 XMIT READY H
DL-4 XMIT INT ENB (1)H
DL-4 MAINT (1)H
DL-4 BREAK (1)H
DL-5 XCSR TO BUS H
DL-4 RCVR DONE H
DL-4 RCVR INT ENB (1)H
DL-4 DATASET INT ENB (1)H
DL-4 SEC XMIT (1)H
DL-4 REQ TO SEND (1)H
DL-4 DATA TERMINAL READY (1)H
BUS D03 L
BUS D02 L
BUS D01 L
BUS D00 L
DL-5 RCSR TO BUS L
DL-5 RBUF TO BUS L
ERROR H
DL-4 OR ERR H
DL-4 FR ERR H
DL-4 P ERR H
DL-7 DATASET INT (1)H
DL-7 RING H
DL-7 CLEAR TO SEND H
DL-7 CARRIER H
DL-5 RCSR TO BUS H
DL-4 RCVR BUSY (1)H
DL-7 SEC REC DATA H
BUS D15 L
BUS D14 L
BUS D13 L
BUS D12 L
BUS D11 L
BUS D10 L
FIRST USED ON OPTION/MODEL
DL11
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
EQUIPMENT CORPORATION
PARTS LIST
ASYNCHRONOUS LINE INTERFACE (BUS RECEIVERS & DRIVERS)
D CS M7800



Y1		844.8 KHZ		1.0296 MHZ		1.152 MHZ		4.608 MHZ	
		BAUD	uSEC	BAUD	uSEC	BAUD	uSEC	BAUD	uSEC
SWITCH POS.	1	36.7	1700	[illegible]	1342	[illegible]	1250	200	[illegible]
	2	55	1135	67.3	928	[illegible]	[illegible]	300	[illegible]
	3	110	567	134.5	464	150	417	600	104
	4	220	284	269	232	300	[illegible]	1200	[illegible]
	5	440	42	538	116	600	104	2400	26
	6	880	71	1076	58	1200	52	4800	[illegible]
	7	1320	47.4	1614	38.7	1800	[illegible]	7200	8.7
	8	1760	35.5	[illegible]	29	2400	26	9600	[illegible]
	9	BERG CLOCK INPUT - COMMON TO RCVR AND XMIT							
	10	EXTERNAL CLOCK INPUT - RCVR: DSI, XMIT: DRI							

NOTES:
1. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. (EXAMPLE: (K))
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE TOOKERS CABLE. THIS CABLE ALSO CONNECTS BERG PINS H TO E.

FIRST USED ON OPTION/MODEL: DL11

UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES

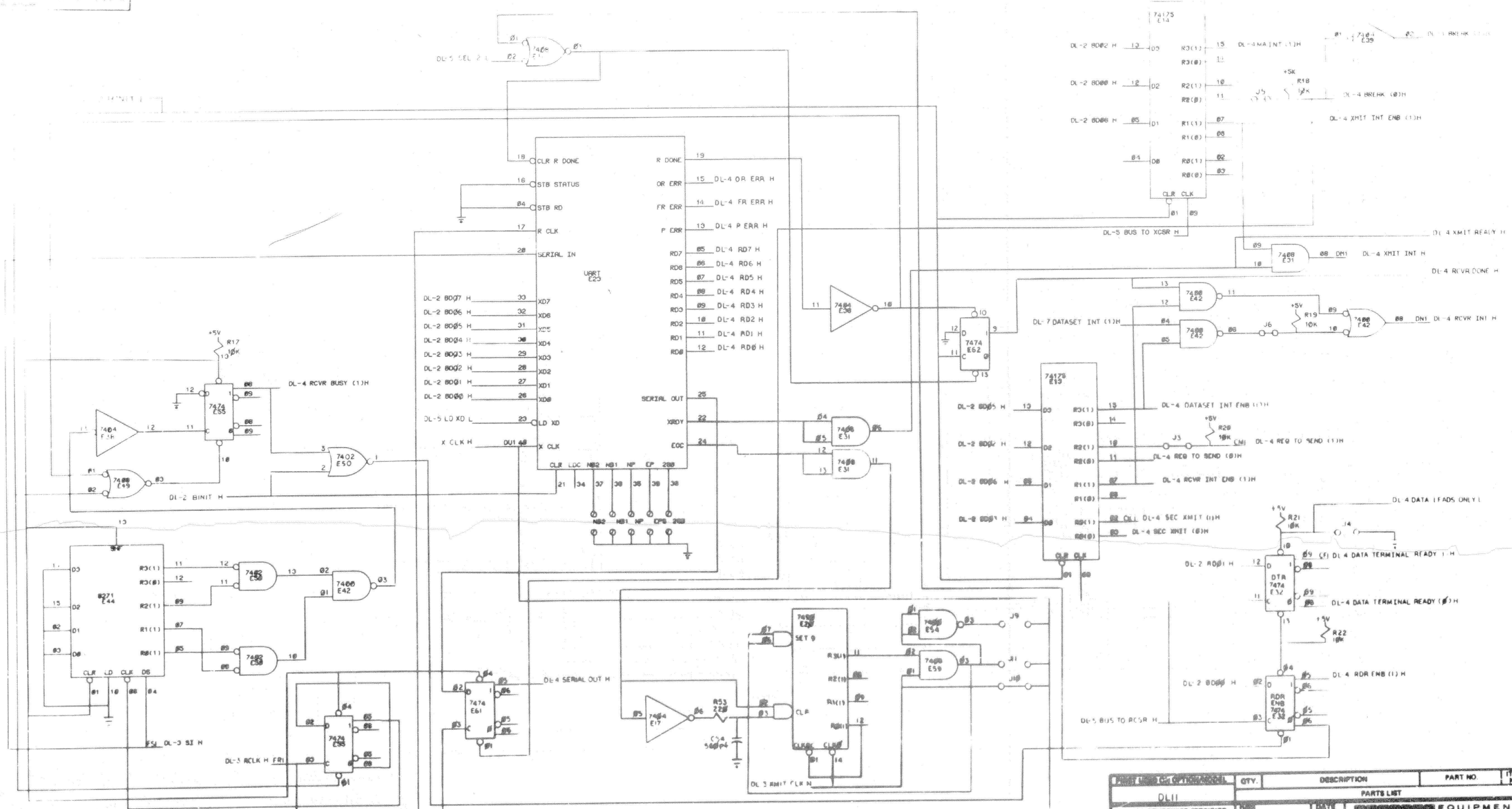
PARTS LIST — QTY. | DESCRIPTION | PART NO. | ITEM NO.

DIGITAL EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (CLOCK & CURRENT LOOPS) DL-3

SIZE D CODE CS NUMBER M7800-0-1

SHEET 3 OF 7



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DL11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES

DECIMALS	ANGLES
.XXX = ±.005	±0° 30'
.XX = ±.02	
.X = ±.1	

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —/—

FINISH —/—

DRN. / CHKD. / ENG. / PROD. ENG. — DATE

NEXT HIGHER ASSY.

SCALE — SHEET OF

DIGITAL EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

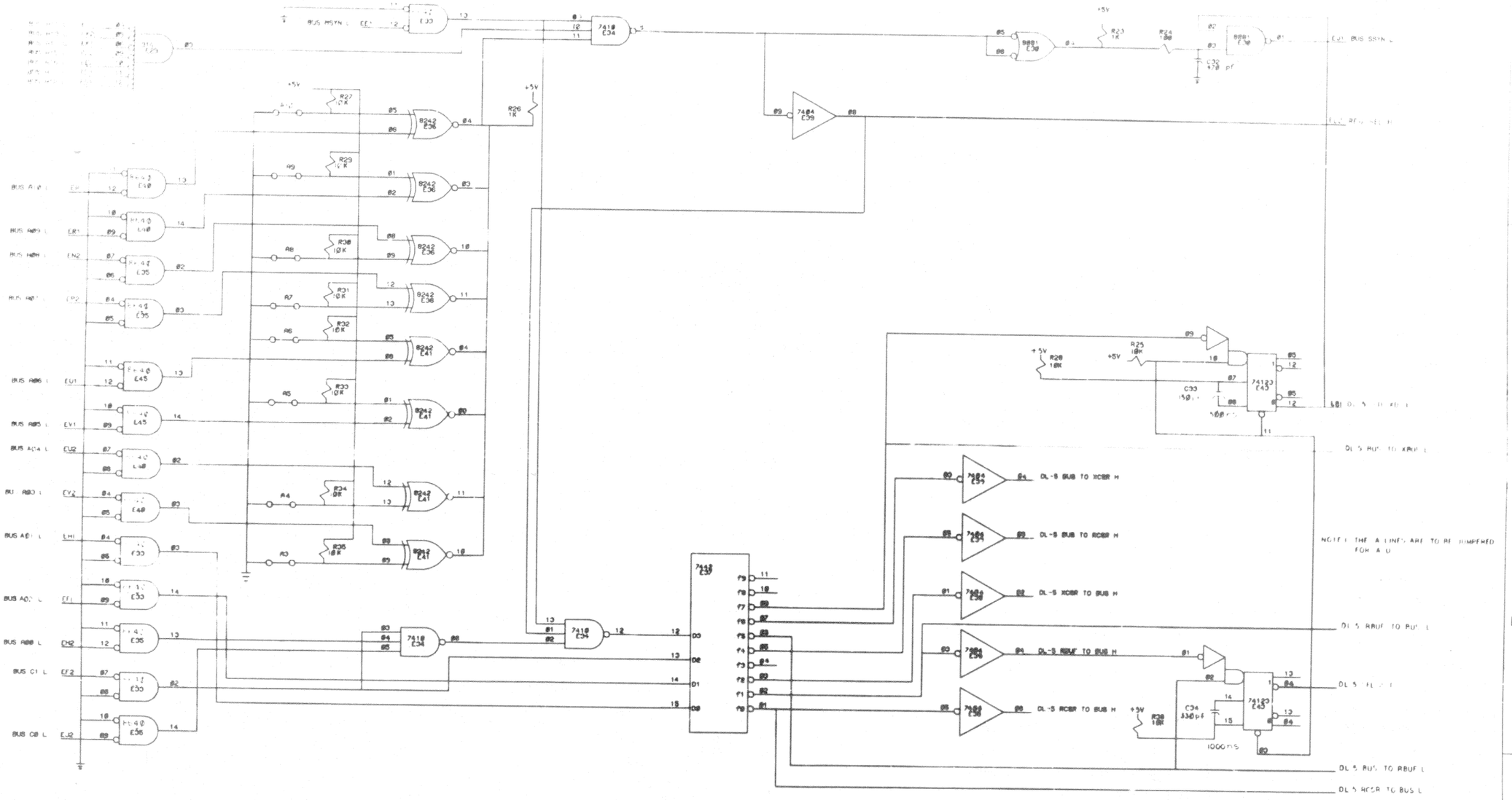
TITLE ASYNCHRONOUS LINE INTERFACE (UART & STATUS) DL-4

SIZE	CODE	NUMBER	REV
D	CS	M7800-0-1	

DIST.

REVISIONS

CHK	CHANGE NO	REV



REVISIONS		
CHK	CHANGE NO.	REV.

PRINT UNIT ON DWG	QTY.	DESCRIPTION	PART NO / ITEM NO.
DL11	PARTS LIST		
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES: DECIMALS .XXX ± .005, .XX ± .02, X ± 1; ANGLES ±0° 30'	DRWN	DATE	EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
	CHKD	DATE	
	ENGR	DATE	TITLE ASYNCHRONOUS LINE INTERFACE (ADDRESS SELECTION) DL-5
REMOVE BURRS AND BREAK SHARP EDGES SURFACE QUALITY ✓	MFG	DATE	
MATERIAL	NEXT HIGHER ASSY		CODE D C S NUMBER M7800-0 1 REV -
FINISH	SCALE		
	SHEET 1 OF 2		SIZE

+5V R37 1ØK

DL-4 RCVR INT H FU1

DL-4 XMIT INT H FY1

BUS NPR L

+5V R35 1ØK

DL-3 RC IN H FB1

R38 39Ø

+5V R40 1K

R41 47

C35 33pF

+5V R42 1K

BUS BBSY L FD1

BUS SSYN L FC1

NOTE: THE 'V' LINES ARE TO BE JUMPERED FOR A L

FP1 DL-6 REQUEST L

FA1 DL-6 BG OUT H

FT2 BUS SACK L

FE2 BUS DØ2 L

V3 FL1 BUS DØ3 L

V4 FH2 BUS DØ4 L

V5 FF1 BUS DØ5 L

V6 FM1 BUS INTR L

V7 FF2 BUS DØ6 L

V8 FH1 BUS DØ7 L

FK1 BUS DØ8 L

REVISIONS		
CHR	CHANGE NO.	REV
1		

FIRST USED ON (SYSTEM/MODEL)	QTY	DESCRIPTION	PART NO.	ITEM NO.
DL11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS: XXX = .000, XX = .00, X = .1; ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓

	NAME	DATE
DRN		
CHK'D		
ENG	Wing Gordon	
MFG ENG		
PROD		

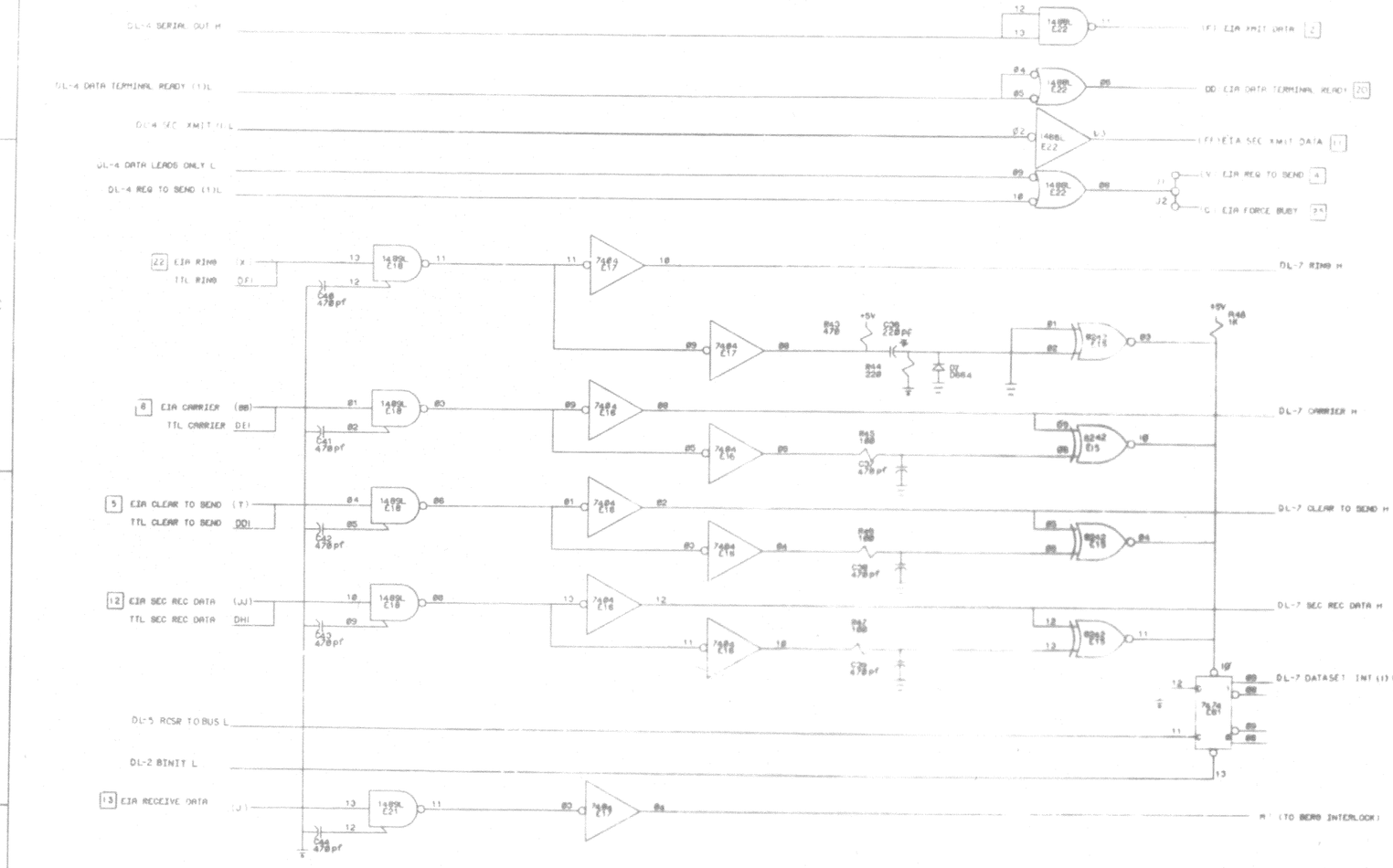
MATERIAL —
FINISH —
NEXT HIGHER ASSY —
SCALE —
SHEET OF

digital EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE (INTERRUPT CONTROL) DL-F

SIZE	CODE	NUMBER	REV
D	CS	M7800-0-1	L

SHEET



NOTES;

1. LETTERS ENCLOSED - EXAMPLE (M) REFER TO PINS ON THE BERG CONNECTOR.
2. NUMBERS WITHIN BOXES REFER TO PINS ON THE MALE CINCH CONNECTOR WHEN USING THE BC05-C CABLE, THIS CABLE ALSO CONNECTS BERG PINS M TO E.

* FOR YC VERSION, C55 VALUE CHANGES TO 1200 pf

REVISIONS		
CHK.	CHANGE NO	REV.

FIRST USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO.	ITEM NO.
DL11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS: XXX = .000, XX = .00, X = .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRN — DATE
CHK'D — DATE
ENG — DATE
PROJ. ENG. — DATE
PROD. — DATE
NEXT HIGHER ASSY
SCALE
SHEET OF

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE ASYNCHRONOUS LINE INTERFACE (EIA DRIVERS & RECEIVERS) DL-7

SIZE	CODE	NUMBER	REV
D	CS	M7800-01	L

DIST

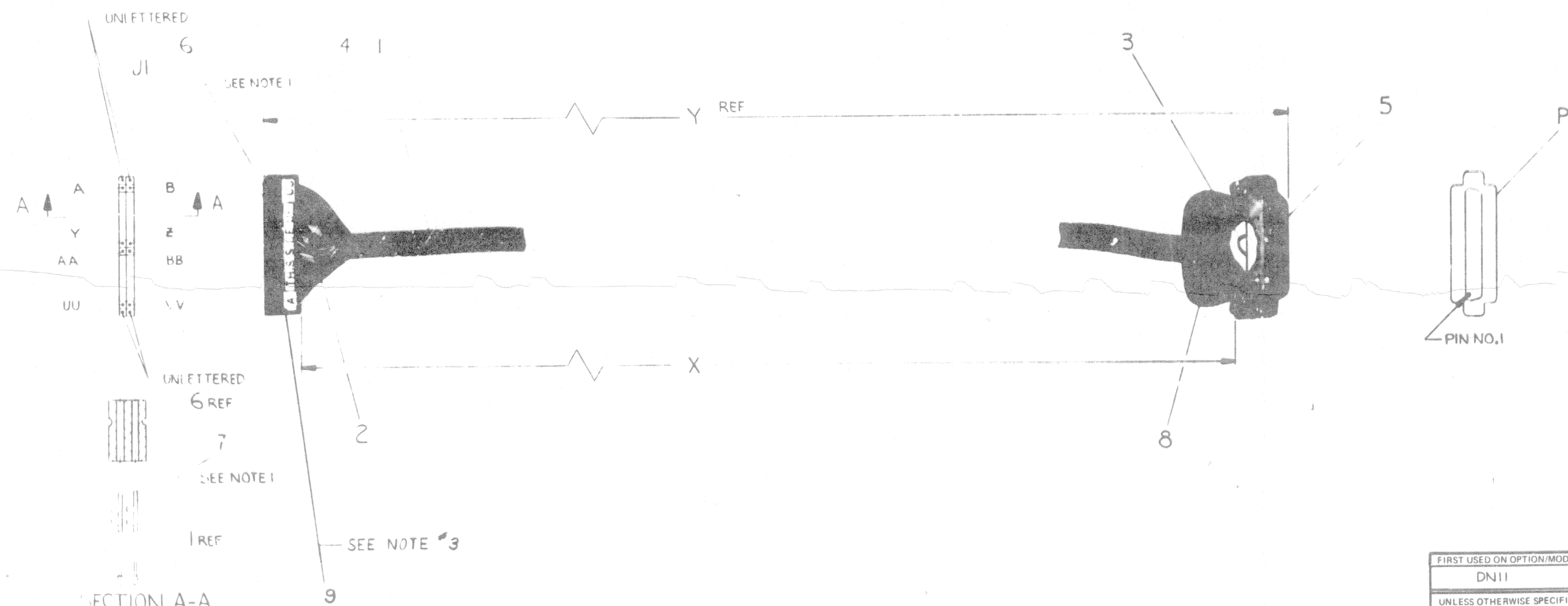
WIRE TABLE

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH
1	22	BLU/WHT	P1-1		J1-VV	
		WHT/BLU	P1-2		J1-F	
		BRN/WHT	P1-3		J1-J	
		WHT/BRN	P1-4		J1-V	
		BRN/WHT	P1-5		J1-T	
		WHT/GRN	P1-6		J1-Z	
		BRN/WHT	P1-7		J1-UU	
		WHT/BRN	P1-8		J1-BB	
		SLA/WHT	P1-9		J1-Y	
		WHT/SLA	P1-Ø		J1-W	
		BLU/RED	P1-11		J1-FF	
		RED/BLU	P1-12		J1-JJ	
		ORN/RED	P1-13		J1-D	
		SLA/RED	P1-14		J1-LL	
1	22	SLA/GRN	P1-15		J1-N	
1	22	RED/BRN	P1-16		J1-NN	
		SLA	P1-17		J1-R	
		RED/SLA	P1-18		J1-U	
		BLU/BLK	P1-19		J1-P	
		BLK/BLU	P1-2Ø		J1-DD	
		ORN/BLK	P1-21		J1-MM	
		BLK/ORN	P1-22		J1-X	
		GRN/BLK	P1-23		J1-RR	
		BRN/RED	P1-24		J1-L	
		RED/ORN	P1-25		J1-C	
		BLK	P1-1	4	J1-A	
1	22	BLK	P1-7	4	J1-B	
3	26	BLK	P1-1		P1-7	
2	26	RED	J1-E		J1-M	

LEGEND

NUMBER	VARIATION DIM X	VARIATION DIM Y (PRECUT)
BCØ5C-25	25'±3"	25' 1.8"
BCØ5C-5Ø	5Ø'±2%	5Ø' 1.8"

NOTES:
1. MANUFACTURING SHOULD USE MACHINE CRIMPER TOOL FOR CRIMPING PINS (ITEM #7) MUST BE HT68 FROM BERG ELECT
2. ONLY DEC PART #1210090-0-0 MAY BE USED AS J1.
3. PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #6 (BERG HOUSING) AS SHOWN.



PARTS LIST

QTY.	DESCRIPTION	PART NO.	ITEM NO.
1	LABEL, THIS SIDE UP	3611557	9
1	HOOD, #DB51226-1 CINCH	12Ø5885	8
29	SOCKET, #HT-68	121ØØ89-5	7
1	HOUSING, #2Ø383 BERG	121ØØ9Ø-Ø-Ø	6
1	PLUG, #DB-25P CINCH	12Ø5886	5
A/R	TUBING, #22 AWG TEF BLK	91Ø7256-ØØ	4
A/R	WIRE, #26 AWG STRD TEF BLK	91Ø7636-ØØ	3
A/R	WIRE, #26 AWG STRD TEF RED	91Ø7636-22	2
A/R	CABLE, 25 CONDUCTOR	91Ø7736	1

FIRST USED ON OPTION/MODEL: DN11

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS: XXX .005, XX .02, X .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL: —//—
FINISH: —//—

DRN: S Roberts — DATE 11/3/71
CHK'D: R Cook — DATE 11/5/71
ENG: Smith — DATE 11/5/71
PROJ ENG: Smith — DATE 11/5/71
PROD — DATE

NEXT HIGHER ASSY: —//—
SCALE: NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

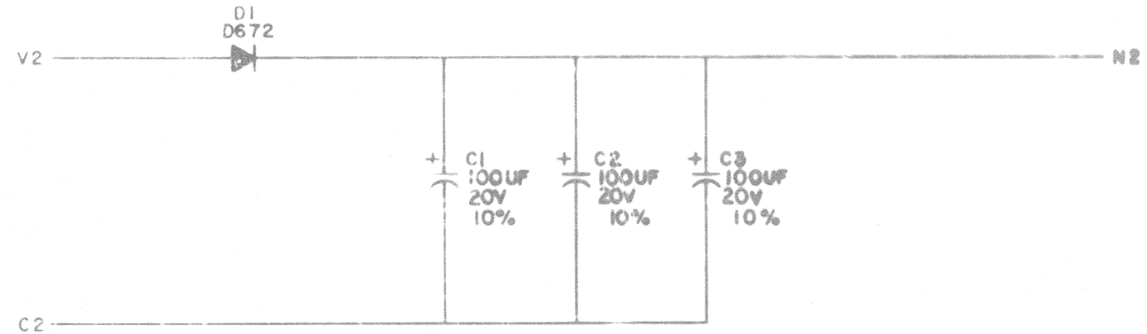
TITLE: CABLE, MODEM BCØ5C

SIZE: D — CODE: UA — NUMBER: BCØ5C-Ø-Ø — REV: B

DIST

Revision: B — ECO BCØ5C-00002 — E ALLain 10-29-73 — B REGAN — 7-14-72

D UA BCØ5C-Ø-Ø B



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ECO 186	1/19/71	

DRN		DATE 1/19/71
CHK		DATE 8/13/71
ENG		DATE 3/11/71
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D672	IN3653		

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: FILTER NETWORK G8000

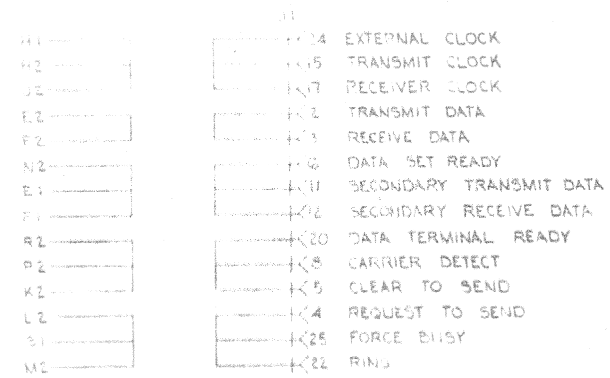
SIZE	CODE	NUMBER	REV
B	CS	G8000-0-1	A

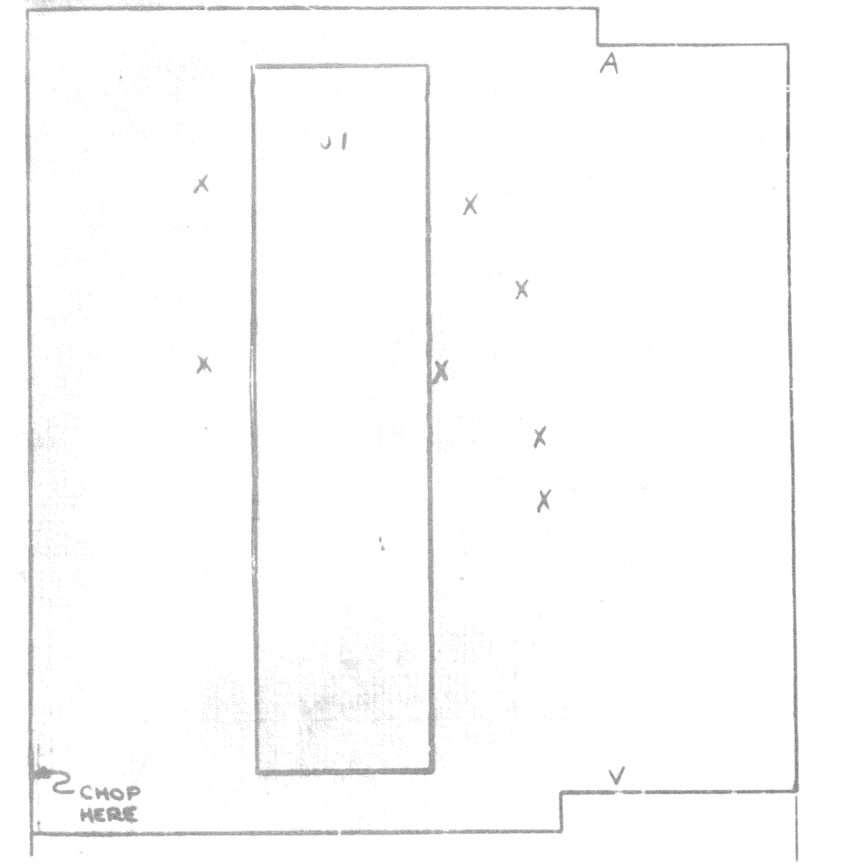
PRINTED CIRCUIT REV A

DEC FORM NO
DRB 102

DIST. 324,434,435 2

4 PINK





QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO
7		EYELET FEED THRU	9006731	[illegible]
1	J1	CONN, CINCH DB-25S-3	1210247	[illegible]
1		ETCHED CIRCUIT BOARD	5010020	4
		MODULE ECO HISTORY	B-MH-H315-0-6	3
		ASSY/DRILLING HOLE LAYOUT	C-AH-H315-0-5	2
		X-Y COORDINATE HOLE LOCATION	K-CO-H315-0-4	1

PARTS LIST

ETCH BOARD REV: A

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

CHK | CHANGE NO. | REVISIONS | REV

DRN. Roger J. Doucette — DATE 3-3-72
CHK'D — DATE 3-16-72
ENG. — DATE 3-17-72
PROD. ENG. — DATE 3-17-72
PROD. — DATE 3/24/72

NEXT HIGHER ASSY
SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE: MODEM TEST CONNECTOR

SIZE: D | CODE: CS | NUMBER: H315-0-1 | REV.
DIST.