digital

DMS11-D
SYNCHRONOUS LINE UNIT

OPTION DESCRIPTION
YM-C061C-00

digital

Computer Special Systems

NOTEBOOK SECTION

3.2-21

OPTION NUMBER

2M-C061A-00

DRAWING SET NUMBER

YM-C061B-00

PROGRAM NUMBER

DECSPEC-11-BCRAD
DECSPEC-11-BCRBD

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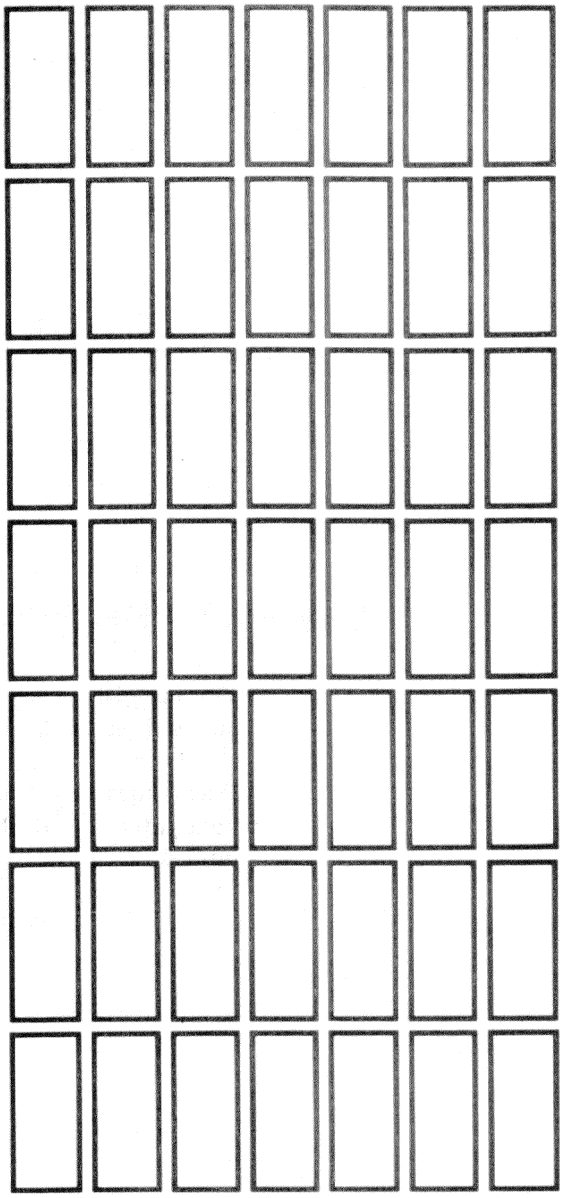

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TABLE OF CONTENTS

Figures

Tables

CHAPTER 1

INTRODUCTION

1.1 GENERAL DESCRIPTION

The DMS11D(A) is a microprocessor (KMC11) controlled eight line synchronous communications line unit on one standard length hex height multilayer module. The DMS11D(A) does not connect directly to the Unibus but is solely controlled by the KMC11 via a one foot BC08R-01 cable. The DMS11D(A) consists of KMC11 interfacing logic, eight Standard Micro Systems Multiprotocol Universal synchronous receiver/transmitter (USYRT) chips, eight dedicated CRC32 chips (DMS11-D only), and associated control logic. The DMS11-DA is identical to the DMS11-D but does not include the CRC32 chips. CRC16 is performed by the USYRT. The KMC11 basically serves as a control for the USYRT chips.

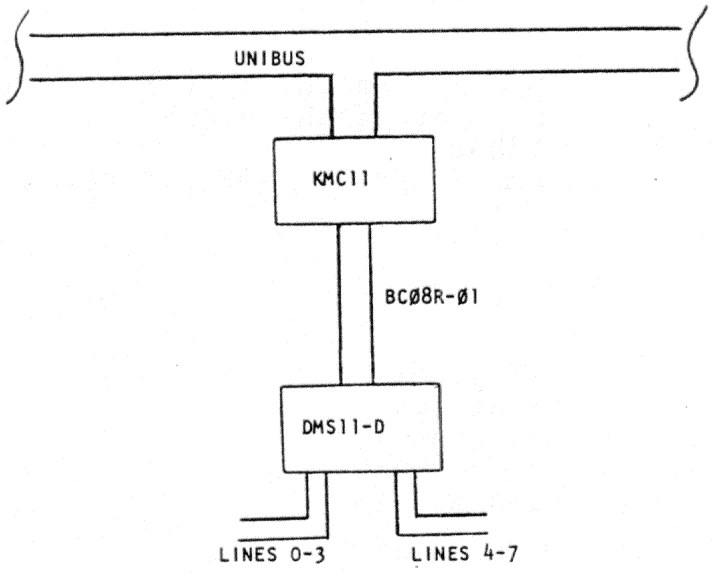


Figure 1-1 DMS11-D System Block Diagram

Connection to the eight synchronous communications lines is via 2 fifty pin Berg connectors (4 lines each) in RS423 standard levels. Signals available for each line are transmit data out, receive data in, transmit clock, and receive clock.

1.2 GENERAL OPERATION

Basically, the KMC11 sets up appropriate parameters in two sets of registers. Eight primary registers control line selection and provide selected line status; while the eight secondary registers are internal to the specified USYRT chip associated with the selected line. Once line parameters are initialized, data may be transmitted to or received from the selected line via a tristate data bus on the board. Line status is polled via KMC11 firmware and appropriate action is taken.

1.3 SPECIFICATIONS*

The DMS11D(A) is a multilayer hex height module with two fifty pin Berg cable connectors for modem clock and data signals, and one forty pin Berg cable connector for connection to the controlling microprocessor.

1.3.1 DMS11-D(A)

a. MECHANICAL:

Logic	One hex height multilayer module.
Mounting Prerequisite	One hex height slot.
Cable (to KMC11)	BC08R-01
Configuration Prerequisite	KMC11 and DD11-DF backplane

b. ELECTRICAL

Logic	TTL, LSI
Module Type	M series
Power Requirements	3.5A at +5V 1A at +15V .5A at -15V

* Specifications are subject to change without notice.

The following specifications are for reference only:

KMC11 Microprocessor

MECHANICAL

Logic	One hex height module
Mounting Prerequisite	One hex height slot in DD11-DF when used with DMS11-D

DD11-DF

a. MECHANICAL

Nine Slot Backplane Mounting Prerequisite	BA11-L Box 4.7 in x 16.5 in

b. ELECTRICAL

KMC11-A	+5V at 5A
KMC11-B	+5V at 7.5A

Total Power Requirements:

2 - DMS11D(A)/KMC11A combinations - 17A at +5, 2A at +15V, 1A at -15V (TYP)

2 - DMS11D(A)/KMC11B combinations - 22A at 5V, 2A at +15V, 1A at -15V (TYP)

CHAPTER 2

INSTALLATION

2.1 GENERAL

The DMS11D(A) being a hex height module is simply placed into a DD11-DF slot adjoining the controlling KMC11. Cabling involves connecting a BC08R-01 between the DMS11D(A) and the KMC11.

2.1.1 Site Considerations

A DMS11D(A) line unit is installed into configuration with a KMC11. Typically 2 KMC11/DMS11D(A) combinations are installed in each DD11-DF backplane.

The DD11-DF mounts in a BA11-F,L,K or P Expander Box. The attached harness (#70-11109) plugs into connector at the top of the cabinet supplying +5V, -15V and +15V, to the logic.

2.1.2 Hardware Installation

Installation of the DMS11-D(A) [M8711(YA)] involves installing the M8711(YA) module into the slot to the left of (next higher numbered slot) the KMC11. Install G727 Bus grant continuity cards in row D of all unused slots.

NOTE

The DD11DF comes with NPG wires installed in all slots. For proper KMC11 operation the wire between CB1 and CA1 must be removed in the slots where a KMC11 is installed. Conversely this wire must be installed if the KMC11 is removed, to insure grant continuity.

2.1.3 Cables

A BC08R-01 is supplied with each DMS11D(A)/KMC11 combination. This cable connects the KMC11 to the DMS11D(A). The cable should not be twisted. Two maintenance plugs (#2ME044B available from CSS) are used for diagnostic checkout and should not be used under normal operation. Instead, the two 50 pin Berg connectors are used to interface to appropriate equipment.

2.2 FIELD CHECKOUT/ACCEPTANCE PROCEDURE

2.2.1 System Test Requirements

2.2.1.1 Hardware -

The following are minimum hardware requirements to test the DMS11D(A):

1. PDP11 with a minimum of 16K of memory
2. KMC11B (or A) microprocessor with associated backplane for inserting DMS11D(A).
3. BC08R-01 KMC11 to DMS11 interconnecting cable.
4. 2 50 pin Berg loop back connectors (for diag use only).

2.2.1.2 Software -

The following software is required for diagnostic checkout of the DMS11D(A).

1. YM-Z136D-10 Static Logic Test (DECSPEC-11-BCRAD for Autodin)
2. YM-Z136D-20 Dynamic Subsystem Test (DECSPEC-11-BCRBD for Autodin)

2.2.2 System Test Procedure

2.2.2.1 Hardware Procedures -

Verify that the backplane slot selected for the KMC11 does not have a wire between CB1 and CA1. If it does, this connection should be removed. This allows NPG to be used by the KMC11. Insert the DMS11D into the next higher numbered DD11DF backplane slot. Insure grant continuity (G727) cards are inserted in unused slots (Row D).

2.2.2.2 Software Procedures -

Previous to running the DMS11 diagnostics, the KMC11 Diagnostics (YM-Z093D-AD and YM-Z093D-B0) must be successfully run. Ensure that the two test connectors (2ME044B) are installed and that the following tests are run in external mode (SW00=1 for BCRAD & BCRBD). Run YM-Z136D-10 (DECSPEC-11-BCRAD for AUTODIN) Static Tests for 5 end passes. YM-Z136D-20 (DECSPEC-11-BCRBD for AUTODIN) Dynamic Tests is to be run for 10 end passes in BOP mode and 10 end passes in CCP mode (Mode I and Mode VI for BCRBD).

2.3 RELATED LITERATURE

Title	Number
KMC11 Microprocessor Users Manual	EK-KMC11-OP
KMC11-B UNIBUS Microprocessor Option Description	YM-C093C-00

CHAPTER 3

OPERATION AND PROGRAMMING

3.1 GENERAL DESCRIPTION

The DMS11-D(A) is a hex height module controlled by the KMC11 microprocessor. The DMS11D(A), via program control of the KMC11, outputs and inputs serial data to 1 through 8 modems. The heart of the DMS11-D(A) is the eight 40 pin USYRT chips (universal synchronous receiver transmitter) one for each line. The remaining logic is responsible for KMC11 interfacing, USYRT and CRC control and line selection.

The DMS11-D(A) is controlled via 16 registers which are loaded via KMC11 firmware. Eight of these registers, called primary registers, are mainly concerned with line selection, parallel data I/O, selection of appropriate secondary registers, and status of the selected line. The other 8 registers called secondary registers are internal to the USYRT and are necessary for KMC11 control of the USYRT itself.

Access of the secondary register set is only possible through primary register 10 (Data Port Register). Primary Register 10 may be considered a "window" into and out of all secondary registers. See Primary Register Chart, Figure 3-1. After the Line Number is selected by writing the appropriate bit in Primary Register 11 [4:6] a secondary register can then be selected by Secondary Register select bits [5:7] of Primary Register 12. Then the selected secondary register may be read or written (depending on the state of USYRT R/W bit [4] of Primary 12 and the specification of the particular secondary registers involved). Also at this time some line status for the selected line will be available in primary register 13 and 14. Primary Registers 16 and 17 always reflect the status of all lines TBMT or TSA signal in Primary Register 16 and RDA or RSA in Primary Register 17.

3.2 PROGRAMMING

Programming of the DMS11D(A) requires a thorough understanding of the USYRT chip, serial communication protocol, and the KMC11 instruction set. Prior to any serial data transfer, the USYRT chip must be initialized for the desired type of communication activity.

Refer to the SMC 5025 USYRT Specification Sheet for details concerning the USYRT chip not covered in this discussion (Appendix B).

3.2.1 Parameter Setup

A typical sequence for parameter setup would proceed as follows:

The microprogram would load Primary Register 11 with the line number and Primary Register 12 with the address of the internal USYRT register and the W/R bit HI to load the mode control and character length register.

1. MOVE LN [0:2] to Primary Register 11.
2. MOVE AS [0:2], w/R bit HI to Primary Register 12.
3. MOVE "character length" to Primary Register 10, which actually goes into previously selected secondary register (data length select register).
4. MOVE AS [0:2], W/R bit HI to Primary Register 12.
5. MOVE "mode selection" to Primary Register 10, which is actually goes into the previously selected secondary (mode control register).

3.2.2 Transmitting A Character

The microprogram would load Primary Register 11 with the line number. It is then necessary to set the (TAC) transmitter active bit by loading at 1 into PR13 [6]. Then load Primary Register 12 with the W/R bit HI and the address of the desired Secondary Register (i.e. transmit data register 12). This would be done after determining that the TBMT bit was true for the selected line. TBMT (transmitter buffer empty) can be monitored by checking PR13 [4] for a HI. This is of course is only valid after loading the desired line number in PR11 [4:6]. The typical transmit sequence would proceed as follows:

1. MOVE LN [0:2] to PR11 [4:6]; line select

2. MOVE a 1 to PR13 [6] which sets (TAC) the transmitter active bit.

3. MOVE AS [0:2], W/R to PR12 [5:7], PR12 [4]; secondary register select for a write.

4. A loop to wait for setting of TBMT in PR13 [4].

5. MOVE DATA (8 bits) to PR10 [0:7] which is the "window" to the secondary "transmit data" Register.

3.2.3 Receiving A Character

The microprogram would first select the line by loading LN [0:2] into PR11 [4:6]. Then MOV at 1 to PR13 [2] to set the receiver active. Followed by a test loop to determine when "RDA" (Receive data available) PR13 [0] was set. Then AS [0:2] would be loaded into PR12 [5:7] to select secondary 0 (receive data register). In this case (receiving), the W/R bit should be low. An input from PR10 (which is the "window" into the secondary receive data register) should be performed to store the receive data byte. A typical receive sequence would proceed as follows:

1. MOVE LN [0:2] to Primary Register 11 (PR11 [4:6].

2. Set RAC (Receive Active) bit in Primary Register 13. 1 throught PR13 [2].

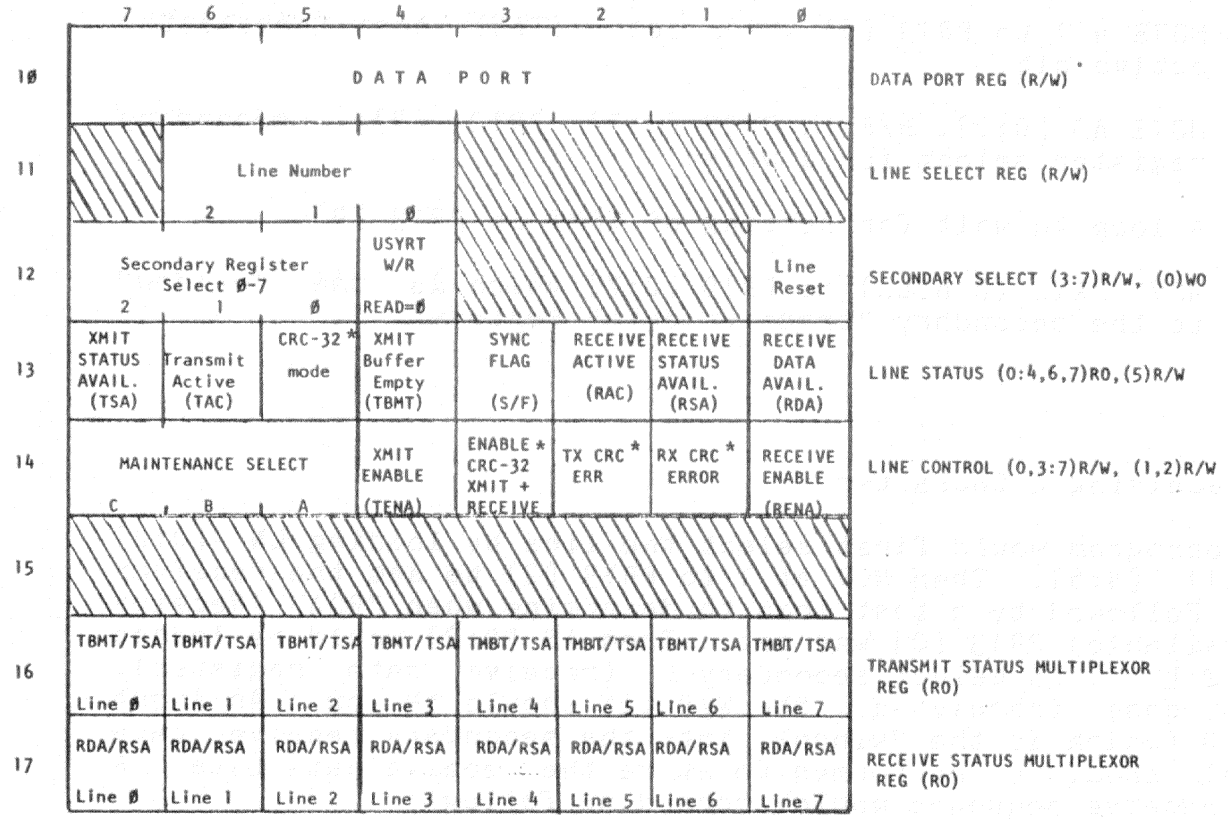
3. A loop to wait for the HI state of RDA (PR13 [0]) indicating that receive data is available.

4. MOV AS [0:2], W/R bit LO to Primary Register 12. (Read of Secondary 0.)

5. MOV Primary 10 into memory; this inputs the data character.

3.2.4 Primary Register Set Description

The primary register set consists of Eight - 8 bit registers which are utilized to control basic line functions. Recall that the secondary registers are internal to the USYRT and are thus concerned solely with USYRT operation. The primary registers then provide a means of controlling and observing status of all functions which are external to the USYRT (including some USYRT status signals). This register set also provides a means of selecting a specific secondary register which you plan to load or read.



*Not Used In DMS11-DA

Figure 3-1 Primary Registers

3.2.4.1 Primary Register 10 - DATA PORT REGISTER -

This 8 bit register serves as "window" or port through which you must access a previously selected secondary register (according to AS [0:2], (PR12 [5:7]). Whenever you wish to read or write any register internal to the USYRT, you must first select the desired secondary register and the direction of data transfer by loading primary register 12 appropriately. Then you may access this register by reading or writing Primary Register 10. Primary Register 10 is an 8 bit wide Read/Write register with the least significant bit being bit 0 (Primary Register Figure 3-2).

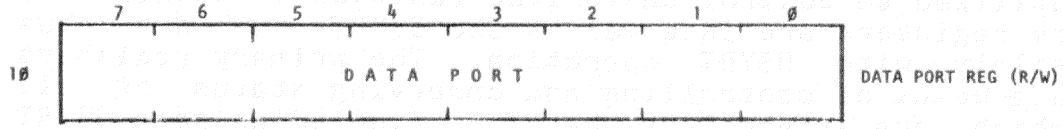


Figure 3-2 Data Port Register

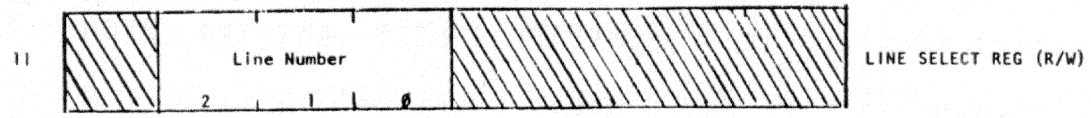


Figure 3-3 Line Select Register

3.2.4.2 Primary Register 11 - LINE SELECT REGISTER -

The sole function of this 8 bit read/write register is to select the desired line you wish to control. Hardware multiplexers allow control of eight individual lines. These multiplexers are forced to select the desired line by the state of primary register 11 bits 4-6 (PR11 [0:6]). These are also referred to as LN [0:2]. Note that only three bits are used (bits 4, 5 and 6) and the others may not be written and are read as zero. PR11 [4] or LN [0] is the least significant bit (Table 3-1).

Table 3-1 Line Selection

SELECTED LINE	LN2 PR11[6]	LN1 PR11[5]	LN0 PR11[4]
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

NOTE

Once a particular line has been selected, any status or data read from or written to Primary Register 10, 12, 13 or 14 will be concerned only with the selected line.

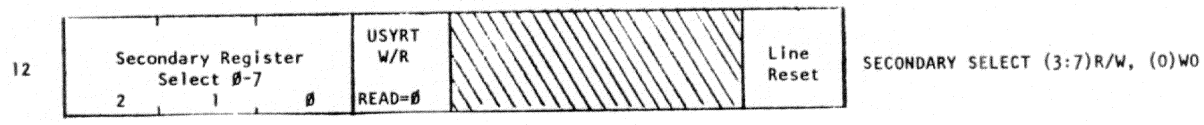


Figure 3-4 Secondary Select Register

3.2.4.3 Primary Register 12 - SECONDARY SELECT REGISTER -

This 8 bit register is used for 3 basic functions:

1. Line Reset PR12 [0]
2. Secondary Register Select PR12 [5:7], (AS [0:2])
3. Direction of transfer PR12 [4]
4. PR12 [1:3] are unused.

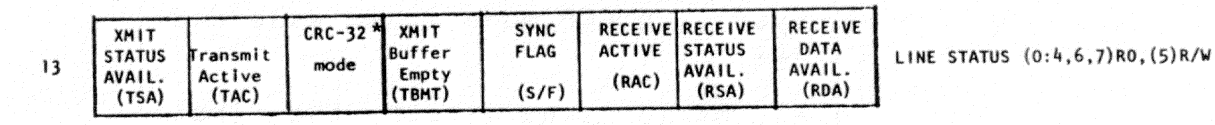
The line reset bit (PR12 [0]) when written as a one, triggers a momentary pulse which initializes the USRYT and other logic associated with the selected line. Since the line reset bit creates a pulse which is not stored, it is a write only bit, and will be read as a zero.

The Secondary Register Select bits (AS [0:2]) are used to specify which secondary register (internal to the USYRT) one wishes to access. Once these bits are written to select a particular secondary register all transfers through Primary Register 10 (data port register) will either go to, or originate from the selected secondary register. One of eight (0-7) registers are selected as indicated in Table 3-2. AS [0] or PR12 [5] is the least significant bit. AS [0:2] may be read as well as written.

SECONDARY REGISTER SELECTED	PR12[7] AS[2]	PR12[6] AS[1]	PR12[5] AS[0]	REGISTER TYPE
0	0	0	0	RCV DATA BUFFER
1	0	0	1	RCVR STATUS REG.
2	0	1	0	TRANSMIT DATA BUFFER
3	0	1	1	TRANSMIT STATUS CONTROL
4	1	0	0	SYNC ADDRESS REG.
5	1	0	1	MODE CONTROL REGISTER
6	1	1	0	NOT IMPLEMENTED
7	1	1	1	DATA LENGTH SELECT REGISTER

Table 3-2 Secondary Register Select

The USYRT write/read bit determines the direction of data flow between the KMC11 and the internal USYRT Registers (Secondary Registers). PR12[4], when set, sets the logic up for a write to the selected secondary register from the KMC11. Conversely when this bit is cleared, the logic is set up for a read from the selected secondary register into the KMC11. PR12[4] may be read or written.



*Not Used in DMS11-DA

Figure 3-5 Line Status

3.2.4.4 Primary Register 13 - LINE STATUS REGISTER -

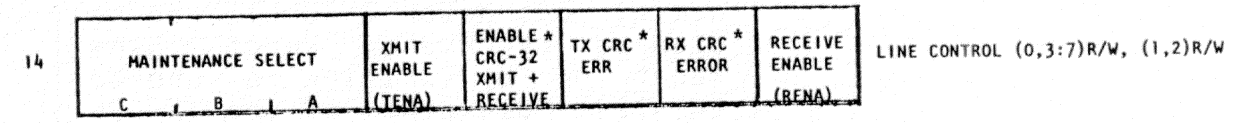
This 8 bit register in conjunction with Primary 14, supplies pertinent status of the line previously selected by the line select register. PR13 [0:4, 6, 7] is actual USYRT status, while PR13 [5] is a control bit which selects a particular mode of CRC chip operation (to be explained later). PR13 [5] "CRC 32 MODE" bit is the only bit in Primary Register 13 which may be read or written.

BIT NAME/DESIGNATOR	DESCRIPTION
RDA, PR13 [0]	Receiver data avaliable. This read only bit is set when the USYRT has assembled an entire character and has transferred it into the receiver data buffer. This is reset by reading the receive data buffer (secondary Register 0).
RSA, PR13 [1]	Receiver Status Available. This read only bit is high: a) In CCP mode in the event of receiver overrun (ROR) or parity error (if selected). b) In BOP mode in the event of ROR, CRC error (if internal CRC mode is selected (i.e. not for CRC32)), or receiving REOM or RAB/GA. This bit is reset by reading the receiver status register or by reseting RAC bit, PR13 [2] (receiver active).
RAC, PR13 [2]	Receiver Active (RXACT). This read only bit is asserted when the USYRT makes the first data character of the message available. In BOP mode the first data character is the first non-flag character (address byte). In CCP mode it is asserted if: a) strip sync is set, the first non sync character is the first data character.

BIT NAME/DESIGNATOR	DESCRIPTION
	b) if strip sync is not set, the first data character is the character following the second sync. In BOP mode the trailing (next) Flag resets RAC. In CCP mode RAC is never reset automatically, but it can be cleared via RENA (RXENA) receiver enable.
S/F PR13 [3]	SYNC Flag Received. This read only bit is asserted for 9 receive clock pulses each time a sync or flag character is received. If consecutive sync/flag characters are being received this bit remains high.
TBMT PR13 [4]	Transmitter Buffer Empty. This read only bit is high when the transmitter data buffer (TDB) (secondary 2) or the transmitter status and control register (secondary 3) may be loaded with new data. TBMT becomes zero on any write access to the TDB or the transmitter Status and Control Register. TBMT returns high when data may be loaded into the transmitter data buffer.
CRC32 MODE PR13 [5] (Not used in DMS11-DA)	CRC32 mode select. This read/write bit PR13 [5] is used in conjunction with PR14 [3] (enable CRC32). When the CRC32 logic is enabled, PR13 [5] determines in which mode the CRC32 chip will operate:

ENABLE CRC32 PR14[3]	CRC32 MODE PR13[5]	DESCRIPTION
0	0	The CRC32 circuitry is disabled. Serial data is passed through the device with no alteration. Serial-in to serial-out delay is 9 bit times.
0	1	Same as above
1	0	This is the CRC32 generate mode for the serial out data. CRC32 calculations begin upon receipt of the first data character after an opening flag character. Upon detection of a closing Flag Character the CRC32 accumulation is shifted out with the closing flag, MSB first.
1	1	This is the CRC32 Check Mode for the serial out data. CRC32 calculations begin upon receipt of the first data character, after an opening flag character. Upon detection of a closing FLAG character, the ERROR is enabled. If the incoming CRC32 does not cause the calculation to reach the proper remainder, the error latch will set and remain set until a line reset is issued. This mode is intended to be used in applications when the CRC32 check character is known and already a part of the data stream (i.e., for reception and checking of CRC32). The CRC32 polynomial implemented is: X32+X26+X23+X22+X16+X12 +X11+X10+X8+X7+X5+X4+X2+X+1 The CRC32 calculated remainder is: 30701156573 (octal)

BIT NAME/DESIGNATION	DESCRIPTION
TAC, PR13 [6]	Transmitter Active (TXACT). This read only bit indicates the status of the internal USYRT transmitter data path. TAC will go high after asserting transmitter enable (TENA PR14 [4]) and TSOM (SR3 [0]) coincidentally with the first TSO data bit. This output will reset one half clock after the byte during which TENA is dropped.
TSA, PR13 [7]	Transmit Status Available. This read only bit is set to indicate a transmitter underflow error has occurred. This can only be reset by master reset or the assertion of TSOM.



*Not Used For DMS11-D

Figure 3-6 Line Control

3.2.4.5 Primary Register 14 - LINE CONTROL REGISTER -

This eight bit register consists of 3 read/write clock select bits PR14 [5:7], two read/write CRC32 error status bits PR14 [1,2] and 3 read/write USYRT/CRC32 control bits. All control/status pertains to the line selected previously in Primary Register 11.

BIT NAME/DESIGNATION	DESCRIPTION
RENA, PR14[0]	Receiver Enable (RXENA). This read/write bit, when written as a one allows USYRT input of the received serial data (RSI). A low level disables the receiver data path (RDP) and resets RDA, RSA and RXACT.
RX CRC ERROR PR14[1] (Always 0 for DMS11-DA)	Receive CRC32 error. This read/write bit indicates that a CRC32 error has been detected in the serial in data stream (receiving). This bit can be cleared by Master Reset or Line Reset or by writing a one to PR14[1]. Clearing of the RX CRC ERROR by writing a one to PR14[1] saves previously loaded USYRT and line control parameters.
PR14[2] TX CRC32 ERROR (Always 0 for DMS11-DA)	This read/write bit indicates that a CRC32 error has been detected during transmission of serial out data. This bit can be cleared by Master Reset, Line Reset or by writing a one to PR14[2]. Clearing of the TX CRC ERROR condition by writing a one to PR14[2] saves previously loaded USYRT and line control parameters.
ENABLE CRC32, PR14[3] (Not used on DMS11-DA)	This read/write bit, when set, enables CRC32 calculations to be performed on incoming or outgoing data. When cleared, data is passed through the CRC32 chip unchanged.

BIT NAME/DESIGNATION	DESCRIPTION
	NOTE Even though data is unchanged it is delayed by nine clock periods (bit times).
TENA, PR14[4]	Transmitter ENABLE (TXENA). This read/write bit, when written as a one allows processing of transmitter data. This bit must be true before any data transmission can take place.
MS [A,B,C], PR14[5:7]	Maintenance Select Bits. These read/write bits control the selection of maintenance clocks and allow the selected line to be placed in maintenance mode.

MSC PR14[7]	MSB PR14[6]	MSA PR14[5]	DESCRIPTION
0	0	0	This is the normal state for data transmission/reception. Clocks come from external modem and the USYRT is not in maintenance mode.
0	0	1	NOT USED (same operation as 000)
0 0	1 1	0 1	Single step mode MSC, MSB select single step mode. MSA is the state of the single step clock. This is primarily used in maintenance mode for diagnostics used with loop around maintenance connectors.
1	0	0	Internal clock mode. Data is received or transmitted at a rate determined by an on board RC oscillator.
1	0	1	NOT USED (same as 4)
1 1	1 1	0 1	This mode is also a single step mode with MSA being the state of the clock. This mode however switches the USYRT into an internal loop mode. In this mode, transmit serial out becomes receive serial in and transmit clock pulse becomes negated and used as receive serial clock.

3.2.4.6 Primary Register 15 -

Primary register 15 is unused at this time.

3.2.4.7 Primary Register 16 - TRANSMIT STATUS MULTIPLEXER -

This 8 bit read only register may be used as a quick transmit status check of all lines. The bits 0 through 7 correspond to the transmit status of lines 7 through 0 respectively. The actual transmit status consists of the "OR" of TBMT and TSA (explained in part 3.2.4.4). Hence one read gives the transmit status of all lines.

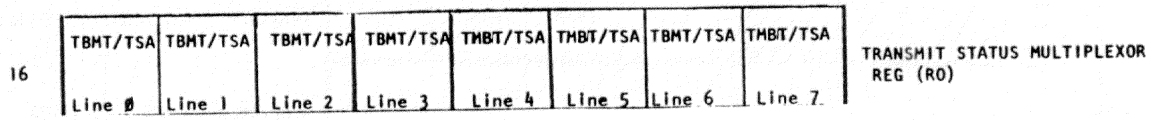


Figure 3-7 Transmit Status Multiplexer

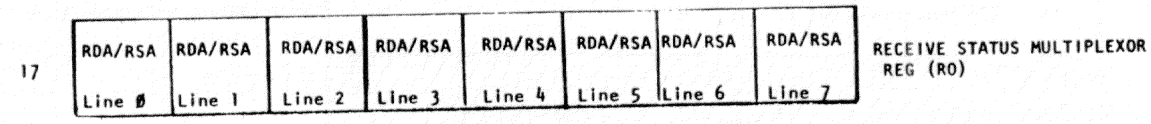


Figure 3-8 Receive Status Multiplexer

3.2.4.8 Primary Register 17 - RECEIVE STATUS MULTIPLEXER -

This 8 bit read only register is similar to the Transmit Status Multiplexer in all functions except that the information presented is the "OR" of RDA (receive data available) and RSA (receive status available)

3.2.5 Secondary Register Set Description

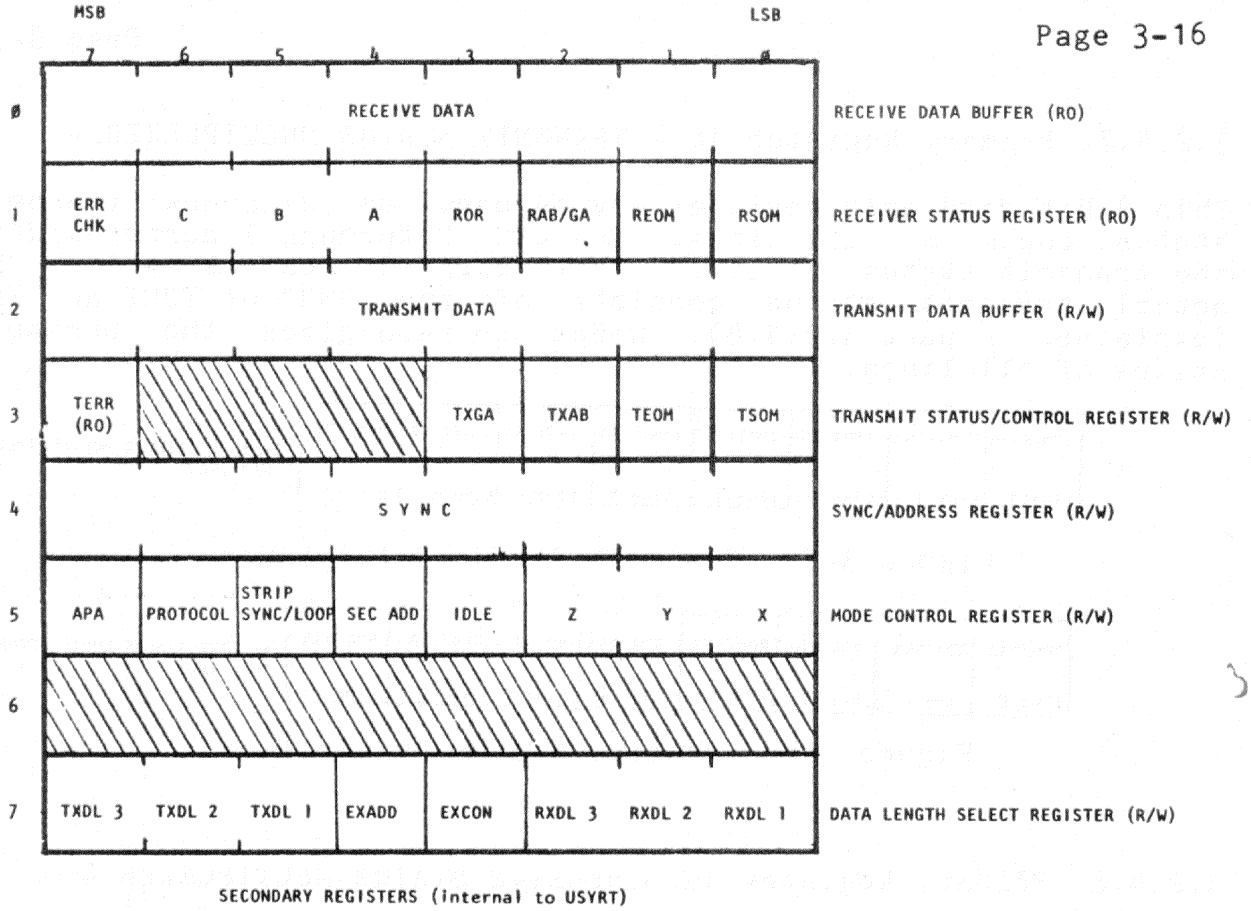


Figure 3-9 Secondary Registers

The Secondary Register Set consists of eight 8 bit registers internal to each USYRT chip. These registers control USYRT operation and allow readability of USYRT status. These registers are selected by Primary Registers 11 and 12, and are accessed through Primary Register 10, (Data Port Register). A brief explanation of these secondary registers follows.

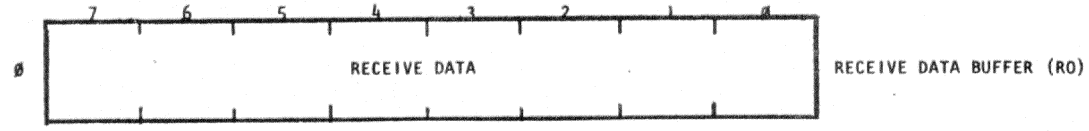


Figure 3-10 Receive Data Buffer

3.2.5.1 Secondary Register 0 - RECEIVE DATA BUFFER -

This eight bit read only register is the register from which receive data may be read. This may be read after PR13[0] RDA goes true indicating that receive data is available. This Register is cleared by RESET and is accessed via the data port Register (PR10).

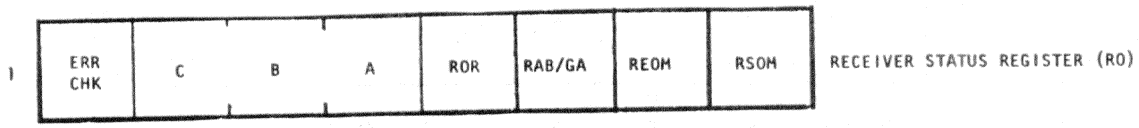


Figure 3-11 Receiver Status Register

3.2.5.2 Secondary Register 1 - RECEIVER STATUS REGISTER -

This eight bit read only register supplies basic status of the USYRT Read operation. This register is accessed via the data port Register (PR10).

BIT NAME	DESCRIPTION
RSOM SR1[0]	Receiver Start of Message-read only bit. In BOP mode only, goes high when first non-flag (address byte) character is loaded into RDB. It is cleared when the second byte is loaded into the RDB.
REOM SR1[1]	Receiver End of Message-read only bit. In BOP mode only, set high when last byte of data loaded into RDB, or when an ABORT character is received. It is cleared on reading of Receiver Status Register or dropping of RXENA.
RAB/GA SR1[2]	Received ABORT or GO AHEAD character, read only bit. In BOP mode only, if LM=0 this bit is set on receiving an ABORT character; if LM=1 this bit is set on receiving a GO AHEAD character. This is cleared on reading of Receive Status Register or dropping of RXENA.

BIT NAME	DESCRIPTION
ROR SR1[3]	Receiver Overrun Read Only Bit. Set high when received data transferred into RDB and previous data has not been read, indicating failure to service RDA within one character time. Cleared on reading Receiver Status Register or dropping of RXENA.
ABC SR1[4:6]	Assembled Bit Count-read only bits. In BOP mode only, examine when REOM=1. ABC=0, message terminated on stated boundary. ABC=XXX, message terminated (by FLAG or GA) on unstated boundary, binary value of ABC = number of valid bits available in RDB (right justified).
ERR CHK SR1[7]	Error Check-read only bit. In BOP mode set high if CRC 16 is selected and data was received in error, examine when REOM=1. In CCP mode: 1. set high if parity selected and received in error, 2. if CRC 16 selected (tested at end of each byte) ERR CHK = 1 if CRC GOOD, ERR CHK = 0 if CRC NOT GOOD. Controller must determine the last byte of the message. This is not used for CRC32.

3.2.5.3 Secondary Register 2 - TRANSMIT DATA BUFFER -

This 8 bit read/write register is the means of outputing parallel 8 bit data words to the USYRT for serial output. Typically this register is loaded with data when the USYRT is ready to accept data which is indicated by the assertion of TBMT PR13[4]. This register is cleared by RESET and is accessed via the data port Register (PR10). Data is Transmitted serially out of the USYRT LSB first.

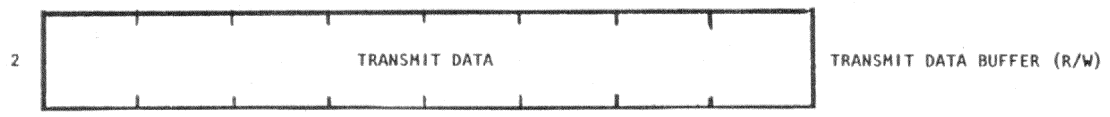


Figure 3-12 Transmit Data Buffer

3.2.5.4 Secondary Register 3 - TRANSMIT STATUS/CONTROL REGISTER -

This 8 bit read/write register supplies some status information and allows control of USYRT transmit operations. Bits [4:6] of this register are not used at this time. Note that although bits SR3[0:3] are read/write, TERR SR3[7] is read only.

Figure 3-13 Transmit Status/Control Register

BIT NAME	DESCRIPTION
TSOM SR3[0]	Transmitter Start of Message-W/R bit. Provided TXENA=1, TSOM initiates start of message. In BOP, TSOM=1 generates FLAG and continues to send FLAG's until TSOM=0, then begins to send data. In CCP:1. IDLE=0, transmit out of SYNC register, continue until TSOM=0 then begins data. 2. IDLE=1 transmit out of TDB. In BOP mode there is also a Special Space Sequence (SSS) of 16-0's initiated by TSOM=1 and TEOM=1. SSS is followed by FLAG.
TEOM SR3[1]	Transmit End of Message-W/R bit. Used to terminate a message. In BOP mode, TEOM=1 sends CRC, then FLAG; if TXENA=1 and TEOM=1 continue to send FLAG's, if TXENA=0 and TEOM=1 MARK line. In CCP:1. IDLE=0, TEOM=1 send SYNC, if TXENA=1 and TEOM=1 continue to send SYNC's, if TXENA=0 and TEOM-1 MARK line. 2. IDLE=1, MARK line.

BIT NAME	DESCRIPTION
TXAB SR3[2]	Transmitter Abort-W/R bit. In BOP mode only, TSAB=1 finish present character then: 1. IDLE=0, transmit ABORT 2. IDLE=1, transmit FLAG.
TXGA SR3[3]	Transmit Go Ahead-W/R bit. In BOP mode only modifies characters called for by TEOM. GA sent in place of FLAG. Allows loop termination-GA character.
TERR SR3[7]	Transmitter Error-read only bit. Underflow, set high when TDB not loaded in time to maintain continuous transmission. In BOP automatically transmit: 1. IDLE=0, ABORT 2. IDLE=1, FLAG In CCP automatically transmit: 1. IDLE=0, SYNC 2. IDLE=1, MARK. Cleard by TSOM.

3.2.5.5 Secondary Register 4 - SYNC/ADDRESS REGISTER -

This 8 bit read/write register is used as a holding register. In CCP mode it stores the sync character to be used by both the transmit and receive data path.

In BOP (Bit Oriented Protocol) mode this register will only be used if the "SEC ADD" (SR5[4]) bit is set. In this case the USYRT compares the first received eight bit character subsequent to the last leading Flag against the contents of this register. This register was previously loaded, under KMC11 control, with the appropriate address character. If the match is successful, this data is presented to the KMC11 as received data. If the match fails, the USYRT reverts to the idle state and continues to search for flag characters. This register is cleared by RESET.

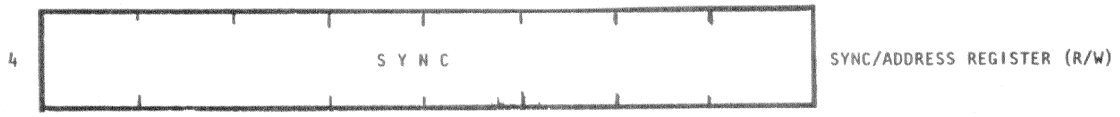


Figure 3-14 Sync Address Register

3.2.5.6 Secondary Register 5 - Mode Control Register -

This 8 bit read/write register is used to select the operating mode and characteristics of the USYRT. The only parameters which are not included within this register is the data length selection which appears in the Data Length Select Register. All bits of this register are cleared by reset.

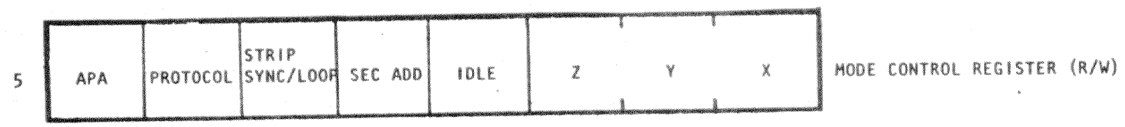


Figure 3-15 Mode Control Register

BIT NAME	DESCRIPTION
XYZ SR5[2:0]	Z Y X — W/R bits. These are the error control bits. 0 0 0 — X16+X12+X5+1 CCITT - Initialize to "1" 0 0 1 — X16+X12+X5+ 1 CCITT - Initialize to "0" 0 1 0 — Not Used 0 1 1 — X16+X12+X2+1 - CRC16 1 0 0 — Odd Parity-CCP Only 1 0 1 — Even Parity-CCP Only 1 1 0 — Not Used 1 1 1 — Inhibit all error detection Note: Do not modify XYZ until both paths are idle.
IDLE SR5[3]	IDLE mode select - W/R bit. Effects transmitter only. In BOP mode, this bit controls the type of character sent when TXAB asserted or in the event of data underflow. In CCP, it controls the method of initial SYNC character transmission and underflow, "1"=transmit SYNC from TDB, "0"=transmit SYNC from SYNC/ADDRESS register.
SEC ADD SR5[4]	Secondary Address Mode - W/R bit. In BOP mode only; after occurrence of a FLAG looks for address match prior to activating RDP. If no match is found, begin FLAG search again. SEC ADD bit should not be set if EXADD=1 or EXCON=1.
STRIP SYNC LOOP SR5[5]	Strip Sync or Loop Mode-W/R bit. Effects receiver only. In BOP mode, allows recognition of a GA character. In CCP, after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping.
PROTOCOL SR5[6]	PROTOCOL-w/r bit, BOP=0, CCP=1.
APA SR5[7]	All Parties Address-W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activiate the RDP.

3.2.5.7 Secondary Register 6 -

This Register has not been implemented.

3.2.5.8 Secondary Register 7 - DATA LENGTH SELECT REGISTER -

This 8 bit read/write register is used to control the character length selection of the USYRT's data paths. This selection can vary from one to eight bits for each data path in BOP mode and from five to eight bits in CCP mode.

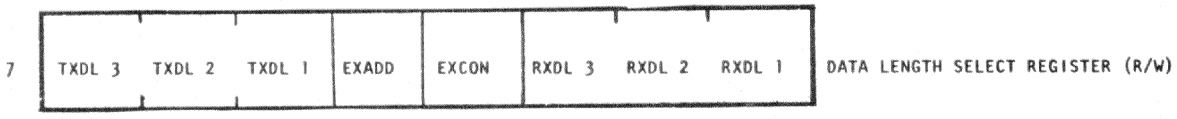


Figure 3-16 Data Length Select Register

<table>
<tr><th>BIT NAME</th><th>DESCRIPTION</th></tr>
<tr><td>TXDL 1,2,3</td><td>Transmitter Data Length-W/R bits.

<table>
<tr><th>TXDL3</th><th>TXDL2</th><th>TXDL1</th><th>LENGTH</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Eight bits per character</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Seven bits per character</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Six bits per character</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Five bits per character</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Four bits per character*</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Three bits per character*</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two bits per character*</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One bit per character*</td></tr>
</table>

*For data length only, not to be used for SYNC character (CCP mode).</td></tr>
<tr><td>RXDL 1,2,3</td><td>Receiver Data Length-W/R bits.
<table>
<tr><th>RXDL3</th><th>RXDL2</th><th>RXDL1</th><th>LENGTH</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Eight bits per character</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Seven bits per character</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Six bits per character</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Five bits per character</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Four bits per character</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Three bits per character</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two bits per character</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One bit per character</td></tr>
</table></td></tr>
</table>

BIT NAME	DESCRIPTION
EXCON	Extended Control Field-W/R bit. In receiver only; if set will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1.
EXADD	Extended Address Field-W/R bit. In receiver only; LSB of address byre tested for a "1". If NO - continue receiving address bytes, if YES go into control field. EXADD bit should not be set if SEC ADD = 1.

3.3 FIRMWARE - AN OVERVIEW

Operation of the KMC11 microprogram is initiated and directed by a user-produced program residing in the main CPU memory space. Communication between the user program and KMC11 firmware is provided by a set of four control and status registers (CSR's), which are integral to the KMC-11 microprocessor. These four 16-bit registers are used for control input, status output, and data input and output.

The two low bytes in the first two registers in this group have a fixed format and serve as the command header for the second two registers. The second two registers form a two-word data port for the exchange of unique control/status commands between firmware and the user program. The contents of the data port are specified by an identification field in the command header. Other specific fields in the two-word command header control interrupt enabling, set up data transfers between the main CPU and the KMC11, and identify the communications line of interest. The second byte of the first word is used to contain a special command issued by the user program for implementing microprocessor start, halt and initialization. (Detailed descriptions of each field in these four words for Modes I, & VI, Autodin are presented in AUTODIN II DESIGN SPECIFICATIONS).

A user program issues a command to KMC11 by storing the command in the pertinent CSR's. The firmware then interprets the command and performs the specified actions. Similarly, firmware issues a command to the user program by storing the command in the pertinent CSR's and notifying the user program that a command is available for retrieval and execution.

Message data received or transmitted by KMC11 is written into or read from user program assigned buffers in the main CPU memory. KMC11 accesses these buffers through Non Processor Requests (NPR) to a UNIBUS address. A UNIBUS address is defined as an 18-bit address of a main CPU memory location which has been reserved for use by an NPR device.

3.3.1 Command Structure

The functions of the six firmware control/status/data commands are described in the sections that follow.

3.3.1.1 INITIALIZATION Command -

The purpose of the single byte INITIALIZATION commmand is to clear all condition sensitive logic in the KMC-11 microprocessor in the RUN state. This command must be issued by the user program once prior to starting the initialization procedure.

3.3.1.2 LINE INITialization Command -

This command is used to initialize each line supported by the specific DMS11 and performed once, generally at start-up time, for each supported KMC11/DMS11 pair. This command informs the KMC11 of line dependant characteristics and assigns a communications line number for each active DMS11. It is also used to inform the KMC11 of cross-line (line independent) characteristics and control information.

3.3.1.3 CONTROL IN Command -

This command would force control action to be taken by the firmware. Such commands would be abort, resync, or force control sequences, and request for line status.

3.3.1.4 BUFFER ADDRESS IN Command -

The user program issues this control command to a KMC11 to assign a new buffer to the designated line. A BUFFER ADDRESS IN command points to and defines only one user defined buffer, and this command must be repeated for each buffer paired to the KMC11. The user program can assign a maximum of two receive and two transmit buffers to each communications line.

The command contains the line number, the starting buffer address (expressed as an 18 bit Unibus address) the character or word count and a single bit control, which can be used for different purposes within each mode. Upon completion of each transmit or receive operation, the firmware returns with the ending memory address and the reason for termination.

3.3.1.5 BUFFER ADDRESS OUT Command -

The firmware issues this control command to the user program when the buffer assigned to a transmit or receive operation is terminated. Generally, a transmit or receive buffer is terminated when the buffer is full (byte count = zero). The first word in the data port for this command always contains the first 16 bits of UNIBUS address for the pertinent buffer with the two extension bits contained in the high order byte of the second word in the port. The reason for termination is given in the lower order byte of the second word. This is expressed as a signed octal number 377 - 177. Negative values represent failure to terminate the buffer successfully.

3.3.1.6 CONTROL OUT Command -

The firmware issues this status command to the main CPU when it detects a transmit or receive error, or on request by the CPU. A control out command is returned whenever there is no buffer available for informational purposes or when there is no need to terminate a buffer. An example of this is sync detect. It is also used to pass up to 16 bits of control information imbedded within a data stream.

3.3.2 Data Transfer Operations

For the purposes of this system overview, the transmit and receive data command sequences described in this section are general and are meant to serve as background for the detailed presentations in the chapters that follow.

3.3.2.1 Initialization Sequence -

After the KMC11 microprogram is loaded, the first action taken by the user program is to issue an INITIALIZATION command which performs a Master Clear on the KMC-11 microprocessor and places the processor in the Run state. With this action complete, KMC11 firmware is ready to accept the first command from the user.

3.3.2.2 Line Initialization Sequence -

This command typically, is a LINE INIT to the LINE designated as device zero. This command establishes the various characteristics of the line, assigns it a line number and enables the line for subsequent transmission and reception. Following this initial command, the user program must issue one LINE INIT command for each addtional DMS11 supported by the KMC11.

3.3.2.3 Receive/Transmit Sequence -

Once the user program has initialized each line interface through LINE INIT commands, the firmware is ready to perform a receive or transmit data operation.

An actual reception or transmission is initiated when the user program issues a BUFFER ADDRESS IN command. Each line requires a buffer assignment through a BUFFER ADDRESS IN command in order to initiate a data transfer.

When a buffer is assigned, it is designated for either reception or transmission.

The firmware informs the user program of a normal data transfer termination by issuing a BUFFER ADDRESS OUT command. The FIRMWARE terminates a normal data transfer operation for one of two reasons: the buffer designated by the last buffer descriptor has been filled or an End-of-Message sequence has been detected. If a transmission or reception error is detected, the firmware informs the user program of the error by issuing a BUFFER OUT command containing the code designating the error condition.

CHAPTER 4

THEORY OF OPERATION

4.1 GENERAL

The DMS11-D(A) Line card is a hex height multilayer module capable of controlling synchronous communication transfers on 8 lines concurrently running at 56Kbd when used with KMC11-B. Only a single line at 56Kbd may be run when the KMC11-A is used. The DMS11-D(A) is controlled by the KMC11 microprocessor and has no direct Unibus connection.

The logic can be divided into six basic functional areas:

OBUS Interface - Interface to KMC11 output bus
IBUS Interface - Interface to KMC11 input bus
LINE SELECT/CONTROL - Control/Select of 1 of 8 lines
REGISTER 14 MUX - Multiplexes line status to KMC11 IBUS.
LINE INTERFACE - Line specific control/status
MISC - POWER, clock, cable connectors.

The following is an in depth presentation of logic operation.

4.2 CIRCUIT DESCRIPTION

The following description will be in reference to the DMS11-D circuit diagrams and the block diagram. The basic data flow diagram indicates that data is output under KMC11 control in 8 bit bytes in a parallel fashion. The selected USYRT then converts the parallel data to serial data and directs it to the CRC32 chip, which computes a CRC32 check character and appendsit to the end of message (if enabled) (BOP, Mode VI Autodin) and shifts it out through an EIA RS423 driver to the modem. In the receive direction, data comes in serially through the EIA RS423 receiver, the CRC32 chip and then into the selected USYRT. For the variation without CRC32, the data flows directly into/out of the USYRT.

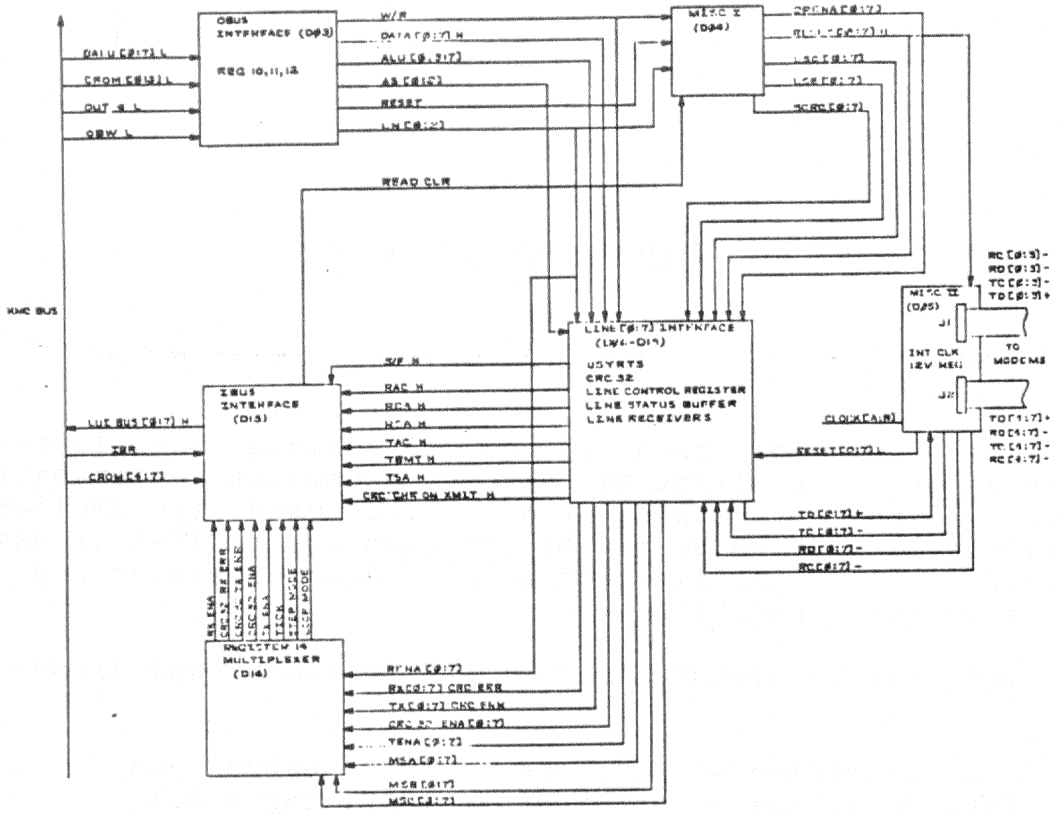


Figure 4-1 DMS11-D Block Diagram

4.2.1 Block Diagram

This is the function block diagram and microprocessor interconnect page. The attempt here, is to show the simplicity of the line unit while showing the functional relationships of the blocks of logic.

4.2.2 OBUS Interface

This page contains the interface to the KMC11 OBUS (write bus), as well as primary registers 10, 11, and 12. The one of eight decoder accepts the register address selection bits (CROM[0:3]), the output strobe (OBW trailing edge strobe), the bus select bit (OUT*), and produces the appropriate decoded register clock load pulses (Figure 4-2).

The KMC data bits (BALU[0:7]) are buffered and inverted to produce ALU[0:7] (true HI) which are then distributed to the internal logic on a tri-state bus.

Register 10 is the DATA PORT REGISTER. This register is read/write and may be considered a "window" into the secondary register selected by register 12. After a secondary register (a secondary register is one of eight control registers actually contained within the USYRT chip) is selected, data may be written into [or read from] the selected secondary register via a write [read] from register 10.

Register 11 is the LINE SELECT REGISTER. Bits ALU[4:6] are written into register 11 as LN[0:2], thereby selecting the desired line. Register 11 bits [0:3,7] are unused. Register 11 bits [4:6] (or LN[0:2]) may be written or read.

Register 12 is the SECONDARY REGISTER SELECT REGISTER. This register selects which secondary register (internal USYRT register) you wish to access and whether you want to write into it or read from it. ALU[5:7] may be written or read as secondary register select bits AS[0:2]. ALU[4] is the USYRT W/R bit. This bit may be read or written . A logic H indicates that a write will be performed to the selected secondary register, while a logic L indicates a read. ALU[0] is a write only bit which resets the selected line to the initialzed state. The signal which actually enables data in to and out of the USYRT ("DPENA") is initiated by "DELAYED SEL 12" or "DELAYED SEL 10" which originate on this page. These two signals are delayed to allow setup time of the AS[0:2], and the W/R bits at the USYRT input before the strobe occurs.

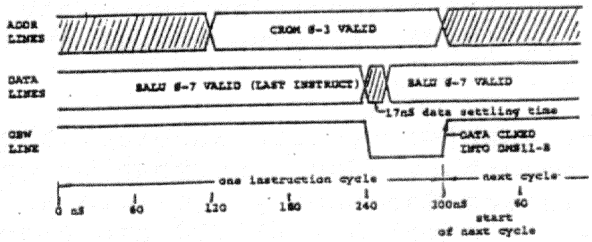


Figure 4-2 Typical KMC11A Out Bus Timing

4.2.3 MISC I

The logic functions performed on this page are as follows:

Individual line reset RESET[0:7] H.
Line unit reset.
Clocking of individual line control register LCS[0:7] L.
Decode of individual line select signal LSE[0:7] L.
Clocking of individual CRC32 select SCRC[0:7] L.
Origination of individual DPENA pulse DPENA[0:7] H.

The reset logic consists of two individual input path with a common tri-state output path. This logic must cause an individual line reset or a common reset (all lines) with a minimum duration of 500 ns. The common reset can only be initiated by the KMC11 "clear" line or a power up condition. This signal initiates a 500 ns. pulse from the CLEAR TIMER one-shot which simultaneously raises all eight reset lines. An individual line reset is caused by writing the selected line number into register 12 along with the "LINE RESET" bit set. This "RESET" bit is loaded into a flip flop by "DELAYED SEL 12 L". The RESET TIMER is then triggered, which initiates a 250 ns. "T CLEAR" pulse thereby causing the selected lines "RESET" pulse.

The LINE CONTROL STROBE logic is a one of eight decoder that initiates the pulse which clocks the data into the LINE CONTROL REGISTER for the selected line (this is what is written into or read from register 14). Register 14 contains; maintenance clock select bits, USYRT transmit enable, USYRT receive enable, receive and transmit CRC error flags, and CRC32 enable bit.

The LINE SELECT DECODER is basically a one of eight decoder which enables the selected LINE STATUS BUFFER (see line interface pages) data onto the tri-state status bus which then becomes input data for the IBUS MULTIPLEXERS and the KMC11.

The CRC32 SELECT logic (DMS11-D only) is also a one eight decoder, but this creates a clock pulse which loads the present state of the "CRC32 MODE" (register 13 bit 5) bit into the selected lines "check on transmit" flop. Register 13 explained in section 3.2.4.4 is the LINE STATUS REGISTER. Individual line status information may be read via register 13. Register 13 contains; transmit status available (TSA), transmit active (TAC, CRC32 check on transmit, transmit buffer empty (TBMT), sync flag (S/F), receive active (RAC), receive status available (RSA), and receive data available (RDA).

The DPENA (dataport enable) decoder supplies the strobe to the USYRT which is necessary for any read or write to any of the internal USYRT registers (secondary registers).The DPENA logic decodes the line selected by LN[0:2] and asserts DPENA for any read or write of an internal USYRT register.

The sequence for writing an internal USYRT register via primary register 10 is as follows: Via PR12 the AS[0:2] must be set to indicate which secondary register you wish to access and the W/R bit must be set to indicate the fact that you will be writing into register 10 (this is true for any secondary register). This W/R signal will now be present at the input of all USYRTS; however without DPENA, no action is taken by the USYRTS. The data is actually output to register 10 which in turn is presented at the data inputs of the USYRT chips, "DELAYED SEL 10" strobes the DPENA decoder with a 250ns. pulse which actually loads the data into the selected secondary register of the selected USYRT. This DPENA pulse is of fixed length determined by a 9602 one shot.

The sequence for a read of register 10 is initiated by first loading register 12 with the desired secondary register AS[0:2] and the W/R bit low (indicating a read from the selected secondary register). "DELAYED SEL 12" clocks the state of the W/R bit which then causes the selected DPENA signal. This will stay high until register 10 is read. At this time the KMC11 bus signal "IBR" in conjunction with register 10's address on the CROM[4:7] lines initiates "READ CLEAR" which resets the READ ENABLE flop and drops DPENA, thereby terminating the read operation.

4.2.4 MISC II

This page contains the maintenance clock circuitry, 12 volt regulators, a reset decoder, and the two fifty pin berg connectors for connection to eight external modems.

The voltage regulators supply constant 12 volts to the level converters and the USYRTS. The maintenance clock consists of two TTL inverters operating in the linear region at approximately 112khz which is halved to provide approximately 56kb for use by internal circuitry. The oscillator frequency varies from 80KHz to 120KHz depending on components.

4.2.5 PAGES 6-13 Line Interface

These eight pages contain eight identical logic circuits which are used by each line. Each line circuit contains: a line control register (register 14), clock multiplexer, line status buffer, level converters, synchronous communications chip (USYRT), and a CRC32 chip.

The LINE CONTROL REGISTER consists of a hex D flop, one additional flip flop and the CRC32 chip. The above components store and/or provide data for a write/read to primary register 14 for the selected line.

The clock multiplexer selects which type of clock will be used to drive the USYRT chip by the states of MSA, MSB, and MSC. The choices are:

MSC	MSB	MSA	SELECTED CLOCK
0	0	X	Modem clock; (external)
0	1	1	State of clock follows the state of MSA bit.
0	1	0	
1	0	X	Places USYRT in internal loopback and allows internal free running maint. clock.
1	1	0	Internal USYRT loopback with clock following state of MSA.
1	1	1	

When pin 40 of the USYRT is HI, "maintenance mode" is initiated. This mode simply loops transmit data back to the receive data.

NOTE

This is done internal to the chip and the data is therefore not accessible at the transmit pin (TSO pin 38) of the USYRT.

The LINE STATUS BUFFER is a tristate octal buffer which is enabled by the previously mentioned line select decoder. The LINE STATUS BUFFER distributes the USYRT status which is always available (ie. without accessing internal USYRT registers) to the LUI BUS multiplexers.

4.2.5.1 Universal Synchronous Receiver/Transmitter Chip (USYRT) -

The USYRT itself is a 40 pin LSI serial communications chip that contains the serial to parallel, parallel to serial, bit stuffing, CRC computing (16 bit), control logic. The USYRT contains eight internal registers (referred to as secondary registers in this document) that are accessed through the bidirectional tristate bus. The individual internal registers are selected through primary register 12 bits [5:7]; the write bit ([4]) controls the transfer direction, and the DPENA signal is considered the strobe. The timing constraints are such that a data setup time is required when reading or writing the USYRT. This is the reason for the "DELAYED SEL 10 (waiting for W/R bit to be setup before the DPENA strobe). The DPENA signal for writing is a pulse with a minimum required width of 250ns. The DPENA pulse for reading has a required settle time of 150ns. before data can be guaranteed valid.

In order to allow the KMC11 to run at maximum speed, a psuedo protocol between the KMC and line unit was implemented in

hardware as follows: The KMC writes into register 11 and 12 what it intends to do with the USYRT. After one NOP the KMC can do what it had intended, (the NOP is due to the required USYRT setup time) for example, assume a write to the Line Unit transmitter control register (internal USYRT register 3). First, the KMC11 writes the line number , W/R bit, and address select bits into register 11 and 12. Then the KMC11 writes the desired data into register 10. A delay of one instruction time is necessary between a setup of register 12 for a read and the actual input instruction. This is due to the required length of the DPENA signal for correct USYRT operation. The serial data is then shifted out of the USYRT LSB first.

The USYRT is an important part of the DMS11D line unit. The above information assumes knowledge of this component. Appendix B provides the 5025 USYRT specifications in its entirety for a more detailed description of internal USYRT operaton and capabilities.

4.2.5.2 CRC32 Chip (DMS11-D Only) -

The CRC32 chip is an LSI 20 pin chip which is placed in the serial data stream for CRC32 calculation on the serial data. This chip is capable of various operations depending on the state of the two control leads. One lead is the ENABLE; when this is low, serial data is passed through the device with no alteration or calculation. Serial in to serial out delay is nine bit times. When the enable pin is HI, operation is selected by the state of the "CRC32 MODE" bit. This is bit [5] of primary register 13. With this bit LOW the CRC32 chip is in "CRC generate mode".CRC calculations begin upon receipt of the first data character after an opening flag character. Upon detection of a closing flag character, the CLOCK OUT lead is disabled, and the CRC accumulation is shifted out with the closing flag. If this bit is a HI, the chip is in "CRC check mode". CRC calculations begin upon receipt of the first data character after an opening flag character. Upon detection of a closing flag character, the ERROR CHECK LATCH is enabled. If the incoming CRC does not cause the calculation to reach the proper remainder, the latch will set, and remain set until the ERROR RESET lead is strobed (register 12 bit [0]).This mode is intended to be used in applications where the CRC32 check character is known and already a part of the data stream, (ie. for the reception and checking of CRC32). This chip is used for bit oriented protocol only. The CRC32 character, appended to the data stream in generate mode, is shifted out MSB first byte by byte.

4.2.6 Register 14 Multiplexer

This page contains eight eight-to-one multiplexers which multiplex status from all eight lines onto the LUI BUS multiplexers. The output selected is determined by the state of register 11 bits[4:6] (LN[0:2]).

4.2.7 IBUS Interface

This logic multiplexes all readable data to the KMC via the LUI BUS. All eight primary registers are multiplexed onto the LUI BUS as LUI BUS[0:7]. The registers are selected by the state of CROM[4:6] during a read.The READ CLEAR signal is generated from the bus IBR and a read from register 10 (dataport register). This READ CLEAR pulse clears the "read enable" flip flop on page MISC I.

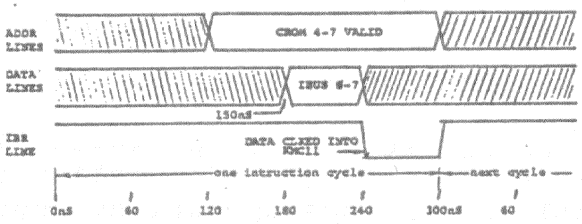


Figure 4-3 KMC11 Input Timing

CHAPTER 5

MAINTENANCE

5.1 GENERAL

In general, the DMS11D(A) consists of control logic and multifunction LSI integrated circuits, such as the USYRT and CRC32 chips. Because the board can be divided into control logic and 8 identical line interface circuits, it becomes much more straight forward to troubleshoot.

5.2 FAULT ISOLATION

Fault isolation can be accomplished by using standard troubleshooting techniques. Proper selection of diagnostic parameters will allow you to localize the fault to the logic that controls all lines, that is, a fault common to all lines, or to the logic concerned with a specific line. Typically, a control logic failure will be a basic failure; one which doesn't allow you to read or write or clear a particular register or group of registers. This type of problem can usually be found to be a loss in signal flow between the KMC11 OBUS/IBUS and the USYRT chip itself. A fault which has been isolated to a particular line through proper diagnostic parameter selection is even more straight forward in that the failing line can be compared with a working line. After some familiarization with the module and USYRT operation a problem may be localized to a USYRT failure by diagnostic printouts. An example of this might be a single line in which you cannot write some secondary register however, other secondary registers can be loaded properly. Since all lines use common circuitry up to the point of USYRT entry, this fault, in all probability, should be a faulty USYRT (assuming diagnostics have run in the past).

5.3 DIAGNOSTIC SOFTWARE

It is assumed that the KMC11 being used has passed the appropriate diagnostics. The two diagnostics used for fault isolation on the DMS11D(A) are YM-Z136D-10 static test (BCRAD for Autodin) and YM-Z136D-20 Dynamic Test (BCRBD for Autodin). These two diagnostics test both the hardware and firmware for proper operation.

5.3.1 Static Diagnostic

YM-Z136D-10
DECSPEC-11-BCRAD for AUTODIN

As the name implies, YMZ136D-10 (BCRAD) tests the functionality of the DMS11-D(A) in a static mode; that is by using the internal maintenance mode of the USYRT and a program controlled single step clock. The internal maintenance mode wraps data and clock back inside the USYRT, therefore data will not be visible at the "TSO" output of the USYRT during various tests.

The static diagnostic proceeds through various register load/read tests to actual data transfers, checking line status after pertinent clock ticks. This diagnostics tests virtually all the line unit logic in a single step fashion, except the CRC32 chip and the RS423 Line Driver Receivers.

YMZ136D-10 (BCRAD) allows KMC11 instruction execution by loading single instructions into KMC11 registers in a single instruction step mode. No KMC11 firmware is loaded or tested during this test. This diagnostic has the capability of testing individual lines and selecting individual tests. Both of these features facilitate fault isolation.

5.3.2 Dynamic Diagnostic

YM-Z136D-20
DECSPEC-11-BCRBD for AUTODIN

The dynamic diagnostic assumes YMZ136D-20 Static Test (BCRAD) runs without errors. This high level diagnostic, through operator commands, allows testing of lines singly or concurrently. YMZ136D-20 (BCRBD), through appropriate operator commands, loads the firmware and then hardware and firmware interaction at data rates determined by an on board RC oscillator.

The dynamic nature of this diagnostic simulates an application software routine reading and writing data buffers. With proper

switch settings, this diagnostic can be used with or without the external loopback connector (internal or external) however good practice suggest running this diagnostic with the loopback connector installed to allow checkout of the CRC32 chip and basic line driver/receiver combinations.

5.4 PREVENTIVE MAINTENANCE

Periodicly run both the Static and Dynamic diagnostics to verify the DMS11-D(A) operation.

5.5 SPECIAL ADJUSTMENTS

There are no special adjustments for operation of this option. All jumpers and variations are set at the factory and should not be changed.

CHAPTER 6

CSS BUILT PARTS

6.1 MODULE M8711 (M8711-YA)

This board is the line module of the DMS11-D (DMS11-DA) line unit. It is available through Computer Special Systems, Nashua N.H.

6.2 DMS11-D TEST CONNECTORS

The test connector (loopback jumper) used to test DMS11-D operation under diagnostics is available by ordering P/N 2ME044B. Two test connectors are shipped with the DMS11-D(A).

APPENDIX A

SHIPPING/ACCESSORIES LIST

A.1 EQUIPMENT FURNISHED

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

SHIPPING LIST

ITEM NO	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION		
			DMS11-D (AUTODIN)	DMS11-D	DMS11-DA
1	YM-C061C-00	DMS11-D OPTION DESC.	1	1	1
2	D-UA-M8711-0	DMS11-D DWG. SET	1	1	1
3	DECSPEC-11-BCRAD	DMS11-D STATIC TEST MEDIA (AUTODIN)	1	-	-
4	DECSPEC-11-BCRAD	DMS11-D LISTING (AUTODIN)	1	-	-
5	DECSPEC-11-BCRBD	DMS11-D DYNAMIC TEST MEDIA (AUTODIN)	1	-	-
6	DECSPEC-11-BCRBD	DMS11-D DYNAMIC TEST LISTING (AUTODIN)	1	-	-
7	YM-Z136D-10	DMS11-D STATIC TEST MEDIA	-	1	1
8	YM-Z136E-10	DMS11-D STATIC TEST LISTING	-	1	1
9	YM-Z136D-20	DMS11-D DYNAMIC TEST MEDIA	-	1	1
10	YM-Z136E-20	DMS11-D DYNAMIC TEST LISTING	-	1	1
11	M8711	DMS11-D SYNCH LINE UNIT (CRC32)	1	1	-
12	M8711-YA	DMS11-DA SYNCH LINE UNIT (CRC16)	-	-	1
13	2ME044B	Test Conn.	2	2	2
14	BC03R-01	KMC11 to DMS11 Interconnect Cable	1	1	1

TITLE: DMS11-D 8 Line Synchronous Line Unit

DOCUMENT NUMBER: YM-C061C-00

REV.: A

APPENDIX B

SPECIFICATIONS FOR COMPLEX CIRCUITS

SMC Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
(516) 273-3100
TWX: 510-227-8898

A Standard Microsystems Company

COM 5025
μPC FAMILY

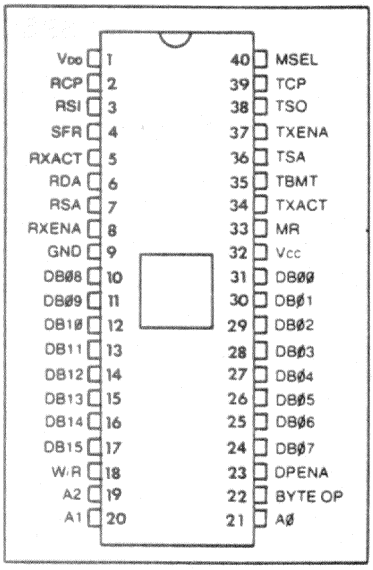
Multi-Protocol Universal Synchronous Receiver/Transmitter

USYNR/T

FEATURES

- ☐ Selectable Protocol—Bit or Byte oriented
- ☐ Direct TTL Compatibility
- ☐ Tri-state Input/Output Bus
- ☐ Processor Compatible—8 or 16 bit
- ☐ High Speed Operation—2.0M Baud—typical
- ☐ Fully Double Buffered—Data, Status, and Control Registers
- ☐ Full or Half Duplex Operation—independent Transmitter and Receiver Clocks
  —individually selectable data length for Receiver and Transmitter
- ☐ Master Reset—resets all Data, Status, and Control Registers
- ☐ Maintenance Select—built-in self checking

PIN CONFIGURATION



BIT ORIENTED PROTOCOLS—SDLC, HDLC, ADCCP

- ☐ Automatic bit stuffing and stripping
- ☐ Automatic frame character detection and generation
- ☐ Valid message protection—a valid received message is protected from overrun
- ☐ Residue Handling—for messages which terminate with a partial data byte, the number of valid data bits is available

SELECTABLE OPTIONS:

- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —None
- ☐ Primary or Secondary Station Address Mode
- ☐ All Parties Address—APA
- ☐ Extendable Address Field—to any number of bytes
- ☐ Extendable Control Field—to 2 bytes
- ☐ Idle Mode—idle FLAG characters or MARK the line
- ☐ Point to Point, Multi-drop, or Loop Configuration

BYTE ORIENTED PROTOCOLS—BiSync, DDCMP

- ☐ Automatic detection and generation of SYNC characters

SELECTABLE OPTIONS:

- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Variable SYNC character—5, 6, 7, or 8 bits
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —VRC (odd/even parity)
  —None
- ☐ Strip Sync—deletion of leading SYNC characters after synchronization
- ☐ Idle Mode—idle SYNC characters or MARK the line

APPLICATIONS

- ☐ Computer to Modem Interface
- ☐ Modem to Computer Interface
- ☐ Terminal to Modem Interface
- ☐ Modem to Terminal Interface
- ☐ Peripheral to Modem Interface
- ☐ Modem to Peripheral Interface
- ☐ Serial Data Bus

General Description

The COM 5025 is a COPLAMOS® n channel silicon gate MOS/LSI device that meets the majority of synchronous communications requirements, by interfacing parallel digital systems to synchronous serial data communication channels while requiring a minimum of controller overhead.

The COM 5025 is well suited for applications such as computer to modem interfaces, computer to computer serial links and in terminal applications. Since higher level decisions and responses are made or initiated by the controller, some degree of intelligence in each controller of the device is necessary.

Newly emerging protocols such as SDLC, HDLC, and ADCCP will be able to utilize the COM 5025 with a high degree of efficiency as zero insertion for transmission and zero deletion for reception are done automatically. These protocols will be referred to as Bit Oriented Protocols (BOP). Any differences between them will be discussed in their respective sections. Conventional synchronous protocols that are control character oriented such as BISYNC can also utilize this device. Control Character oriented protocols will be referred to as CCP protocols. Other types of protocols that operate on a byte or character count basis can also utilize the COM 5025 with a high degree of efficiency in most cases. These protocols, such as DDCMP will also be referred to as CCP protocols.

The COM 5025 is designed to operate in a synchronous communications system where some external source is expected to provide the necessary received serial data, and all clock signals properly synchronized according to EIA standard RS334. The external controller of the chip will provide the necessary control signals, intelligence in interpreting control signals from the device and data to be transmitted in accord with RS334.

The receiver and transmitter are as symmetrical as possible without loss of efficiency. The controller of the device will be responsible for all higher level decisions and interpretation of some fields within message frames. The degree to which this occurs is dependent on the protocol being implemented. The receiver and transmitter logic operate as two totally independent sections with a minimum of common logic.

References:

1. ANSI—American National Standards Institute
   X353, XS34/589
   202-466-2299
2. CCITT—Consultative Committee for International
   Telephone and Telegraph
   X.25
   202-632-1007
3. EIA—Electronic Industries Association
   TR30, RS334
   202-659-2200
4. IBM
   General Information Brochure, GA27-3093
   Loop Interface—OEM Information, GA27-3098
   System Journal—Vol. 15, No. 1, 1976; G321-0044

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}−1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V_{OL}			0.4	V	I_{OL}=1.6ma
High Level, V_{OH}	2.4				I_{OH}=40μa
INPUT LEAKAGE					
Data Bus		5.0	10.0	μa	0≤V_{IN}≤5v, DPENA=0 or W/R=I
All others				μa	V_{IN}=+5v
INPUT CAPACITANCE					
Data Bus, C_{IN}				pf	
Address Bus, C_{IN}				pf	
Clock, C_{IN}				pf	
All other, C_{IN}				pf	
POWER SUPPLY CURRENT					
I_{CC}				ma	
I_{DD}				ma	
A.C. Characteristics					T_A=25°C
CLOCK-RCP, TCP					
frequency		2.0		MHz	
PW_H		250		ns	
PW_L		250		ns	
t_r, t_f		10		ns	
DPENA, T_{WDPENA}		350	50 μs	ns	
Set-up Time, T_{AS}		100		ns	
Byte Op, W/R					
A_2, A_1, A_0					
Hold Time, T_{AH}		60		ns	
Byte Op, WIR,					
A_2, A_1, A_0					
DATA BUS ACCESS, T_{DPA}		250		ns	
DATA BUS DISABLE DELAY, T_{DPD}		50		ns	
DATA BUS SET-UP TIME, T_{DBS}		100		ns	
DATA BUS HOLD TIME, T_{DBH}		60		ns	
MASTER RESET, MR		300		ns	

Description of Pin Functions

Pin No.	Symbol	Name	I/O	Function
1	V_{DD}	Power Supply	PS	+12 volt Power Supply.
2	RCP	Receiver Clock	I	The positive-going edge of this clock shifts data into the receiver shift register.
3	RSI	Receiver Serial Input	I	This input accepts the serial bit input stream.
4	SFR	Sync/Flag Received	O	This output is set high, for 1 clock time of the RCP, each time a sync or flag character is received.
5	RXACT	Receiver Active	O	This output is asserted when the RDP presents the first data character of the message to the controller. In the BOP mode the first data character is the first non-flag character (address byte). In the CCP mode: 1. if strip-sync is set; the first non-sync character is the first data character 2. if strip-sync is not set; the first data character is the character following the second sync. In the BOP mode the trailing (next) FLAG resets RXACT. In the CCP mode RXACT is never reset, it can be cleared via RXENA.
6	RDA	Receiver Data Available	O	This output is set high when the RDP has assembled an entire character and transferred it into the RDB. This output is reset by reading the RDB.
7	RSA	Receiver Status Available	O	This output is set high: 1. CCP—in the event of receiver over run (ROR) or parity error (if selected), 2. BOP—in the event of ROR, CRC error (if selected) receiving REOM or RAB/GA. This output is reset by reading the receiver status register or dropping of RXENA.
8	RXENA	Receiver Enable	I	A high level input allows the processing of RSI data. A low level disables the RDP and resets RDA, RSA and RXACT.
9	GND	Ground	GND	Ground
10	DBØ8	Data Bus	I/O	Bidirectional Data Bus.
11	DBØ9	Data Bus	I/O	Bidirectional Data Bus.
12	DB1Ø	Data Bus	I/O	Bidirectional Data Bus.
13	DB11	Data Bus	I/O	Bidirectional Data Bus.
14	DB12	Data Bus	I/O	Bidirectional Data Bus.
15	DB13	Data Bus	I/O	Bidirectional Data Bus.
16	DB14	Data Bus	I/O	Bidirectional Data Bus.
17	DB15	Data Bus	I/O	Bidirectional Data Bus. "OR" with DPØ7.
18	W/R	Write/Read	I	Controls direction of data port. W/R=1, Write. W/R=0, Read.
19	A2	Address 2	I	Address input—MSB.
20	A1	Address 1	I	Address input.
21	AØ	Address 0	I	Address input—LSB.
22	BYTE OP	Byte Operation	I	If asserted, byte operation (data port is 8 bits wide) is selected. If BYTE OP=0, data port is 16 bits wide.
23	DPENA	Data Port Enable	I	Strobe for data port. After address, byte op, W/R and data are set-up DPENA may be strobed. If reading the port, DPENA may reset (depending on register selected by address) RDA or RSA. If writing into the port, DPENA may reset (depending on register selected by address) TBMT.
24	DBØ7	Data Bus	I/O	Bidirectional Data Bus—MSB.
25	DBØ6	Data Bus	I/O	Bidirectional Data Bus.
26	DBØ5	Data Bus	I/O	Bidirectional Data Bus.
27	DBØ4	Data Bus	I/O	Bidirectional Data Bus.
28	DBØ3	Data Bus	I/O	Bidirectional Data Bus.
29	DBØ2	Data Bus	I/O	Bidirectional Data Bus.
30	DBØ1	Data Bus	I/O	Bidirectional Data Bus.
31	DBØØ	Data Bus	I/O	Bidirectional Data Bus—LSB.
32	V_{CC}	Power Supply	PS	+5 volt Power Supply.
33	MR	Master Reset	I	This input should be pulsed high after power turn on. This will: clear all flags, and status conditions, set TBMT=1, TSO=1 and place the device in the primary BOP mode with 8 bit TX/RX data length, CRC CCITT initialized to all 1's.
34	TXACT	Transmitter Active	O	This output indicates the status of the TDP. TXACT will go high after asserting TXENA and TSOM coinsidently with the first TSO bit. This output will reset one half clock after the byte during which TXENA is dropped.
35	TBMT	Transmitter Buffer Empty	O	This output is at a high level when the TDB or the TX Status and Control Register may be loaded with the new data. TBMT=0 on any write access to TDB or TX Status and Control Register. TBMT returns high when the TDSR is loaded.
36	TSA	Transmitter Status Available	O	TERR bit, indicating transmitter underflow. Reset by MR or assertion of TSOM.
37	TXENA	Transmitter Enable	I	A high level input allows the processing of transmitter data.
38	TSO	Transmitter Serial Output	O	This output is the transmitted character.
39	TCP	Transmitter Clock	I	The positive going edge of this clock shifts data out of the transmitter shift register.
40	MSEL	Maintenance Select	I	Internally RSI becomes TSO and RCP becomes $\overline{TCP}$. Externally RSI is disabled and TSO=1.

Definition of Terms

Register Bit Assignment Chart 1 and 2

Term	Definition
RSOM	Receiver Start of Message—read only bit. In BOP mode only, goes high when first non-flag (address byte) character loaded into RDB. It is cleared when the second byte is loaded into the RDB.
REOM	Receiver End of Message—read only bit. In BOP mode only, set high when last byte of data loaded into RDB, or when an ABORT character is received. It is cleared on reading of Receiver Status Register or dropping of RXENA.
RAB/GA	Received ABORT or GO AHEAD character, read only bit. In BOP mode only, if LM=0 this bit is set on receiving an ABORT character; if LM=1 this bit is set on receiving a GO AHEAD character. This is cleared on reading of Receiver Status Register or dropping of RXENA.
ROR	Receiver Over Run—read only bit. Set high when received data transferred into RDB and previous data has not been read, indicating failure to service RDA within one character time. Cleared on reading of Receiver Status Register or dropping of RXENA.
ABC	Assembled Bit Count—read only bits. In BOP mode only, examine when REOM=1. ABC=0, message terminated on stated boundary. ABC=XXX, message terminated (by FLAG or GA) on unstated boundary, binary value of ABC = number of valid bits available in RDB (right hand justified).
ERR CHK	Error Check—read only bit. In BOP set high if CRC selected and received in error, examine when REOM=1. In CCP mode: 1. set high if parity selected and received in error, 2. if CRC selected (tested at end of each byte) ERR CHK = 1 if CRC GOOD, ERR CHK = 0 if CRC NOT GOOD. Controller must determine the last byte of the message.
TSOM	Transmitter Start of Message—W/R bit. Provided TXENA=1, TSOM initiates start of message. In BOP, TSOM=1 generates FLAG and continues to send FLAG's until TSOM=0, then begin data. In CCP: 1. IDLE=0, transmit out of SYNC register, continue until TSOM=0, then begin data. 2. IDLE=1 transmit out of TDB. In BOP mode there is also a Special Space Sequence of 16-0's initiated by TSOM=1 and TEOM=1. SSS is followed by FLAG.
TEOM	Transmit End of Message—W/R bit. Used to terminate a message. In BOP mode, TEOM=1 sends CRC, then FLAG; if TXENA=1 and TEOM=1 continue to send FLAG's, if TXENA=0 and TEOM=1 MARK line. In CCP: 1. IDLE=0, TEOM=1 send SYNC, if TXENA=1 and TEOM=1 continue to send SYNC's, if TXENA=0 and TEOM=1 MARK line. 2. IDLE=1, TEOM=1, MARK line.
TXAB	Transmitter Abort—W/R bit. In BOP mode only, TXAB=1 finish present character then: 1. IDLE=0, transmit ABORT 2. IDLE=1, transmit FLAG.
TXGA	Transmit Go Ahead—W/R bit. In BOP mode only, modifies character called for by TEOM. GA sent in place of FLAG. Allows loop termination—GA character.
TERR	Transmitter Error—read only bit. Underflow, set high when TDB not loaded in time to maintain continuous transmission. In BOP automatically transmit: 1. IDLE=0, ABORT 2. IDLE=1, FLAG. In CCP automatically transmit: 1. IDLE=0, SYNC 2. IDLE=1, MARK. Cleared by TSOM.
XYZ	Z Y X —W/R bits. These are the error control bits. 0 0 0 $X^{16}+X^{12}+X^{5}+1$ CCITT—Initialize to "1" 0 0 1 $X^{16}+X^{12}+X^{5}+1$ CCITT—Initialize to "0" 0 1 0 Not used 0 1 1 $X^{16}+X^{15}+X^{2}+1$—CRC16 1 0 0 Odd Parity—CCP Only 1 0 1 Even Parity—CCP Only 1 1 0 Not Used 1 1 1 Inhibit all error detection Note: Do not modify XYZ until both data paths are idle
IDLE	IDLE mode select—W/R bit. Affects transmitter only. In BOP—control the type of character sent when TXAB asserted or in the event of data underflow. In CCP—controls the method of initial SYNC character transmission and underflow, "1" = transmit SYNC from TDB, "0"=transmit SYNC from SYNC/ADDRESS register.
SEC ADD	Secondary Address Mode—W/R bit. In BOP mode only—after FLAG looks for address match prior to activating RDP, if no match found, begin FLAG search again. SEC ADD bit should not be set if EXADD=1 or EXCON=1.
STRIP SYNC/LOOP	Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping.
PROTOCOL	PROTOCOL—W/R bit. BOP=0, CCP=1
*APA	All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP.
TXDL	Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 0 1 Five bits per character 1 0 0 Four bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character* 0 0 1 One bit per character* *For data length only, not to be used for SYNC character (CCP mode).
RXDL	Receiver Data Length—W/R bits. RXDL3 RXDL2 RXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 0 1 Five bits per character 1 0 0 Four bits per character 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character
EXCON	Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD =1.
EXADD	Extended Address Field—W/R bit. In receiver only; LSB of address byte tested for a "1". If NO—continue receiving address bytes, if YES go into control field. EXADD bit should not be set if SEC ADD =1.

*Note: This feature does not exist in the present version of the COM5025. It is in the Rev. A version due out in early 3Q77.

Register Bit Assignment Chart 1

REGISTER	DPØ7	DPØ6	DPØ5	DPØ4	DPØ3	DPØ2	DPØ1	DPØØ
Receiver Data Buffer (Read Only- Right Justified- Unused Bits=0)	RD7 MSB	RD6	RD5	RD4	RD3	RD2	RD1	RDØ LSB
Transmitter Data Register (Read/Write- Unused Inputs=X)	TD7 MSB	TD6	TD5	TD4	TD3	TD2	TD1	TDØ LSB
Sync/Secondary Address (Read/Write- Right Justified- Unused Inputs=X)	SSA7 MSB	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSAØ LSB

Register Bit Assignment Chart 2

REGISTER	DP15	DP14	DP13	DP12	DP11	DP1Ø	DPØ9	DPØ8
Receiver Status (Read Only)	ERR CHK	C	B	A	ROR	RAB/GA	REOM	RSOM
TX Status and Control (Read/Write)	TERR (Read Only)	0	0	0	TXGA	TXAB	TEOM	TSOM
Mode Control (Read/Write)	*APA	PROTOCOL	STRIP SYNC/ LOOP	SEC ADD	IDLE	Z	Y	X
Data Length Select (Read/Write)	TXDL3	TXDL2	TXDL1	EXADD	EXCON	RXDL3	RXDL2	RXDL1

*Note: This feature does not exist in the present version of the COM5025. It is in the Rev. A version due out in early 3Q78.

Register Address Selection

1) BYTE OP = 0, data port 16 bits wide

A2	A1	AØ	Register
0	0	X	Receiver Status Register and Receiver Data Buffer
0	1	X	Transmitter Status and Control Register and Transmitter Data Buffer
1	0	X	Mode Control Register and SYNC/Address Register
1	1	X	Data Length Select Register

X = don't care

2) BYTE OP = 1, data port 8 bits wide

A2	A1	AØ	Register
0	0	0	Receiver Data Buffer
0	0	1	Receiver Status Register
0	1	0	Transmitter Data Buffer
0	1	1	Transmitter Status and Control Register
1	0	0	SYNC/Address Register
1	0	1	Mode Control Register
1	1	0	———
1	1	1	Data Length Select Register

TRANSMITTER OPERATION

Apply Power

Pulse MR:

TSO = 1	Protocol = BOP
TBMT = 1	APA = NO
TXACT = 0	Loop = NO
TSA = 0	Sec Add = NO
RXACT = 0	IDLE = ABORT Character
RDA = 0	ZYX = CCITT-1
RSA = 0	TXDL3, TXDL2, TXDL1 = 8 bit
	RXDL3, RXDL2, RXDL1 = 8 bit
	EXADD = NO
	EXCON = NO
	All register bits set to zero

Set Byte Op = 1 (8 bits)

Apply TCP

Note: Example below based on initially Master Resetting. If other conditions are required (different Mode Control settings) load prior to TSOM = 1.

CONTROLLER		USYNRT	COMMENT
TXENA = 1 TXGA = TXAB = TEOM = 0, TSOM = 1	→		
	→		writing into TX Status & Control Register
		←TBMT = 0	
		←TXACT = 1 TSO = FLAG	
		←TBMT = 1	
TXGA = TXAB = TEOM = TSOM = 0	→		take down TSOM
		←TBMT = 0	ignore
Load Address Byte	→		must be loaded prior to TBMT = 1
		←TBMT = 1 TSO = Address Character	
Load Control Byte	→		
		←TBMT = 0	
		←TBMT = 1 TSO = Control Character	
Load Data Length	→		if other than 8 bits desired, must be finished prior to TBMT returning to a "1"
Load Data	→		
		←TBMT = 0	
		←TBMT = 1 TSO = DATA	
Load Data	→		
		←TBMT = 0	
		←TBMT = 1	
		⋮	repeat sequence until all DATA loaded
		←TBMT = 1 TSO = Last Data Byte	last data character being transmitted

Typical Ending Sequences

TXGA = TXAB = TSOM = 0, TEOM = 1	→		end of message
		←TBMT = 0 TSO = CRC	
		←TBMT = 1 TSO = FLAG	
TSGA = TXAB = TSOM = TEOM = 0	→		share flag, for next frame
		←TBMT = 0	ignore
Load Address Byte	→		must be loaded prior to TBMT = 1
		⋮	

OR

TXGA = TXAB = TSOM = 0, TEOM = 1	→		end of message
		←TBMT = 0 TSO = CRC	
		←TBMT = 1 TSO = FLAG	if desired, repeat FLAG sequence
TXGA = TXAB = TEOM = 0, TSOM = 1	→		
		←TBMT = 0	
		←TBMT = 1 TSO = FLAG	of next frame
TXGA = TXAB = TEOM = TSOM = 0	→		take down TSOM
		←TBMT = 0	ignore
Load Address Byte	→		must be loaded prior to TBMT = 1
		⋮	

OR

TXGA = TXAB = TSOM = 0, TEOM = 1	→		end of message
		←TBMT = 0 TSO = CRC	
		←TBMT = 1 TSO = FLAG	flag will be sent
TXENA = 0	→		
		TSO = 1	after FLAG, shut down TX, mark line
		←TXACT = 0	

RECEIVER OPERATION

Apply Power

Pulse MR:

TSO = 1	Protocol = BOP
TBMT = 1	APA = NO
TXACT = 0	Loop = NO
TSA = 0	Sec Add = NO
RXACT = 0	IDLE = ABORT Character
RDA = 0	ZYX = CCITT-1
RSA = 0	TXDL3, TXDL2, TXDL1 = 8 bit
	RXDL3, RXDL2, RXDL1 = 8 bit
	EXADD = NO
	EXCON = NO
	All register bits set to zero

Set Byte Op = 1 (8 bits)

Apply RCP

Note: Example below based on initially Master Resetting. If other conditions are required (different Mode Control or Data Length settings) load prior to RXENA = 1.

CONTROLLER		USYNRT	COMMENT
W/R=1, DPENA	→		if required, load Mode Control and Data Length Select Registers
RXENA=1	→		enable reception begin FLAG search
		←SFR=1	USYNRT synchronized begin filling pipeline
		←RDA=1, RXACT=1, RSOM=1	address byte (8 bit) available RSA not raised
W/R=0, DPENA	→		read address byte
		←RDA=0	
		←RDA=1, RSOM=0	control byte (8 bit) available
W/R=0, DPENA	→		read control byte
		←RDA=0	
		←RDA=1	first data byte (n bits) available
W/R=0, DPENA	→		read data byte
		←RDA=0	
		⋮	
		←SFR=1	
		RDA=1, RSA=1 REOM=1, RXACT=0	last data byte available
W/R=0, DPENA	→		read data byte
	←	RDA=0	
W/R=0, DPENA	→		read status
		←RSA=0	
RXENA=0	→		receiver inactive

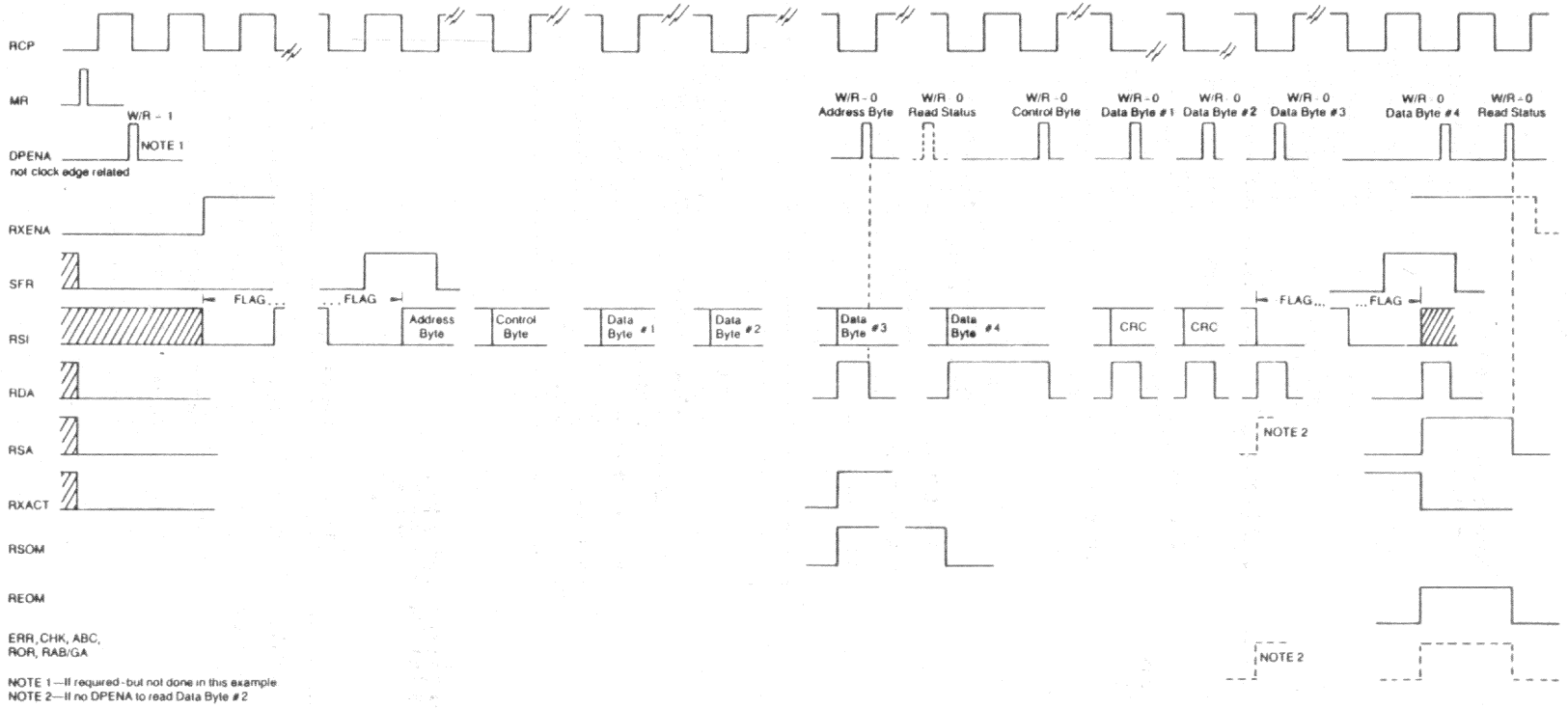
OR

		⋮	
		←RDA=1	Nth byte available controller fails to read
		←RSA=1, ROR=1	RDB overwritten
W/R=0, DPENA	→		read data byte
		←RDA=0	
W/R=0, DPENA	→		read status
		←RSA=0	
RXENA=0	→		terminate reception
		←RXACT=0	

Terminology

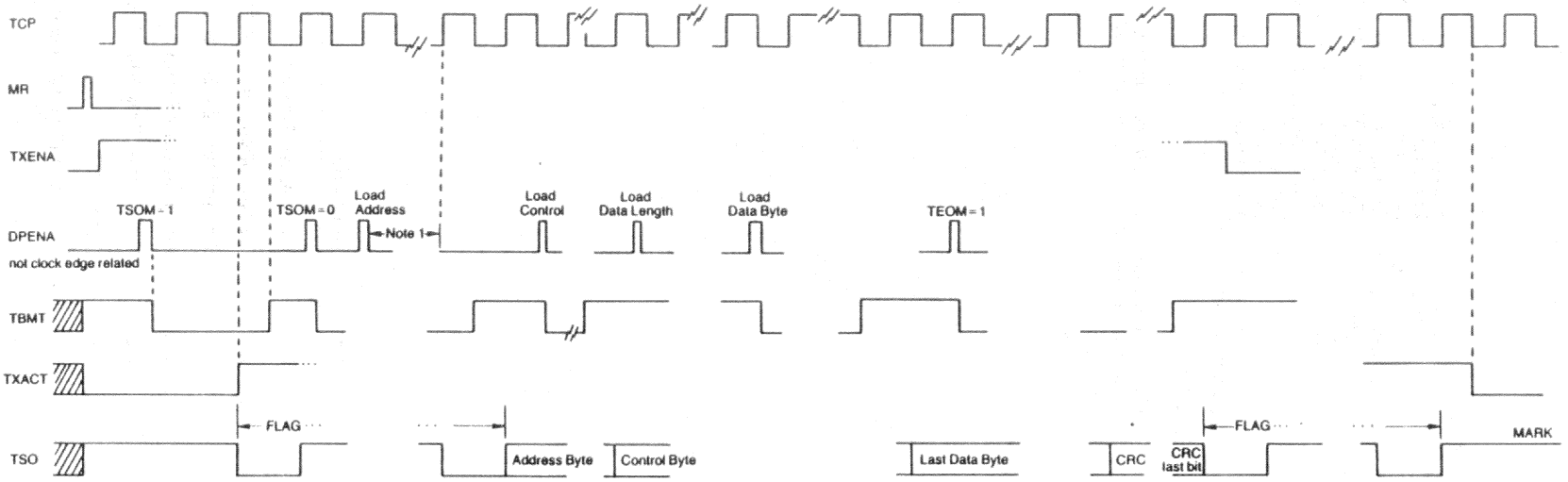
Term	Definition	Term	Definition
BOP	Bit Oriented Protocols: SDLC, HDLC, ADCCP	GA	01111111 (0 (LSB) followed by 7-1's)
CCP	Control Character Protocols: BiSync, DDCMP	LSB	First transmitted bit, First received bit
TDB	Transmitter Data Buffer	MSB	Last transmitted bit, Last received bit
RDB	Receiver Data Buffer	RDP	Receiver Data Path
TDSR	Transmitter Data Shift Register	TDP	Transmitter Data Path
FLAG	01111110	LM	Loop Mode
ABORT	11111111 (7 or more contiguous 1's)		

RECEIVER TIMING



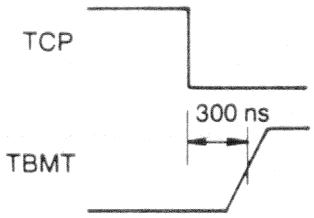
NOTE 1—If required - but not done in this example
NOTE 2—If no DPENA to read Data Byte #2

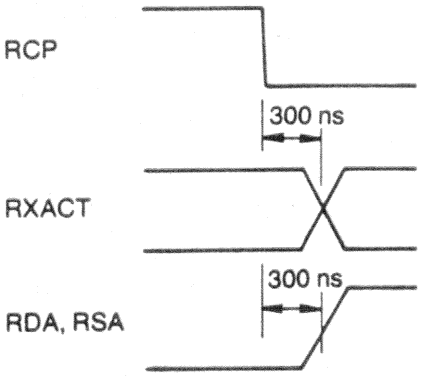
TRANSMITTER OPERATION

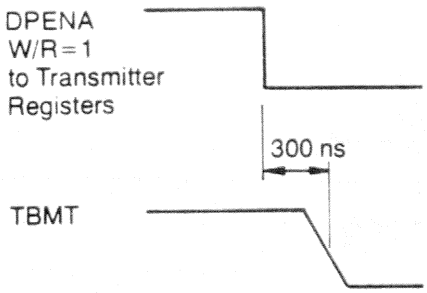


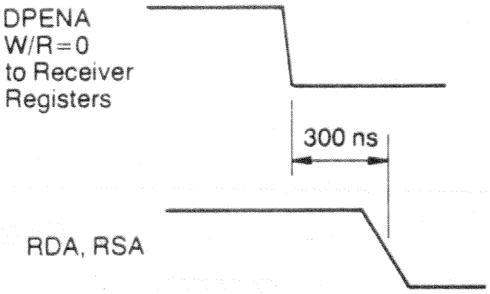
Note 1—Trailing edge of DPENA must occur at least one-half clock pulse prior to TBMT = 1. To avoid underrun.

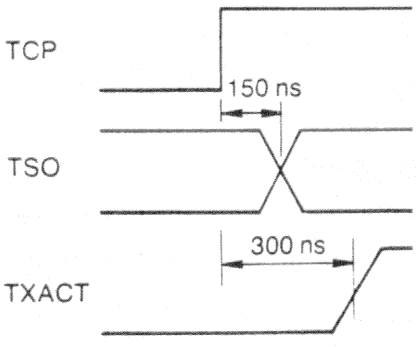
AC TIMING DIAGRAMS

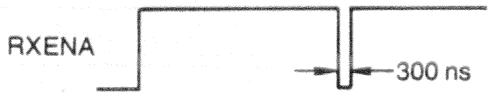










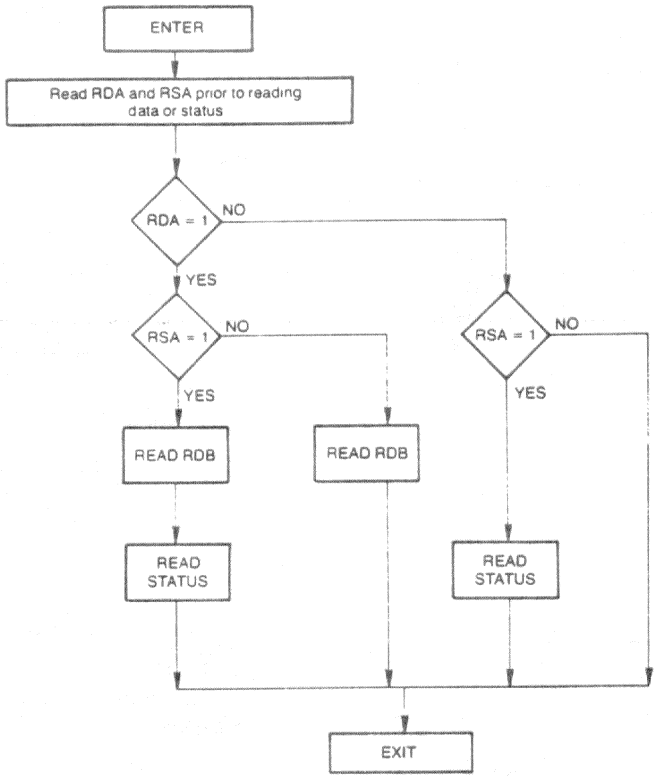


Resets: RDP-RDA, RSA, RXACT, receiver into search mode (for FLAG)

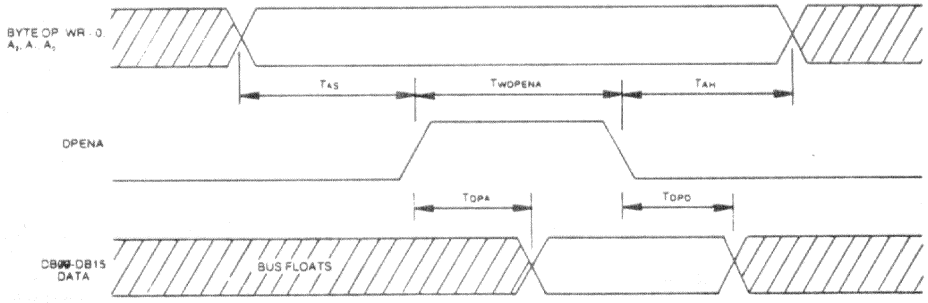
Receiver Data and Receiver Status

Access Sequence

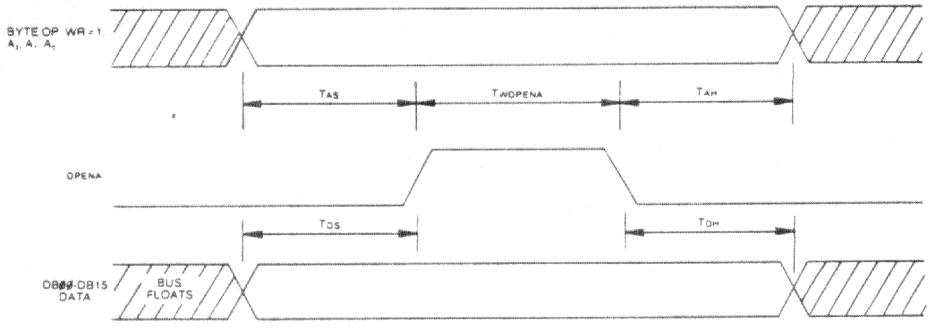
Preferred reading sequence of receiver RDA and RSA.



Data Port Timing

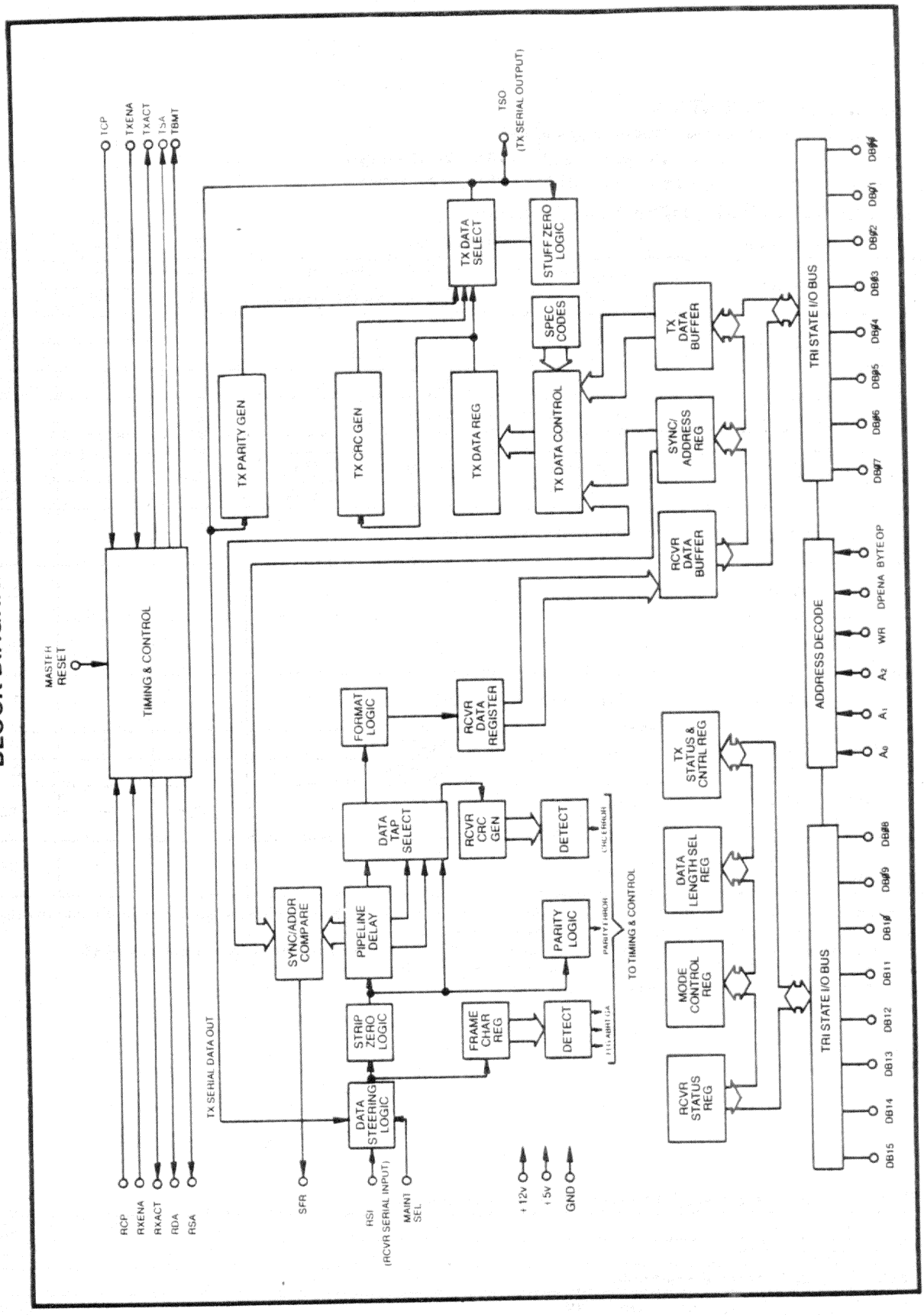


READ FROM USYNR/T



WRITE TO USYNR/T

BLOCK DIAGRAM



SMC Microsystems Corporation 35 Marcus Blvd., Hauppauge, N.Y. 11787 Phone (516) 273-3100 TWX 510-227-8898

378 2.5K

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	MIN. = 4.75V	MAX. = 5.25V
MIL	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%	MIN. = 4.50V	MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.0mA (MIL)	2.4	3.4		Volts
			I_{OH} = −2.6mA (COM'L)	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 5)	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	V_O = 0.4V			−20	µA
			V_O = 2.4V			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			21	34	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = $\overline{E}_1$ = $\overline{E}_2$ = GND : E_3 = E_4 = POL = $\overline{OE}_1$ = $\overline{OE}_2$ = 4.5V.
5. V_{OL} is specified with total device I_{OL} = 60mA (max.).

Am25LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

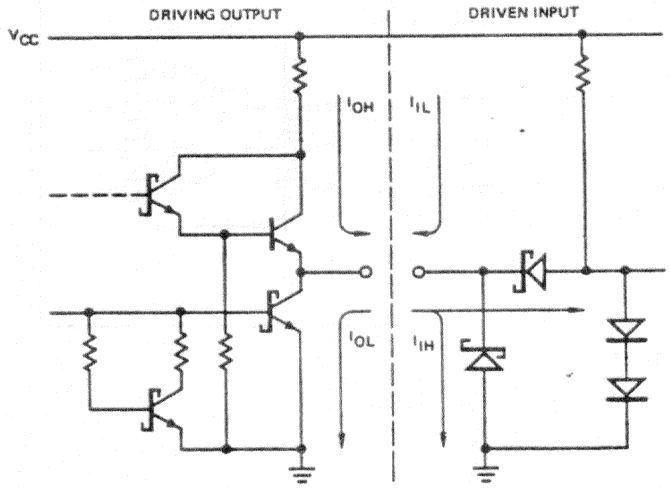
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	A, B, C to Y_i	C_L = 15pF, R_L = 2.0kΩ		20	30	ns
t_{PHL}				15	22	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to Y_i			19	28	ns
t_{PHL}				20	30	
t_{PLH}	E_3, E_4 to Y_i			21	31	ns
t_{PHL}				23	34	
t_{PLH}	POL to Y_i			16	24	ns
t_{PHL}				20	30	
t_{ZH}	$\overline{OE}_1$, $\overline{OE}_2$ to Y_i			17	25	ns
t_{ZL}				14	21	
t_{HZ}	$\overline{OE}_1$, $\overline{OE}_2$ to Y_i	C_L = 5.0pF, R_L = 2.0kΩ		17	25	ns
t_{LZ}				20	30	

Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Test Conditions	Am25LS COM'L: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%		Am25LS MIL: T_A = –55°C to +125°C, V_{CC} = 5.0V ±10%		Units
			Min.	Max.	Min.	Max.	
t_{PLH}	A, B, C to Y_i	C_L = 50pF, R_L = 2.0kΩ		36		42	ns
t_{PHL}				29		37	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to Y_i			34		39	ns
t_{PHL}				38		45	
t_{PLH}	E_3, E_4 to Y_i			38		45	ns
t_{PHL}				43		52	
t_{PLH}	POL to Y_i			29		34	ns
t_{PHL}				39		49	
t_{ZH}	$\overline{OE}_1$, $\overline{OE}_2$ to Y_i			38		45	ns
t_{ZL}				23		25	
t_{HZ}	$\overline{OE}_1$, $\overline{OE}_2$ to Y_i	C_L = 5.0pF, R_L = 2.0kΩ		29		33	ns
t_{LZ}				33		36	

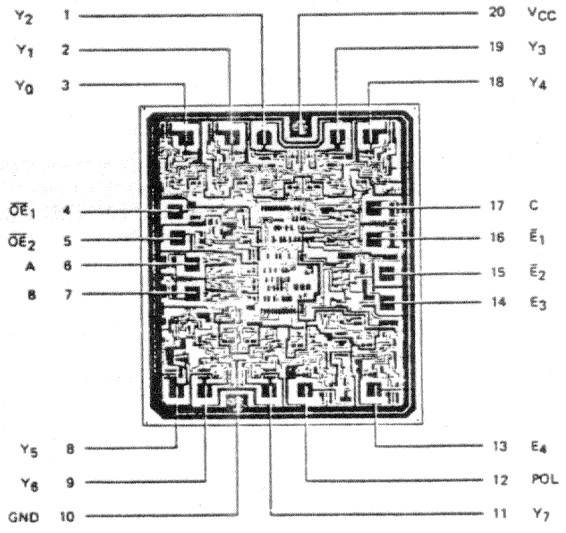
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS • Am54/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Metallization and Pad Layout



DIE SIZE 0.081" X 0.096"

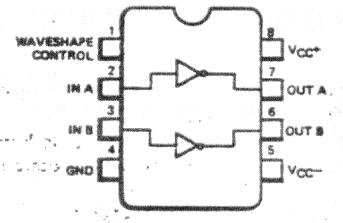
9636

DUAL SINGLE-ENDED LINE DRIVER

The 9636 Dual Single-Ended Line Driver meets the driver requirements of EIA standards RS-423 and RS-232C, provides TTL and CMOS compatible inputs and operates over the military and industrial temperature ranges. It also meets the CCITT standard X.26 driver requirements. The output slew rate can be controlled with a single external resistor; all outputs are short circuit protected and can withstand EIA-RS-232C fault conditions. The mini DIP provides high package density.

- Output Short-Circuit Current Limiting
- Adjustable Slew Rate Limiting
- TTL and CMOS Input Compatible
- Meets EIA-RS-423 and RS-232C
- Meets CCITT X.26
- Wide Supply Range (± 9 V to ± 15 V)

CONNECTION DIAGRAM
8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



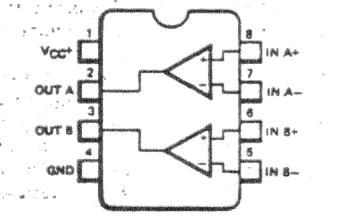
9637

DUAL DIFFERENTIAL LINE RECEIVER

The 9637 Dual Differential Line Receiver meets the receiver requirements of EIA standards RS-422 and RS-423 and provides a TTL compatible output while operating over the military and industrial temperature ranges. It uses a single 5 V power supply. This receiver has an input threshold accuracy of ±200 mV over a ±7 V common mode range. It also converts the CCITT X.26 and X.27 standard signals to TTL levels and can withstand RS-232C fault conditions. The mini DIP provides high package density.

- Dual Channels
- Single 5 V Supply
- Satisfies EIA Standards RS-422 and RS-423
- Converts CCITT Standards X.26 and X.27 to TTL
- Withstands EIA Standard RS-232C Signal Levels
- High Common Mode Range
- High Input Impedance
- TTL Compatible Output

CONNECTION DIAGRAM
8-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



DEFINITION OF FUNCTIONAL TERMS

A, B, C, D — The three select inputs to the decoder/demultiplexer.

$\overline{E}_1$, $\overline{E}_2$ — The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled.

E_3, E_4 — The active LOW enable inputs. A LOW on either E_3 or E_4 inputs forces all the decoded functions to be inhibited.

POL — Polarity Control. A LOW on the polarity control input forces the output to the active-HIGH state while a HIGH on the polarity control input forces the Y outputs to the active-LOW state.

$\overline{OE}_1$, $\overline{OE}_2$ — Output Enable. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the Y outputs are enabled. If either $\overline{OE}_1$ or $\overline{OE}_2$ input is HIGH, the Y outputs are in the high impedance state.

Y_i — The eight outputs for the decoder/demultiplexer.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Am25LS Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	Y_2	—	50	130	33	33
2	Y_1	—	50	130	33	33
3	Y_0	—	50	130	33	33
4	$\overline{OE}_1$	1.0	—	—	—	—
5	$\overline{OE}_2$	1.0	—	—	—	—
6	A	1.0	—	—	—	—
7	B	1.0	—	—	—	—
8	Y_5	—	50	130	33	33
9	Y_6	—	50	130	33	33
10	GND	—	—	—	—	—
11	Y_7	—	50	130	33	33
12	POL	1.0	—	—	—	—
13	E_4	1.0	—	—	—	—
14	E_3	1.0	—	—	—	—
15	$\overline{E}_2$	1.0	—	—	—	—
16	$\overline{E}_1$	1.0	—	—	—	—
17	C	1.0	—	—	—	—
18	Y_4	—	50	130	33	33
19	Y_3	—	50	130	33	33
20	V_{CC}	—	—	—	—	—

FUNCTION TABLE

FUNCTION	INPUTS										OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	POL	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
High Impedance	H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	H	X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	H	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	H	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	L	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	L	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	X	L	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	X	L	H	X	X	X	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	L	L	H	H	L	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	L	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	L	H	H	H	L	L	L	L	L	L	L	H
Active-LOW Output	L	L	L	L	H	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH L = LOW X = Don't Care Z = High Impedance

Am25LS2538

One-Of-Eight Decoder With Three-State Outputs And Polarity Control

Advanced Micro Devices

Low-Power Schottky Integrated Circuits

DISTINCTIVE CHARACTERISTICS

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- Am25LS family has improved sink current, source current, and noise margin characteristics
- 100% reliability assurance testing in compliance with MIL-STD-883

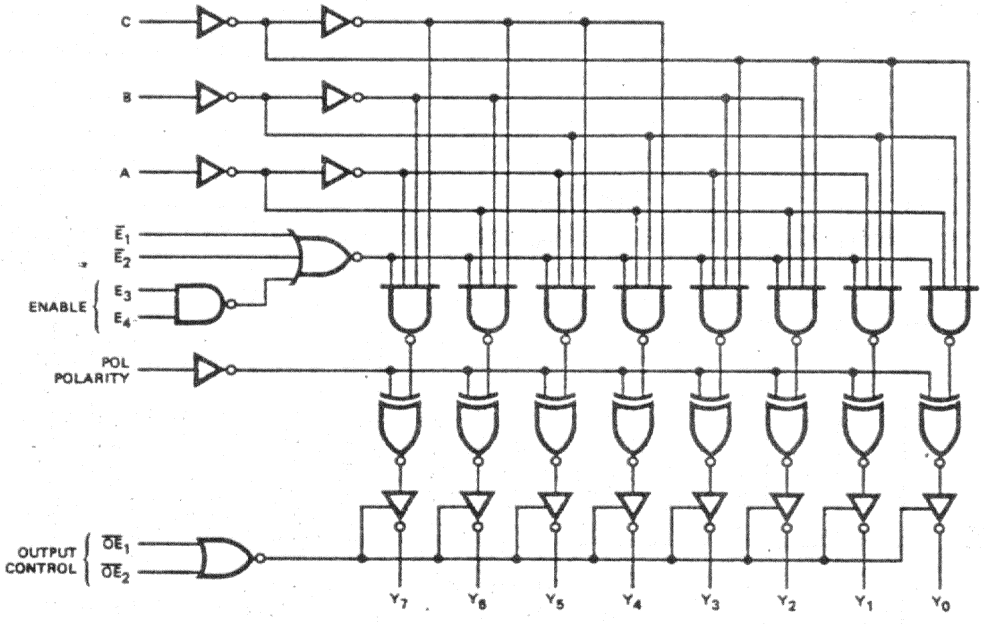
FUNCTIONAL DESCRIPTION

The Am25LS2538 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs—A, B, and C—that are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

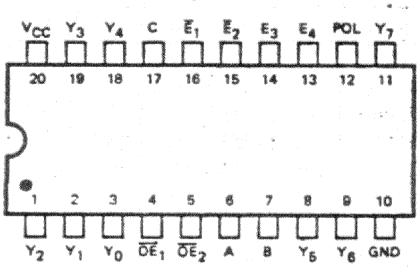
A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

The device is packaged in a space saving (0.3-inch row spacing) 20-pin package. It also features Am25LS family improved switching specifications, higher noise margin, and twice the fan-out over the military temperature range.

LOGIC DIAGRAM
One-of-Eight Decoder

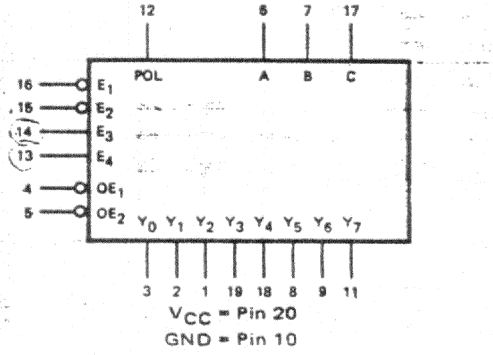


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

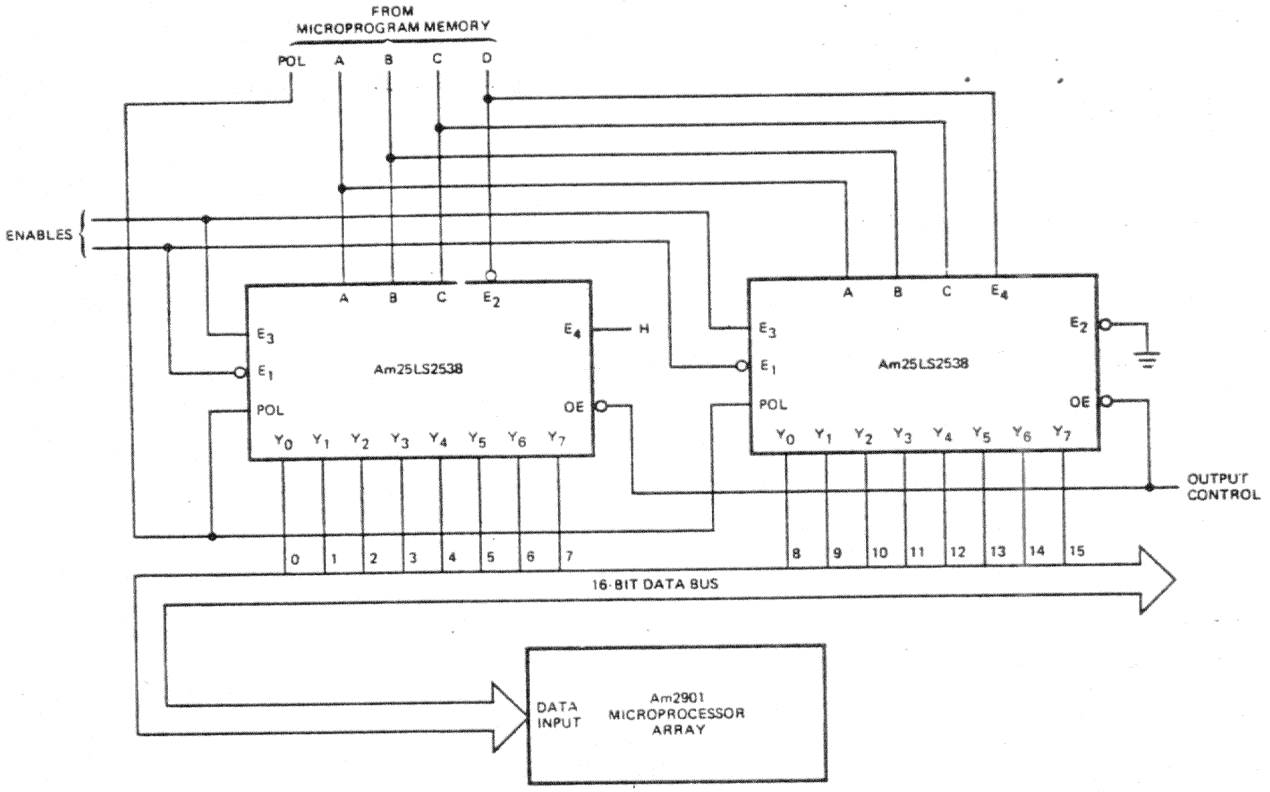


V_{CC} = Pin 20
GND = Pin 10

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25LS2538PC
Hermetic DIP	0°C to +70°C	AM25LS2538DC
Dice	0°C to +70°C	AM25LS2538XC
Hermetic DIP	–55°C to +125°C	AM25LS2538DM
Hermetic Flat Pak	–55°C to +125°C	AM25LS2538FM
Dice	–55°C to +125°C	AM25LS2538XM

APPLICATIONS



Two Am25LS2538s can be used to perform a one-of-sixteen-bit mask function or a one-of-sixteen-bit select function to perform bit manipulation in a microprocessor system.

Examples:

D	C	B	A	POL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Function
0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Bit Select
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	Bit Select
0	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	Bit Mask
1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	Bit Mask

digital

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