EK-PC500-TD-001

VAXmate™

Technical Description

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Preface

Audience

This manual provides a technical description of the VAXmate workstation. The manual describes the hardware down to the functional block diagram level. The book includes descriptions of the CPU module, the I/O - video module, the monitor module, the diskette drive, the expansion box with the hard disk, the keyboard, and the power supply subsystem. This manual follows general technical description conventions. Where high voltages are present, such as in the monitor module, the descriptions contain sufficient detail to avoid any misunderstanding of components and test points.

Classified as a reference document, this manual is written for Field Service depot repair personnel, Europe and GIA Field Service, Educational Services instructors, and engineers. Experienced programmers or software engineers should refer to the *VAXmate Technical Reference Manual* in the technical documentation kit (Digital part number Q6ZCS-GZ) for programming the hardware registers.

Manual Organization

Chapter 1 provides an introduction to the VAXmate workstation components, its options, and the expansion box. The functional block diagram in this chapter provides an overview of the internal logic.

Chapter 2 describes the Central Processor Unit (CPU) module, including the 80286 microprocessor, an optional 80287 math coprocessor, 1 Mbyte of memory, the bus structure, an interrupt controller, a direct memory access controller, a real-time clock, a 3-channel counter/timer, and the mouse logic.

Chapters 3, 4, and 5 provide information on the I/O module. Chapter 3 describes the common logic, the communications logic, and the network interface. Chapter 4 describes the video circuits on the I/O board and the video monitor board. Chapter 5 describes the diskette (floppy) controller.

Chapters 6 and 7 provide information on the VAXmate Expansion box. Chapter 6 describes the hard disk controller and the hard disk. Chapter 7 describes the auxiliary power controller, the expansion box bus, and the card cage for industry-standard hardware options.

Chapter 8 describes the LK250 VAXmate keyboard logic, which includes an 8051 microprocessor, the keyboard scanning matrix, the speaker control, and the light emitting diode (LED) control. This chapter also has information on the 8042 keyboard interface controller on the CPU module.

Chapter 9 describes the VAXmate power supply, the physical layout, a circuit level technical description, and the expected input and output voltage signals.

Appendix A has the system specifications, Appendix B has the expansion box bus signals, and Appendix C has a block diagram of the CPU module.

Industry Standardization

The VAXmate workstation is an industry-standard compatible personal computer. The computer industry recognizes two open architectures as industry standards: the IBM-PC/AT bus structure and the Microsoft disk operating system (MS-DOS). To support MS-DOS, the VAXmate workstation implements a defined set of ROM-BIOS services. In this manual, the term industry-standard refers to compatibility with these open architectures.

Chapter 1
General Description

1.1 Introduction

The VAXmate workstation is a high performance, desktop personal computer that executes industry-standard software in an Ethernet network environment. The network may comprise several VAXmate workstations connected by ThinWire Ethernet cable, and may include a VAX or MicroVAX II computer as a network server. This networking environment is referred to as Digital's Personal Computing Systems Architecture (PCSA).

The VAXmate workstation also has a hard disk storage device provided in an optional expansion box, so the VAXmate can be configured as the network server. The VAXmate workstation with the expansion box may also serve as a standalone personal computer.

Base System – The VAXmate workstation is comprised of three major parts: the VAXmate system unit (including the CPU, I/O module, and video display), a keyboard, and a mouse.

The system unit has the following features.

- 8 MHz 80286 Central Processor Unit (CPU)
- 1 Mbyte memory
- 1.2 Mbyte, 96 tracks-per-inch, half-height diskette drive (RX33)
- A high resolution, 14-inch monochromatic monitor with industry-standard and Digital modes for text and graphics.
- Communication ports
- Tilt screen
- Convection cooling

The system package housing is constructed of plastic. The workstation features

- AC power switch on back of the workstation
- Connectors identified with icons
- Mass storage device behind an access panel
- Brightness and contrast controls for the monitor on the left side of the workstation
- A mechanical interlock with a door that opens to install options.

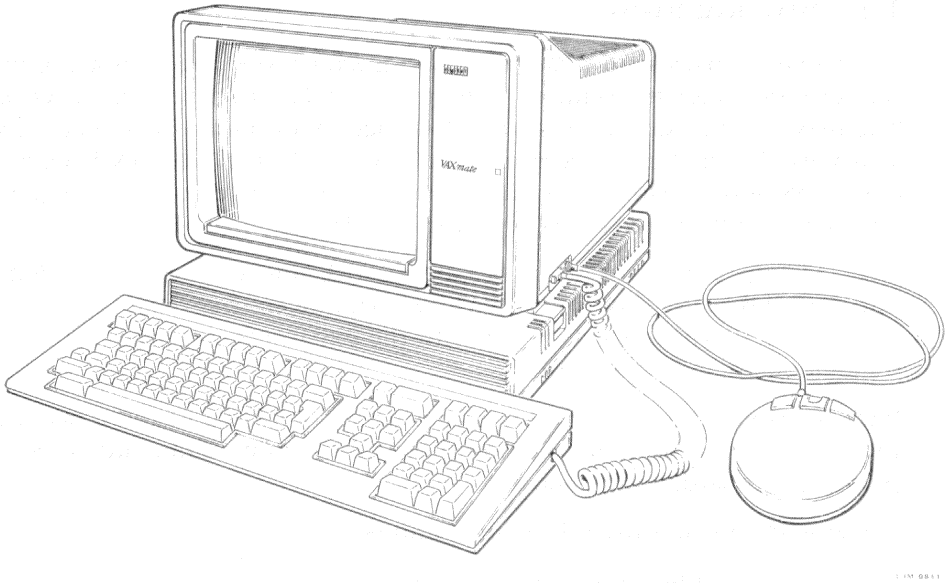


Figure 1-1 VAXmate Workstation - Front View

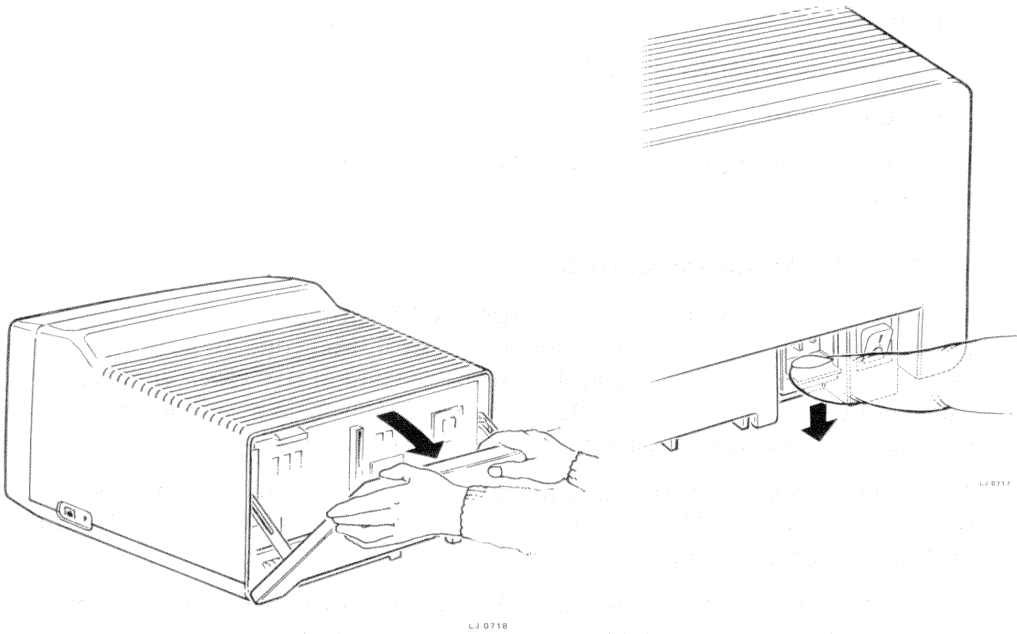


Figure 1-2 VAXmate Workstation - Rear View

1.2 Hardware

The VAXmate base system (Section 1.3) consists of the following components.

1. VAXmate Workstation (CPU/CRT)
   a. CPU/Memory Module
   b. I/O-Video Module
   c. CRT (Amber or Green)
   d. RX33 1.2 Mbyte Diskette Drive
   e. Communication ports
   f. Power Supply
2. LK250 Keyboard

3. Mouse
4. ThinWire Ethernet cable kit
5. Power cord

The following paragraphs describe the components within the VAXmate workstation.

1.2.1 CPU/Memory Module

The CPU/Memory module has an 8 MHz 80286 processor with associated logic, including DMA control, interrupt control, bus control, and command/status registers. The module also has a time-of-day clock and event timer. An optional 5.33 MHz 80287 numeric coprocessor can be added to enhance the CPU with floating point and other data types.

The memory portion of the module has 1 Mbyte dynamic memory with byte parity. An optional 2 Mbyte memory module can be added to provide a total of 3 Mbytes of usable memory.

The CPU/Memory module also has 256 bits of nonvolatile memory (NVM), accessible by the system control and status register (CSR 1), and 64KB of ROM for Basic I/O System (BIOS) firmware and diagnostics. In addition, the module has a 32 byte Ethernet address ROM.

Other circuits on the CPU/Memory module are the keyboard interface, the mouse interface, and the programmable speaker logic.

1.2.2 I/O-Video Module

The I/O-Video Module accepts the 16-bit bus signals generated by the CPU/Memory module. The I/O-Video module provides all the non-optional I/O, peripheral interface, and video display control functions of the VAXmate system. The module contains a video display controller, a serial printer port, a ThinWire Ethernet interface, a serial communications port, diskette controller logic, and a connection for an integral modem (or other future integrated options).

1.2.2.1 Video Controller

The VAXmate video display controller resides on the I/O-Video board and drives a monochrome or color monitor. The VAXmate system unit contains a monochrome CRT subsystem. Within the video controller, the display processor is capable of displaying up to 16 colors or 16 shades of gray.

Industry-Standard Text and Graphics Features – The VAXmate video controller has the following industry-standard text and graphics features.

- 80 × 25 and 40 × 25 text display
- 256-character soft font
- 8 × 8 character cell (using an 8 × 16 font matrix)
- The following character attributes
  - 16 foreground colors/intensity levels
  - 16 background colors/intensity levels, or 8 background colors/intensity levels plus the capability for each color to blink
- Bit map graphics with industry-standard color palettes
  - 320 × 200 2-colors
  - 320 × 200 4-colors
  - 640 × 200 2-colors

Enhancements to Industry-Standard Features – The video controller has the following enhancements to industry-standard features.

- Screen resolution is 640 horizontal pixels by 400 scan lines. The 200-line industry-standard graphics display is accomplished by displaying each scan line twice.
- Character font matrix is 8 horizontal pixels by 16 scan lines, resulting in a higher quality font for text modes.
- Font is fully programmable for flexibility in terminal emulation and multilingual applications.
- Dual-port video memory eliminates annoying screen flicker, because the screen does not have to be cleared before accessing memory.
- 16-bit video memory data path, coupled with the dual-port access, results in faster screen updates.

Display Processor – The display processor includes a parameter translation ROM, 6845 CRT control, text video logic, graphics video logic, a video look-up table (color palette), and status and control registers.

The video controller has a 4 Kbyte programmable font RAM for up to 256 character patterns. The video look-up table is a 16-word RAM that allows rapid selection of the color or intensity levels for the various operating modes.

Video Modes – The display processor converts memory data into various raster formats, depending on the mode of operation. Some video controller modes have a mode number, indicating that the ROM BIOS supports these modes. Unsupported modes are available for programmers. The difference between color and monochrome modes is the presence of a color burst signal in the composite video output signal for color modes. Because the VAXmate video controller does not provide a composite video output, there is no difference in the video output for these modes.

Mode 0	40 × 25 Text mode monochrome (industry-standard)
Mode 1	40 × 25 Text mode color (industry-standard)
Mode 2	80 × 25 Text mode monochrome (industry-standard)
Mode 3	80 × 25 Text mode color (industry-standard)
Mode 4	320 × 200 4-color graphics mode (industry-standard)
Mode 5	320 × 200 monochrome graphics (industry-standard)
Mode 6	640 × 200 monochrome graphics mode (industry-standard)
	320 × 200 16-color graphics mode (VAXmate unique)*
Mode D0	640 × 400 2-color graphics mode (VAXmate unique)
Mode D1	640 × 400 4-color graphics mode (VAXmate unique)
Mode D2	800 × 250 4-color graphics mode (VAXmate unique)†
	640 × 200 4-color graphics mode (VAXmate unique)*

1.2.2.2 Monitor - Amber or Green Screen

The monitor consists of a 14 in. diagonal display Cathode Ray Tube (CRT) and associated analog circuitry, which generates either 800 × 250 or

* No ROM-BIOS support

† Limited ROM-BIOS support

640 × 400 raster lines. It accepts synchronization signals and digital video signals from the video controller. A 4-bit digital-to-analog converter allows video images to be displayed in up to 16 shades of gray. The monitor switches to 250 scan or 400 scan operation whenever it receives a control signal from the video controller.

The CRT can be tilted downward or upward to change your viewing angle by pressing the bar located at the base of the screen. Contrast and brightness controls are located on the left side of the system unit.

1.2.3 RX33 1.2 Mbyte Diskette Drive

The RX33 is a 5-1/4 in, double-sided, dual-speed, half-height, 96 tracks per-inch, diskette drive. It has full RX50 single-sided, read/write compatibility, and industry-standard 1.2 megabyte compatibility.

Diskette Drive Controller – The floppy disk drive controller provides the interface between the VAXmate workstation system bus and the diskette drive. The controller supports the RX33 5-1/4 inch, high-capacity diskette drive with standard (250K bit) or high capacity (500K bit) media.

The controller operates in either DMA or non-DMA mode. The controller uses DMA mode to transfer data between itself and the system memory. In DMA mode, the processor issues the command to the disk controller. Then, the controller and system DMA controller implement the data transfer. In non-DMA mode, the disk controller generates interrupts to the processor each time the controller transfers a data byte.

1.2.4 ThinWire Ethernet

The VAXmate workstation includes an integral ThinWire Ethernet interface, a 12-ft cable, a T-connector, and a terminator. The ThinWire Ethernet interface enables customers to connect multiple VAXmate workstations using small sections of cable and simple connectors. No tools are needed to establish these connections.

ThinWire Ethernet is a cost-effective means of linking desktop computers, such as the VAXmate, to the MicroVAX II. The Ethernet has a 10 Mbits per second data rate, and is compatible with IEEE standard 802.3. In addition, all previous Digital Ethernet devices can connect to the ThinWire Ethernet through adapters.

The network interface, which resides on the I/O-Video module, uses a Local Area Network Controller (LANCE), a Serial Interface Adapter (SIA), and a Coaxial Transceiver Interface (CTI) to control data transmission between the CPU module and other devices on the ThinWire Ethernet.

The LANCE is a 10 Mbit per second device that performs the link-level Ethernet protocol. The LANCE also provides the Carrier-Sense Multiple-Access/Collision-Detect (CSMA/CD) network access, memory management (on-board DMA), error reporting, packet handling, and CPU interface functions.

The SIA provides Manchester phase encoding and decoding of the serial bit stream, and interfaces the TTL output of the LANCE to the differential inputs of the CTI. The SIA also has a phase-locked loop to recover clock from an incoming signal from a 20 MHz crystal oscillator.

The CTI couples the network interface to the cable. The CTI provides collision-detect, noise-control, and line driver/receiver functions.

1.2.5 Communications

The serial communications elements in the VAXmate workstation provide asynchronous communications for the communications port, the printer port, and the modem port. These elements provide full modem control signals with a programmable baud rate generator, and are register compatible with industry-standard applications. The receive data format includes a start bit, five to eight data bits, a parity bit (if programmed), and 1, 1-1/2, or 2 stop bits.

Communications Port – The communication port is interfaced via a 25-pin, male, D-subminiature (DB25) connector located on the rear panel of the VAXmate workstation. This connector is functionally compatible with RS-232-C and electrically compatible with an RS-423 configured as Data Terminal Equipment (DTE). The communications port interface complies with Digital Standard 52.

Printer Port – The printer port is a 6-pin, female, modular (MMJ) connector, located on the rear panel of the VAXmate workstation. The serial printer port communicates with an ASCII protocol printer that generates transmit data and accepts receive data. It supports two modem control lines and is compatible with Digital Standard 052, Section 4.

1.2.6 LK250 Keyboard

The VAXmate keyboard executes both industry-standard and Digital-developed applications on the VAXmate workstation. It also functions on industry-standard PC, XT, and AT-compatible computers. Use of this keyboard with an industry-standard computer requires a compatible cable for that machine.

The keys on the keyboard have gold labels to identify special functions of Digital WPS-PLUS word processing software, and blue labels to identify special functions developed for industry-standard application software. The keyboard is connected to the system by a 6-conductor cable.

1.2.7 Mouse

The VAXmate mouse is the standard Digital mouse. It is a hand-held pointing device used to move the cursor around the VAXmate video display screen. As the mouse is moved along a flat surface, the cursor makes corresponding movements on the screen. When the pointer is placed at the appropriate position, press one of the mouse buttons to make your selection.

The mouse has three buttons and a 7-pin, miniature circular connector.

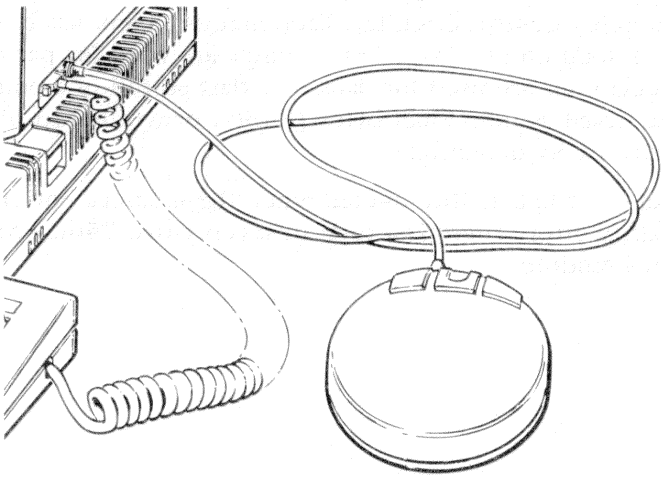


Figure 1-3 VAXmate Mouse

1.2.8 Power Supply

The power supply in the VAXmate workstation operates from 120 V or 240 V.

The power supply is a high frequency, switch-mode power supply, which delivers all the dc power required by the system package. This power goes to the CPU card, I/O card, CRT monitor, and diskette drive, as well as I/O devices such as the keyboard and the mouse. The power supply also provides unregulated dc (±150 V) to the expansion box.

1.2.9 Hardware Options

The following hardware options for the VAXmate workstation are available from Digital Equipment Corporation.

PC50X-AA 2 Mbyte Additional Memory

The 2 Mbyte Memory option is a customer-installable module provided on a double-sided surface mount card. The card can be mounted to a connector located on the CPU module. This connector is accessible through a door at the rear of the workstation.

This option card contains 4 banks of dynamic memory with memory control circuitry. Each memory bank has eighteen 256K × 1 RAM chips. Two of these chips are used for parity. The remainder are used for data. The data stored in memory may be accessed as individual bytes (8 bits) or words (16 bits), with byte parity detection.

An error LED is illuminated when the memory option detects a parity error. There is a total of seventy-two 256K RAM chips on this module.

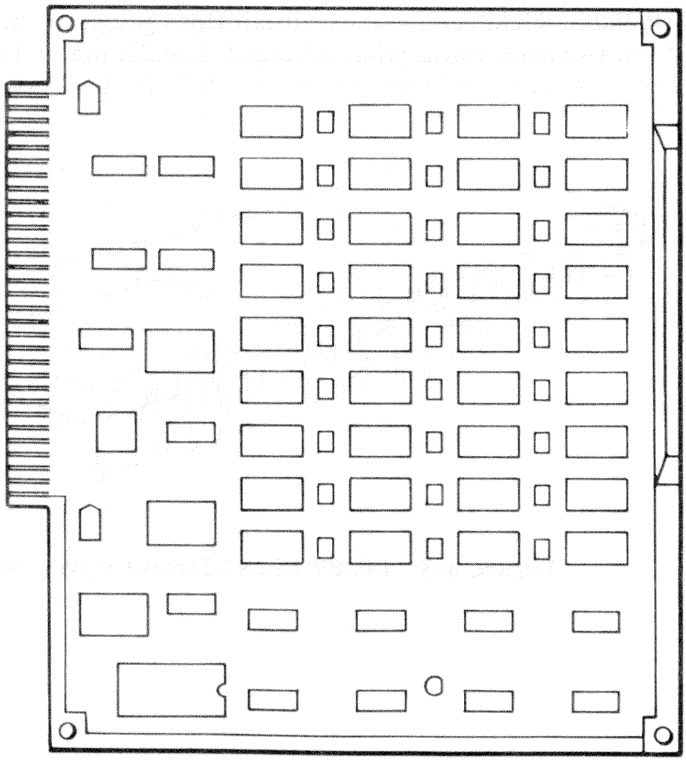


Figure 1-4 PC50X-AA 2 Mbyte Memory Module Option

FP287 Intel 80287 Math Coprocessor

The VAXmate workstation can accept an optional 80287 math coprocessor for increased graphics performance and instructions for a variety of numeric data types. The coprocessor operates at 5.33 MHz. This option is a 40-pin DIP integrated chip that plugs into a socket on the CPU module. This option is not customer installable. Field Service must install this option, or the warranty of the VAXmate workstation is voided. Installation by Digital Field Service is included in the list price (MLP) of this option.

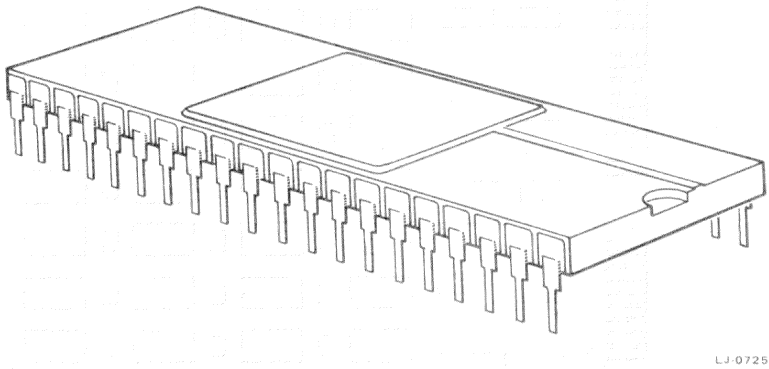


Figure 1-5 FP287 80287 Math Coprocessor

Expansion Box

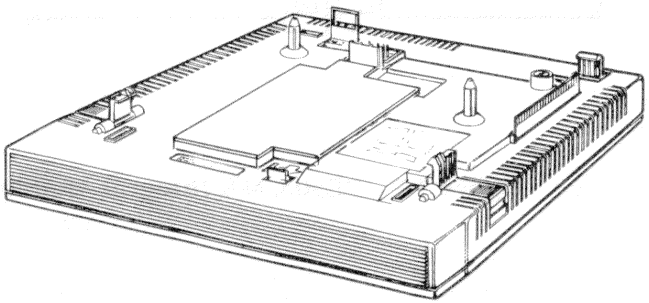
The expansion box includes a hard disk drive, a hard disk controller, a battery back-up unit, and a card cage with two slots for industry-standard hardware options.

The VAXmate workstation supports a 3-1/2 inch or 5-1/4 inch, half-height hard disk drive, which resides in the expansion box. For example, the expansion box can support the RD31-A hard disk drive, which contains two double-sided, 5-1/4 inch disks that provide the system processor with a total of 20 Mbytes of mass storage; or it can support the RD32-A hard disk drive, which contains two double-sided, double-density 5-1/4 inch disks that provide the system processor with a total of 40 Mbytes of mass storage. The operating system can be booted off the hard disk.

The VAXmate workstation hard disk controller connects the hard disk drive to the workstation system bus. All control and data transfers between the system processor and the disk controller use system programmed I/O. Direct Memory Access (DMA) transfers are not supported for either control or data transactions.

The expansion box also provides battery back-up for the time-of-day (real-time) clock/event timer in the CPU/Memory module. The expansion box includes two 5-year Lithium batteries.

In addition, the expansion box has two slots for industry-standard hardware options. See Chapter 7 for information on installing industry-standard options in the expansion box.



LJ-0744

Figure 1-6 Expansion Box

PC50X-MA

Integral Modem Option for North America

A user-installable, integral modem option is available for the VAXmate workstation. This modem option connects to the CPU 8-bit bus through a connector on the I/O module, which is accessible through a door at the rear of the workstation. The modem will support Bell 212, Bell 103, V22-compatible, and V22 bis-compatible modes.

The modem module has two modular telephone line connectors that protrude through the rear panel of the VAXmate workstation. The connector uses an 8-pin, keyed, modular housing for an RC11C jack (or CA11 jack in Canada).

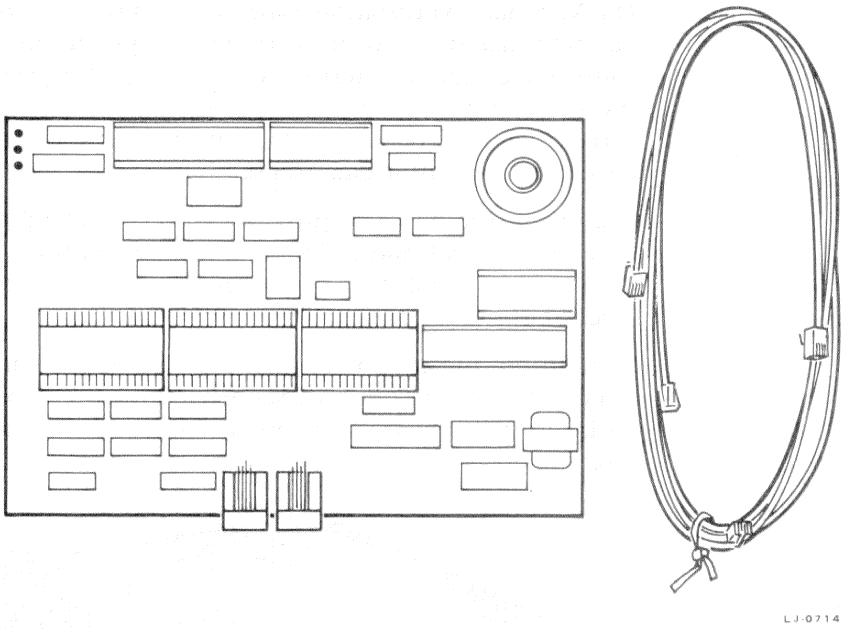


Figure 1-7 PC50X-MA Integral Modem Option

DEMPR

Digital ThinWire Ethernet Multiport Repeater

The Digital ThinWire Ethernet Multiport Repeater (DEMPR) is a radial hub that connects up to eight ThinWire coaxial cable segments, each up to 185 meters in length. Up to 29 stations can be connected on each segment, for a total 232 stations.

The DEMPR can also be used as a stand-alone hub to link desktop systems in several offices to a resource-sharing network. The DEMPR can be placed on a wall, in a rack, or on a table.

DESTA

Digital ThinWire Ethernet Station Adapter

The Digital ThinWire Ethernet Station Adapter (DESTA) is a compact Ethernet transceiver that is used to retrofit standard Ethernet products for connection to ThinWire Ethernet.

The DESTA has a 15-pin connector at one end for attachment to standard Ethernet devices, and a BNC connector at the other end for connection to the ThinWire Ethernet. The MicroVAX II would use a DESTA to communicate to the VAXmate workstation over ThinWire Ethernet cable.

LA75

The LA75 is a low-cost, single-user, entry-level, dot-matrix companion printer for the VAXmate workstation. The LA75 features the ability to insert single sheets of paper without removing the continuous form paper, a separate feed for envelope addressing, and very quiet operation.

The LA75 uses Digital printer protocols as well as industry-standard protocols for text and bit map graphics.

LN03S

The LN03 Plus is a letter-quality laser printer that operates at 8 pages per minute. Like the LA75, the LN03 uses Digital printer protocols. With the addition of a plug-in ROM cartridge, the LN03 provides industry-standard compatibility.

LN03X-IC

This plug-in ROM cartridge enables the LN03 Plus to use industry-standard protocols.

1.3 Country Specific Configurations

The following example is a typical VAXmate workstation.

PC500-BA Model Number	Component
PC500-B2	Building block
LK250-AA	English language keyboard
VSXXX-AA	Mouse
PC50X-CB	ThinWire assembly kit
BN19P-1K	Power cord 17-00606-02
RX33K-01	Blank RX33 diskette

The following tables supply country specific component information for VAXmate base systems.

VAXmate Model PC500	Screen Color	Base System User
-BA	Green	U.S.A.
-BC	Green	French Canada
-BD	Green	Denmark
-BE	Green	English speaking users outside U.S.A.
-BF	Green	Finland
-BG	Green	Germany
-BI	Green	Italy
-BK	Green	French Swiss
-BL	Green	German Swiss
-BM	Green	Sweden
-BN	Green	Norway

-BP	Green	France
-BQ	Green	Canada
-BR	Green	Israel
-BZ	Green	Australia and New Zealand
-CA	Amber	U.S.A.
-CC	Amber	French Canada
-CD	Amber	Denmark
-CE	Amber	English speaking users outside U.S.A.
-CF	Amber	Finland
-CG	Amber	Germany
-CI	Amber	Italy
-CK	Amber	French Swiss
-CL	Amber	German Swiss
-CM	Amber	Sweden
-CN	Amber	Norway
-CP	Amber	France
-CQ	Amber	Canada
-CR	Amber	Israel
-CS	Amber	Spain
-CZ	Amber	Australia and New Zealand
-FD	Green	Canada, bi-lingual
-GD	Amber	Canada, bi-lingual

Base Systems

Base System	Model Number	Component
PC500-X2	PC500-B2	building block
	VSXXX-AA	mouse
	PC50X-CB	ThinWire assembly kit
	RX33K-01	blank RX33 diskette
PC500-X3	PC500-B3	building block
	VSXXX-AA	mouse
	PC50X-CB	ThinWire assembly kit
	RX33K-01	blank RX33 diskette
PC500-Y2	PC500-C2	building block
	VSXXX-AA	mouse
	PC50X-CB	ThinWire assembly kit
	RX33K-01	blank RX33 diskette
PC500-Y3	PC500-C3	building block
	VSXXX-AA	mouse
	PC50X-CB	ThinWire assembly kit
	RX33K-01	blank RX33 diskette

Power Cords

Model Number	Country	Part Number
BN19A-2E	U.K./Ireland power cord	17-00209-08
BN19C-2E	Austria, Belgium, Brazil, Finland, France, Germany, Holland, Norway, Portugal, Spain, Sweden power cord	17-00199-12
BN19E-2E	Switzerland power cord	17-00210-05
BN19H-2E	Australia/New Zealand power cord	17-00198-07
BN19K-2E	Denmark power cord	17-00310-05

BN19M-2E	Italy power cord	17-00364-08
BN19P-1K	North American, Japan, Mexico power cord	17-00606-02
BN19S-2E	India/Africa power cord	17-00456-08
BN19U-2E	Israel power cord	17-00457-08

Keyboards

Model Number	Country
LK250-AA	English language keyboard
LK250-AC	Canadian/French language keyboard
LK250-AD	Danish language keyboard
LK250-AF	Finnish language keyboard
LK250-AG	German language keyboard
LK250-AI	Italian language keyboard
LK250-AK	Swiss/French language keyboard
LK250-AL	Swiss/German language keyboard
LK250-AM	Swedish language keyboard
LK250-AN	Norwegian language keyboard
LK250-AP	French language keyboard
LK250-AR	Hebrew language keyboard
LK250-AS	Spanish language keyboard
LK250-ED	Canadian bi-lingual language keyboard

VAXmate Manual

AZ-JC47A-TH *VAXmate System Handbook* (English)

Or another language manual.

1.4 Technical Block Diagram

Figure 1-8 depicts the relationship of the VAXmate workstation components. The optional components appear in dashed lines. The CPU module and the I/O module use a common bus to communicate with one another, and with industry-standard peripheral devices. VAXmate workstation components connected to the bus can request to use the bus without consuming valuable processor time. Such a component that qualifies as a DMA device can request to become bus master. As bus master, the DMA device can access memory quickly without using the processor's services. Any option added to the system also connects to the system bus using either an 8-bit bus or a 16-bit bus. The processor also recognizes interrupt requests from peripheral devices along the bus, such as the serial communications port. When the processor acknowledges the interrupt request, communication along the bus takes place.

The bus also extends into the expansion box, if installed. Devices, such as the hard disk controller, also place interrupt requests on the bus. Industry-standard options plugged into the expansion box card cage can also use this bus. The expansion box has its own power controller to provide dc voltages to the disk drive and industry-standard options. There are also two Lithium batteries that provide battery-backup for the real-time clock/event timer on the VAXmate CPU module. Notice that battery-backup is available only when an expansion box is present.

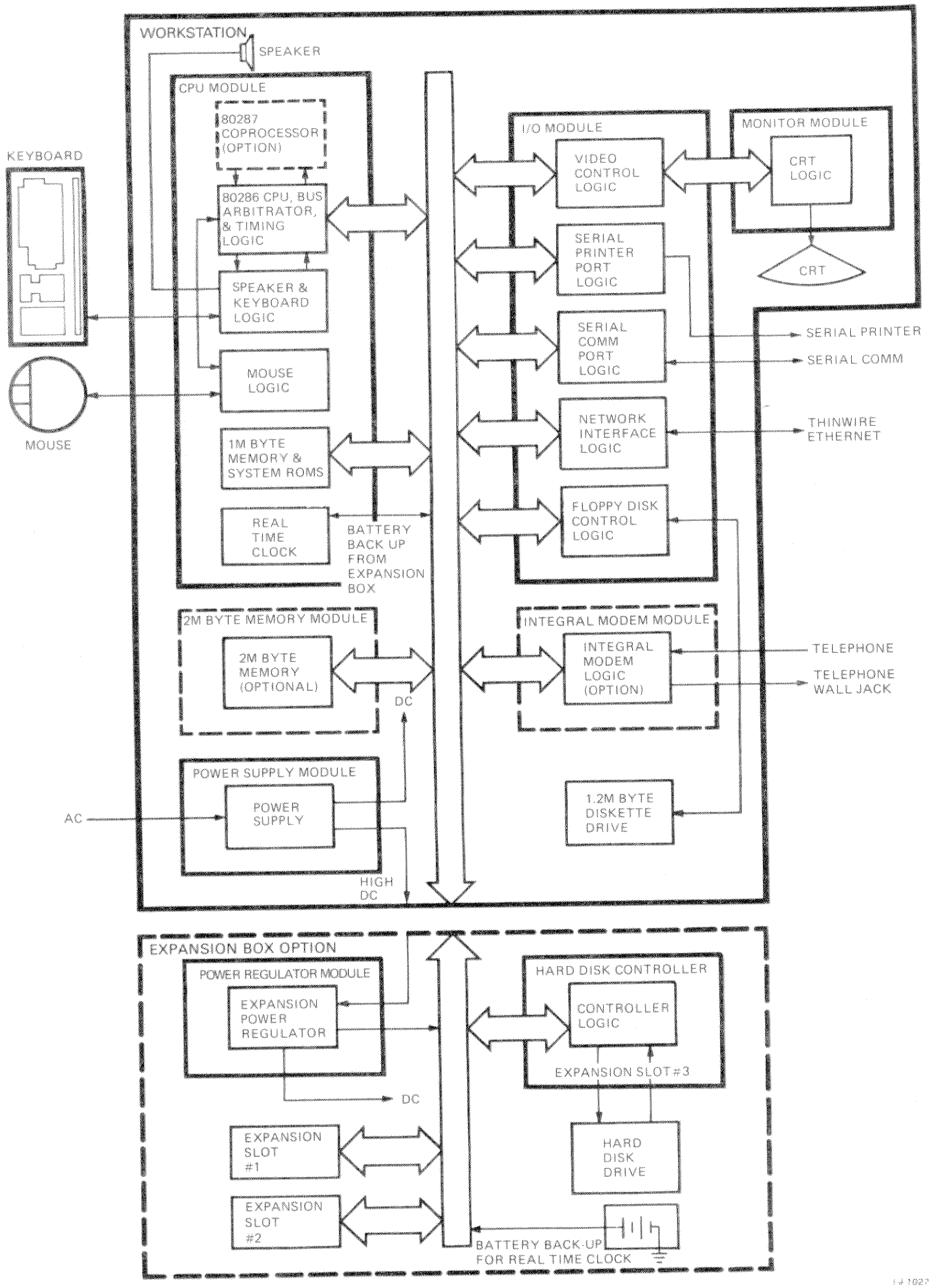


Figure 1-8 Block Diagram of VAXmate Components

Chapter 2
VAXmate CPU Module

2.1 Introduction

The VAXmate central processor unit (CPU) module is a single-board module that contains a clock generator, central processor unit, coprocessor, one megabyte memory, bus control circuitry, interrupt controllers, direct memory access (DMA) controller, real-time clock, 3-channel counter/timer, keyboard, and mouse control circuitry. It also contains buffers, registers, and counters, which are used to interface various bus structures within the module. Appendix C contains a detailed block diagram of the CPU module.

2.2 Clock System

The CPU module clock system is run by a 31.95 MHz oscillator (Engineering Print Set, PC500 CPU 286, Sheet 3) that is subdivided to provide clock signals as follows.

- 16 MHz clock – used by the CPU, Coprocessor, and the reset logic. Also used for bus timing (sheet 14).
- 8 MHz clock – used by the refresh control logic (sheet 8), keyboard logic (sheet 11), bus timing and the wait state generator (sheet 14). It is also routed to the memory interface, I/O interface, and the expansion box.
- 4 MHz clock – used by the DMA controller (sheet 7), DMA and LAN control (sheet 8), and the wait state generator (sheet 14).

Additional timing is provided by the following oscillators.

- 32.768 KHz oscillator – generates the clock for the event timer (sheet 9).
- 14.318 MHz oscillator – generates the clock for the expansion box and the timer logic (sheet 3).
- 5.0688 MHz oscillator – generates the clock for the mouse interface logic (sheet 10).

2.3 Microprocessor

The VAXmate workstation microprocessor is a 68-pin VLSI 80286 Central Processor Unit (CPU). This CPU is a high performance 8 MHz microprocessor with a 16-bit external data path. The 80286 CPU provides two modes of operation: real address mode and protected virtual address mode. Additional components support Direct Memory Addressing (DMA), timing, interrupts, data buffering, and bus structures. An optional 80287 numeric processor extension (coprocessor) can be added to include extended integer and floating-point data types in numeric processing.

2.4 Coprocessor

The optional 80287 coprocessor is a high performance numeric processor that extends CPU capability with the addition of floating-point, extended-integer, and binary-coded-decimal (BCD) data types. The Coprocessor obtains instructions from the CPU, and processes the high-precision numeric instructions in conjunction with the CPU.

2.5 Memory

The basic VAXmate workstation computer memory comprises 1 Mbyte of RAM memory and 64 Kbyte of ROM memory. An additional 2 Mbyte RAM memory can be supported if needed.

2.5.1 1 Mbyte RAM Memory

The 1 Mbyte RAM memory connects to the 16-bit bus. The memory has a maximum data access time of 150 ns, a Column Address Strobe (CAS) access time of 75 ns, and a cycle time of less than 375 ns (which includes one wait state). This memory consists of two banks (bank 0 and bank 1), each containing two 256K × 9 RAMs with byte parity generation and checking (Figure 2-1, 1 Mbyte RAM Memory).

A DMA-type refresh controller refreshes the dynamic memory in the system. Two rows of dynamic memory are refreshed every 30 microseconds in a period of six bus cycles (750 nanoseconds per refresh), and all 256 rows of RAM are refreshed every 4 microseconds.

The total memory address space is 16 Mbytes in length and divided into two access modes: real address mode (1 Mbyte) and protected address mode (15 Mbytes). (See Figure 2-3, Memory Address Partitioning).

Because of PC compatibility, the first megabyte of RAM is mapped into three non-contiguous address spaces: 000000-09FFFF, 0D0000-0EFFFF, and F20000-F5FFFF. The 2 Mbyte optional RAM is mapped into a single address space, 100000 – 2FFFFF.

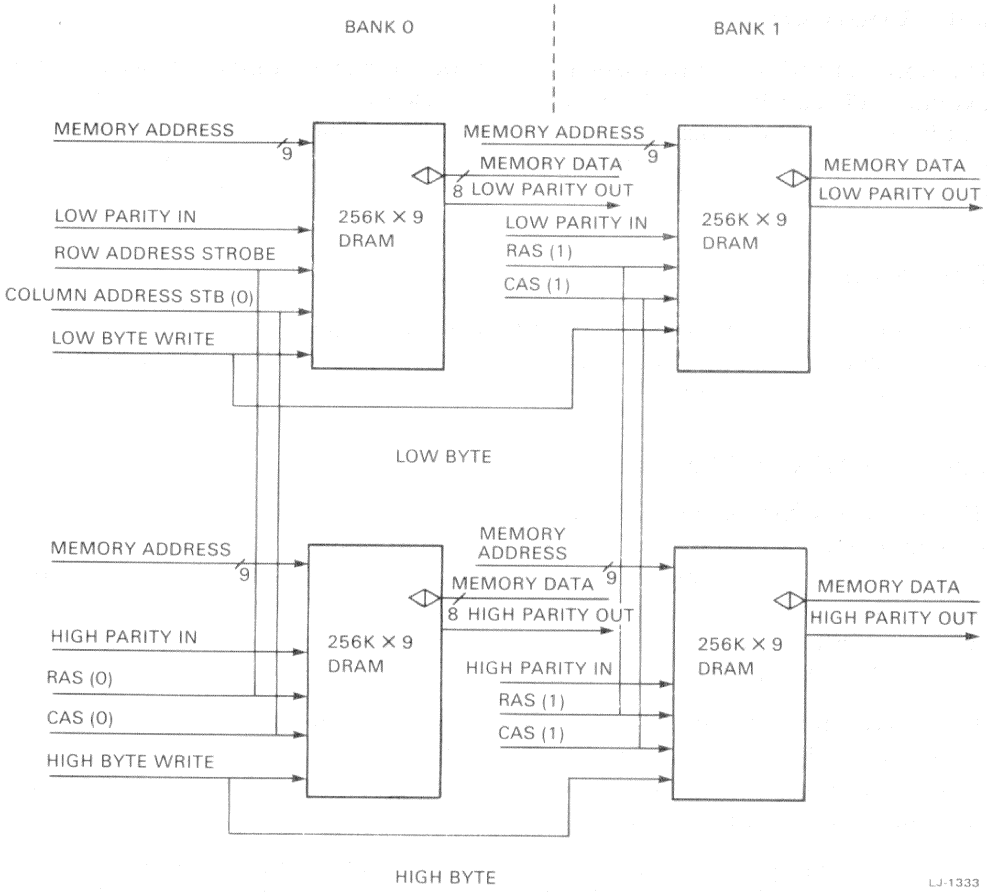


Figure 2-1 1 Mbyte RAM Memory

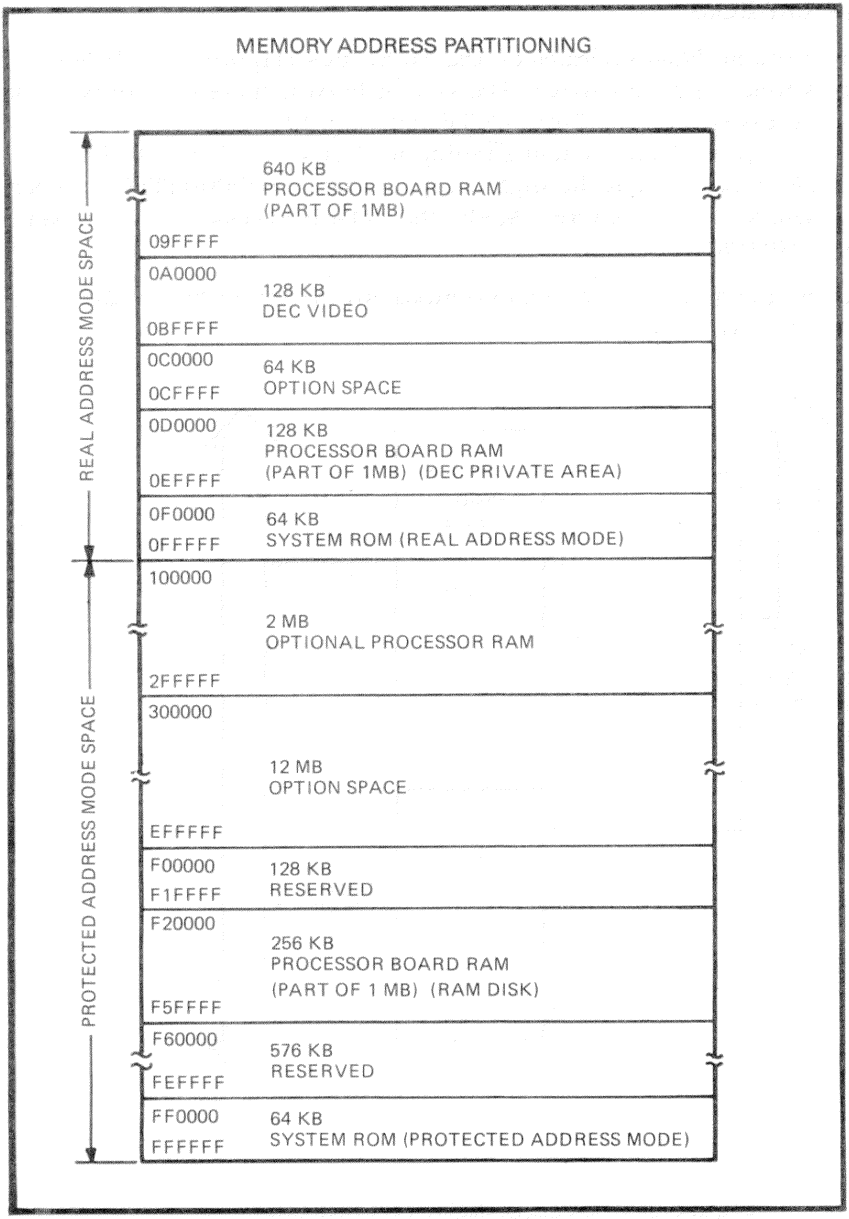


Figure 2-2 Memory Address Partitioning

2.5.2 System ROM

The 64 Kbyte system ROM operates on the 16-bit bus (Figure 2-3). It has a 250 ns access time (one wait state). The system ROM is mapped into two non-contiguous address spaces: 0F0000-0FFFFF and FF0000-FFFFFF (Figure 2-2). At initial power-up, with the system running in Protected Virtual Address mode, the ROM is accessed at the high address range (FF0000-FFFFFF). When the system switches to Real Address Mode, the ROM is accessed in the lower address range (0F0000-0FFFFF).

Reserved areas, and areas for video and options, are shown in Figure 2-2, Memory Address Partitioning.

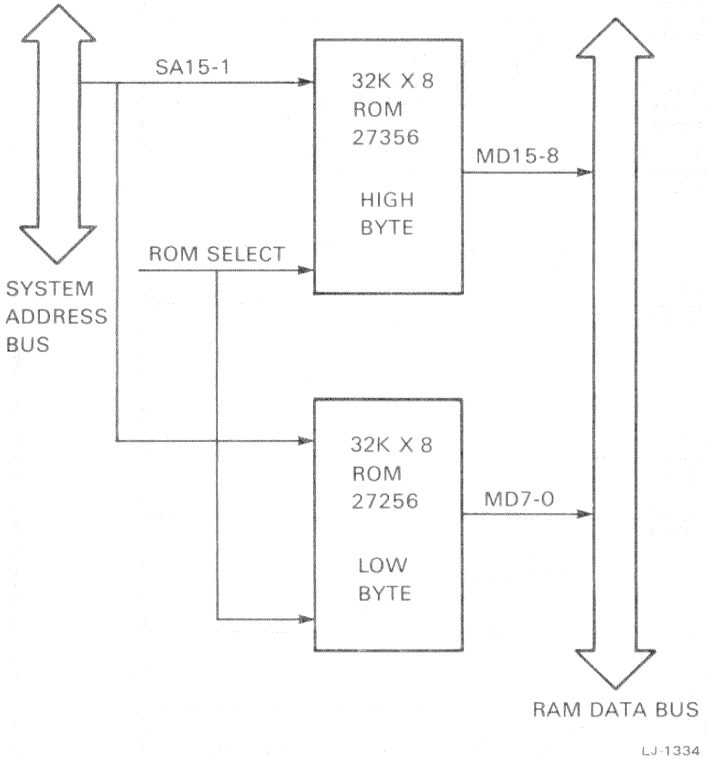


Figure 2-3 System ROM (UVEPROM)

2.5.3 2 Mbyte Memory Option

The 2 Mbyte memory option provides the VAXmate workstation with additional dynamic memory. This option is mounted on a daughter card that connects to the CPU module through a 62-pin connector. Memory timing mode is identical to the CPU memory. Each contains an additional wait state in the standard 80286 read/write cycles, which results in a 375 ns memory cycle time. The option performs byte parity generation and parity error detection.

Memory addressing is decoded from the Unlatched Address (UA) lines, and is allocated as shown in Table 2-1. Figure 2-2 shows the location of the 2 Mbyte memory addressing space.

Table 2-1 2 Mbyte Memory Map

Hex Address	Function
100000-17FFFF	Memory Option (Bank 0)
180000-1FFFFF	Memory Option (Bank 1)
200000-27FFFF	Memory Option (Bank 2)
280000-2FFFFF	Memory Option (Bank 3)

The 80286 CPU must operate in protected mode to access the 2 Mbyte memory. During normal read/write operations, only one memory bank is enabled at a time. All four banks are enabled simultaneously during refresh operations.

The option board contains four banks of dynamic memory and memory control circuits (Engineering Print Set PC500 RAM BD, sheets 4 and 5). Each memory bank has 18, 256K × 1 parts (16 for data, 2 for parity). Data may accessed in 8-bit bytes or 16-bit words, each with byte parity detection. When the memory option detects a parity error, an error LED (sheet 3) is illuminated. The CPU can enable or disable the LED using the EN RAM PCHK H signal (PC500 CPU 286, sheet 11).

2.5.3.1 Timing Modes

Read/Write Cycles – As mentioned previously, the memory option read/write cycle timing is identical to that of the processor board. Read or write cycles are completed in three CPU clock cycles running at 8 MHz. The first clock cycle is for address hold time from the previous bus cycle and address setup time for the current bus cycle. The second clock cycle is for command time (random read or early write command). The third clock cycle is an automatic wait state added by the processor board hardware.

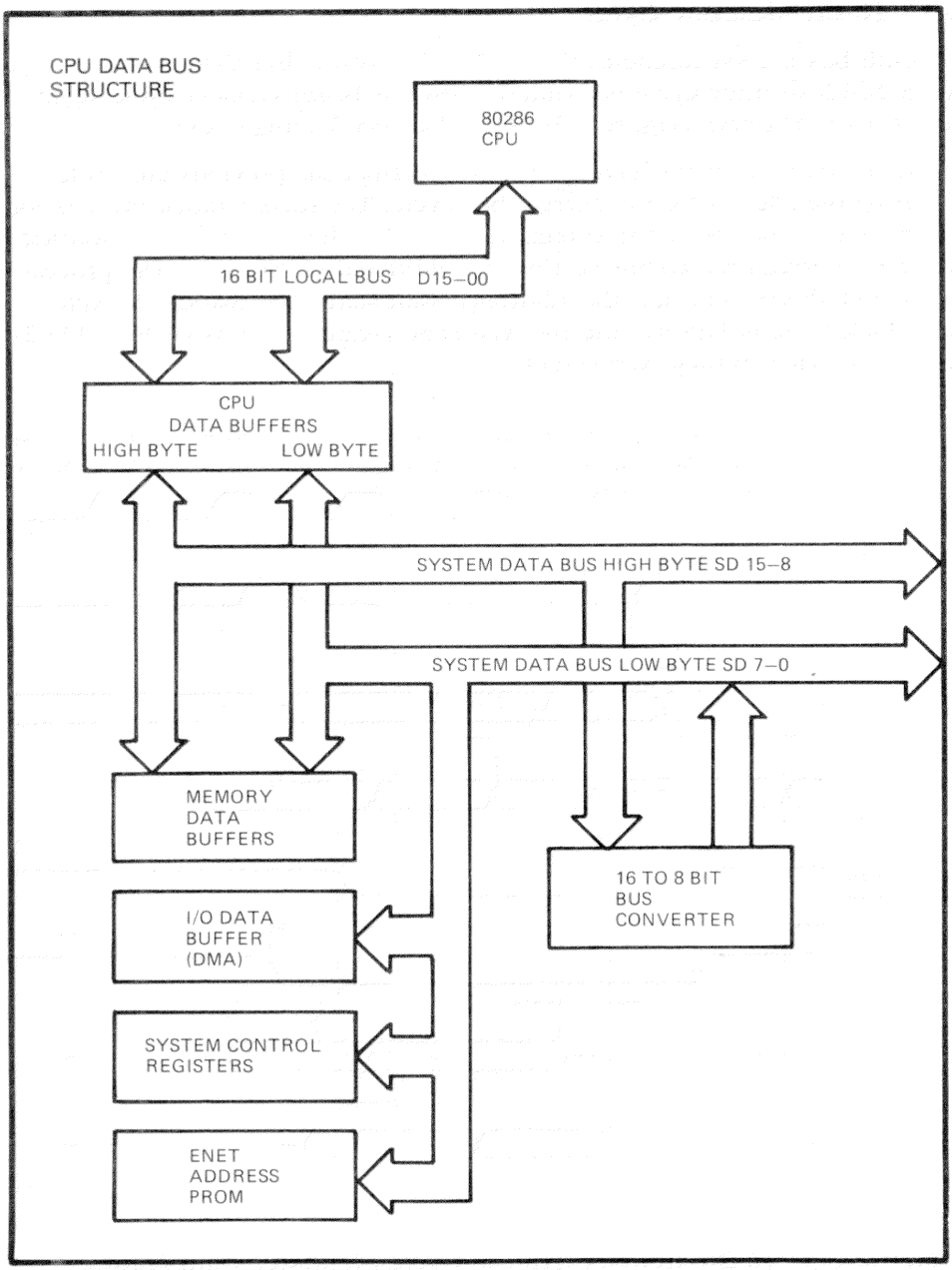
Refresh Cycles – The processor DMA controller refreshes two rows of the memory optionand CPU module RAM every 30 microseconds. The CPU module generates and transmits all refresh addresses and refresh timing signals to the memory option during refresh mode. The CPU refreshes its on-board memory and optional memory at the same time. During refresh mode, all four banks of the memory option RAM are enabled, all Row Address Strobe (RAS) signals are enabled, and Column Address Strobe (CAS) signals are disabled.

2.5.3.2 Memory Option Module Interface

The edge connector of the 2 Mbyte memory option module plugs into a 62-pin memory interconnect socket on the CPU module. Although the connector is the same size as the industry-standard 8-bit bus, it does not have similar signals. The memory option connector only connects to the VAXmate memory option module.

2.6 Bus Structure

There are two separate industry-standard bus structures within the VAXmate workstation: a 16-bit bus (buffered CPU bus), and an 8-bit bus (subset of the 16-bit bus). These structures are defined in Figure 2-4, CPU Data Bus Structure.



LJ-1191

Figure 2-4 CPU Data Bus Structure

2.6.1 16-Bit Memory Cycle

The 16-bit bus is a synchronous, three CPU-clock cycle bus that runs at 8 MHz. A 16-bit memory cycle is enabled when the 16-bit memory cycle signal (MEM16 L) is asserted. (Figure 2-5, 16-Bit Memory Timing Cycle.)

The first clock cycle is for holding the address from the previous bus cycle and setting the address for the current bus cycle. The second clock cycle is for memory read or memory write command time. The third cycle is an automatic wait state to extend the command time an additional clock cycle. The processor board hardware generates the additional wait state. The two clock cycles (each clock cycle is 125 ns) and the wait state create a 375 ns cycle. Table 2-2 lists the memory timing parameters.

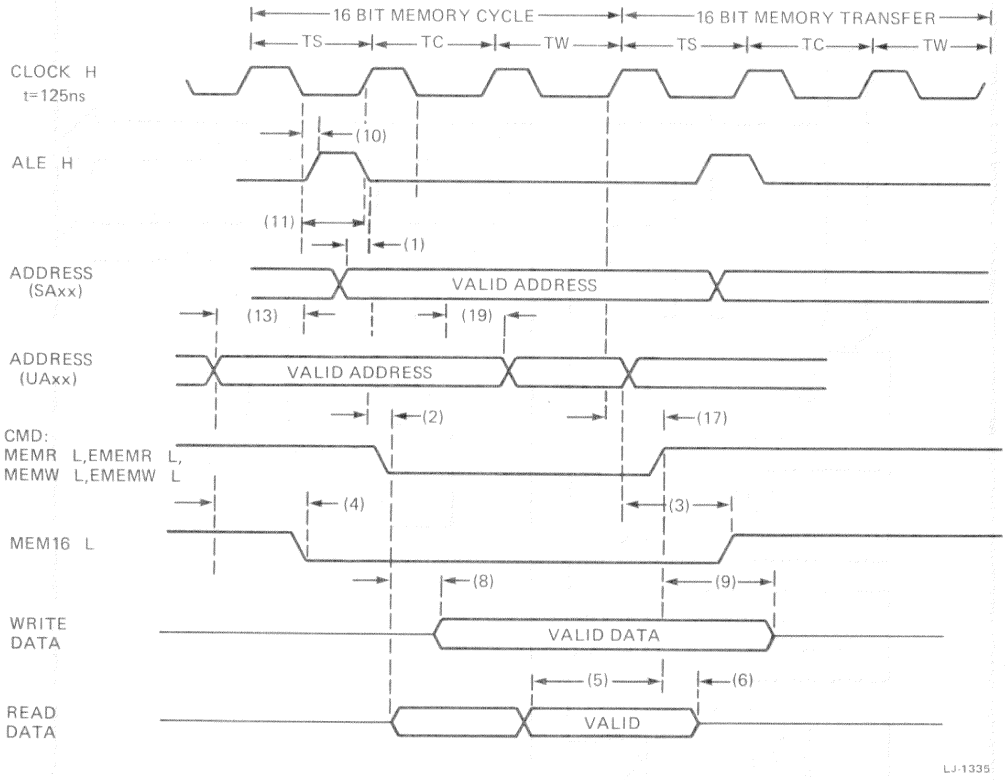


Figure 2-5 16-Bit Memory Timing Cycle (Transfer Data Mode)

Table 2-2 16-Bit Memory Timing Parameters

Ref. No.	Signal	Minimum (ns)	Maximum (ns)
1	Address set up to ALE trailing edge	51.5	74.5
2	CMD leading edge from CLOCK rising edge	5.5	26.5
3	MEM16 falling edge from address (UAxx)	0	80
4	MEM16 leading edge from address (UAxx)	0	80
5	DATA valid to MEMR trailing edge	23	–
6	DATA hold from MEMR trailing edge	5	–
7	CMD disable from CLOCK rising edge	5.5	26.5
8	DATA valid from MEMW trailing edge	0	20
9	DATA hold from MEMW trailing edge	40	–
10	ALE valid to CLOCK falling edge	6	21
11	Address valid to CLOCK trailing edge	8	18
12	CMD leading edge from CLOCK falling edge*	5.5	26.5
14	DATA valid from MEMW leading edge*	0	55
15	DATA hold from MEMW trailing edge*	23	–
17	CMD disable from CLOCK rising edge*	5.5	26.5
18	Address (UAxx) stable to CLOCK falling edge	55	–
19	Address (UAxx) hold from CLOCK falling edge	0	65

* 8-bit Memory

NOTE

All parameters assume total bus load of 50 pF. The bus clock (CLOCK H) is synchronous to the 80286 clock, but may lead the 80286 clock by 3 ns maximum.

2.6.2 16-Bit I/O Cycle

The 16-bit I/O cycle has one more wait state than the memory cycle. Also, the start of command is delayed one-half clock cycle, which allows a full clock cycle for setting up the address. I/O cycles are enabled by asserting the I/O signal (16 L) which indicates a 16-bit I/O cycle will be performed (Figure 2-6, 16-Bit I/O Timing Cycle). The system bus high enable signal (SBHE L) and system data bus bits (SD 15-0 H) are also active. Table 2-3 lists the I/O timing parameters.

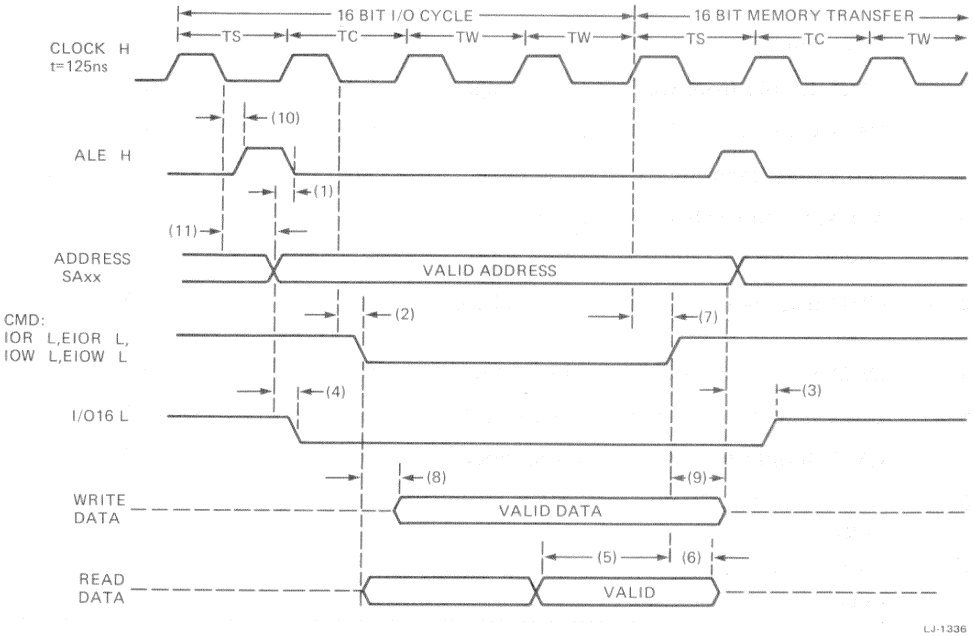


Figure 2-6 16-Bit I/O Timing Cycle (Transfer Data Mode)

Table 2-3 16-Bit I/O Timing Parameters

Ref. No.	Signal	Minimum (ns)	Maximum (ns)
1	Address set up to ALE trailing edge	51.5	74.5
2	CMD leading edge from CLOCK rising edge	5.5	26.5
3	I/O16 falling edge from address (SAxx)	0	80
4	I/O16 leading edge from address (SAxx)	0	80
5	DATA valid to IOR trailing edge	23	–
6	DATA hold from IOR trailing edge	5	–
7	CMD disable from CLOCK rising edge	5.5	26.5
8	DATA valid from IOW trailing edge	0	20
9	DATA hold from IOW trailing edge	40	–
10	ALE valid to CLOCK falling edge	6	21
11	Address valid to CLOCK falling edge	8	18
12	CMD leading edge from CLOCK falling edge*	5.5	26.5
14	DATA valid from IOW leading edge*	0	55
15	DATA hold from IOW trailing edge*	23	–
17	CMD disable from CLOCK rising edge*	5.5	26.5

* 8-bit I/O

NOTE

All parameters assume total bus load of 50 pF. The bus clock (CLOCK H) is synchronous to the 80286 clock, but may lead the 80286 clock by 3 ns maximum.

2.6.3 8-Bit Memory Byte Transfer

The 8-bit bus connects memory, I/O, and expansion options to the local data bus. This bus is synchronous to the 8 MHz bus clock. Data is transferred across SD7-0 H. SBHE H is not used (as in the 16-bit bus).

Memory byte transfers occur automatically when the 16-bit memory cycle signal (MEM16 L) is not asserted (Figure 2-7, 8-Bit Memory Timing Cycle). Address hold and address setup require 1-1/2 clock cycles. Command time requires 4-1/2 clock cycles, and includes four wait states, thus creating a cycle time of 750 ns.

Memory word transfers use two memory byte transfers for a cycle time of 1500 ns.

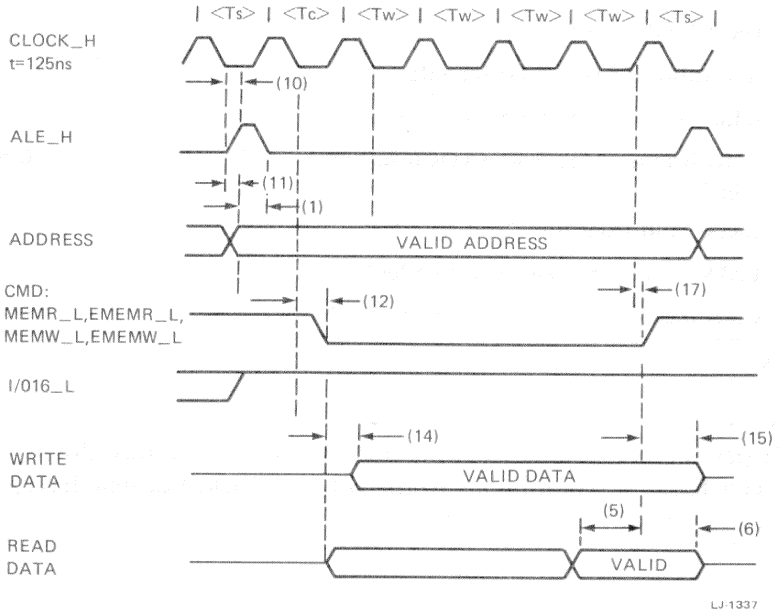


Figure 2-7 8-Bit Memory Timing Cycle

Table 2-4 8-Bit Memory Timing Parameters

Ref. No.	Signal	Minimum (ns)	Maximum (ns)
1	Address set up to ALE trailing edge	51.5	74.5
2	CMD leading edge from CLOCK rising edge	5.5	26.5
3	MEM16 falling edge from address (UAxx)	0	80
4	MEM16 leading edge from address (UAxx)	0	80
5	DATA valid to MEMR trailing edge	23	–
6	DATA hold from MEMR trailing edge	5	–
7	CMD disable from CLOCK rising edge	5.5	26.5
8	DATA valid from MEMW trailing edge	0	20
9	DATA hold from MEMW trailing edge	40	–
10	ALE valid to CLOCK falling edge	6	21
11	Address valid to CLOCK trailing edge	8	18
12	CMD leading edge from CLOCK falling edge*	5.5	26.5
14	DATA valid from MEMW leading edge*	0	55
15	DATA hold from MEMW trailing edge*	23	–
17	CMD disable from CLOCK rising edge*	5.5	26.5
18	Address (UAxx) stable to CLOCK falling edge	55	–
19	Address (UAxx) hold from CLOCK falling edge	0	65

* 8-bit Memory

NOTE

All parameters assume total bus load of 50 pF. The bus clock (CLOCK H) is synchronous to the 80286 clock, but may lead the 80286 clock by 3 ns maximum.

2.6.4 8-Bit I/O Byte Transfer

I/O byte transfers also occur automatically when I/O16 L is not asserted (Figure 2-8). Address hold and setup requires 2-1/2 clock cycles, and command time requires 6-1/2 clock cycles, including 7 wait states. The cycle time for this process is 1125 ns.

I/O word transfers are performed as two byte transfers in succession. Thus, the cycle time is 2250 ns.

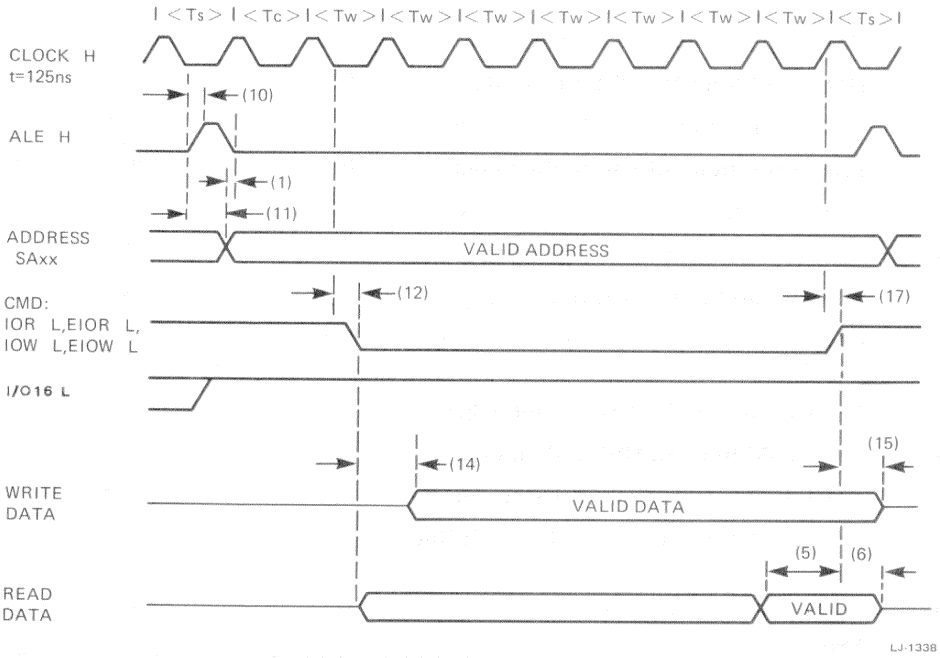


Figure 2-8 8-Bit I/O Timing Cycle

Table 2-5 8-Bit I/O Timing Parameters

Ref. No.	Signal	Minimum (ns)	Maximum (ns)
1	Address set up to ALE trailing edge	51.5	74.5
2	CMD leading edge from CLOCK rising edge	5.5	26.5
3	I/O16 falling edge from address (SAxx)	0	80
4	I/O16 leading edge from address (SAxx)	0	80
5	DATA valid to IOR trailing edge	23	–
6	DATA hold from IOR trailing edge	5	–
7	CMD disable from CLOCK rising edge	5.5	26.5
8	DATA valid from IOW trailing edge	0	20
9	DATA hold from IOW trailing edge	40	–
10	ALE valid to CLOCK falling edge	6	21
11	Address valid to CLOCK falling edge	8	18
12	CMD leading edge from CLOCK falling edge*	5.5	26.5
14	DATA valid from IOW leading edge*	0	55
15	DATA hold from IOW trailing edge*	23	–
17	CMD disable from CLOCK rising edge*	5.5	26.5

* 8-bit I/O

NOTE

All parameters assume total bus load of 50 pF. The bus clock (CLOCK H) is synchronous to the 80286 clock, but may lead the 80286 clock by 3 ns maximum.

2.7 Interrupt Controllers

The 8259A programmable interrupt controller (PI) is a 24-pin DIP chip. There are two interrupt controllers (a master and a slave) in the VAXmate workstation, each one capable of handling up to eight interrupt requests. The main function of the controllers is to accept interrupt requests, determine the request with the highest priority, and interrupt the CPU. The controller then supplies an interrupt vector to the CPU to identify the source of the interrupt. Once the CPU recognizes an interrupt operation, it transfers program execution to the interrupt vector address to perform one of 256 possible interrupt routines.

2.7.1 Interrupt Processing

The VAXmate 80286 CPU has two interrupt input lines: the interrupt request signal (PINTR H), and the nonmaskable interrupt signal (NMI H). (See the Engineering Print Set, PC500 CPU 286, Sheet 1.) When either of these input lines is active, the CPU suspends execution of the current program and begins execution of an interrupt handler. An interrupt handler is a program or program segment that responds to a specific event. This allows an immediate response to asynchronous external events, and the segregation of program responsibility for handling those events.

The interrupt lines have different classes of events. The NMI is for two catastrophic events: memory parity errors and I/O bus errors. The PINTR is assigned all other external interrupt sources, such as the diskette, the hard disk, the clock, or the serial and parallel ports. The reason for this division is the way in which the CPU handles the interrupts. The CPU handles the interrupts in the following ways.

1. The NMI has higher priority than the PINTR.
2. The CPU cannot disable the NMI input.
3. The CPU does not provide handshaking protocol during NMI processing.
4. The NMI generates only one interrupt vector, which is fixed.

Because the CPU does not provide handshaking during NMI processing, the CPU cannot communicate with an interrupt controller. Therefore, the NMI sources are connected directly to the NMI input. The NMI interrupt handler must read the status output of the sources to determine the origin of the interrupt.

The interrupt controllers reduce CPU interrupt processing overhead in the following ways.

1. They resolve the priority of simultaneous, or overlapping, interrupt requests.
2. They concentrate multiple interrupts into one source.
3. They provide the vector number of the interrupt handler.

As mentioned previously, each controller handles eight interrupt requests (Figure 2-9). Although the controllers are physically identical, they have a master/slave relationship. The output of the slave (controller 2) is connected to the interrupt request input line (IRQ2 H) of the master (controller 1). The output of the master is connected to the PINTR H input of the 80286 CPU. Table 2-6 lists the 8259A controller request input lines.

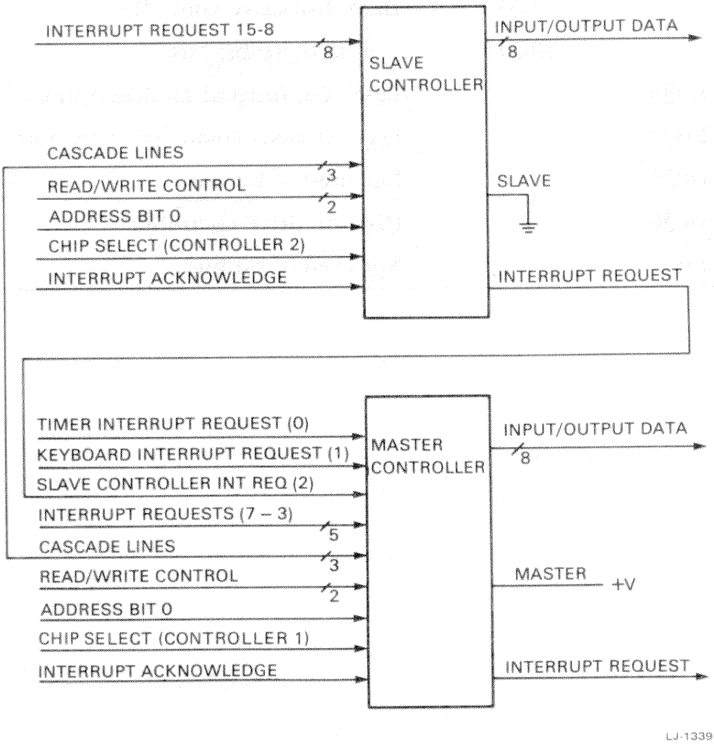


Figure 2-9 Interrupt Controllers

Table 2-6 Interrupt Request Lines

Priority	Master	Slave	Function
1	IRQ0		Event timer output 0
2	IRQ1		Keyboard buffer full
3	IRQ2		Slave interrupt controller(IRQ15-8)
3.1		IRQ8	Real time clock
3.2		IRQ9	Software re-direction to IRQ2
3.3		IRQ10	Lance (Ethernet)
3.4		IRQ11	Serial printer
3.5		IRQ12	Mouse UART
3.6		IRQ13	coprocessor error
3.7		IRQ14	Hard disk drive controller
3.8		IRQ15	Not used, 16-bit bus
4	IRQ3		Reserved, integral modem option
5	IRQ4		Asynchronous communication port
6	IRQ5		Not used, 8-bit bus
7	IRQ6		Diskette drive controller
8	IRQ7		Not used, 8-bit bus

2.7.2 Read/Write Control

The read/write control logic accepts two types of command words from the CPU: an Initialization Command Word (ICW), and an Output Command Word (OCW). The ICW registers bring the system to a starting point. The OCW registers store various control formats for device operation.

Although the 8259A controller has many registers, it has only two input/output (I/O) ports. Table 2-7 shows the master and slave I/O addresses.

Table 2-7 Master and Slave I/O Addresses

Port	Master	Slave
0	0020H	00A0H
1	0021H	00A1H

A brief description of the interrupt controller registers follows.

Initialization Command Words – There are four initialization command words (ICW1-ICW4). They establish the operating conditions of the interrupt controller and are only written during system initialization. The interrupt controllers do not have a hardware reset. After power is applied to the system, the controllers are in an undefined state until they are initialized. The VAXmate start-up code initializes the interrupt controllers. From two to four initialization command words are required to initialize the interrupt controller.

The interrupt controller recognizes ICW1 as the start of the initialization sequence. ICW1 resets the controller as follows.

1. The trigger mode is cleared to edge trigger mode and the edge sense circuit is reset. After initialization, an interrupt request input (IRQ H) must be made to the controller to generate an interrupt.
2. The interrupt mask register (IMR) is cleared.
3. Interrupt request line IRQ7 is assigned priority 7 (lowest).

4. Slave mode address is set to 7.
5. If bit 0 in ICW1 is 0, ICW4 is cleared.
6. In the output command word register OCW3, the special mask mode is cleared and status read bits are set to read the interrupt request register (IRR).
7. The interrupt controller enters fully nested mode.

   In fully nested mode, the interrupt inputs have a fixed order of decreasing priority (0 is highest, and 7 is lowest). While the CPU is servicing an interrupt, the controller inhibits interrupts of equal or lower priority. However, the current interrupt service can be nested in favor of a higher-priority interrupt as follows.

   a. The higher-priority interrupt input must be unmasked (enabled).

   b. The interrupt request input to the CPU must be enabled.

   NOTE
   The 8259A interrupt controller has the following methods of indicating whether a controller is a master or a slave.

   1. The initialization sequence selects nonbuffered mode in ICW4. In this mode, a hardware connection to the SP/EN pin of the controller determines whether the controller is a master or a slave. A high level indicates a master (see Sheet 10 of PC500 CPU 286, circuit E1), and a low level indicates a slave (circuit E8).
   2. The initialization sequence selects a buffered master or a buffered slave in ICW4 (refer to the *VAXmate Technical Reference Manual*, Q6ZCS-GZ).

The context of the master/slave relationship in the VAXmate workstation is determined in ICW3. When ICW3 contains all ones, the interrupt register input has a slave. If ICW3 has all zeros, the register input does not have a slave.

2.7.3 Operation Command Words

Operation command words command the interrupt controller to operate in various interrupt modes. The following words can be programmed into the controller anytime after initialization as operation command words.

- Read or write the interrupt mask register (IMR)
- Accept specific or nonspecific end of interrupt commands
- Enable or disable various automatic priority rotation schemes
- Set or reset the special mask
- Read poll data
- Read the interrupt request register (IRR)
- Read the in-service register (ISR)

Priority Rotation – In nonspecific or automatic end-of-interrupt (EOI) mode, priority rotation assigns equal priority to all interrupt inputs. When the interrupt controller receives the EOI, the controller assumes that the active interrupt input with the highest priority is the interrupt just completed. The priority bits are then rotated until the last completed interrupt is assigned the lowest priority (7). If that interrupt requires further service, it must wait until it becomes the highest priority interrupt, or until all other interrupts of higher priority are inactive.

For example, Figure 2-10 shows the priority and in-service status Set-Up with interrupt request 2 having the highest, and interrupt request 5 having the next highest priority requesting service. The priority will rotate as shown in Figure 2-11 .

Before rotation, in-service bit 2 has the highest priority, and bits 5 and 6 follow sequentially.

In-Service Bits

7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	0

Priority Status

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0

Figure 2-10 Priority Interrupt Status Before Rotation

After interrupt servicing, priority rotation causes bit 2 to have the lowest priority, and bit 3 to have the highest priority. Therefore, bit 5, which requires interrupt processing, has become the highest priority bit.

In-Service Bits

7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	0

Priority Status

7	6	5	4	3	2	1	0
4	3	2	1	0	7	6	5

Figure 2-11 Priority Interrupt Status After Rotation

Another method of setting priority is with specific rotation. In this method, the lowest priority is set, thereby fixing all other priorities. For example, if interrupt request 2 has been programmed as the lowest priority, then interrupt request 3 will be the highest. The Set Priority command is issued in output control word 2 (OCW2). Low order bits 2-0 define the priority level code of the lowest priority device.

Special Mask Mode – Some operations may require an interrupt service routine to change the priority structure during program execution. The service routine might want to disable low priority requests for part of its execution, and enable some low priority requests at another point during execution. The Special Mask mode is issued using output control word 3 (OCW3), which selectively enables interrupts by loading the mask register (IMR).

Poll Command – The polling method of interrupt processing may be used when there is a routine command common to several levels, and interrupt acknowledge processing is not required, thereby saving ROM space. This method may also be used to expand the number of priority levels beyond 64. The poll command is issued using OCW3.

2.7.4 Interrupt Registers

The Interrupt Request Register (IRR) and the In-Service Register (ISR) control interrupts from the interrupt request lines. The IRR stores all interrupt levels requesting service, and the ISR stores all interrupt levels being serviced. The interrupt controller determines the priority from the bits set in IRR, and then passes the information into corresponding bits in ISR. An interrupt mask register (IMR) stores the bits that will mask the interrupt lines that require masking. Masking a higher priority input does not affect the request lines of lower priority. Table 2-8 lists the interrupt controller I/O addressing scheme. The bit maps that follow the table describe the interrupt controller registers.

Table 2-8 Interrupt Controller I/O Addressing

Master	Slave	A0	Register
20	A0	0	ICW1, OCW2, OCW3
21	A1	1	ICW2, ICW3, ICW4, OCW1

2.7.5 Interrupt Sequence

The Interrupt Controller is programmed with interrupt routine addressing, which allows direct or indirect jumping to the specific interrupt routine requested without polling the interrupting devices. The normal sequence of events during an interrupt is as follows.

1. One or more interrupt lines (IRQn) become active, setting the corresponding IRR bits.
2. The interrupt controller evaluates these requests and, if appropriate, sends an interrupt signal to the CPU.
3. The CPU acknowledges the interrupt line and responds with an acknowledge pulse.

4. Upon receiving the acknowledge, the interrupt controller sets the highest priority ISR bit and resets the corresponding IRR bit.

5. A second acknowledge is issued by the CPU, causing the controller to place an 8-bit pointer onto the I/O data bus that is read by the CPU.

2.7.6 Interrupt Processing

The list of events and the flow chart that follows describe interrupt processing (see the flowchart in Figure 2-12). Each item in the list describes a system state or event. Following the description of a state or event is an additional statement pointing to the next state or event. In this section, assume that the interrupt controllers are initialized.

1. The interrupt controller is idle until one or more interrupt controller input lines become active. When one or more input lines are active, go to 2.

2. If any of the newly active inputs are unmasked (enabled), go to 4; otherwise, go to 3.

3. If other interrupt inputs are pending, go to 5; otherwise, go to 1.

4. When no other interrupts are pending, go to 7; otherwise, go to 6.

5. If the controller is waiting for an end of interrupt (EOI) command, go to 6; otherwise, go to 7.

6. If any interrupt has a higher priority than the one being processed by the CPU, nest the interrupts and go to 7; otherwise, go to 8.

7. The controller activates its interrupt request output line (INTR H) and waits for an acknowledge signal (INTA16 L) from the CPU.

   a. If the interrupt controller input indicates a slave input, then the slave interrupt output line (IRQ2 H) activates the master interrupt controller IRQ2 input (the master interrupt process starts at step 2). The IRQ2 input becomes the highest priority master interrupt line that is active, and the master controller arrives at this point. At this time, both master and slave controllers are waiting for the CPU acknowledge signal.

b. In either case, the master controller activates its interrupt request line (INTR H), which triggers an external latch, and drives the CPU interrupt request input (PINTR H).

c. When the CPU request input is disabled, the interrupt controller continues to wait. If other interrupt controller inputs become active during this waiting period, go to 2. When the CPU request input is enabled, the CPU accepts the request and responds with an acknowledge signal (INTA16 L).

d. When the interrupt controller receives the acknowledge, it sets the highest priority bit in the in-service register (ISR), and resets the corresponding bit in the interrupt request register (IRR). This allows the controller to accept another interrupt request.

e. Next, the CPU issues a second acknowledge signal. When the master interrupt controller accepts the second acknowledge signal, it determines whether or not the interrupt input source is a slave interrupt controller. If the interrupt input source is not a slave, the master controller places a preprogrammed 8-bit interrupt vector on the input/output (I/O) data bus. When the interrupt source is a slave controller, the master controller places the slave address (master interrupt input number 0-7) on the cascade lines. This enables the slave controller to place the preprogrammed 8-bit interrupt vector on the I/O data bus. In either case, the CPU reads the 8-bit interrupt vector, stacks the current state, and begins executing the interrupt handler that is specified by the contents of the interrupt vector.

f. The interrupt controllers are waiting for an end of interrupt (EOI) command. When a slave interrupt is processed, both the slave and the master require an EOI command. If an interrupt occurs during this waiting period, go to step 2. When the CPU writes the end of interrupt command, go to step 1.

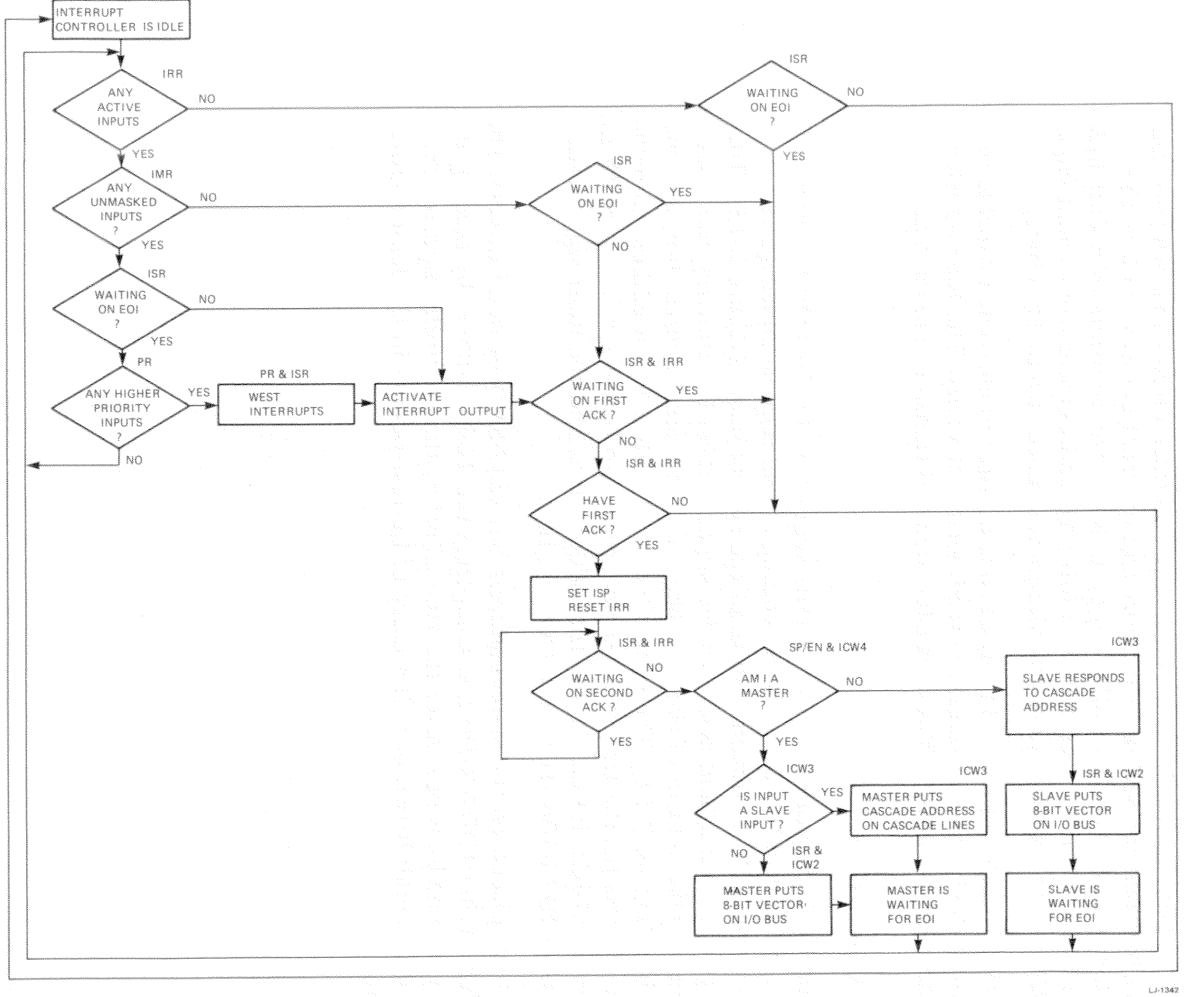


Figure 2-12 Interrupt Processing Flowchart

2.8 DMA Controller

The 8237A DMA controller is a 40-pin DIP interface circuit that permits data transfers between the VAXmate memory and external devices, such as the RX33 floppy disk. This controller supports 8-bit data transfers over four independent DMA channels, each having a full 64K address and word count capability. DMA page registers perform address references up to 16 Mbytes.

The DMA controller operates in one of four transfer modes, each capable of performing three types of transfers: read, write, or verify. The four transfer modes are single transfer, block transfer, demand transfer, and cascade.

2.8.1 Operation

When the DMA controller receives a DMA request (DRQ3-DRQ0 H) on a DMA channel, the controller responds by sending a hold request signal (8237 REQ H) to the CPU to obtain control of the system buses (Figure 2-13). The CPU responds with a hold acknowledge signal (HLDA L), allowing the DMA controller to take control of the I/O data bus, the system address bus, and the control bus (Figure 2-14). The controller then sends a 16-bit address to memory. The address for the first transfer occurs in two bytes: the least significant eight bits (BA7-BA0 H) on the internal address bus, and the most significant eight bits (IOD7-IOD0 H) on the I/O data bus.

BA7-BA0 are placed on the system address bus (SA7-SA0) by octal drivers. The controller latches IOD7-IOD0 and completes the 16-bit address by placing it on the system address bus. After the first transfer, the controller updates the latched data (high byte), only if a carry or borrow occurs in the least significant byte.

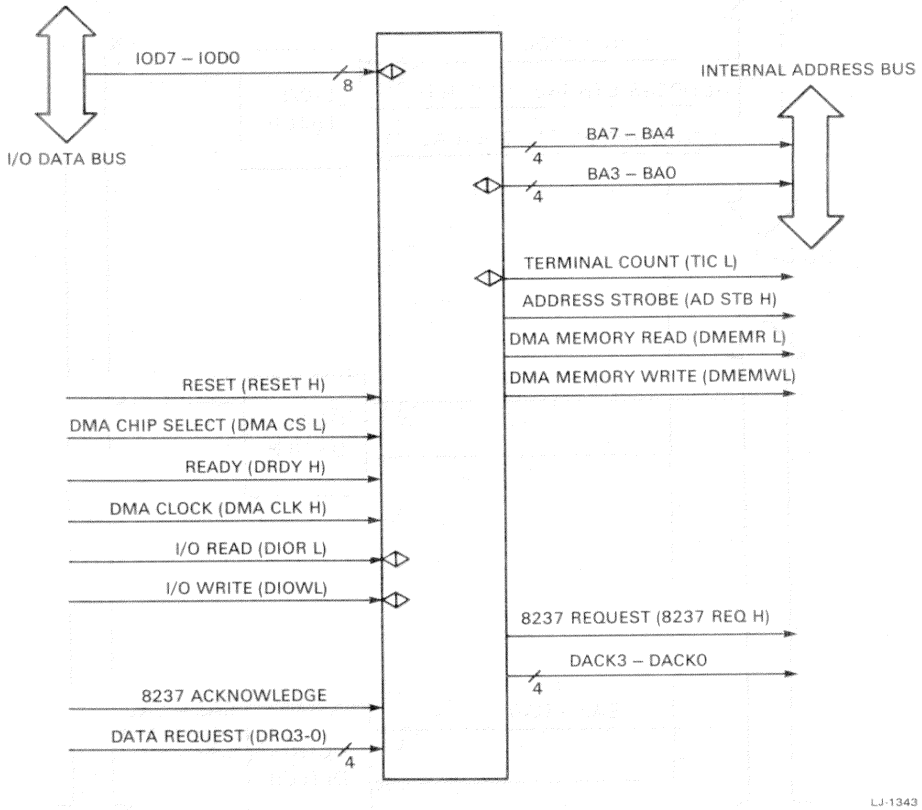


Figure 2-13 Programmable DMA Controller

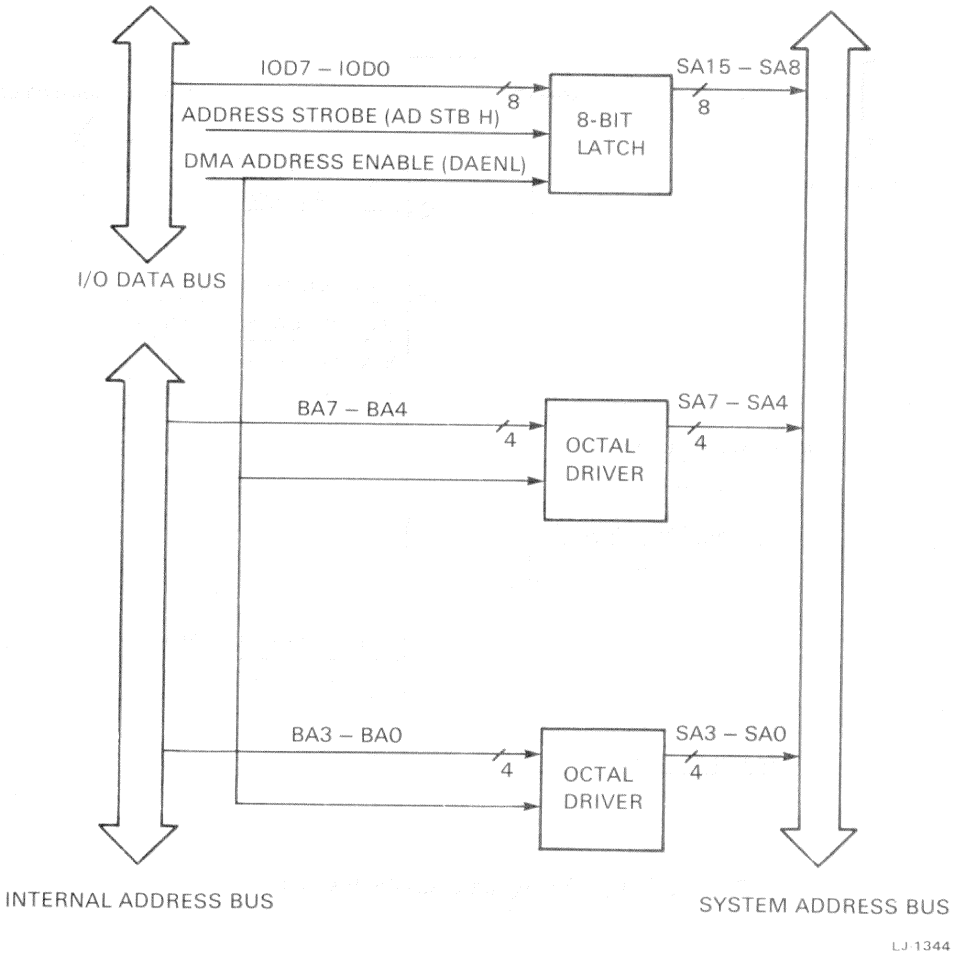


Figure 2-14 DMA Address/Data Buffers Functional Block Diagram

The DMA controller operates in two major cycles: idle and active. Each device cycle consists of from one to seven states, each being one full clock period in duration. Table 2-9 describes the various controller states.

Table 2-9 DMA Controller States

State	Description
SI	Inactive state: No valid DMA requests pending. The CPU can program the DMA controller.
SO	First state of DMA service: The controller has requested a hold (8237 REQ H), but the processor has not returned an acknowledge (HLDA L). Programming the DMA can continue until the acknowledge is received, signifying that DMA transfers may begin.
S1-S4	DMA working states: When more time is required to complete a transfer, wait states (SW) can be inserted between S2 and S3 or S3 and S4 by sending a ready signal (DRDY H) to the controller.

2.8.1.1 Device Cycles

Idle Cycle – If there are no I/O channels requesting DMA service, the DMA controller enters the idle cycle and performs inactive states (SI states). While in the idle cycle, the controller samples the data request lines (DRQ3-DRQ0 H) every clock cycle, to determine if a channel is requesting service. The controller also samples the chip select signal (see DMA CS L in Figure 2-13), to determine if the CPU is attempting to communicate with the DMA controller. If DMA CS L is active and the CPU has control of the system buses, the CPU can program the DMA controller by reading from or writing to the controller internal registers.

Active Cycle – The active cycle is entered from the idle cycle when a nonmasked channel requests DMA service. When this occurs, the controller issues a hold request (8237 REQ H) to the CPU and enters the active cycle. DMA service then occurs in one of the following modes.

Single Transfer Mode – The DMA controller performs only one transfer. After the transfer, the word count is decremented, and the address is either decremented or incremented. When the word count goes from 0000 to FFFF(hex), a Terminal Count (T/C) signal is generated that will auto-initialize the selected nonmasked channel to its original value if it had been programmed to do so. When T/C L occurs, the 8237 terminates service and resets the request. In addition, if auto-initialize is enabled, the 8247 writes the Base Word Count Register and Base Address Count Register to the Current Word Count Register and Current Base Address Register of the selected channel. The mask bit and T/C bit in the Status Word Register are set to the active channel by the end of process signal (EOP), unless the channel is programmed for auto-initialize.

The DMA request line (DRQn H) must remain high until the acknowledge line (DACKn L) goes low. If the request line is held high throughout the transfer, the hold request line (8237 REQ H) will go low and release the bus to the processor. When 8237 REQ H goes high again and another 8237 ACK H is received, another single transfer can be performed.

Block Transfer Mode – In this mode, a DMA request activates the DMA controller, which continues making transfers until a T/C (word count has reached FFFF) or an external end-of-process (EOP) signal occurs. If the channel has been programmed for auto-initialization, the transfer occurs at the end of service. A program should limit this mode to eight transfers to prevent interference with refresh cycles. (NOTE: There should be no additional wait states.)

Demand Transfer Mode – The DMA controller performs transfers until a T/C or an external EOP occurs, or until there is no DMA request. These transfers continue until the data capacity of the I/O device is exhausted. Once the I/O device obtains new data, DMA service is re-established through a DMA request. While the CPU is running, the intermediate values of address and word count are contained in the current address register and current word count register during the time between services. At the end of the DMA service, only an EOP can cause an auto-initialize to occur. A program should limit this mode to four transfers per demand to prevent interference with LANCE cycles.

Cascade Mode – This mode is used when DMA controllers are connected for system expansion. In this configuration, the initial controller determines the priority of the additional controllers. Each of the additional controllers establishes priority within itself, and sends the DMA request to the initial controller. The initial controller does not output any address or control signals, since these signals could conflict with the outputs of the added controller.

2.8.1.2 Data Transfers

The DMA controller performs read, write, or verify operations in each transfer mode. Read operations transfer data from memory to an I/O device, write operations transfer data from an I/O device to memory, and verify operations are pseudo-data transfers. In verify mode, the controller operates as if it were in read or write mode, except the memory and I/O control lines are not active.

Auto-Initialize – The auto-initialize mode restores the selected DMA channel to its original value following an end-of-process (EOP) signal. This is accomplished by restoring the original values of the Current Address and Current

Word Count registers from the Base Address and Base Word Count registers. The CPU simultaneously loads the current registers and base registers, which do not change during the DMA service. When the channel is in auto-initialize mode, the mask bit is not set. After auto-initialization and a DMA request is received, the channel can perform DMA service without CPU intervention.

Priority – The two types of priority are fixed and rotating.

1. Fixed Priority – In fixed priority, the channels are placed in order based on the descending value of their assigned number. The assigned number range is from zero to three (0-3), with zero having the highest priority.
2. Rotating Priority – The channel being serviced is assigned lowest priority value, and all other channels rotate to the next higher value.

Address Generation – The eight high-order address bits (15-08) are multiplexed on the I/O data lines (IOD7-IOD0 H), and are output to an external latch and then placed on the system address bus (SA15-SA8) at time state S1. The low-order bits are output directly from the DMA controller to the system address bus. For multiple transfers, such as block and demand transfers, the addresses are generated sequentially. The data in the external latch (high-order byte) can remain the same for many transfers, and only has to be changed when a borrow or carry takes place in the normal sequence of addresses. The controller executes S1 states only when an update of the high order byte is required.

2.8.2 DMA Page Registers

The DMA page registers are used to provide additional addresses not supplied by the 8237A DMA controller (Figure 2-15). The controller drives SA15-SA0, which permits transfers on 64 Kbyte boundaries, and the page registers provide address references to 16 Mbytes. Page register control is programmed through processor I/O commands.

The DMA page registers, which are write only, are as follows.

Port	DMA Channel	Address Lines
081 H	2	Bit 7-0, SA16, UA23-UA17
082 H	3	Bit 7-0, SA16, UA23-UA17
083 H	1	Bit 7-0, SA16, UA23-UA17
087 H	0	Bit 7-0, SA16, UA23-UA17

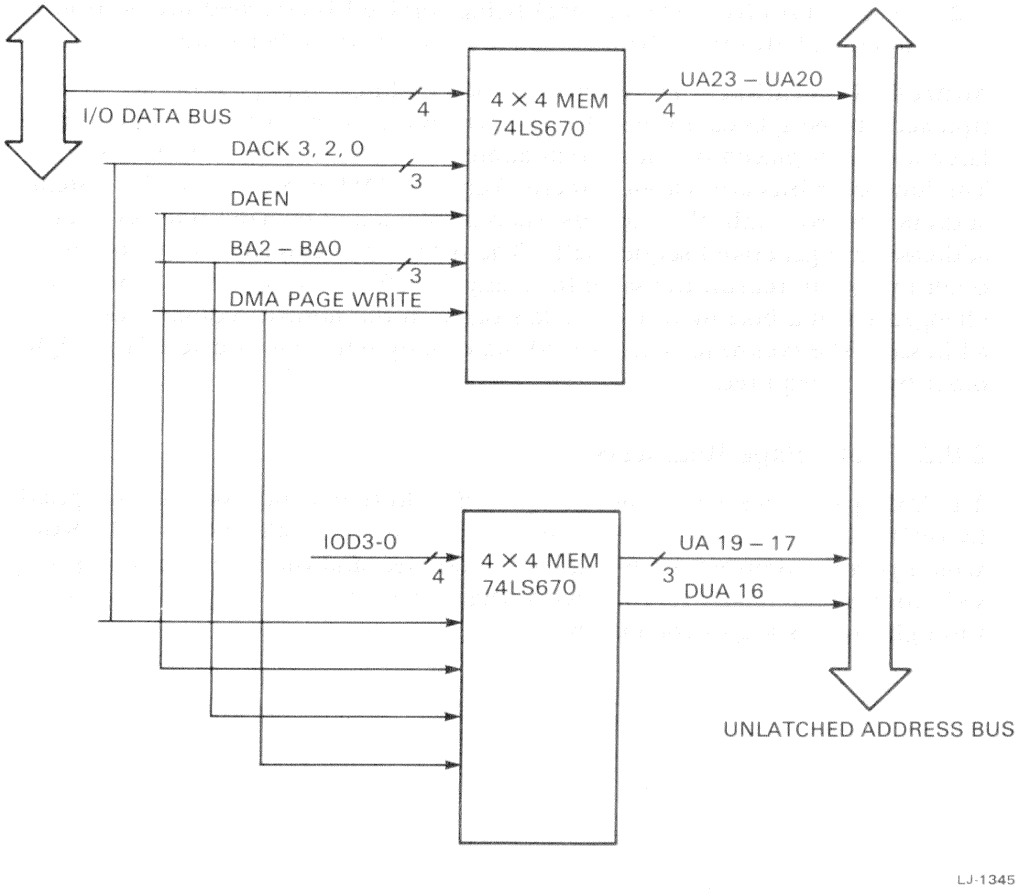


Figure 2-15 DMA Page Register Functional Block Diagram

2.8.3 Bus Mastership

An option plugged into the expansion box backplane can take control of the VAXmate bus from the processor board. The option taking control becomes the bus master, and processing takes place as follows.

A channel of the 8237A DMA controller is set up in cascade mode. The channel then asserts the DMA request line (DRQn H). When the DMA controller receives the acknowledge (DACKn L) from the processor, the bus has been released to the bus master. During the entire bus master cycle, ALE H and AEN H are held in the asserted state.

When the master signal (MASTER L) is asserted, the bus master has control of UA23-UA17, SA16-SA0, SBHE L,EMEMn L, and SD15-SD0. If the address is from 0 to 1 Mbyte, and EMEMn L is asserted, the processor board asserts MEMn L.

A bus master can only access memory on the processor board; it cannot access I/O devices on the processor board. To prevent the local area network (LAN) on the I/O board from getting a data overrun or underrun, a bus master should not hold the bus for more than 3 microseconds.

The bus is released when DREQn H is deasserted. Bus control should be released prior to, or at the same time as, DREQn H is deasserted.

2.8.4 Bus Arbitrator

A 3-channel bus arbitrator allows arbitration between the Local Area Network (LAN), DRAM refresh, and the 8237A DMA controller (Figure 2-16). The order of priority is LAN, refresh, and the 8237A controller. Therefore, if all three contend simultaneously for the bus, the LAN request will win, and the other two requests will be held until they gain control. When two requests are made simultaneously, the higher priority request will be serviced first, and the other request will be held. If a higher priority request occurs before the second request is started, the higher priority will again be serviced before the request that was held. The arbitrator uses two 8 MHz clock cycles, and the 80286 CPU uses the remaining cycles to grant the bus (using hold and hold acknowledge).

The I/O interface connector provides the path for the LAN to obtain bus control. The signals used for this purpose are bus request (LANREQ L) and LAN acknowledge (LANACK L). The following rules are required for LAN usage.

1. The bus should not be held for more than 5 microseconds after LANACK L is received. This allows other bus masters to use the bus for periods up to 3 microseconds. Deasserting LANREQ L releases the bus.
2. The bus may be used as soon as LANACK L is received. Within 125 ns after LANREQ L is deasserted, the bus must be released.
3. When LANREQ L is deasserted, the LAN should not request the bus until 125 ns after LANACK L is deasserted. This allows the 8237A controller to become bus master if it has a request pending.

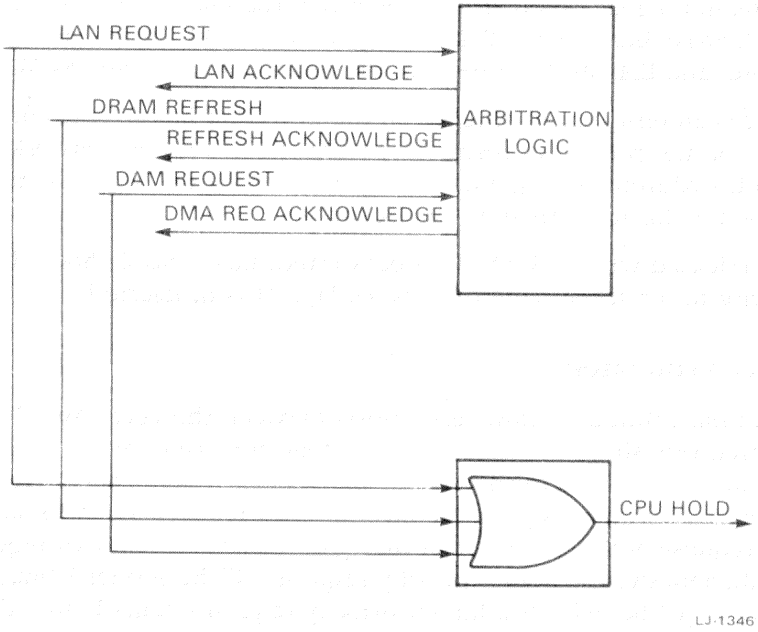


Figure 2-16 DMA Arbitration Functional Block Diagram

2.8.5 DMA Read Cycle

The 8237A DMA controller allows the transfer of data from a specific I/O device to sequential addresses in memory, as programmed by the controller. The following is a basic example of data being read from an RX33 diskette.

Whenever the RX33 requests to have data read, it must have a byte of data to send. It requests service from the DMA controller over the DRQ2 H signal line (Figure 2-17). The controller then issues a request (8237 REQ H) to the processor to gain control of the bus system. The processor responds by sending a hold acknowledge (8237 ACK H) to the controller, thereby releasing the bus. When the controller recognizes the I/O read (DIOR L), it generates DAEN L, which allows the data to be read from the I/O data buffer. The memory location where the data is to be stored is placed on system address lines (SA15-SA0), and the controller issues the memory write control signal (DMEMW L), which allows the data to be written to memory.

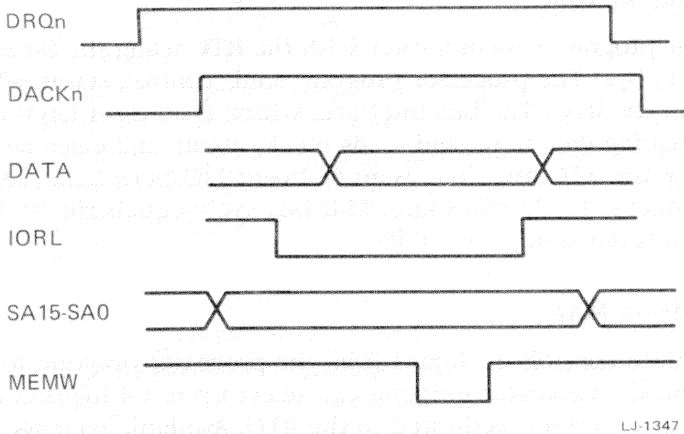


Figure 2-17 DMA Read Cycle Example

2.9 Real Time Clock and CMOS RAM

The VAXmate CPU board has an MC146818 real-time clock (RTC) with CMOS (complimentary metal-oxide silicon) RAM resident on a 24-pin dual-in-line chip. The RTC runs on +5 Vdc from the power supply when the VAXmate workstation is powered-up, and from a battery-backup circuit in the expansion box when the workstation is powered-down. The battery-backup circuit uses two lithium batteries. The RTC consists of the following major logic sections.

- Bus interface (8-bit latch)
- Control and status registers (four bytes)
- Clock, alarm, and calendar RAM (10 bytes)
- General purpose RAM (50 bytes) not dedicated to the RTC

- Internal time base and oscillator
- Programmable interrupts and square-wave generator
- Battery backup from expansion box

2.9.1 Overview

The RTC (Figure 2-18) functions under the control of a processor program in the ROM BIOS (basic input-output system).

2.9.1.1 Input/Output

The processor program communicates with the RTC using the 8-bit I/O (input/output) bus. The processor program sends control, status, address, and data signals to the RTC. The bus interface, which is an 8-bit latch on the RTC, receives addressing data from, and sends clock, alarm, and calendar data to the I/O bus. Since the RTC functions as an on-board I/O peripheral, local I/O 8-bit transfers occur at a 1125 ns rate. This bus cycle equals the 250 ns processor cycle with seven wait states added.

2.9.1.2 Address Map

The bus interface controls all inputs from the processor program to the RTC. Addresses from the processor program can select up to 64 bytes of RAM; however, 50 bytes are not dedicated to the RTC. Available memory on the RTC consists of 4 bytes for control and status registers A through D, and 10 RAM bytes for time, calendar, and alarm data. The processor program can write the address of the RAM, then read/write data indirectly to all bytes except registers C and D, which are read-only. Bit 7 of register A and the seconds register are read-only also. Bit 7 of the second byte always reads 0.

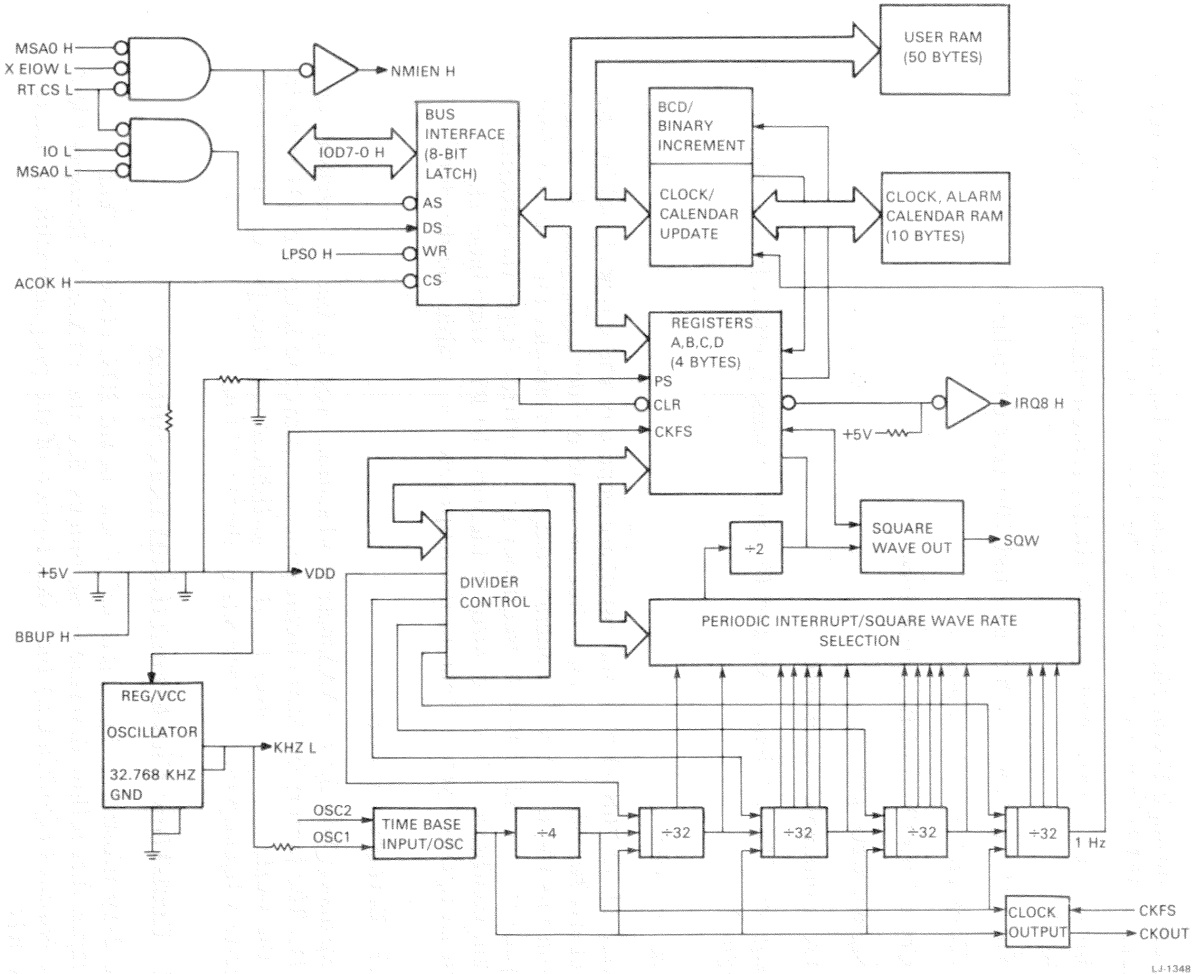


Figure 2-18 Real Time Clock and CMOS RAM Block Diagram

2.9.1.3 Control and Status

Registers A through D contain control and status bit information. These registers affect all RTC functions. Some of the functions include

- Binary or binary-coded-decimal (BCD) representation of date, time, and alarm
- Time of day clock with alarm and 100 year calendar
- Clock and calendar update
- Crystal oscillator-driven time base
- Square wave generator
- Programmable interrupts

Two signals, CLR L (clear low) and PS (power sense), affect bits in registers B through D.

2.9.1.4 Clocking

An external 32.768 KHz crystal oscillator generates the clock signal for the time of day functions by using a time base and divider tap logic. The time base outputs the oscillator frequency to a series of divider taps. As the time base presents the 32.768 KHz frequency to the divider taps, the processor program configures divider control to identify the RTC time base, start or inhibit an update cycle, select an interrupt rate, or disable the divider.

2.9.1.5 Battery Backup

The expansion box for the VAXmate workstation provides battery backup for the RTC. The battery-backup circuit generates power to keep the RTC running when the workstation's power is off. Two lithium batteries power the circuit. The battery-backup circuit connects to the +5 V line.

2.9.2 Real-Time Clock Functional Description

Figure 2-19 illustrates the functional blocks of the RTC circuitry. The paragraphs that follow describe these blocks. See the *VAXmate Technical Reference Manual* (Q6ZCS-GZ) for a description of the programmable registers on the RTC.

2.9.2.1 Power

The RTC receives power at pins VDD (+5 V) and VSS (ground). The following signals require a minimum input high voltage of 2.0 V.

- CE L = Chip-Enable
- DS = Data Strobe
- WR L = Write
- AS = Address Strobe
- AD7-0 = Address and Data bits 7 through 0
- PS = Power Sense

2.9.2.2 Bus Interface

The bus interface serves to latch the following control and status signals, except CE L, from the ROM BIOS into RAM.

1. The CE L signal controls all bus inputs to the RTC. When the power source supplies +5 V to the CPU module, CE L is asserted and remains asserted until the power source removes +5 V. The processor program can read/write the RTC as long as the CPU module is running on the +5 V supply.

   When the VAXmate workstation is powered-down, and the RTC functions by battery backup, CE L is deasserted. A pullup resistor holds CE L high.

2. The WR L signal indicates whether the current cycle is a write or read. When WR L and DS H are asserted, a write cycle occurs. When WR L is deasserted and DS H is asserted, a read cycle occurs.

3. The AS signal, when asserted, serves to demultiplex the bus. When the processor program writes to I/O port 0070H, it activates the AS signal. At the falling edge of AS, the bus interface latches the address.

4. The DS signal identifies the time period when the RTC drives the bus with read data. When the processor program writes to or reads from I/O port 0071H, it activates the DS signal.

5. The AD7-0 signals are multiplexed bidirectional address and data lines to the RTC. The I/O bus presents the address to the bus interface during the first portion of the bus cycle, and presents the data to the bus interface

during the second portion of the bus cycle. To address the RTC, the processor program loads the 8-bit latch with addresses at I/O port 0070H. It sends the read/write data through I/O port 0071H.

NOTE
The address latch is write only. The function of the address latch (I/O port 0070H) is to generate the nonmaskable interrupt enable high (NMIEN H) signal.

1. The processor program uses the PS signal to control the Valid RAM and Time (VRT) bit. The PS signal functions in the following ways with or without battery backup.

   a. If the VAXmate workstation has battery backup, the PS signal always stays high.

   b. If the VAXmate workstation does not have battery backup, the PS signal changes conditions. When the workstation is powered-up, it holds PS low externally for approximately 300 milliseconds. When PS is low, the VRT function is cleared. This indicates that the contents of the RAM, time registers, and calendar are not guaranteed. When the workstation commences normal operation, PS goes high.

2.9.2.3 Registers A through D

Registers A through D are 8-bit registers that the processor program can access during the update cycle. CLR L and PS are two inputs that affect the registers.

Register A is a read/write register, except for the update in progress function. Paragraph 2.9.1.4 describes this register.

Register B is a read/write register. It controls update cycles, and enables or disables periodic interrupt, alarm interrupt, update-ended interrupt, square wave, and daylight savings. It also indicates 12- or 24-hour mode.

Register C is a read-only register. It contains interrupt request, periodic interrupt, alarm interrupt, and update-ended interrupt flags. A hardware reset, or reading register C, clears the register. Writing to register B does not modify the register.

Register D is a read-only register. It controls the valid RAM and time (VRT) function, which indicates if the RTC lost power or remained stable. A hardware reset does not modify VRT.

NOTE
Refer to the *VAXmate Technical Reference Manual* (Q6ZCS-GZ) for a detailed description of registers A through D on the RTC.

2.9.2.4 Clock, Alarm, and Calendar RAM

The clock, alarm, and calendar RAM consists of ten bytes of data registers (Table 2-10). These registers are used to format the date and time in either binary or binary-coded-decimal (BCD) format.

Table 2-10 RTC Data Register Ranges

Latch Value	Register	Function	Binary Range	BCD Range
00H	Seconds	All modes	0 to 59	00H to 59H
01H	Seconds alarm	Specific time	0 to 59	00H to 59H
		Each second	192 to 255	C0H to FFH
02H	Minutes	All modes	0 to 59	00H to 59H
03H	Minutes alarm	Specific time	0 to 59	00H to 59H
		Each minute	192 to 255	C0H to FFH
04H	Hours	24-hour mode	0 to 23	00H to 23H
		12-hour mode, a.m.	1 to 12	01H to 12H
		12-hour mode, p.m.	129 to 140	81H to 92H
05H	Hours alarm	Specific time (24-hour mode)	0 to 23	00H to 23H
		Specific time (12-hour mode, a.m.)	1 to 12	01H to 12H
		Specific time (12-hour mode, p.m.)	129 to 140	81H to 92H
		Each hour (all modes)	192 to 255	C0H to FFH
06H	Day of Week		1 to 7	01H to 07H
07H	Day of month		1 to 31	01H to 31H
08H	Month		1 to 12	01H to 12H
09H	Year		0 to 99	00H to 99H

2.9.2.5 BCD/Binary Increment

All data registers must use the same format, either binary or BCD. If the data format is changed, the data registers must be initialized in the new format. Register B controls the format. The ROM BIOS uses the BCD format.

Register B also controls the range of the hour and hour alarm registers. Register C indicates the state of the alarm interrupt, which asserts IRQ L when the time registers match all the alarm registers. IRQ L is inverted and connected to IRQ8.

2.9.2.6 Clock/Calendar Update

Once per second, the RTC performs an update cycle. With a 32.768 KHz time base, the update cycle requires 1948 microseconds. During an update cycle, the data registers are disconnected from the external I/O bus. Therefore, while an update is in progress, attempts to read or write the data registers will produce invalid results.

2.9.2.7 Internal Time Base and Oscillator

An external 32.768 KHz crystal oscillator generates the clock signal for the time of day functions. The oscillator output connects to Oscillator Clock 1 (OSC1) at the time base input. OSC2 is not connected.

The time base shapes OSC1 into a stream of evenly spaced clock pulses vibrating at a 32.768 KHz frequency. The time base outputs the frequency to the clock output, and to a series of divider taps. The Clock Output (CKOUT) signal is not connected. The Clock Frequency Select (CKFS) pin is tied to +5 Vdc, but is not used.

As the time base presents the 32.768 KHz frequency to the divider taps, the processor program configures divider control to perform the following tasks.

1. Start an update cycle by outputting a 1 Hz signal to the clock/calendar update logic, or inhibit the update cycle.
2. Identify the time base to use. The RTC time base is 32.768 KHz.
3. Select an interrupt rate or disable the divider. If the registers enable an interrupt, the divider's output interrupt request low (IRQ L) is inverted to produce IRQ8, which goes to the interrupt circuit.

2.9.2.8 Divider Control

Register A controls the divider control function. Divider control has four uses.

1. Start an update cycle by outputting a 1 Hz signal to the clock/calendar update logic, or inhibit the update cycle. The divider control holds the divider chain in the reset state during the update cycle. One second after removing the divider reset, the first update cycle begins.
2. Identify the time base to use. The RTC time base is 32.768 KHz.
3. Select an interrupt rate or disable the divider. If the registers enable an interrupt, the dividers output interrupt request low (IRQ L) is inverted to produce IRQ8, which goes to the interrupt circuit.
4. Test the RTC.

2.9.2.9 Square-Wave Output Selection

The square-wave (SQW) output signal is not connected.

2.9.2.10 Interrupt Selection

The RTC can send three interrupts to the interrupt logic: alarm interrupt, periodic interrupt, and update-ended interrupt. The alarm interrupt can occur at rates from once-per-second to once-per-day. The periodic interrupt may be selected for rates from 1/2 s to 3.90625 ms. The update-ended interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupt, if any, it wishes to receive. Register B enables the three interrupts. The output IRQ L is inverted to produce IRQ8 H (interrupt request 8 high), which goes to the interrupt circuit. Register B also disables the interrupts.

If an interrupt flag is already set when the interrupt becomes enabled, IRQ is activated immediately, though the interrupt initiating the event may have occurred much earlier.

When an interrupt event occurs, a flag is set in register A. Each of the three interrupt sources have a separate flag in register A. These flags are set, regardless of the state of the corresponding enable function in register B. The flag may be used with or without enabling the corresponding enable function.

2.10 Three-Channel Programmable Counter/timer

The VAXmate CPU module uses an 8254 programmable counter/timer (Figure 2-19), resident on a 24-pin chip, to provide three independent 16-bit counters for system counting or timing tasks.

2.10.1 Overview

Counters 0, 1, and 2 function independently, but operate in the same manner. They operate from the same crystal oscillator, but each counter has its own internal clock. Each counter is programmable by using the control and address lines that go to the read/write logic, and the data lines that go to the data bus buffer. The read/write logic connects to the system address bus, and the data bus buffer connects to the I/O data bus. Both buses are on the CPU module. The output of each counter is used by the ROM Basis Input/Output System (ROM-BIOS) in the following way.

1. Counter 0 is a general purpose timer that provides a constant time base on the CPU module. Counter 0 outputs an interrupt that goes directly to the IRQ0 (interrupt 0) input line of the interrupt logic.
2. Counter 1 is programmed to provide the dynamic RAM refresh to the bus arbitrator on the CPU module. The counter is programmed for 15 microseconds; then the CPU board does an additional divide by 2 to provide a refresh every 30 microseconds.
3. Counter 2 generates periodic waveforms used for programming a pulse train, a square wave, or a modulated waveform to the speaker interface.

2.10.2. Functional Description

The three-channel counter/timer operates using the circuitry in the functional blocks in Figure 2-20. The functional blocks consist of the read/write logic, the Control Word (CW) register, the data bus buffer, and counters 0, 1, and 2. The programmable registers on the three-channel counter/timer are defined in the *VAXmate Technical Reference Manual* (Q6ZCS-GZ).

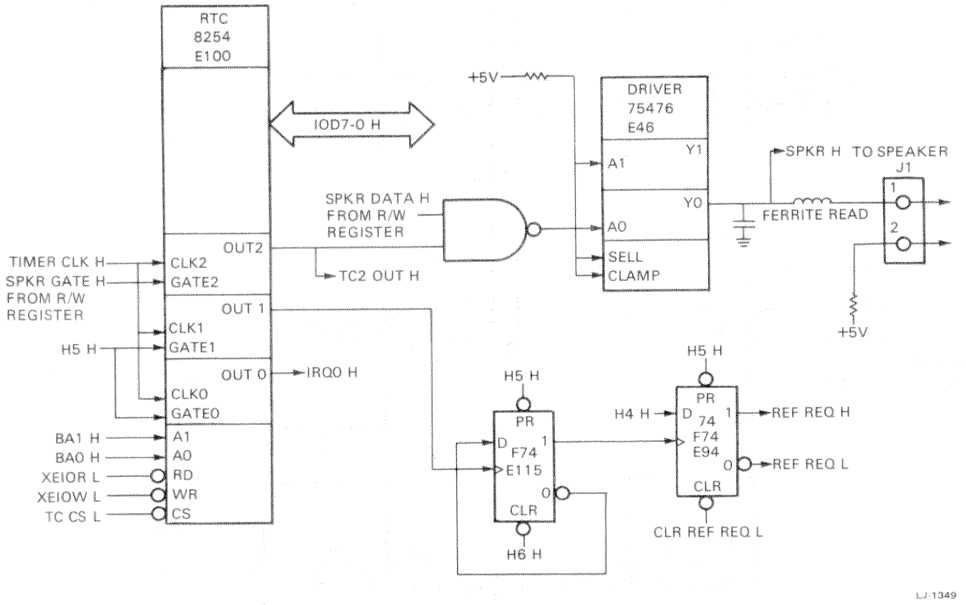


Figure 2-19 Counter/Timer and Speaker Interface Block Diagram

2.10.2.1. Read/Write Logic

The read/write logic accepts address and control signals from the system bus, and generates the same signals for the CW register and each counter. The value on input address lines A1 and A0 determines whether a read/write operation will be performed on one of the three counters, or on the CW register. Table 2-11 lists the address of counters 0, 1, and 2, and the read-back command word. When Read (RD L) is asserted, the 80286 CPU reads one of the counters. When Write (WR L) is asserted, the 80286 CPU writes either a control word to the CW register, or an initial count to one of the counters. Both RD L and WR L are qualified by counter select (CS L). They are selected only by holding CS L low.

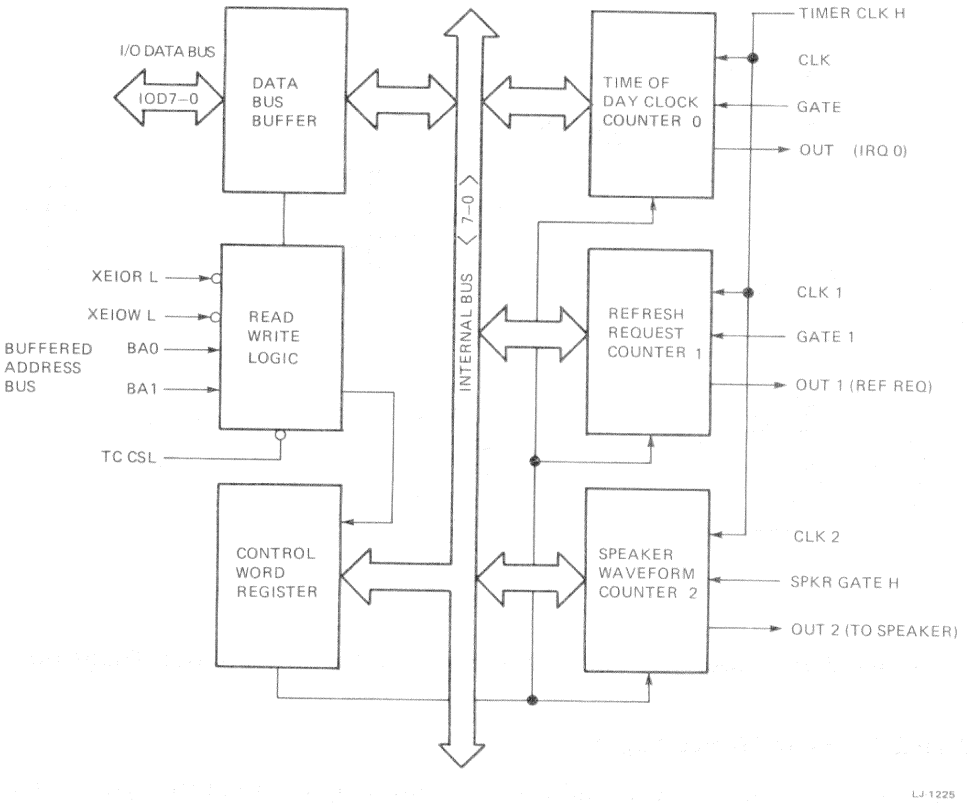


Figure 2-20 Three-Channel Counter/Timer Block Diagram

Table 2-11 Command Word Addresses

Register	Address
Counter 0	0040H
Counter 1	0041H
Counter 2	0042H
Command Word	0043H

2.10.2.2. Control Word (CW) Register and Data Bus Buffer

The CW register is selected by the read/write logic when A1:A0=11. When the read/write logic receives a binary 11, the data from lines IOD7-0 in the data bus buffer goes to the CW register over the internal bus. This data defines the operation of the CW register and each counter. The *VAXmate Technical Reference Manual* (Q6ZCS-GZ) provides a detailed description of the CW register. The CW register is a write-only register. The CPU can read the status of the CW register and each counter by using the read-back command.

2.10.2.3. Counters 0, 1, and 2

The paragraphs that follow will describe only the operation of a single counter (Figure 2-21), because counters 0, 1, and 2 function identically and independently. The counter has control logic, a status register, a status latch, two 8-bit input latches/count registers (CRm and CRl), a counting element (CE), and two 8-bit output latches (OLm and OLl). The m and l following the latch abbreviation stand for most significant byte and least significant byte respectively. The CW register in Figure 2-21 is not part of counter 0, 1, or 2, but its contents determine how the counter operates.

Output Latch (OLm and OLl) – A program can read the value of a counter without disturbing the count in progress. While a count is in progress, the OL (functioning as a unit) follows the CE. Whenever the CPU wants to read the counter, it can use three possible methods. One method is to send a counter latch command to the three-channel counter/timer. The command is received by the CW register and sent to the selected counter. The counter's OL latches the present count until it is read by the CPU, at which time it returns to its position following the CE. Only one latch at a time is enabled by the control logic to drive the internal bus. After OLm and OLl are read, the output of a 16-bit counter (two 8-bit latches) is sent over the 8-bit internal bus. It is important to note that the CPU reads the OLl, not the CE.

Count Register (CRm and CRl) – When the CPU wants to write to the counter, it uses two 8-bit count registers (CRm and CRl). When the CPU writes a new count to the counter, the count is stored in the CR, and later transferred to the CE. The control logic allows one CR at a time to be loaded from the internal bus. In the process, both bytes from CRm and CRl are transferred to the CE simultaneously. When the counter is programmed, CRm and CRl are cleared. If the counter has been programmed for one byte counts (either the most significant byte or the least significant byte), the other byte will be zero. It is important to note that the CPU cannot write into the CE. The CPU writes the count into the CR.

CLK, Gate, and Out Signals – The CLK, Gate, and Out signals are all connected to control logic on the CPU module. The CLK pulse sent to all counters comes from a 14.318 MHz oscillator that is divided by 12 to provide a 1.1931816 MHz CLK pulse. A high level at the Gate input enables counting, and a low level at the Gate input disables counting. Software controls the Gate input for Counter 2 (SPKR GATE H) through the CPU system status register. The Out signal is dependent upon the mode of operation of the three-channel counter/timer and its hardware connection.

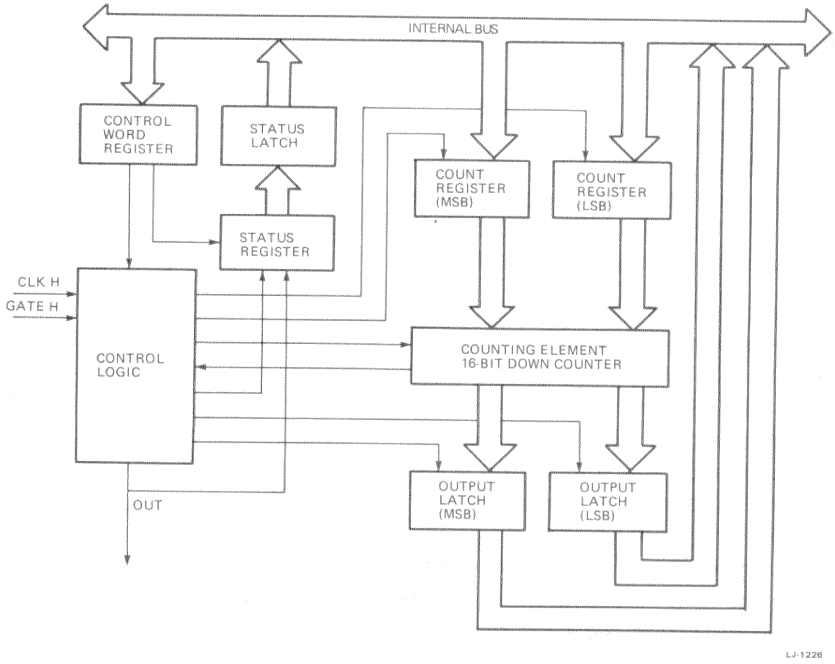


Figure 2-21 Counter Block Diagram

2.10.3 Mode Definitions

The paragraphs that follow provide a brief description of the six modes in which the three-channel counter/timer operates. The *VAXmate Technical Reference Manual* (Q6ZCS-GZ) provides a detailed description of the following modes.

- Mode 0 Interrupt on terminal count (not used)
- Mode 1 Hardware retriggerable one-shot (not used)
- Mode 2 Rate generator
- Mode 3 Square wave mode
- Mode 4 Software triggered strobe
- Mode 5 Hardware triggered strobe (retriggerable)

Table 2-12 lists the default mode and function of each counter in the VAXmate workstation (as established by the ROM BIOS).

Table 2-12 Operating Modes: Counters 0, 1 and 2

Counter	Function	Mode	Description	Output
0	Time of Day Clock	2	Rate generator	IRQ0
1	Refresh timing	2	Rate generator	Refresh counter
2	Speaker waveform	3	Square wave	Speaker driver

2.10.3.1 Mode 0 (Interrupt on Terminal Count)

Since mode 0 is used for one-shot event timing, it is not normally used on the VAXmate workstation.

2.10.3.2 Mode 1 (Hardware Retriggerable One-Shot)

Since mode 1 is used for one-shot event timing, it is not normally used on the VAXmate workstation. Mode 1 could be used for sound generation, but it is not normally used on the VAXmate workstation.

2.10.3.3 Mode 2 (Rate Generator)

Counter 1 uses mode 2 to provide the refresh timing signal.

2.10.3.4 Mode 3 (Square Wave)

Mode 3 generates a square wave at the OUT signal.

2.10.3.5 Mode 4 (Software Triggered Strobe)

Mode 4 provides a decremented count of n clock cycles. In mode 4, writing a new count to the counter triggers a count cycle.

2.10.3.6 Mode 5 (Hardware Triggered Strobe)

Counter 2 uses mode 5 to provide a decremented count of n clock cycles. In mode 5, the Gate input triggers another count cycle.

2.11 Mouse Information

The VAXmate workstation mouse is a hand-held, high performance pointing device that provides X-Y coordinate output data to the VAXmate CPU for controlling the cursor on the workstation display screen. You can move the mouse unit around on any suitable flat surface to direct the cursor (arrow) movements on the screen. The mouse has three switches to select functions or items from a menu on the screen (Figure 2-22).

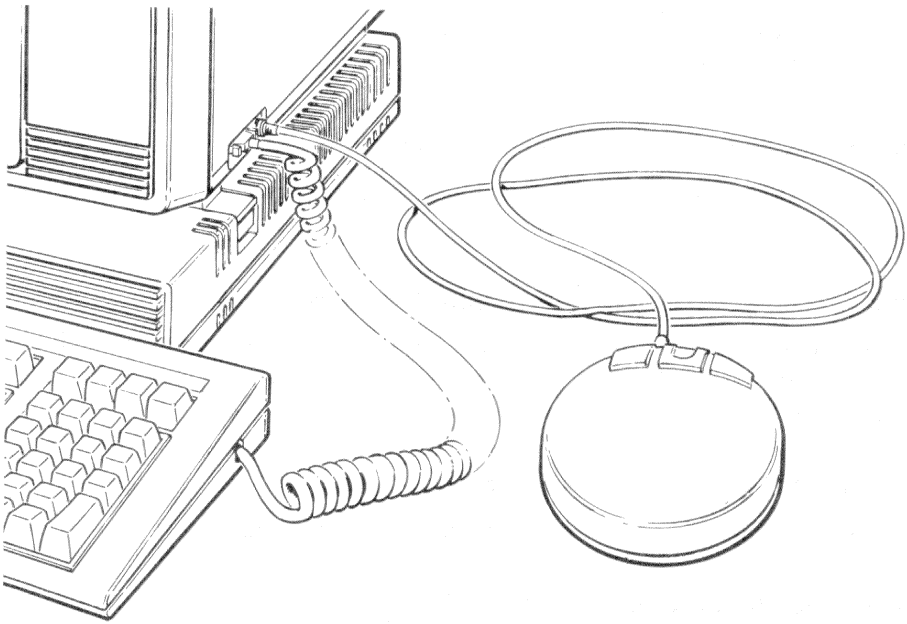


Figure 2-22 VAXmate Workstation Mouse

2.11.1 Operation

The mouse uses optical-mechanical technology to detect movement created by a rubber coated ball extending from the bottom of the mouse enclosure. A pair of plastic wheels resting on the surface of the ball, transmit the ball movement through shafts to a pair of slotted disks. Adjacent to these disks are optical sensors that read the light pulses created by the slots in the rotating disks (Figure 2-23).

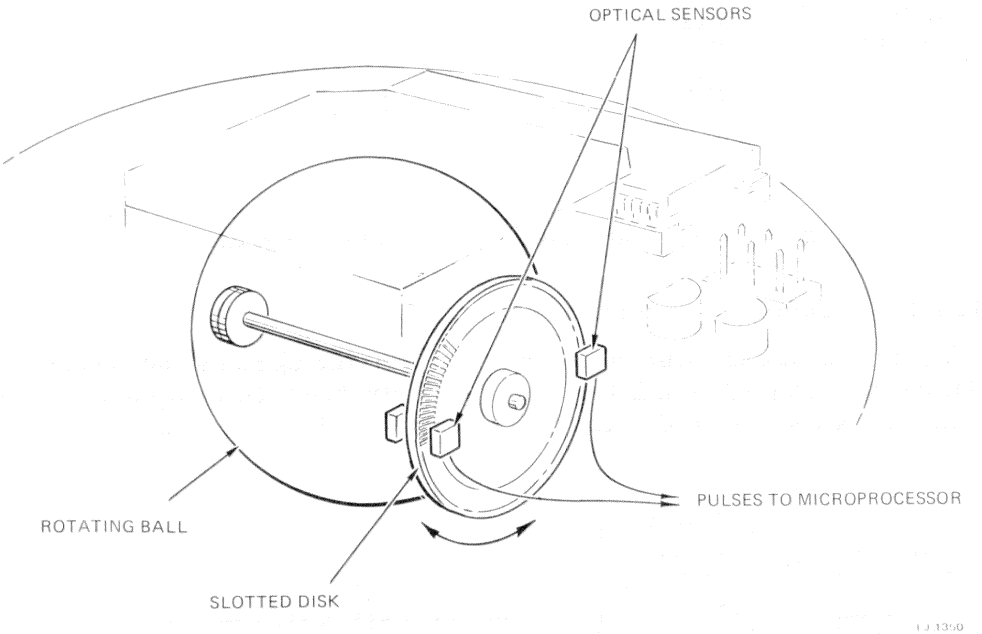


Figure 2-23 Mouse Movement Detector Mechanics

This information is relayed as X-Y pulses to a microprocessor located on the mouse module. The microprocessor converts the X-Y pulses into relative X-Y coordinates, and transmits these coordinates as serial data to the data controller logic on the CPU module (Figure 2-24).

As the mouse moves, the cursor on the screen moves in the corresponding direction: right when the mouse moves to the right; left when the mouse moves to the left; up when the mouse moves away from the operator; and down when it moves toward the operator. Picking up the mouse to reposition it has no effect on the cursor.

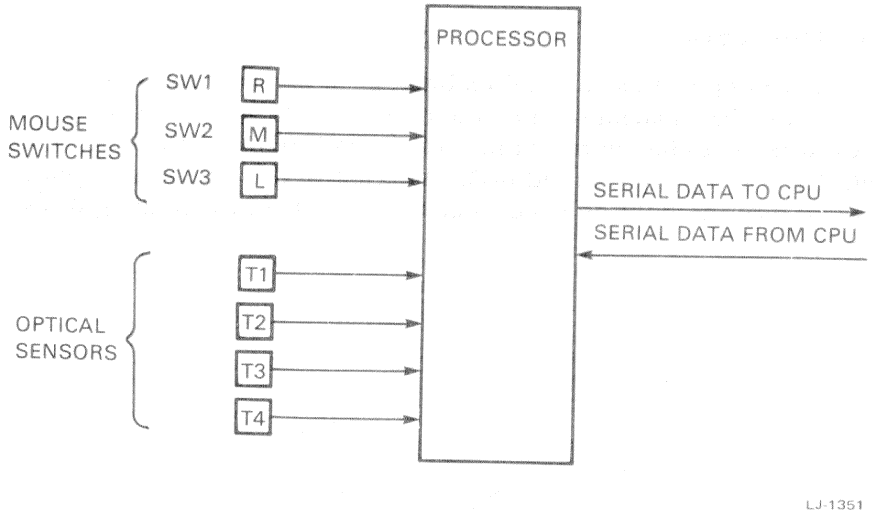


Figure 2-24 Mouse Module Functional Diagram

2.11.1.1 Communication Interface

The workstation mouse communicates with the CPU through an asynchronous serial interface chip (24-pin DIP SCN2661) at 4800 baud. This chip is a synchronous/asynchronous data communications controller (Figure 2-25).

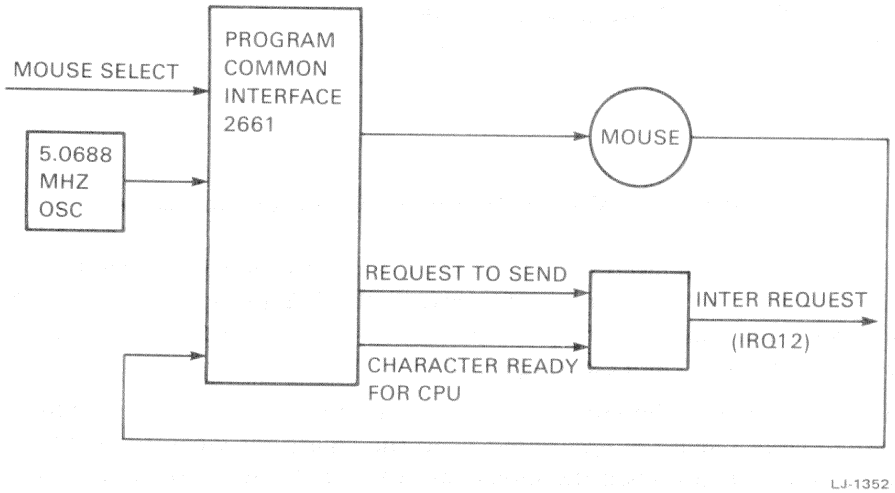


Figure 2-25 Mouse Controller Logic – Functional Block Diagram

Control words supplied by the VAXmate CPU program the 2661 chip. These control words specify asynchronous mode, baud rate, and the number of bits per character. The receiver portion of the 2661 performs serial to parallel conversion of data received from the mouse (MS RX DATA, PC500 CPU 286, sheet 10). The 2661 transmitter circuit converts CPU parallel data to serial data (MS RX DATA), which is then sent to the mouse.

The mouse supports half-duplex communication. If the mouse is transmitting and receives a byte of data, the mouse aborts the data being transmitted, and immediately processes the new command. If the mouse receives a byte between the characters of a multibyte report, the mouse is still considered to be transmitting and will abort the report.

2.11.1.2 Data Format

The mouse microprocessor converts the mouse movement into position reports, and sends the reports to the data controller. Data is transferred in a 9-bit byte format: 8 data bits and 1 parity bit. The mouse transmits odd parity but ignores parity errors when they are received. The mouse transmits a 3-byte position report as shown in the following section. A start bit and a stop bit frame each byte (Figure 2-26). The selected format determines the parity and the number of bits per byte.

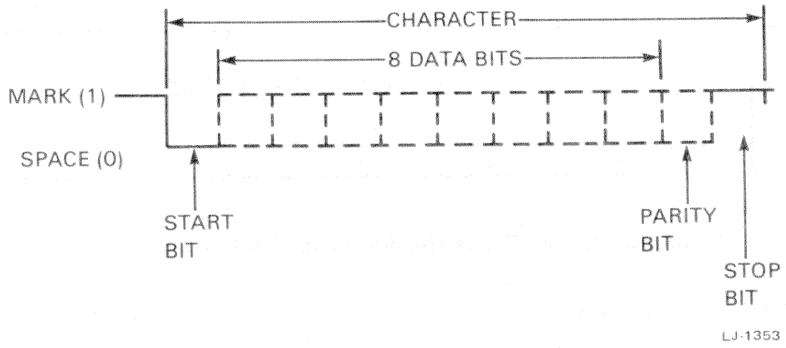


Figure 2-26 Mouse Transmit and Receive Character Format

2.11.1.3 Position Reports

The X and Y values in the mouse position report give the movement in units of resolution since the last report.

Position Report - Byte 1

7	6	5	4	3	2	1	0
1	0	0	SIGN-X	SIGN-Y	LEFT BUTTON	MIDDLE BUTTON	RIGHT BUTTON

SX,SY — Sign bit
1 = positive
0 = negative

L,M,R — Left, middle, right button position
1 = button depressed

Position Report - Byte 2

7	6	5	4	3	2	1	0
0	X-AXIS DISPLACEMENT						

X6-X0 — X displacement, X0 is the least significant bit

Position Report - Byte 3

7	6	5	4	3	2	1	0
0	Y-AXIS DISPLACEMENT						

Y6-Y0 — Y displacement, Y0 is the least significant bit

2.11.2 Operating Modes

There are two mouse operating modes that determine when, and how often, the mouse transmits a position report. They are prompt mode and incremental mode. In prompt mode, which is the power-up default, the mouse generates a report in response to a Request Mouse Position command. In incremental stream mode, the mouse generates a report whenever it is moved. It also reports a change in button position since the last report. When the mouse is motionless, and no buttons have been changed, it generates no report.

2.11.2.1 Mouse Commands

Table 2-13 lists the mouse commands. The listed modes are selected by sending the appropriate ASCII (or HEX) command code. A brief description of the three commands not previously described follows the table.

Table 2-13 Mouse Command Summary

ASCII	HEX	Function
D	44	Select Prompt Mode
R	52	Select Incremental Stream Mode
P	50	Request Mouse Position
T	54	Invoke Self Test
Zx	5A xx	Vendor Reserved function

Request Mouse Position – After the command is issued, the mouse responds with a position report. This command also switches the mouse to Prompt mode if it has not been selected.

Self Test and Identify – Self test leaves the mouse in the reset or power-up state. When a self-test command has been issued, data sent to the mouse is invalid until the last byte of the self test report has been received. The mouse ignores any data received during self test. (See the section on Power-up Self Test and Identification that follows.)

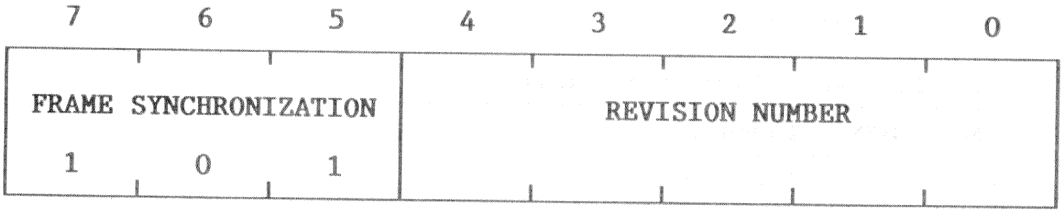
Vendor Reserved Commands – This command byte, followed by any single printable character, allows vendors to add special mouse functions for their own testing or quality control. The manufacturer determines these functions,

which may include transmitting specialized reports. These commands may not include new modes. The mouse must be restored to its previous state when any of these commands is completed.

2.11.2.2 Power-Up Self Test and Identification

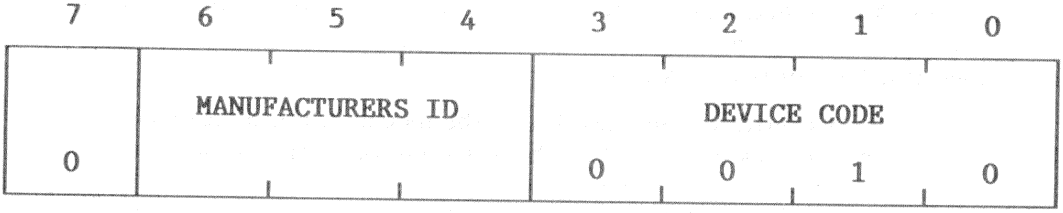
The mouse automatically checks its internal logic and circuits upon mouse power-up, or upon command from the CPU. The mouse then transmits a 4-byte self-test report, consisting of a 2-byte identification code and a 2-byte status code, which describes the condition of the circuitry and firmware. The 4-byte self-test report is transmitted as follows.

Self-Test Report - Byte 1



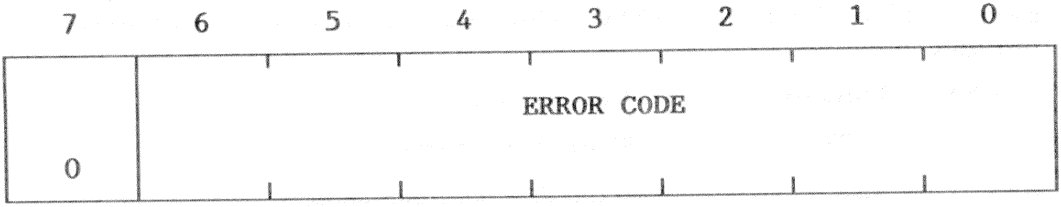
7-5	Frame synchronization. 101 indicates the start of a self-test report.
R3-R0	Revision number (zero for initial release).

Self-Test Report - Byte 2



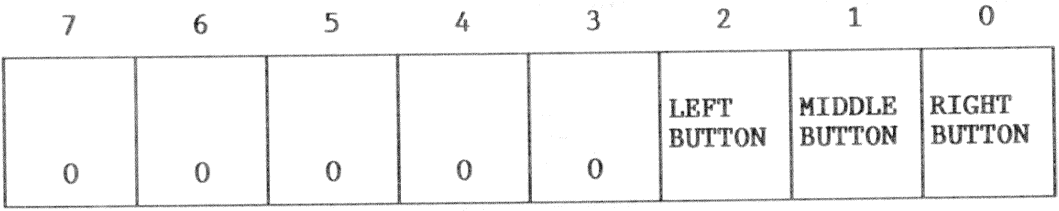
M2-M0	Manufacturer's ID
3-0	Device code (0010 indicates mouse data)

Self-Test Report - Byte 3



E6-E0 Error code, 0 = OK
Error code ASCII ">" (3E HEX), indicates RAM or ROM checksum error.
No checksum error, ASCII "=" (3D HEX), indicates a button error.

Self-Test Report - Byte 4



L,M,R Button code, 0 = OK. Indicates which buttons are down, or have failed.

2.11.3 Mouse Connectors

There are two connectors associated with the VAXmate mouse: the VAXmate connector and the module connector. The VAXmate connector plugs into the VAXmate workstation, and the module connector plugs into the mouse module (internally).

2.11.3.1 VAXmate Connector

The VAXmate plug is a 7-pin micro-DIN style connector (male type). The pin assignments and functions are shown below. The connector layout is illustrated in Figure 2-27.

Pin No.	Function	Description
1	GND	Signal and power return
2	TXD	Serial data out from mouse
3	RXD	Serial data to mouse
4	−12 V	−12 V for RS-232 operation
5	+5 V	+5 V
6	+12 V	+12 V for tablet
7	NC	No connection
SHELL	GND	Ground

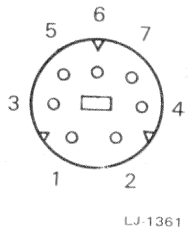


Figure 2-27 7-Pin DIN Connector Layout

2.11.3.2 Module Connector

A 6-pin connector attaches the mouse cable to the mouse module. The mouse enclosure must be disassembled in order to access the connection. Remove the four screws from the bottom of the mouse enclosure. Place the mouse in the normal operating position and lift the top cover off. The number 1, located on the circuit board, is a reference designator for the number 1 on the connector. The cable and connector can now be easily removed from the module. The pin assignments and layout are described as follows, and are illustrated in Figure 2-28.

Pin No.	Function	Description
1	TXD	Serial data to CPU mouse controller
2	RXD	Serial data from CPU to mouse
3	+5 V	+5 V
4	GND/−12 V	GND for TTL mode, −12 V for RS-232 operation
5	SHIELD	
6	GND	Ground

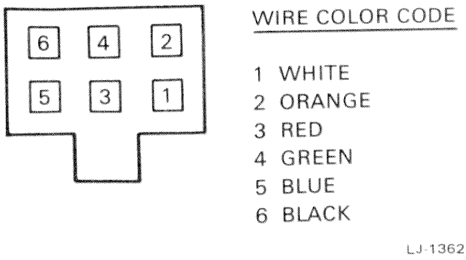


Figure 2-28 Mouse Module Connector – Pin Assignments

Chapter 3
VAXmate
I/O-Video Module

3.1 Introduction

The VAXmate input/output-video (I/O-Video) module (Figure 3-1) is a single printed circuit board that provides the following system functions.

- Video display controller
- Network interface
- Asynchronous serial printer port interface
- Asynchronous serial communications port interface
- Diskette drive controller
- 8-bit option interconnect

This chapter describes the common logic, the connectors, and all I/O-Video module system functions except the video display controller (Chapter 4) and the diskette drive controller (Chapter 5).

All subsystems on the I/O-Video module, except the 8-bit option interconnect, share the common logic section. The common logic selects the microperipherals addressed by the CPU, and controls address/data transfers to or from the microperipherals through the CPU bus interconnect.

The network interface, which connects to ThinWire Ethernet, operates at 10 megabits per second using collision sense multiple access/collision detection (CSMA/CD) network technology. The interface is compatible with IEEE STD, 802.3 (10 Base 2), and conforms to the Digital Ethernet Specification, Digital STD 134. The interface uses a BNC-type connector to connect to the ThinWire coaxial cable.

The serial printer port is an asynchronous, RS-423 electrically compatible interface. The port supports two modem control signals: Data Terminal Ready (DTR) and Data Set Ready (DSR). The serial printer port complies with the Local Direct Connection (no modem) for Serial Asynchronous Terminals and System Interfaces (Digital STD 052-4). A 6-pin modified modular jack (MMJ) connector and a 17-00721 cable connect the port to a serial printer. An MMJ to DB-25 passive adapter connect the port to standard DB-25 serial printer connectors.

The serial communications port is an asynchronous, RS-232-C functionally compatible and RS-423 electrically compatible interface. The port supports full modem control signals and is register compatible with industry-standard applications. The serial communications port complies with Local Direct Connection (No Modem) for Serial Asynchronous Terminals and System Interfaces (Digital STD 052-4). A DB-25P connector connects the port to a serial communications device. The connector is defined as Data Terminal Equipment (DTE).

The diskette drive controller supports one or two diskette drives. The controller uses a 5-1/4 inch high-capacity (1.2 Mbyte) disk drive. It supports 250 Kbyte per second or 500 Kbyte per second data rates. The diskette controller can read standard capacity diskettes, and is register compatible with industry-standard applications.

The 8-bit option connector connects directly to the CPU bus interconnect. A hardware option such as an integral modem can be installed at this connector. The interface is electrically and functionally compatible, but is mechanically incompatible with the industry-standard 8-bit bus.

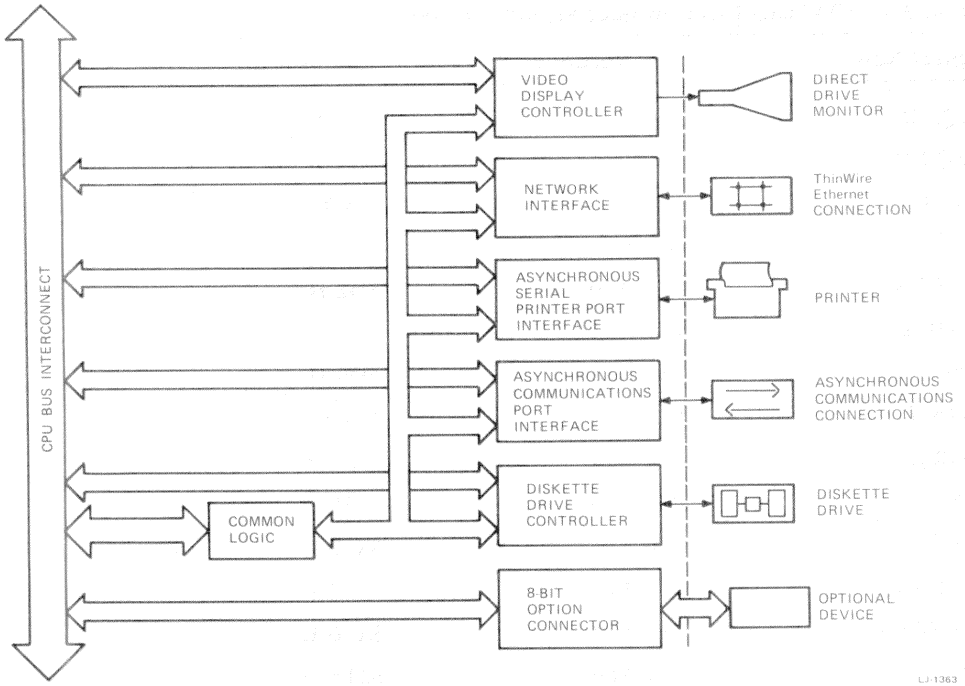


Figure 3-1 I/O-Video Module Block Diagram

3.2 CPU BUS Interconnect

A 120-pin card-edge connector on the I/O-Video module is the interconnection between the system functions on the I/O-Video module, and the processing functions on the CPU module. Table 3-1 defines the CPU bus interconnect signals.

Table 3-1 CPU Bus Interconnect Signals

Signal Name	Pin Number	Signal Name
−12 Vdc	B1 A1	−12 Vdc
+12 Vdc	B2 A2	+12 Vdc
+5 Vdc	B3 A3	+5 Vdc
I/O CHK L	B4 A4	SD7 H
RESET H	B5 A5	SD6 H

Table 3-1 CPU Bus Interconnect Signals *(cont.)*

Signal Name	Pin Number	Signal Name
IRQ9 H	B6 A6	SD5 H
DRQ2 H	B7 A7	SD4 H
0WS L	B8 A8	GND
GND	B9 A9	SD3 H
MEMW L	B10 A10	SD2 H
MEMR L	B11 A11	SD1 H
GND	B12 A12	SD0 H
EIOW L	B13 A13	GND
EIOR L	B14 A14	AEN H
IOW L	B15 A15	SA19 H
IOR L	B16 A16	SA18 H
DACK3 L	B17 A17	SA17 H
I/O RDY H	B18 A18	SA16 H
DRQ3 H	B19 A19	SA15 H
GND	B20 A20	SA14 H
DACK1 L	B21 A21	SA13 H
DRQ1 H	B22 A22	SA12 H
REFRESH L	B23 A23	SA11 H
GND	B24 A24	SA10 H
CLOCK H	B25 A25	GND
GND	B26 A26	SA9 H
IRQ7 H	B27 A27	SA8 H
IRQ6 H	B28 A28	SA7 H
IRQ5 H	B29 A29	SA6 H
IRQ4 H	B30 A30	SA5 H
IRQ3 H	B31 A31	GND
DACK2 L	B32 A32	SA4 H
T/C H	B33 A33	SA3 H
ALE H	B34 A34	SA2 H

Table 3-1 CPU Bus Interconnect Signals *(cont.)*

Signal Name	Pin Number	Signal Name
GND	B35 A35	SA1 H
LPS0 L	B36 A36	GND
GND	B37 A37	SA0 H
+5 Vdc	B38 A38	+5 Vdc
VMEM16 L	B39 A39	SBHE L
I/O 16 L	B40 A40	UA23 H
IRQ10 H	B41 A41	UA22 H
IRQ11 H	B42 A42	UA21 H
GND	B43 A43	UA20 H
IRQ12 H	B44 A44	UA19 H
IRQ15 H	B45 A45	UA18 H
IRQ14 H	B46 A46	UA17
DACH0 L	B47 A47	IRQ8 H
DRQ0 H	B48 A48	GND
GND	B49 A49	EMEMR L
LANACK L	B50 A50	EMEMW L
LANREQ L	B51 A51	GND
GND	B52 A52	SD08 H
−9 Vdc	B53 A53	SD09 H
GND	B54 A54	SD10 H
−9 VRET	B55 A55	SD11 H
GND	B56 A56	SD12 H
I/O ENAB L	B57 A57	SD13 H
MASTER L	B58 A58	SD14 H
GND	B59 A59	SD15 H
+5 Vdc	B60 A60	+5 Vdc

3.3 8-Bit Option Interconnect

A 64-pin header connector on the I/O-Video module is the interconnection between an 8-bit option device, and the processing functions on the CPU module. Table 3-2 defines the 8-bit option interconnect signals.

Table 3-2 8-Bit Option Interconnect Signals

Signal Name	Pin Number	Signal Name
GND	B1 A1	I/O CHK L
RESET H	B2 A2	SD7 H
+5 Vdc	B3 A3	SD6 H
IRQ9 H	B4 A4	SD5 H
GND	B5 A5	SD4 H
DRQ2 H	B6 A6	SD3 H
GND	B7 A7	SD2 H
OWS L	B8 A8	SD1 H
GND	B9 A9	SD0 H
GND	B10 A10	I/O RDY H
MEMW L	B11 A11	AEN H
MEMR L	B12 A12	SA19 H
EIOW L	B13 A13	SA18 H
EIOR L	B14 A14	SA17 H
DACK3 L	B15 A15	SA16 H
DRQ3 H	B16 A16	SA15 H
DACK1 L	B17 A17	SA14 H
DRQ1 H	B18 A18	SA13 H
REFRESH L	B19 A19	SA12 H
CLOCK H	B20 A20	SA11 H
IRQ7 H	B21 A21	SA10 H
IRQ6 H	B22 A22	SA9 H
IRQ5 H	B23 A23	SA8 H
IRQ4 H	B24 A24	SA7 H

Table 3-2 8-Bit Option Interconnect Signals *(cont.)*

Signal Name	Pin Number	Signal Name
IRQ3 H	B25 A25	SA6 H
DACK2 L	B26 A26	SA5 H
T/C H	B27 A27	SA4 H
ALE H	B28 A28	SA3 H
+5 Vdc	B29 A29	SA2 H
RESERVED	B30 A30	SA1 H
GND	B31 A31	SA0 H
−12 Vdc	B32 A32	+12 Vdc

3.4 Common Logic

The Common Logic (Figure 3-2) consists of the following circuits.

- Local Address/Data (LAD) bus transceiver
- Partial address bus buffer
- I/O address decoder
- Local Address/Data bus (LAD) transceiver control
- Delayed IORD/IOWR generator

The circuits that make up the common logic interface to the CPU and the microperipherals use the following buses.

- System Data (SD15:0 H) bus
- Local Address/Data (LAD15:8 H and LAD7:0 H) bus
- System Address (SA15:0 H) bus
- Buffered Address (BA15, 14, 12, and 4:0 H) bus

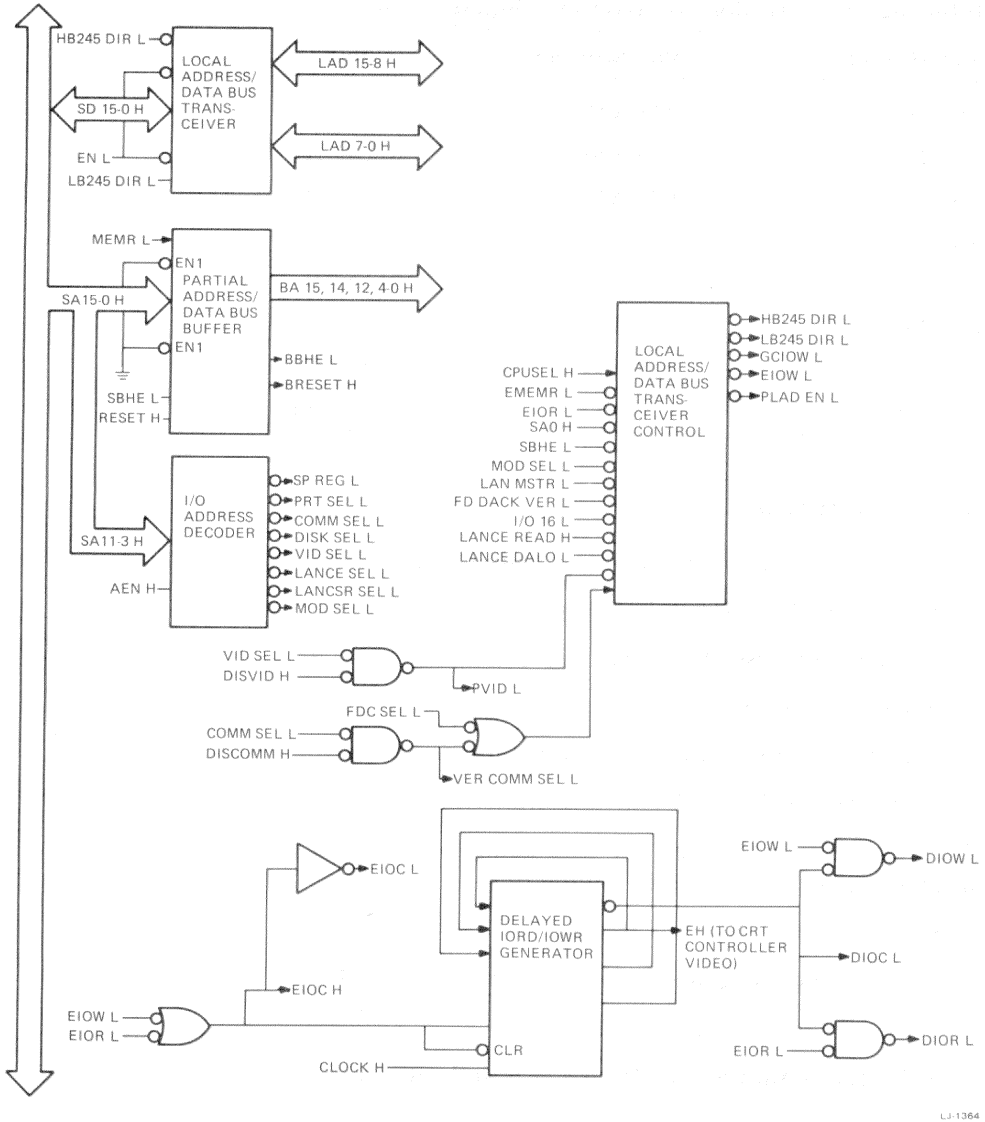


Figure 3-2 Common Logic Block Diagram

3.4.1 Overview

All the microperipherals on the I/O-Video module share the common logic circuits. They rely on the outputs of the common logic to decode addresses and provide chip selects, data transmission control signals, and compatible timing. The LAD bus transceiver controls the two-way transfer of information between the 16-bit SD bus and the 16-bit LAD bus.

The SD bus is bidirectional, and supports both word and byte transfers. SD15 is the most significant bit (MSB), and SD0 is the least significant bit (LSB). The bus signals are active high. The LAD bus is bidirectional. LAD15:8 is the high byte and LAD7:0 is the low byte. LAD15 is the MSB and LAD0 is the LSB.

The microperipherals on the I/O-Video module, which are NMOS LSI devices, use the LAD bus to communicate with the SD bus. The LAD bus transceiver control logic generates the signals that control the enabling and direction of the LAD bus transceiver. The partial address bus buffer and the I/O address decoder connect to the system address bus (SA15-0). The partial address bus buffer drives a local address bus to provide buffered address lines for the microperipherals. The I/O address decoder logic provides the chip selects for the microperipherals. The delayed IORD/IOWR generator creates delayed control signals, to make the 80286 CPU timing compatible with slower microperipherals on the I/O-Video module. This enables the VAXmate workstation to operate all industry-standard applications.

3.4.2 Local Address/Data Bus Transceiver

The LAD bus transceiver consists of two 74LS245 3-state octal bus transceivers. The two transceivers combined (Figure 3-2) contain 16 3-state drivers that provide two-way communication between the system data (SD) bus and the LAD bus. The drivers are connected to 16 data lines from the SD bus, and 16 data lines from the LAD bus.

The signals LB245 DIR and HB245 DIR (Low Byte 245 DIRection and High Byte 245 DIRection) control the direction of data transmission using the 74LS245 octal bus transceivers. LB245 DIR, HB245 DIR, and LAD EN L (local address/data enable low) come from the LAD bus transceiver control circuit. When LAD EN L is asserted, the high byte and low byte from each transceiver are transferred simultaneously between the two buses. When LB245 DIR L and HB245 DIR L are asserted, both bytes are transferred from the LAD bus to the SD bus. When LB245 DIR L and HB245 DIR L are deasserted, both bytes are transferred from the SD bus to the LAD bus.

Table 3-3 defines the LAD bus transceiver inputs and outputs.

Table 3-3 Address/Data Bus Transceiver Signals

Signal Name	Definition
LAD EN L	Local Address/Data Bus Enable
HB245 DIR L	High Byte 245 Direction
LB245 DIR L	Low Byte 245 Direction
SD15 H to SD08 H	System Data
SD7 H to SD 0 H	System Data
LAD15 H to LAD08 H, LAD7 H to LAD0 H	Local Address/Data

3.4.3 Partial Address Bus Buffer

The partial address bus buffer consists of two 74LS244 octal drivers. The two chips combined (Figure 3-2) contain eight 3-state drivers that provide one-way transmission from the SA bus to the buffered address bus. The inputs to the drivers are eight address lines from the SA bus (SA15 H, 14 H, 12 H, and 4 H to 0 H). The outputs from the drivers are eight address lines to the BA bus (BA15 H, 14 H, 12 H, and 4 H to 0 H). Pins EN1 and EN2 (Enable 1 and 2) are always asserted.

When the CPU asserts the Memory Read (MEMR L) signal, the microperipheral that is accessed will move its data onto the LAD bus. MEMR L is active only for the first megabyte of address space.

The CPU asserts the Reset (RESET H) signal to initialize all circuits during the power on or power down sequence.

The buffer uses the System Bus High Enable (SBHE L) and SA0 signals together, to select the proper bytes of the SD bus word when reading or writing to memory. SHBE L may be driven by a bus master.

Table 3-4 defines the partial address/data bus buffer inputs and outputs.

Table 3-4 Partial Address/Data Bus Buffer Signals

Signal Name	Definition
RESET H	Reset
SBHE L	System Byte High Enable
SA15, 14, 12, 4-0 H	System Address
BRESET H	Buffered Reset
BBHE L	Buffered Byte High Enable
BA15, 14, 12, 4-0 H	Buffered Address
MEMR L	Memory Read
BMEMR L	Buffered Memory Read

3.4.4 I/O Address Decoder

The I/O address decoder (Figure 3-2) consists of a 16L8 Programmable Array Logic (PAL). The PAL contains an array of programmable AND and OR gates that generate the chip selects from system addresses (SA11:3 H) for the LAD bus transceiver control circuit (Table 3-5).

The PAL is programmed with the following equations.

```
o IF [VCC] MODSEL=SA11*SA10*/SA9*/SA8*SA7*/SA6*SA5*/SA4*/AEN+
  SA11*SA10*/SA9*/SA8*/SA7*SA6*SA5*/SA4*/SA3*/AEN
o IF [VCC] LANCSRSEL=SA11*SA10*/SA9*/SA8*/SA7*SA6*SA5*/SA4*SA3*
  /AEN
o IF [VCC] LANCESEL=SA11*SA10*/SA9*/SA8*/SA7*SA6*SA5*/SA4*/SA3*
  /AEN
o IF [VCC] VIDSEL=/SA11*/SA10*SA9*SA8*SA7*SA6*/SA5*SA4*/AEN
o IF [VCC] DISKSEL=/SA11*/SA10*SA9*SA8*SA7*SA6*SA5*SA4*/SA3*
  /AEN
o IF [VCC] COMMSEL=/SA11*/SA10*SA9*SA8*SA7*SA6*SA5*SA4*SA3*/AEN
o IF [VCC] PRTSEL=SA11*SA10*/SA9*/SA8*SA7*/SA6*SA5*/SA4*/AEN
o IF [VCC] SPREG=SA11*SA10*/SA9*/SA8*SA7*/SA6*/SA5*/SA4*/AEN
```

The product terms of the programmed AND array are fed to a fixed OR array, which gates the summation term (ORed result) to the output pin. In the equations, a "/" is a logical NOT; an "*" is a logical AND, and a "+" is a logical OR. When the CPU asserts AEN H (address enable high), it disables the address decoder process. The CPU uses AEN H to indicate that the current bus cycle is a Direct Memory Address (DMA) cycle.

Table 3-5 I/O Address Decoder Signals

Signal Name	Definition
AEN H	Address Enable
SA11 to 3 H	System Address
MOD SEL L	Mode Select
LANCSR SEL L	LAN Command Status Register Select
LANCE SEL L	LANCE Chip Select
VID SEL L	Video Select
DISK SEL L	Disk Select
COMM SEL L	Communications Select
PRT SEL L	Printer Select
SP REG L	Special Purpose Register

3.4.5 Local Address/Data Bus Transceiver Control

The LAD bus transceiver control (Figure 3-2) consists of a 16L8 PAL. The PAL contains an array of programmable AND and OR gates that generate the signals (Table 3-6) to control the enabling and direction of the LAD bus transceiver.

The I/O 16 L signal is issued by an option to indicate that a 16-bit I/O cycle should be performed. I/O 16 L is a decode of the system address lines only.

The PAL is programmed with the following equations.

```
o IF [VCC] LADEN=LANMSTR+/LANCEREAD+LANCEDALO
o IF [VCC] LB245DIR=CPUSEL*/EMEMR*/SA0+/EIOR*/FDDACKVER+
  /EIOR*MODSEL*LANMSTR+/EIOR*INP1+/EIOR*/INP2+
  LANCEREAD*/LANMSTR
o IF [VCC] HB245DIR=CPUSEL*/FDDACKVER*SA0*/EIOR+
  /EIOR*/MODSEL*LANMSTR*IO16*/SBHE+CPUSEL*/EMEMR
  +/LANCEREAD*/LANMSTR
o IF [VCC] GCIOW=/INP2*/EIOW+CPUSEL*SA0*/SBHE
```

The product terms of the programmed AND array are fed to an OR array, which gates the summation term (ORed result) to the output pin.

Table 3-6 Local Address/Data Bus Transceiver Control Signals

Signal Name	Definition
VER COMM SEL L	Verified Communications Select Low
DISCOMM H	Disable asynchronous Communications
COMM SEL L	Communications Select
FDC SEL L	Floppy Disk Controller Select
PVID L	Pre-Video
DISVID H	Disable Video Output
VID SEL L	Video Select
LANCE DALO L	LANCE Data Address Lines Output
LANCE READ H	LANCE Read
I/O 16 L	Input/Output 16
FD DACK VER L	Floppy Disk DMA Acknowledge Verified
LAN MSTR L	Local Area Network Master
MOD SEL L	Mode Select
SBHE L	System Byte High Enable
SA0 H	System Address 0
EIOR L	Extended Input/Output Read
EMEMR L	Extended Memory Read
CPUSEL H	CPU Select
PLAD EN L	Pre-Local Address/Data Enable
EIOW L	Extended Input/Output Write
GCIOW L	Graphics Controller Input/Output Write
LB245 DIR L	Low Byte 245 Direction
HB245 DIR L	High Byte 245 Direction
3D5WR L	3D5 (Hexadecimal) I/O address Write
LAD EN L	Local Address/Data Bus Enable

3.4.6 Delayed IORD/IOWR Generator

The delayed I/O Read or I/O Write (IORD/IOWR) generator consists of a 74F175 chip. The 74F175 (Figure 3-2) consists of four D-type flip flops that generate delayed IORD/IOWR control signals that synchronize the 80286 CPU timing with slower NMOS microperipherals.

An 8 MHz clock pulse synchronizes the operation of the flip flops with the CPU. The Extended Input/Output Command (EIOC) control signal connects to the input of the delay chain of flip flops. EIOC is the logical OR of Extended Input/Output Read or Extended Input/Output Write (EIOR L or EIOW L). When the command signal at pin 4 meets the setup time requirements, the data is transferred to the output on the rising edge of the clock pulse.

The output of the first flip-flop, R0, becomes the input to the next flip flop, D1, until the input to the third flip flop, D2, sets the flip flop and activates the Enable (E H) output. E H goes to the CRT controller in the video display logic. The output of the third flip flop also becomes the input to the last flip flop, D3. When D3 is set, the high output is not used, but its logical complement, Delayed Input/Output Command (DIOC L) is used. DIOC L is a delayed version of EIOC. It is delayed from the original EIOC by four stages of 125 ns (500 ns total). Delayed Input/Output Read (DIOR L) and Delayed Input/Output Write (DIOW L) are created by ANDing EIOR L and EIOW L with DIOC L. DIOR L and DIOW L go to the inputs of the 8237 DMA controller. Table 3-7 defines the delayed IORD/IOWR generator inputs and outputs.

Table 3-7 Delayed IORD/IOWR Generator Signals

Signal Name	Definition
CLOCK H	Clock
EIOR L	Extended Input/Output Read
EIOW L	Extended Input/Output Write
EIOC H, EIOC L	Extended Input/Output Command
E H	Enable High
DIOR L	Delayed Input/Output Read
DIOW L	Delayed Input/Output Write
DIOC L	Delayed Input/Output Command

Notes

Command is the generic description of either a read or a write operation.

Timing parameters are the same as those for Figure 2-8 and Table 2-5.

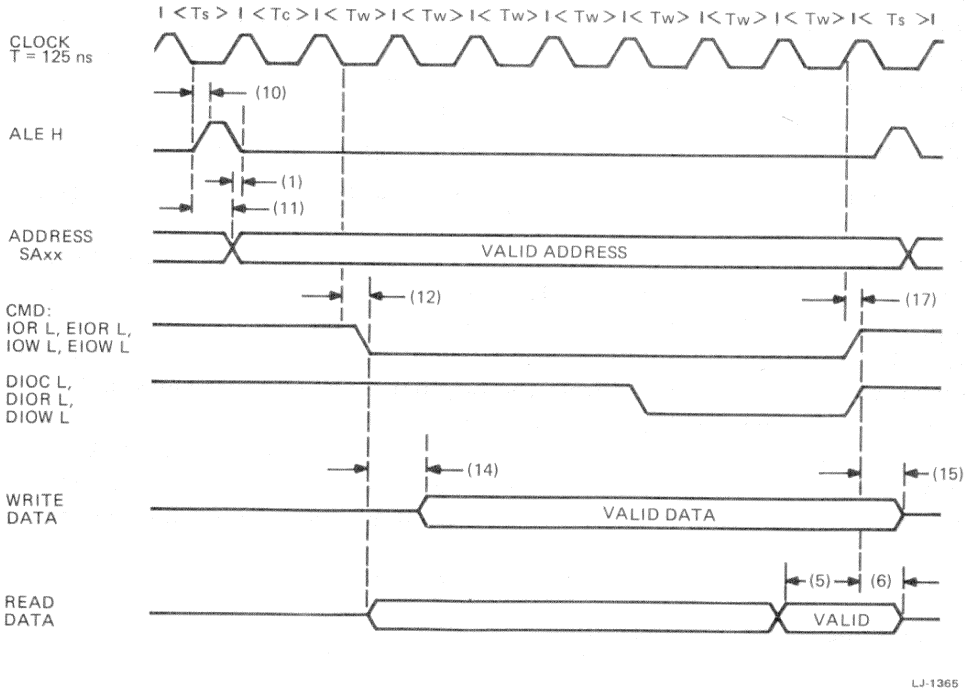


Figure 3-3 Delayed IORD/IOWR Generator Timing Diagram

3.5 Network Interface

The network interface (Figure 3-4), which resides on the I/O-Video module, controls data transmission between the CPU module and a transmitting or receiving device on the ThinWire Ethernet. The network interface consists of a BNC connector, a coaxial transceiver interface (CTI), a serial interface adapter (SIA), a local area network controller (LANCE), a small number of discrete components, and system bus interfacing devices. The common logic is not part

of the interface. However, the network interface and other microperipherals on the I/O-Video module use the common logic to control parallel data transfers between the 16-bit system bus and the 16-bit local address/data (LAD) bus. The controller and supporting circuits, with the exception of the coaxial cable transceiver, operate from the +5 V system power supply. The transceiver operates from the isolated −9 V line.

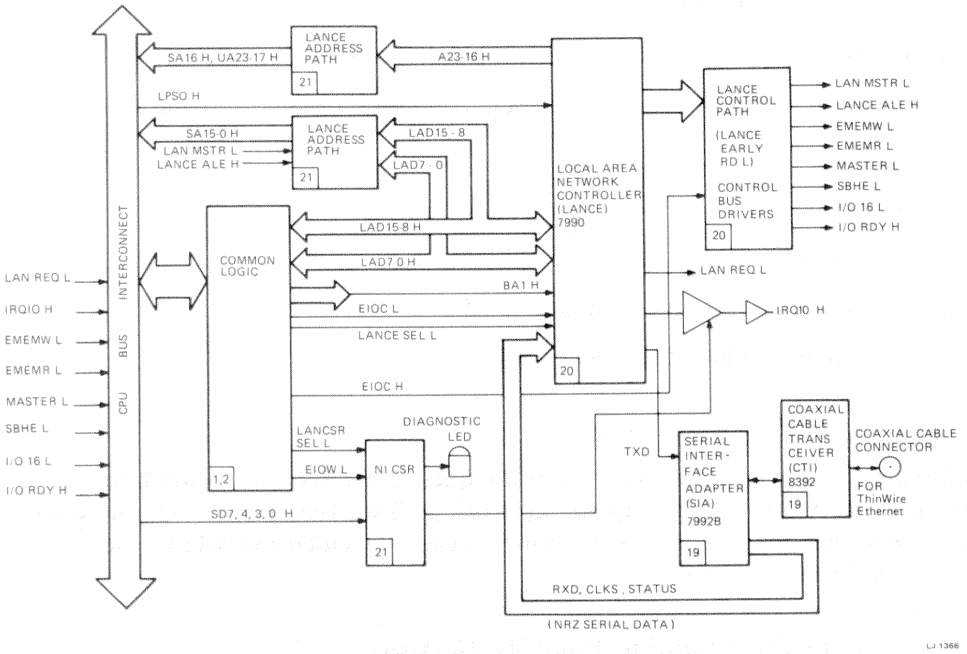


Figure 3-4 Network Interface Block Diagram

3.5.1 Overview

The network interface provides the following functions.

1. Data transmission to/from the network
   a. Transmit
   b. Receive
   c. Collision detect
2. Encoding/decoding of data transmitted/received
3. Data transmission to/from the CPU and system memory using DMA
   a. Transmit
   b. Receive
   c. Control
4. Internal and external loopback modes
5. I/O-Video module diagnostic LED

3.5.1.1 Physical Interconnect

A female BNC-type connector, which mounts to the I/O-Video module, connects the network interface to the network. A BNC T-connector, mounted to the female BNC-type connector, connects the I/O-Video module to the ThinWire Ethernet coaxial cable.

3.5.1.2 Data Transmission From/To Network

The CTI connects directly to the coaxial cable. The CTI performs the transmit, receive, and collision detect functions for the network interface.

Receive Data – The CTI receives the serial data from the cable, and sends it to the SIA.

Transmit Data – The CTI transmits data onto the coaxial cable from the LANCE and SIA. If the CTI detects a collision while transmitting on the cable, it generates a collision detect signal for the SIA. If the CTI accesses the cable without a collision, it transmits the data as formatted.

3.5.1.3 Encoding/Decoding

The SIA decodes data received from the CTI for the LANCE, and encodes data transmitted from the LANCE for the CTI. The SIA runs on a 20 MHz crystal oscillator clock that is divided in half internally, thus producing a 10 MHz data rate. The oscillator feeds into the Manchester phase encoder section, to internally synchronize data streams for transmission.

Decoding – Data received from the CTI enters a noise filter to determine if the data is a valid signal, or noise on the network. The data receiver separates the clock and the data in the Manchester phase decoder section. The Carrier Detect indicates to the LANCE that data of sufficient amplitude is available. The clock for the receiver is generated by an internal phase locked loop in the incoming data stream.

Encoding – Data to be transmitted from the LANCE to the CTI is phase encoded into a standard Manchester serial bit pattern by the encoder section. Then, the encoded data is driven onto the coaxial cable by the transmit secion of the CTI. The clock runs at 10 MHz.

3.5.1.4 Data Transmission From/To CPU and System Memory

The LANCE is a Direct Memory Access (DMA) controller that operates in bus master mode while receiving or transmitting information. The LANCE supports only synchronous memory cycles at 600 ns per cycle.

DMA Capability – The LANCE is a DMA master because it has control, address, and data functions that allow it to gain control of the system bus from the CPU, and transfer data directly between its internal buffer and system memory.

Bus Master Mode – The LANCE operates as bus master when it initiates data, command, and parameter transfers to or from system memory in 16-bit memory cycles.

Bus Slave Mode – The LANCE operates as bus slave when it responds to 16-bit I/O cycles to access its internal registers.

Receiving Information – When the LANCE receives data from the SIA, it loads the data into a FIFO. The FIFO buffers incoming data so the packet can be loaded into a memory buffer using DMA. The LANCE strips the preamble, sync bits, and cyclical redundancy check (CRC) bits from the packet. The packet then consists of destination, type, and data information that is ready to

be stored in memory. The LANCE issues an interrupt to the CPU, informing the CPU that it has completed the DMA transfer, or that an error occurred during receiving.

Transmitting Information – When the CPU sends data to the LANCE, the LANCE prepares it for transmission to the cable through the SIA and CTI. The LANCE encapsulates the data into a frame, which attaches a preamble, sync bits, and CRC. Then, the LANCE converts the frames from a parallel format to a serial format, and sends the frames to the SIA for transmission over the cable.

3.5.1.5 Internal and External Loopback Modes

The network interface provides internal and external loopback modes for testing purposes. These modes are prevented from emulating an actual network interaction, because the maximum loopback frame is 32 bytes and the LANCE FIFO is 48 bytes. Otherwise, the loopback modes test all network interface functions from the LANCE to the coaxial connector. A loopback connector must be connected to the BNC connector labeled to use the external loopback mode.

Internal Loopback Mode – This mode enables you to test the LANCE. When operating in this mode, data loops or frames back within the LANCE. The data does not go to the SIA, CTI, or cable.

External Loopback Mode – This mode enables you to test the hardware between the LANCE and the BNC connector. When operating in this mode, the LANCE sends data onto and receives data from the cable.

3.5.1.6 I/O-Video Module Diagnostic LED

The network interface contains an amber-colored LED that is used to indicate failures in all circuits on the I/O-Video module. Software controls the LED from a bit in the NI CSR.

A default state is indicated when the I/O-Video module diagnostic LED is extinguished. This LED operation is the opposite of the CPU module LED operation. At the start of the self-test for the I/O-Video module, the test illumines the LED. If the I/O-Video module completes the self-test successfully, the test extinguishes the LED.

3.5.2 Coaxial Transceiver Interface

A DP8392 CTI, contained on a 16-pin dual-in-line chip, connects to the coaxial media to perform transmit, receive, and collision detect functions for the LANCE. Because of IEEE 802.3 requirements, the CTI is electrically isolated from the other devices in the workstation.

3.5.3 Serial Interface Adapter

A 7992B SIA, contained on a 24-pin dual-in-line chip, connects to the CTI through an isolation transformer, and performs Manchester phase encoding and decoding of data transmitted and received from the network.

3.5.4 Local Area Network Controller

A 7990 LANCE, contained on a 48-pin dual-in-line chip, uses its address, data, and control lines to support its DMA capability. These lines are described as follows.

1. Address/Data Lines – The LANCE provides 24 address lines for DMA transfers. Local Address/Data bus lines (LAD15-0 H) are 3-state bidirectional lines. During the address portion of a memory transfer, LAD0-15 H contains the lower 16 bits of the memory address. Address lines (A23-16 H), which are 3-state and one-directional, contain the upper 8 bits of the memory address.

   During the data portion of a memory transfer, LAD15-0 H contains the read/write data, depending on the type of transfer.

   The LANCE drives LAD15-0 H lines as a bus master and as a bus slave, but A23-16 H lines as bus master only.

2. Interrupt Request 10 (IRQ10 H) – When the LANCE asserts this 3-state signal, it is interrupting the CPU. The LANCE holds IRQ10 H high until the CPU acknowledges the interrupt through the interrupt service routine.

3. LANCE Request (LAN REQ L) – This signal is an asynchronous channel request generated by the LANCE to become the bus master. LAN REQ L must be held low until the CPU asserts the LANCE ACKnowledge (LAN ACK) signal. LAN REQ L is a 3-state line that goes to a special arbitrator between the CPU and DMA controller. This special arbitrator controls three request lines, and the LANCE has higher priority than the 8237 DMA controller on the CPU module.

3.5.5 LANCE Control Path and Control Bus Drivers

The network interface provides control path logic which enables the LANCE to control read/write functions between the system bus and system memory. The control path logic is used for slave mode I/O access to the LANCE by the CPU. The control path also generates the I/O Ready (I/O RDY H) signal, to synchronize CPU timing with I/O cycle timing for the LANCE. Because the LANCE registers are implemented in microcode, as opposed to hardware register implementation, they have a slower response time than standard 80286 I/O cycle timing. The LANCE uses the bus drivers to drive the read/write commands, while in bus master mode. The LANCE control and bus driver signals are as follows.

1. LANCE Master (LAN MSTR L) and MASTER L – These signals are asserted when the LANCE bus obtains mastership of the bus.
2. LANCE Address Latch Enable (LANCE ALE H) – This is the address strobe for read/write operations. It occurs at the beginning of each read/write cycle in master mode.
3. I/O Ready (I/O RDY H) – When the CPU selects internal LANCE registers, I/O RDY H is deasserted on the system bus. This process introduces wait states into CPU I/O cycle timing, keeping all address, data, and control lines stable on the system bus until I/O RDY H goes high. When the LANCE completes its register operation, it replies to the CPU by asserting I/O RDY H high. Then, the CPU resumes its operation.
4. I/O16 L – This signal indicates that a 16-bit I/O cycle should be performed. I/O16 L is a decode of the system address lines only.
5. Extended Memory Read (EMEMR L) – When asserted, this signal instructs system memory to drive data onto the 16-bit data bus. It is active for the entire 16 megabytes of address space. EMEMR L may be driven when the LANCE is bus master.
6. Extended Memory Write (EMEMW L) – When asserted, this signal instructs system memory to store the data that is present on the 16-bit data bus. It is active for the entire 16 megabytes of address space. EMEMR L may be driven when the LANCE is bus master.
7. LANCE EARLY Read (LANCE EARLY RD L) – When the LANCE is reading from system memory in master mode, it generates the LANCE EARLY

RD L signal. This signal causes the memory read cycle to occur earlier than standard LANCE memory timing, thereby creating more access time for read cycles. This logic optimizes read/write memory timing.

8. System Bus High Enable (SBHE L) – The LANCE uses SBHE L and System Address 0 (SA0) to select the proper bytes of the data bus word when reading from or writing to system memory. SBHE L may be driven when the LANCE is bus master.

3.6 Asynchronous Serial Printer Port Interface

The asynchronous serial printer port interface (Figure 3-5) resides on the I/O-VIDEO module. This port controls asynchronous data transmission between the CPU module and a serial printer. The interface consists of a programmable asynchronous communications controller, an EIA driver and receiver, and a modified modular jack (MMJ) connector. The common logic is not part of the interface. However, the serial printer port interface and other microperipherals on the I/O-VIDEO module use the common logic block to control parallel data transfers between the 16-bit system bus and the 8-bit local address/data (LAD) bus.

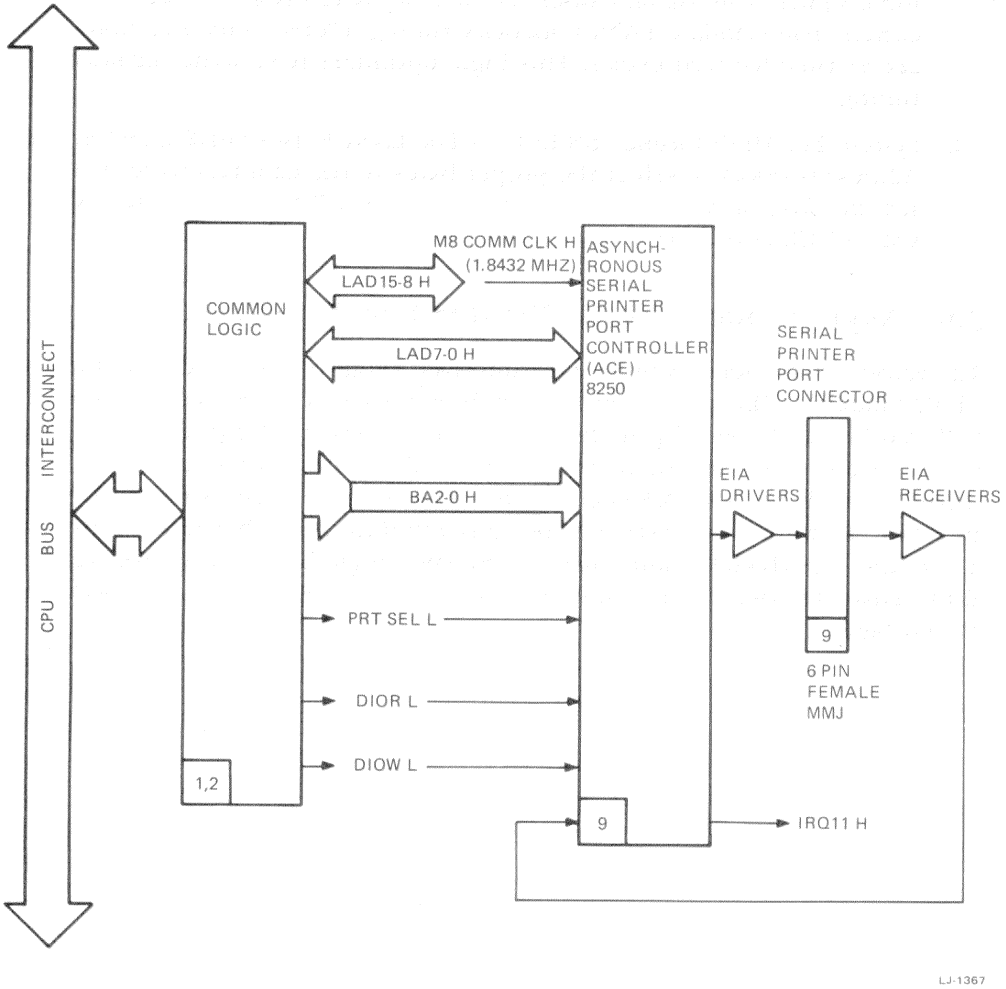


Figure 3-5 Serial Printer Port Interface Block Diagram

3.6.1 Overview

The asynchronous serial printer port interface performs the following major functions.

1. Data transmission
   a. Transmit
   b. Receive
   c. Control
2. EIA interface signal levels
3. Physical Interconnect

3.6.2 Data Transmission

A WD8250 programmable Asynchronous Communications Element (ACE), a 40-pin dual-in-line chip, contains several registers (Figure 3-6) that control the transmit, receive, and control functions for the asynchronous serial printer port interface. The paragraphs that follow provide a brief functional description of the registers. Refer to volumes 1 and 2 of the *VAXmate Technical Reference Manual* (Q6ZCS-GZ) for more information on the hardware registers.

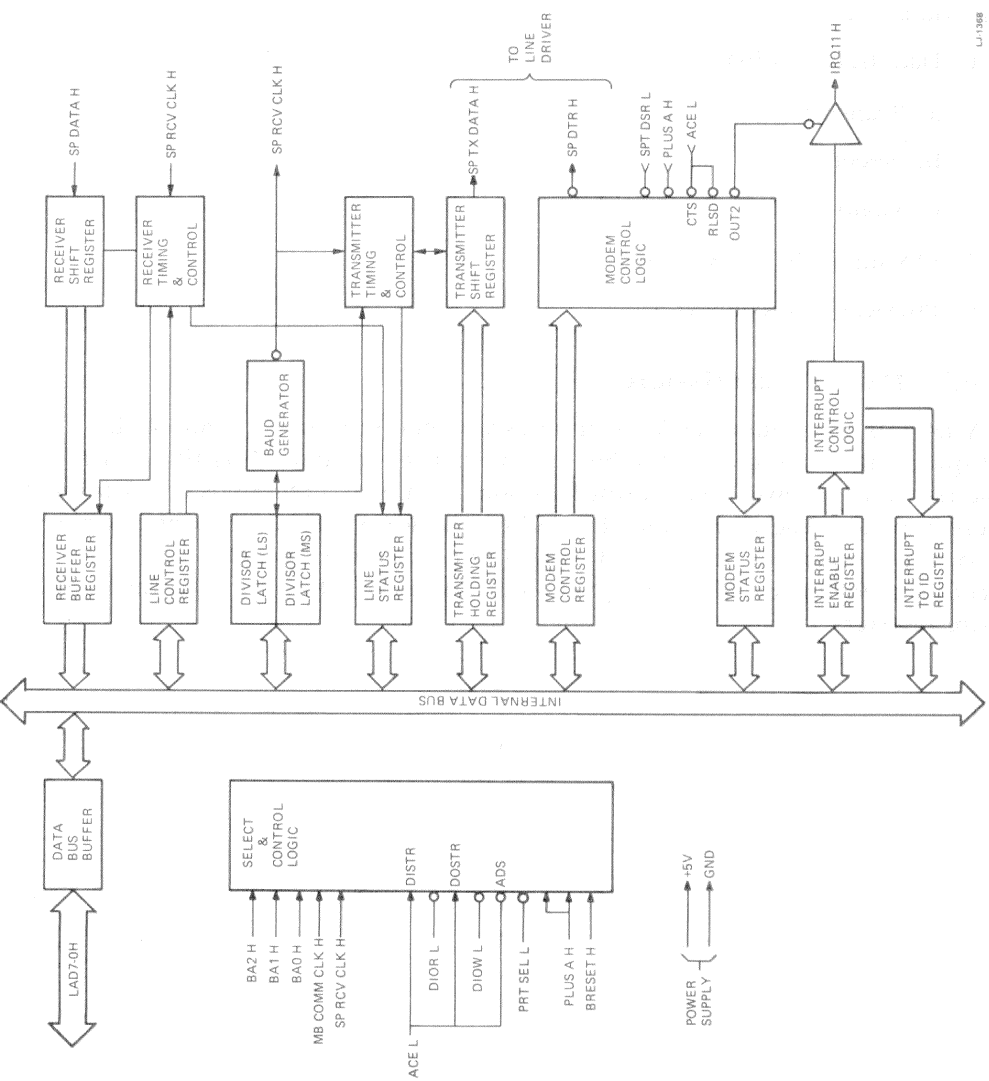


Figure 3-6 Asynchronous Communications Element Block Diagram for Printer Port Interface

The ACE transmitter performs parallel-to-serial data conversions. It accepts parallel input data, adds the start, parity, and stop bits, and outputs the formatted character, one bit at a time, over the serial output line. The serial format (in order of transmission and reception) is as follows.

1. Start bit
2. Five to eight data bits
3. Parity bit (if programmed)
4. One, one and a half, or two stop bits

The ACE receiver performs the opposite conversion of the transmitter section. Whenever the receiver detects a start bit at the serial input, it converts the stream of bits to a parallel output. During this data conversion, the receiver removes the start and stop bits from the incoming character. If the optional parity bit accompanies the data, the receiver uses it to check for possible data transmission errors.

The internal operations of the transmitter and receiver are synchronized by an external clock signal. The clock signal, MB COMM CLK H, is supplied to an internal programmable baud rate generator. The output frequency of the clock signal is 16 times the serial baud rate. The ACE will operate in either a polling or interrupt driven system, which is programmed by writing to the internal registers.

The following is a brief description of the internal registers that implement the transmit and receive functions of the ACE.

Data Bus and Data Bus Buffer – The data bus consists of eight 3-state I/O lines. The bus provides bidirectional communications between the ACE and the common logic. The bus handles data, control words, and status information. This 3-state, bidirectional, 8-bit buffer connects the ACE to the common logic. The buffer does double buffering by providing separate 8-bit registers for command status, input data, and output data.

Receive Buffer Register – This read-only register holds input data bits 7 to 0.

Receive Shift Register – This register receives the serial input (SIN) data from the communications link. This register determines if the data is properly formatted, and then shifts out a parallel 8-bit word.

Transmitter Holding Register – This write-only register holds output data bits 7 to 0.

Transmitter Shift Register – This register receives the composite serial output (SOUT) data from the CPU. It determines if the data is properly formatted, and then shifts out serial data. The SOUT signal is set to the marking state during a master reset operation.

Line Status Register – This 8-bit register provides status information to the CPU concerning the data transfer.

Programmable Baud Rate Generator – The baud rate generator takes the clock input, M8 COMM CLK, which is the output of a 1.8432 MHz crystal, and divides it by any divisor from 1 to $2^{16} - 1$. The output frequency of the baud rate generator is 16 times the baud rate. Two 8-bit latches store the divisor in a binary format. These divisor latches must be loaded during initialization, in order to ensure desired operation of the baud rate generator. When either of the latches is loaded, a 16-bit baud counter is immediately loaded. The signal serial printer receive clock (SP RCV CLK H) goes to both the receiver and transmitter sections to provide the baud rate clocking. Table 3-8 lists the divisors used to obtain the desired baud rate, and the specified percent of error. Note that the ACE does not support 200 baud.

Table 3-8 Asynchronous Communications Element Baud Rates for Printer Port

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–

Table 3-8 Asynchronous Communications Element Baud Rates for Printer Port *(cont.)*

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Between Desired and Actual
9600	12	–
19200	6	–
38400	3	–

The ACE control section inputs control signals that determine how the ACE will format the serial data. Control signals are input to the select and control logic, modem control logic, interrupt control logic, receiver timing and control, and transmitter timing and control. The select and control logic implements the following signals.

- PRT SEL L – When this signal is asserted, the ACE is selected. ACE selection is complete when the decoded chip select signal is latched with an active ACE L at the ADS input.
- ACE L and DIOR L – If both of these signals are asserted while the ACE is selected, the CPU can read status information or data from a selected register.
- ACE L and DIOW L – If both of these signals are asserted while the ACE is selected, the CPU can write data or control words into a selected register.
- BRESET H – When this signal is high, it clears the ACE control logic and all registers except the receiver buffer, the transmitter holding register, and the divisor latches. Also, an active BRESET H signal affects the states of the SP TX DATA H, IRQ11 H, OUT2 L, and SP DTR H output signals.
- ACE L at ADS – When ACE L is low, it provides latching for the register select (BA2-H), and PRT SEL L signal.
- BA2-0 H – Buffered address bits 2 to 0 select the read or write register as indicated in Table 3-9.

Table 3-9 Printer Control Register Addresses

Printer Addr	DLAB	A2	A1	A0	Register
		x	x	x	
CA0	0	0	0	0	Receive buffer (read) or Transmit holding register (write)

Table 3-9 Printer Control Register Addresses *(cont.)*

Printer Addr	DLAB	A2	A1	A0	Register
CA1	0	0	0	1	Interrupt enable
CA0	1	0	0	0	Divisor latch (LSB)
CA1	1	0	0	1	Divisor latch (MSB)
CA2	x	0	1	0	Interrupt identification (read only)
CA3	x	0	1	1	Line control
CA4	x	1	0	0	Modem control
CA5	x	1	0	1	Line status
CA6	x	1	1	0	Modem status
CA7	x	1	1	1	None

The modem control logic determines the state of the communications link and transfer data. The modem signals are as follows.

- ACE L at CTS L – Whenever the CTS function of the modem status register changes state, an interrupt is generated if the modem status interrupt is enabled. At this input, ACE L is a modem control function input. The CPU can test the input condition by reading the CTS function in the modem status register.
- SPT DSR L – When this signal is low, the ACE is ready to establish the communications link and transfer data. The CPU can test the condition of this signal by reading the modem status register.
- ACE L at RLSD L – When this signal is low, the ACE has been detected as the data carrier. The CPU can test the condition of this signal by reading the modem status register. Whenever the RLSD function changes state, and the modem status interrupt is enabled, an interrupt is sent to the CPU.
- SP DTR H – When this signal is asserted, the ACE is ready to communicate with the printer.
- OUT2 – This signal is a user-designated output to enable/disable the 3-state driver that generates the IRQ11 H signal.

The interrupt control logic uses IRQ11 H to interrupt the CPU when the printer data is available, the transmitter holding register is empty, the printer encounters an error, or the modem reports its status. The IRQ11 H signal goes high whenever the interrupt conditions are active high, and are enabled by the interrupt enable register. IRQ11 H is reset low during the appropriate interrupt service or a master reset operation.

The control registers for the receiver section generate the following output.

Line Control Register – The system programmer specifies the format of the asynchronous data communications exchange using the line control register. In addition to controlling the format, the programmer may retrieve the contents of the register for inspection.

Receiver Timing and Control Register – This register contains the serial printer receive clock (SP RCV CLK H) signal bits, which define the 16 times baud rate clock for the receiver section of the ACE. SP RCV CLK H also provides the timing for the transmitter section.

The transmitter timing and control provides timing and control signals for the transmitter section of the ACE. The output from the baud rate generator, SP RCV CLK H, is the timing signal for the transmitter section. This output is also the timing signal for the receiver section.

3.6.3 EIA Interface

A 9636 line driver (Figure 3-6) and the quad receivers shared with the asynchronous communications port interface provide the EIA standard interface for connection to a compatible serial printer. These components are described as follows.

Line Driver – One 9636 drives the signals SP TX DATA H and SP DTR H. The signals PLUSV H (+12 V) and MINUSV H (−12 V) power the driver.

Quad Receiver – The quad receiver shared with the asynchronous communication port interface accepts the SP DSR H, SP RECV COM L, and SP RCV DATA L data and control signals from the serial printer. A +5 V line powers the receiver.

3.6.4 Physical Interconnect

A 6-pin MMJ connector (J3) on the I/O-Video module provides the connection between the ACE and the serial printer. Table 3-10 lists the pin assignments for J3. Figure 3-7 is the EIA interface and interconnect block diagram. Components on the transmit lines provide radiated emission filtering. Components on the receive lines provide electrostatic discharge protection. The Local Direct Connection (No Modem) For Serial Asynchronous Terminals And System Interfaces, DEC STD 052-4, specifies the connector configuration. To connect to a standard DB-25 serial printer connector, you must attach a DB-25 passive adapter to the MMJ connector. Cable number 17-00721 connects the printer to the port.

Table 3-10. Connector J3 Pin Assignments

Pin Number	Signal Name
1	Serial Printer Data Terminal Ready (SP DTR H)
2	Serial Printer Transmit Data (SP TX DATA H)
3	Serial Printer Transmit Common (signal ground)
4	Serial Printer Receive Common (SP RECV COM L)
5	Serial Printer Receive Data (SP RCV DATA L)
6	Serial Printer Data Set Ready (SP DSR H)

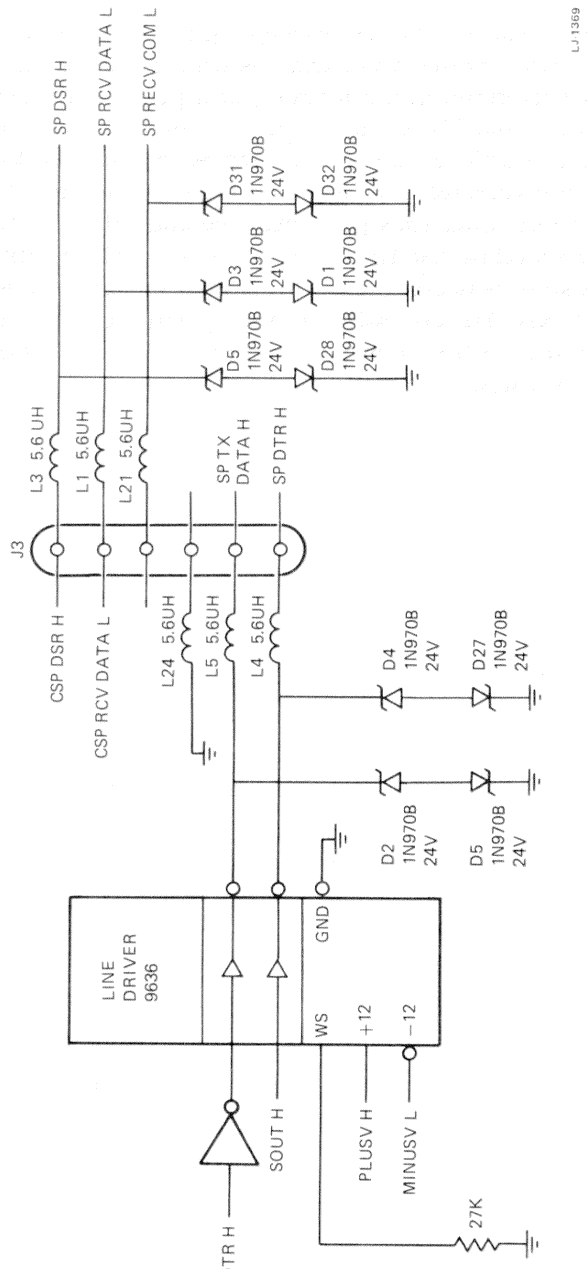


Figure 3-7 EIA Interface and Interconnect Block Diagram

3.7 Asynchronous Communications Port Interface

The Asynchronous Communications Port Interface (Figure 3-8) resides on the I/O-Video module. This port controls asynchronous data transmission between the CPU module and another computer, a modem, or a peripheral device. The interface consists of a programmable asynchronous communications controller, a split baud counter and multiplexer, a special purpose register, an EIA driver and receiver, and a DB-25 connector. The common logic is not part of the interface. However, the communications port interface and other microperipherals on the I/O-Video module use the common logic block to format and control parallel data transfers between the 16-bit system bus and the 8-bit local address/data (LAD) bus. The controller and supporting circuits, except the drivers, operate from the +5 V system power supply. The drivers operate from the +12 V and −12 V lines.

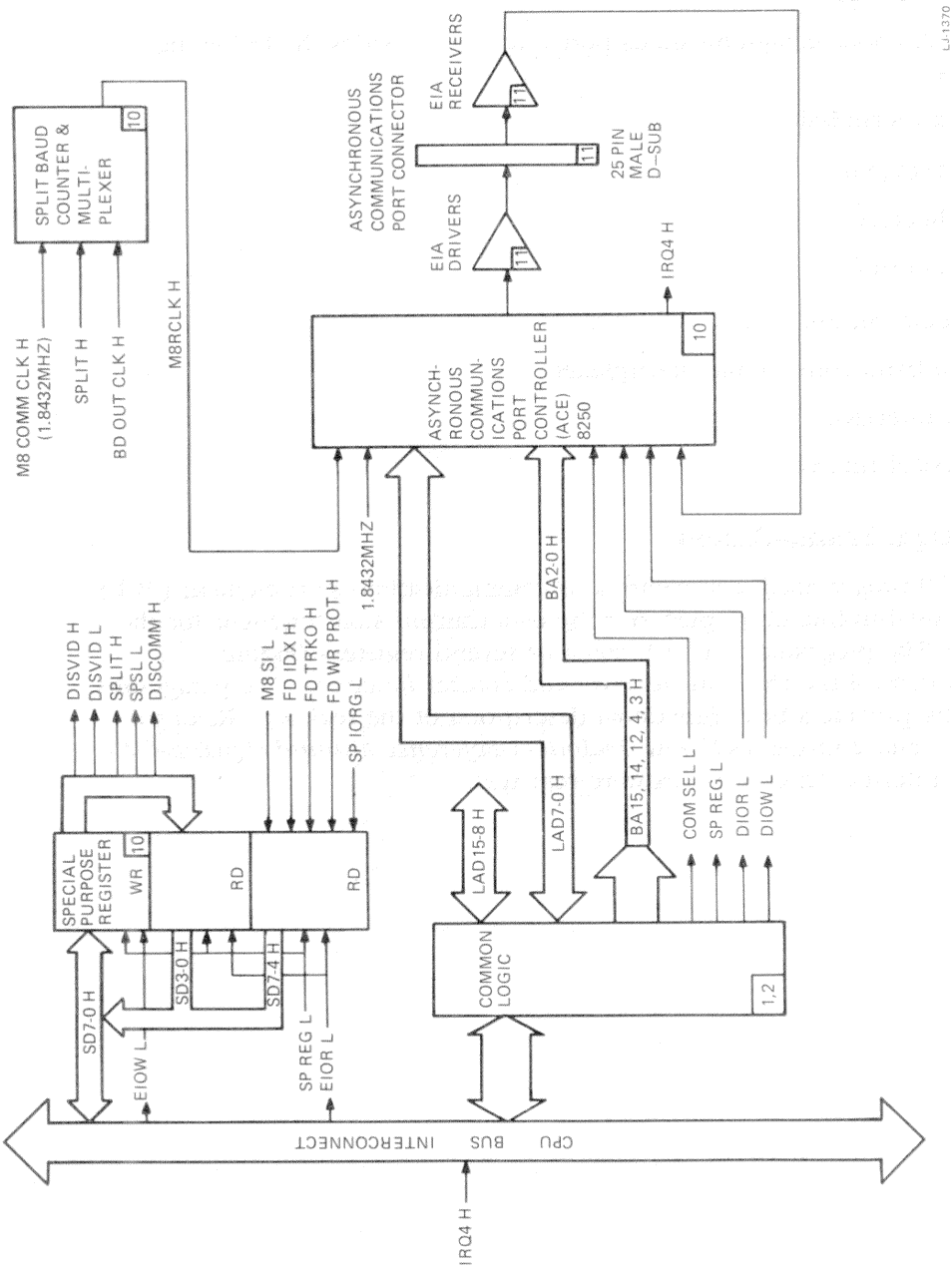


Figure 3-8 Communications Port Interface Block Diagram

3.7.1 Overview

The asynchronous communications port interface provides the following functions.

1. Data transmission
   a. Transmit
   b. Receive
   c. Control
2. Modem control
3. Split baud counter and multiplexer
4. EIA interface
5. Physical Interconnect

3.7.2 Data Transmission

A WD8250 programmable asynchronous communications port element (ACE), a 40-pin dual-in-line chip, performs the data transmission functions for the interface. The programmable ACE contains several registers (Figure 3-9) that control the transmit, receive, and control functions. The paragraphs that follow provide a brief functional description of the registers. Refer to volumes 1 and 2 of the *VAXmate Technical Reference Manual* (Q6ZCS-GZ) for more information on the hardware registers.

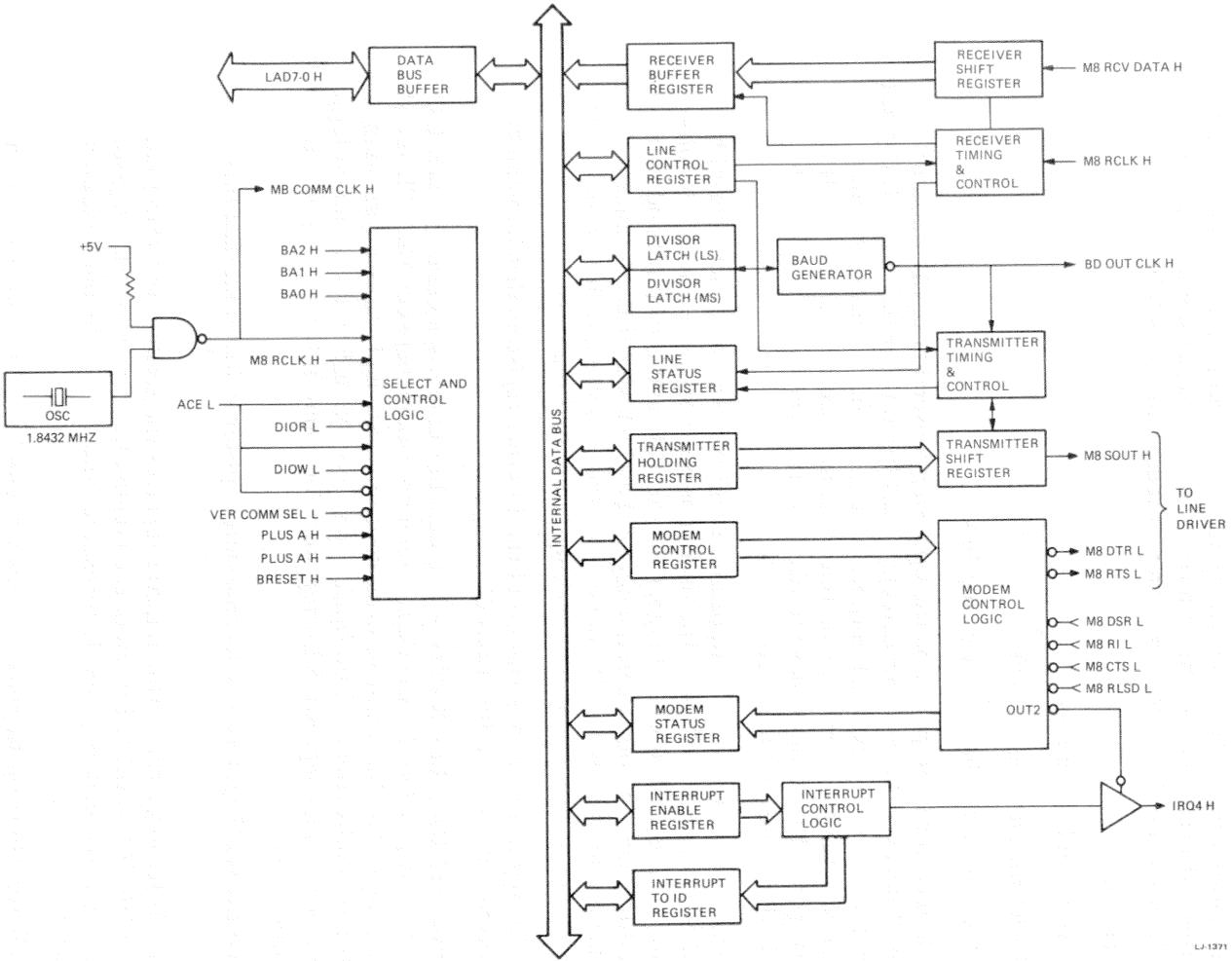


Figure 3-9 Asynchronous Communications Element Block Diagram for Communications Port Interface

The ACE transmitter logic performs parallel-to-serial data conversions. It accepts parallel input data, adds the start, parity, and stop bits, and outputs the formatted character, one bit at a time, over the serial output line. The serial format (in order of transmission and reception) is as follows.

1. Start bit
2. Five to eight data bits
3. Parity bit (if programmed)
4. One, one and a half, or two stop bits

The ACE receiver logic performs the opposite conversion of the transmitter section. Whenever the receiver detects a start bit at the serial input, it converts the stream of bits to a parallel output. During this data conversion, the receiver removes the start and stop bits from the incoming character. If the optional parity bit accompanies the data, the receiver uses it to check for possible data transmission errors.

The internal operations of the transmitter and receiver are synchronized by a 1.8432 MHz crystal oscillator. The oscillator pulse is ANDed with +5 volts to generate the M8 COMM CLK H signal for the ACE, and the split baud counter and multiplexer. The output frequency of the clock signal is 16 times the serial baud rate. The ACE will operate in either a polling or interrupt driven system, which is programmed by writing to internal registers.

The following is a brief description of the internal registers that implement the transmit and receive functions of the ACE.

Data Bus and Data Bus Buffer – The data bus comprises eight, 3-state, I/O lines. The bus provides bidirectional communications between the ACE and the common logic. The bus controls data, control words, and status information. This 3-state, bidirectional, 8-bit buffer connects the ACE to the common logic. The buffer provides separate 8-bit registers for command status, input data, and output data.

Receive Buffer Register – This read-only register holds input data bits 7 to 0.

Receive Shift Register – This register receives the serial input (SIN) data over the M8 RCV DATA H line from the communications link. This register determines if the data is properly formatted, and then shifts out a parallel 8-bit word.

Transmitter Holding Register – This write-only register holds output data bits 7 through 0.

Transmitter Shift Register – This register receives the composite serial output (SOUT) data from the CPU over the M8 SOUT H line. This register determines if the data is properly formatted, and then shifts out serial data. The M8 SOUT H signal is set to the marking state during a master reset operation.

Line Status Register – This 8-bit register provides status information to the CPU concerning the data transfer.

Programmable Baud Rate Generator – The baud rate generator takes the clock input, M8 COMM CLK H, which is the output of a 1.8432 MHz oscillator, and divides it by any divisor from 1 to $2^{16} - 1$. The output frequency of the baud rate generator is 16 times the baud rate. Within the baud rate generator there are two 8-bit latches that store the divisor in a binary format. To ensure desired operation of the baud rate generator, the divisor latches must be loaded during initialization. When either latch is loaded, a 16-bit baud counter is immediately loaded. Then, the M8 COMM CLK H and BD OUT CLK H signals go to the split baud counter and multiplexer simultaneously to generate the transmit/receive clock signal M8 RCLK H. Table 3-11 shows the divisor used to obtain the desired baud rate, and the specified percent of error. Note that the ACE does not support a 200 baud data transmission rate.

Table 3-11 Asynchronous Communications Element Baud Rates for COMM Port

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Between Desired and Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–

Table 3-11 Asynchronous Communications Element Baud Rates for COMM Port *(cont.)*

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Between Desired and Actual
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–

The ACE control section inputs control signals that determine how ACE will format the serial data. Control signals are input to the select and control logic, the modem control logic, the interrupt control logic, the receiver timing and control, and the transmitter timing and control. The select and control logic implements the following signals.

- PLUS A H – When the decoded PLUS A H signal is latched with an active ACE L at the ADS input, the ACE is selected.
- ACE L and DIOR L – When these signals are low and the ACE is selected, the CPU can read status information or data from a selected register.
- ACE L and DIOW L – When these signals are low and the ACE is selected, the CPU can write data or control words to a selected register.
- BRESET H =- When this signal is high, it clears the ACE control logic and all registers (except the receiver buffer, transmitter holding register, and divisor latches). Also, an active BRESET H signal affects the states of the IRQ4 H, M8 SOUT H, M8 RTS L, and M8 DTR H output signals.
- ACE L at ADS L – When ACE L is asserted, it provides latching for the register select PLUS A H signals (BA2 to 0 H).
- BA2 to 0 H – Buffered address bits 2 to 0 select the read or write register as indicated in Table 3-12.

Table 3-12 Asynchronous Communications Element Register Addresses

Comm Addr	DLAB	A2	A1	A0	Register
		x	x	x	
3F8	0	0	0	0	Receive buffer (read) or Transmit holding register (write)
3F9	0	0	0	1	Interrupt enable
3FA	x	0	1	0	Interrupt identification (read only)
3FB	x	0	1	1	Line control
3FC	x	1	0	0	Modem control
3FD	x	1	0	1	Line status
3FE	x	1	1	0	Modem status
3FF	x	1	1	1	None
3F8	1	0	0	0	Divisor latch (LSB)
3F9	1	0	0	1	Divisor latch (MSB)

The modem control logic determines the state of the communications link and transfer data. The modem control signals are as follows.

- M8 CTS L – Whenever the CTS function of the modem status register changes state, the LANCE generates an interrupt if the modem control logic enables the modem status interrupt. M8 CTS L is a modem control function input. The CPU can test the input condition by reading the CTS function in the modem status register.
- M8 DSR L – When this signal is low, the ACE is ready to establish the communications link, and transfer data. The CPU can test the condition of this signal by reading the modem status register.
- M8 RLSD L – When this signal is low, the ACE detected the data carrier. The CPU can test the condition of this signal by reading the modem status register. Whenever the RLSD function changes state, and the modem control logic enables the modem status interrupt, the LANCE generates an interrupt.

- M8 DTR L – When asserted, this signal informs the computer, modem, or peripheral device that the ACE is ready to communicate.
- OUT2 – This signal is a user-designated output to enable/disable the 3-state driver that generates the IRQ4 H signal.

The interrupt control logic uses IRQ4 H to interrupt the CPU when the input data is available, the transmitter holding register is empty, the input device encounters an error, and the modem reports its status. The IRQ4 H signal is asserted whenever the interrupt conditions are active high, and are enabled by the interrupt enable register. IRQ4 H is deasserted upon the appropriate interrupt service or a master reset operation.

The control registers for the receiver section generate the following outputs.

- Line Control Register – The system programmer specifies the format of the asynchronous data communications exchange using the line control register. In addition to controlling the format, the programmer may retrieve the contents of the register for inspection.
- Receiver Timing and Control – This register contains the multiplexer receive clock (M8 RCLK H) signal bits, which define the 16 times baud rate clock for the receiver section of the ACE. M8 RCLK H also provides the timing for the transmitter section.

The transmitter timing and control provides timing and control signals for the transmitter section of the ACE. The output from the split baud counter and multiplexer, M8 RCLK H, is the timing signal for the transmitter section. This output is also the timing signal for the receiver section.

3.7.3 Modem Control

The ACE does not control the modem control signals for speed select and speed indicator. Speed select is controlled by writing to I/O address C80, data bit 0 of the special purpose register. By writing a 0 (low) to this address, the programmer asserts speed select on the Asynchronous Communications Port Interface. Speed indicator is read at I/O address C80 data bit 4. A 0 (low) indicates the asserted state. You can read the contents of the special purpose register at the same I/O address.

3.7.4 Split Baud Counter and Multiplexer

The asynchronous communications port interface supports one mode of split baud rate using a split baud counter and multiplexer (Figure 3-8). By writing

a 1 (high) to I/O address C80, data bit 2 of the special purpose register, you set the receiver clock baud rate to 1200 baud. The baud rate generator controls the transmitter clock baud rate, which allows the ACE to operate in split baud rate mode. By writing a 0 (low) to I/O address C80, data bit 2 of the special purpose register, you return the receiver clock control to the baud rate generator on the ACE. You can read this bit at the same I/O address.

3.7.5 Special Purpose Register

The special purpose register (Figure 3-8) consists of a 74LS175 containing four D-type flip flops, and two 74LS244 octal drivers. The special purpose register is located at I/O address C80 (hex). The asynchronous communications port, the diskette controller, and the video display controller use the register.

The asynchronous communications port uses the following signals to provide Digital extended features.

- Speed Select (SPSL L) – The asynchronous communications port uses this read/write signal to select the modem baud rate.
- Disable Asynchronous Communications (DISCOMM H) – The asynchronous communications port uses this read/write signal to disable I/O reads and writes to this section.
- Split Baud Rate (SPLIT H) – The asynchronous communications port uses this read/write signal to enable the split baud rate mode.
- Speed Indicator (M8 SI L) – The CPU uses this read-only signal to read the status of the modem baud rate.

The diskette controller uses the following signals to provide Digital extended diagnostic features.

- Floppy Diskette Index Pulse (FD IDX H) – The diagnostic engineer uses this read-only signal, which is the real time status of the index pulse of the selected diskette drive, for diagnostic purposes to test the motor speed of the diskette drives.
- Floppy Diskette Track 0 (FD TRK0 H) – The diagnostic engineer uses this read-only signal, which is the track 0 indication signal output from the selected diskette drive, for diagnostic purposes.
- Floppy Diskette Write Protect (FD WR PROT H) – The diagnostic engineer uses this read-only signal, which is the write protect signal output from the selected diskette drive, for diagnostic purposes.

The video display controller uses the special purpose register to provide the following signal.

- Disable Video Output (DISVID L) – The video controller uses this read/write signal to enable/disable the video controller output to the CRT.

3.7.6 EIA Interface

A pair of 9636 line drivers, and a pair of 26LS32 quad receivers (Figure 3-10) provide the EIA standard interface for connection to another computer, a modem, or a peripheral device. These components are described as follows.

Line Drivers – One 9636 drives the M8 RTS L and M8 DTR L signals. The other 9636 drives the SPSL L and M8 SOUT H signals, which transmit the serial data. The signals PLUSV H (+12 V) and MINUSV L (–12 V) power the drivers.

Quad Receivers – Both receivers accept data and control signals from the input device. The asynchronous communications port shares one of the receivers with the serial printer port. A +5 V line powers the receivers.

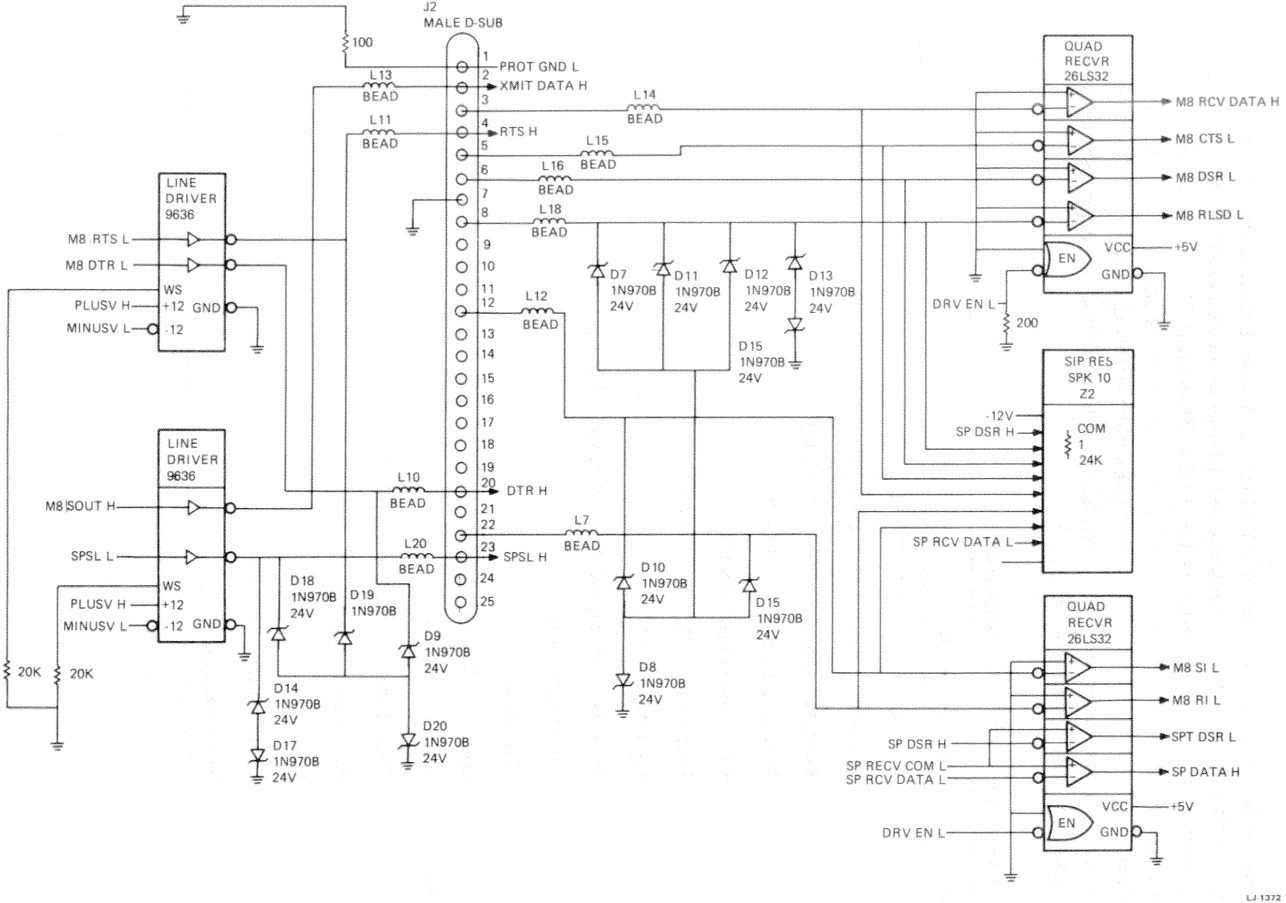


Figure 3-10 EIA Interface and Interconnect Block Diagram

3.7.7 Physical Interconnect

A 25-pin D-subminiature connector (J2) (Figure 3-10) located on the rear panel of the I/O-Video module provides the physical connection between the ACE and the input device. The port is RS-232-C functionally compatible, RS-423 electrically compatible, and configured as Data Terminal Equipment (DTE). Components on the transmit lines provide radiated emission filtering, and components on the receive lines provide electrostatic discharge protection. Table 3-13 lists the pin assignments for J2.

Table 3-13 Connector J2 Pin Assignments

Pin Number	Signal Name
1	Protective Ground (PROT GND L)
2	Transmit Data (XMIT DATA H)
3	Receive Data (M8 RCV DATA H)
4	Request To Send (RTS H)
5	Clear To Send (M8 CTS L)
6	Data Set Ready (M8 DSR L)
7	Signal ground
8	Receive Line Signal Detect (M8 RLSD L)
9 and 10	Not connected
11	Not used
12	Speed Indicator (M8 SI L)
13 through 19	Not connected
20	Data Terminal Ready (DTR H)
21	Not connected
22	Ring Indicator (M8 RI L)
23	Speed Select (SPSL H)
24 and 25	Not connected

Chapter 4
Video Subsystem

4.1 Introduction

This chapter provides a functional description of the video controller, the monitor board, and the CRT circuit. The video controller resides on the I/O board and drives a monochrome or a color monitor. Within the video subsystem, the display processor displays up to 16 colors or 16 shades of gray. In this chapter, the term "color" also means "shades of gray" or "intensity levels." The monochrome VAXmate can display 16 levels of gray.

4.2 Video Controller Functional Description

The VAXmate workstation video controller (Figure 4-1) consists of translation logic, a CRT controller, video memory address logic, 16 Kbytes of static video memory, 48 Kbytes of dynamic video memory, a 4 Kbyte static video font memory, decoding and arbitration logic, and a 144-pin video gate array.

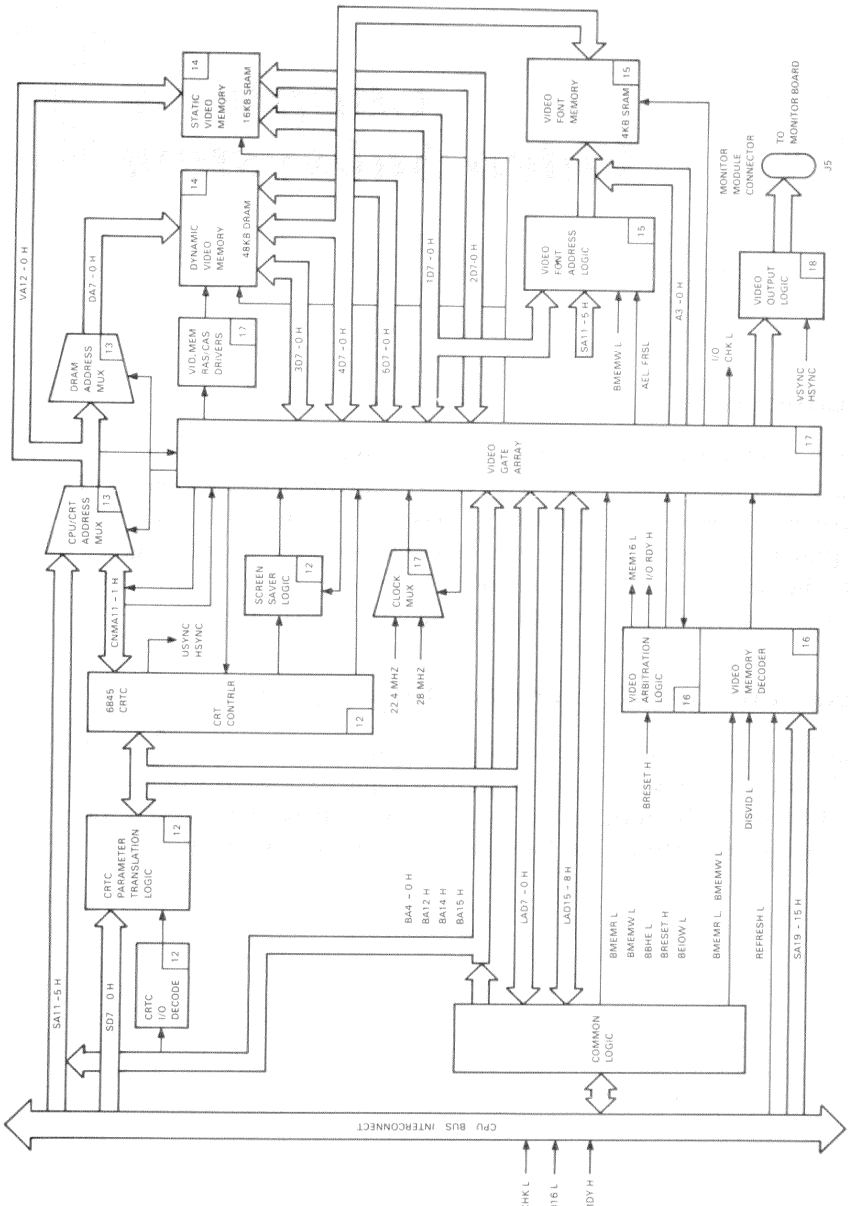


Figure 4-1 Video Subsystem Block Diagram

4.2.1 Translation Logic

The translation logic (Figure 4-2) translates industry-standard hardware data into VAXmate hardware-compatible data. The supporting circuits include an additional I/O decoder, to provide enable signals for the translation ROM and four D-type multiplexers.

Certain parameters in the 6845 are implementation-specific for some industry-standard applications that go directly to the video. The translation logic forces the values written for the industry-standard application into the correct values in our system, so that the CRT timing can match the monitor timings and generate appropriate controls to the video gate array.

An I/O write at 3D4 (hex) into the index register of 6845, latches the lower four bits of data into D-flops (12). An I/O write at location 3D5 (hex) activates the translation ROM. The data (SD7-0) and the previously latched address (LA3-0) form an address into the ROM. The corresponding contents of the ROM, at LAD7-0, is written into the CRT controller.

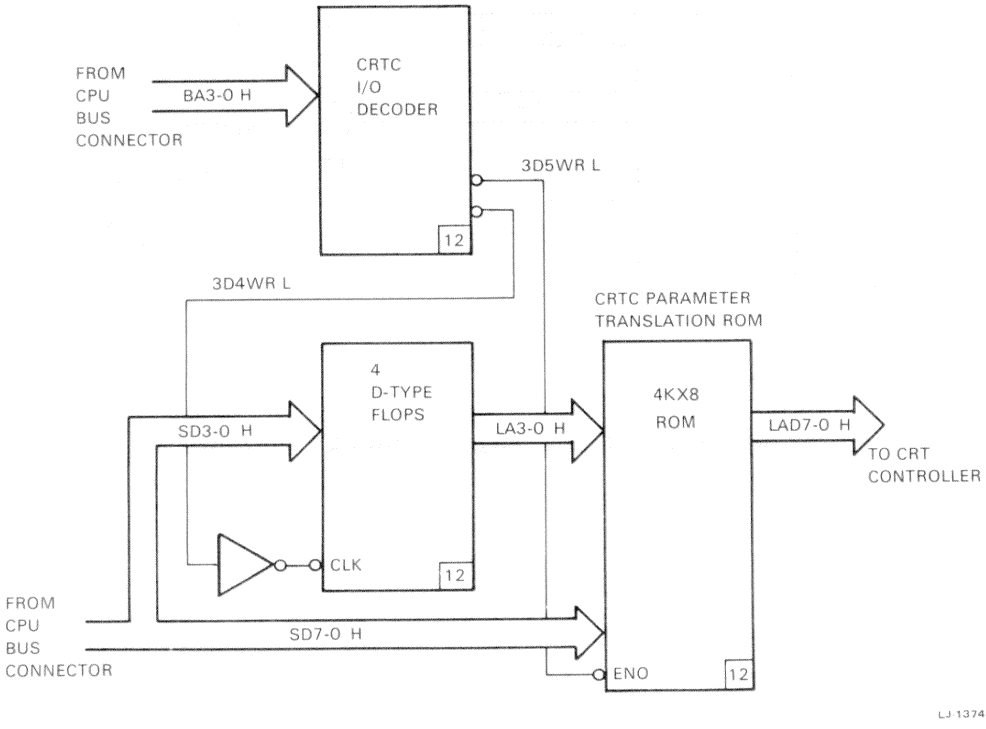


Figure 4-2 Translation Logic Block Diagram

4.2.2 CRT Controller

The CRT controller logic (Figure 4-3) addresses the internal registers of the video gate array. The data lines (LAD7-0 H) are bidirectional between the 6845 CRT controller and the video gate array. The memory address lines (CNMA12-0 H) go through three address multiplexers to directly address the video memory. The internal registers control horizontal and vertical positioning, synchronization, video and cursor starting addresses, and width of video display.

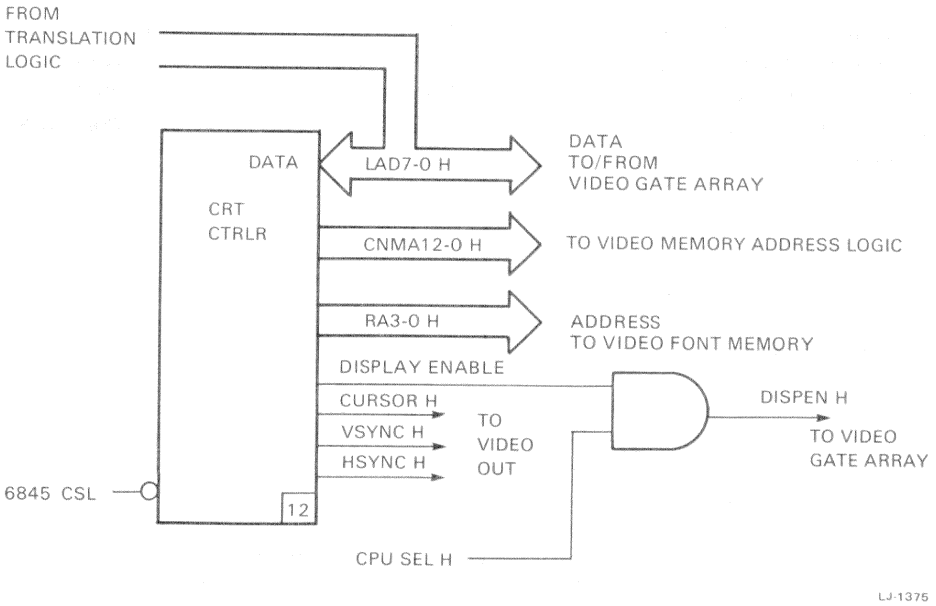


Figure 4-3 CRT Controller Block Diagram

4.2.3 Video Memory Address Logic

Both the CPU and the CRT controller can address the video memory by using the video memory address logic (Figure 4-4). The controller memory address (CNMA12-0 H) and the CPU address (SA8-5 H) are multiplexed in three 4 × 2 multiplexers. The output of these multiplexers is the video address (VA12-1 H), which goes to two 8K × 8 static RAMs. The VA0 H and VA13 H signals come directly from the video gate array. The 14 video address lines are multiplexed with each other to provide an 8-bit data address (DA7-0 H), which is the input to 16K × 4 dynamic video display memory (six DRAMs).

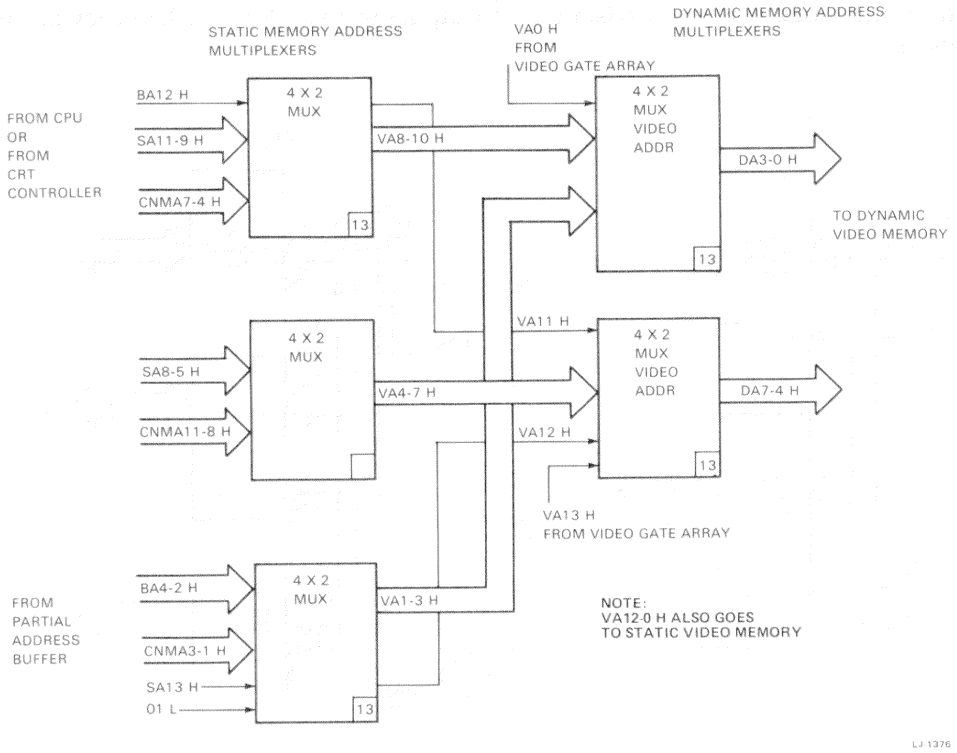


Figure 4-4 Video Memory Address Logic Block Diagram

4.2.4 Video Display Memory

The video memory (Figure 4-5) has 64 Kbytes: a 16 Kbyte static RAM and a 48 Kbyte dynamic RAM. Both memories receive inputs from either the CRT controller, or from the CPU, through the video memory address logic. The memory address space maps into the address space of the CPU. Other inputs to the dynamic video memory are row address strobe (RAS) and column address strobe (CAS). These inputs come from the video gate array through the video memory RAS/CAS drivers. These inputs determine the position of the data on the video screen.

The data enable signal (DATAEN L) determines if the data will be written into the dynamic video memory on the data lines (DA7-0 H). The XMEM H signal from the video gate array tristates the outputs of the DRAMs when they are not used.

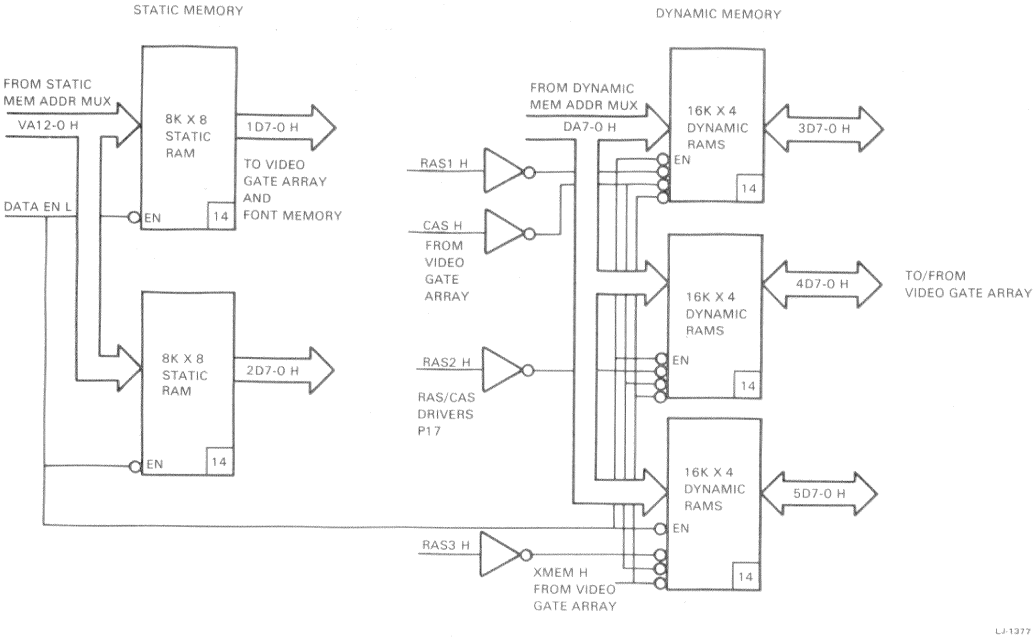


Figure 4-5 Video Display Memory Block Diagram

4.2.5 Video Font RAM

The video subsystem has a 4 Kbyte programmable font RAM (two 2K × 8 RAMs) for up to 256 character patterns. The font RAM select signal (FRS L) enables the octal driver to send SA11-5 signals from the CPU bus to the font memory.

The video font memory (Figure 4-6) contains two 2K × 8 bit RAMs, each with 256 characters contained in an 8 × 16 Digital-enhanced font matrix for text mode. The video gate array controls the video font memory using the font RAM select (FRS L and FRS H), buffered memory write (BMEMW L), font character set selections (FCS1 L and FCS2 L), and font output enable (FOE L) signals. This latter signal enables the bidirectional lines between the video font memory and the video gate array.

The octal D-type flip-flop stores the next character that is to be shipped to the screen.

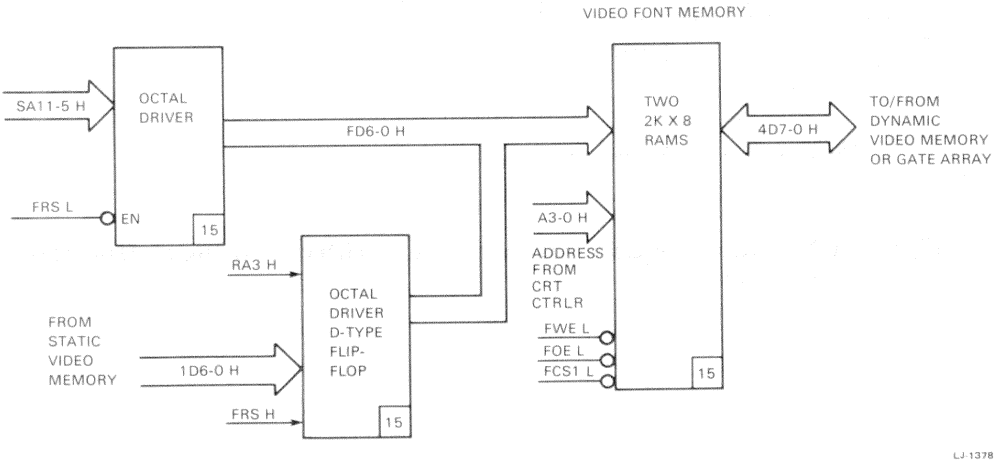


Figure 4-6 Video Font Memory Block Diagram

4.2.6 Video Decoder and Arbitration Logic

The video memory decoder (Figure 4-7) enables addresses B000H – C000H to be decoded. System address lines (SA19-15 H) are monitored to enable video memory (VMEM L). This decoder also monitors the refresh signal (REFRESH L) to disable VMEM L, which goes to the video memory arbitration logic.

The video memory arbitration logic determines priority levels for the CPU and the display processor to access memory. The refresh controller has priority to eliminate a snowy condition that may result on the screen.

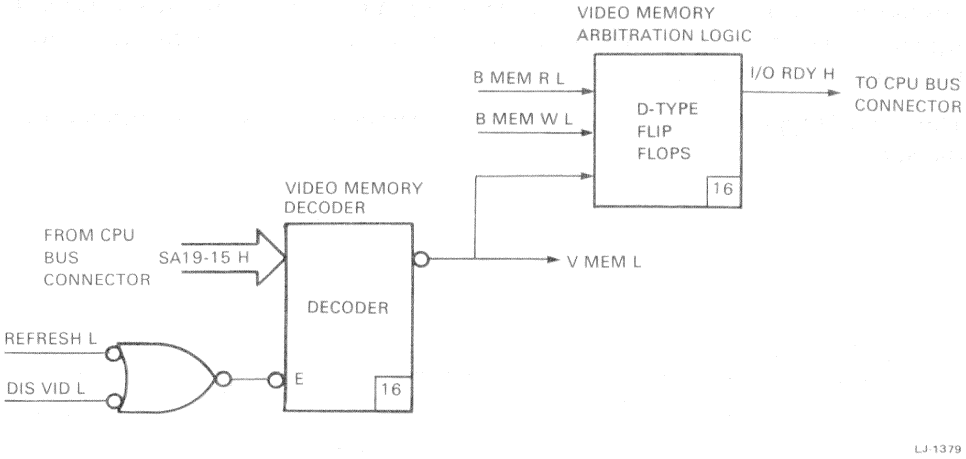


Figure 4-7 Video Memory Decoder and Arbitration Block Diagram

4.2.7 Video Gate Array

The video gate array (Figure 4-8) is a 144-pin, CMOS, Digital-proprietary gate array circuit that provides high reliability. The video gate array uses two external crystals for internal timing. The 27.977244 MHz crystal is used for Digital VT240 emulator mode; the 22.367195 MHz crystal is used for all other modes. The gate array provides many of the control signals and bidirectional lines for the various components of the video subsystem, and also provides the RAS and CAS signals for the video memory.

Within the video gate array is a video look-up table. This table is a 16-word RAM that allows you to rapidly select the color or intensity levels for the various modes of operation.

Also in the video gate array is a display processor that converts memory data into various raster formats, depending on the mode of operation. The display processor provides the output to the video output circuit.

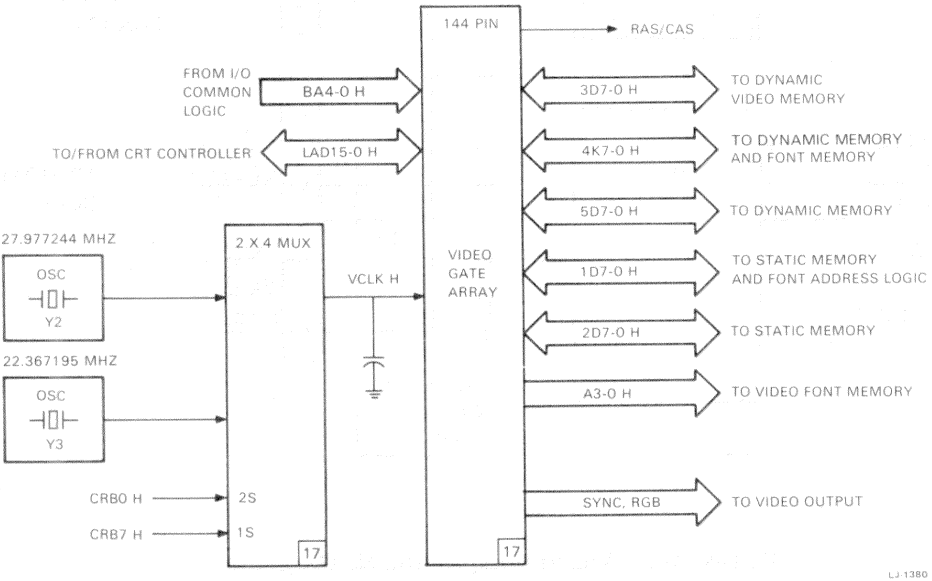


Figure 4-8 Video Gate Array Block Diagram

4.2.8 Video Output Circuit

The video output circuit (Figure 4-9) can drive either a monochrome or a color monitor. This circuit has an octal output driver, which provides the vertical and horizontal synchronization, the intensity, and the red, green, and blue (IRGB) signals to the monitor. The VAXmate monitor module contains the D/A circuits needed to convert the IRGB signals to up to 16 shades of gray. The series resistors and capacitors on the video output lines provide FCC filtering.

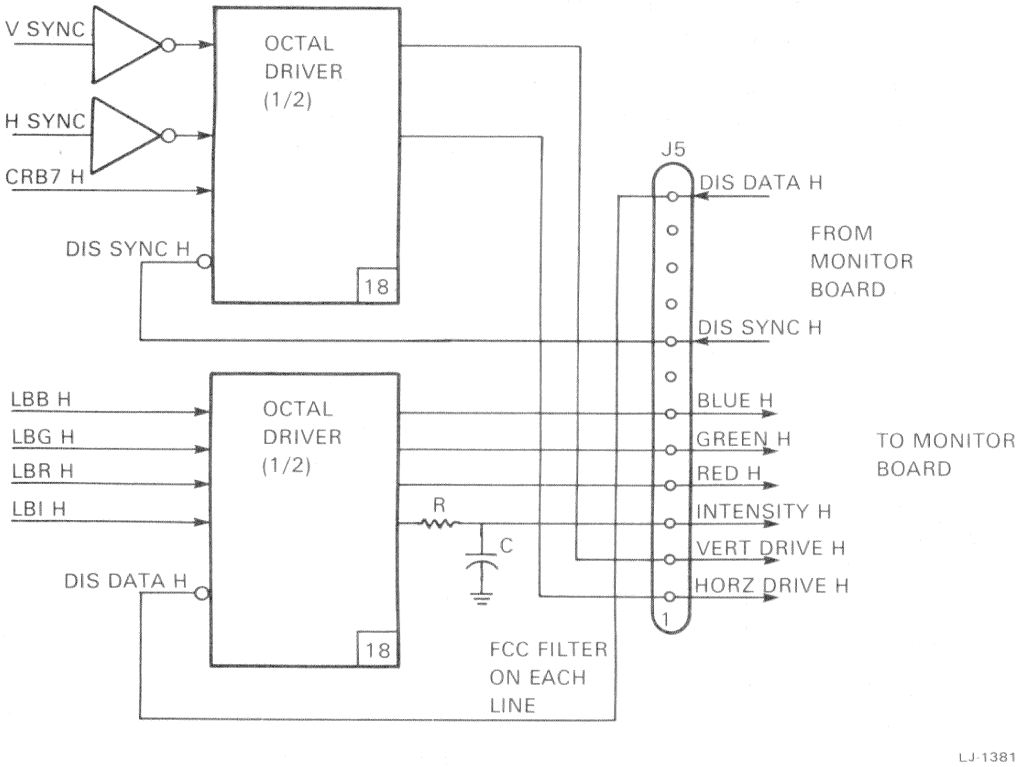


Figure 4-9 Video Output Block Diagram

4.3 Monitor Interface

Table 4-1 lists the monitor interface signals. These signals are applicable to either a monochrome or a color monitor. See Figure 4-10 for the monitor connector pin assignments on the monitor board.

Table 4-1 Monitor Interface Signals

Pin No.	Signal Description
1	Horizontal/Line sync (active low)
2	Vertical/Field sync (active low)
3	Intensity Video (active high)
4	Red Video (active high)
5	Green Video (active high)
6	Blue Video (active high)
7	400/250 select (low for 400 scans, high for 250 scans) Mode signal
8	(reserved)
9	Signal ground
10	+5 return
11	+5 Vdc (200 mA max.)
12	(spare)

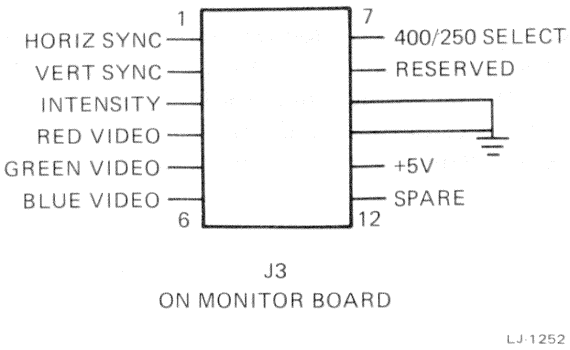


Figure 4-10 CRT Connector Pin Assignments

4.4 Monitor Board Technical Description

The PC500-M is a monitor sub-assembly for the VAXmate workstation. This subassembly (Figure 4-11) consists of a 340 millimeter (14 inch) CRT and yoke assembly, and a monitor board. The board receives operating voltages and signals from the system through two direct connections: J2 for power (+28 V, +12 V and −12 V), and J3 for intensity, red, green, and blue signals, mode, and +5 V. The output signals of the board (focus, cutoff, brightness, and video signals) go though the J4/P4 connector to P3 of the CRT. The scan currents go through J1/P1 connector to the deflection yoke. These connectors provide a strain relief when moving the internal tilt mechanism of the CRT. The monitor board contains the following.

- Phase-locked loop (PLL) line oscillator
- Voltage stabilizer
- Drive circuit
- Line sweep circuit with flyback transformer
- Field deflection system IC
- Video amplifier with 4-bit digital-to-analog converter (DAC)

The user can adjust the CRT brightness and contrast for personal preference, and through software, can switch the height between the 250 and 400 line modes.

> ***CAUTION***
> The components in this description are for the monochrome monitor circuit schematic (54-16828-0-1) in the PC500 Field Maintenance Print Set (MP02252-01). A new monitor board will have etch circuitry on both sides of the board, and may have components labeled differently. Remember that high voltages are present in the system.

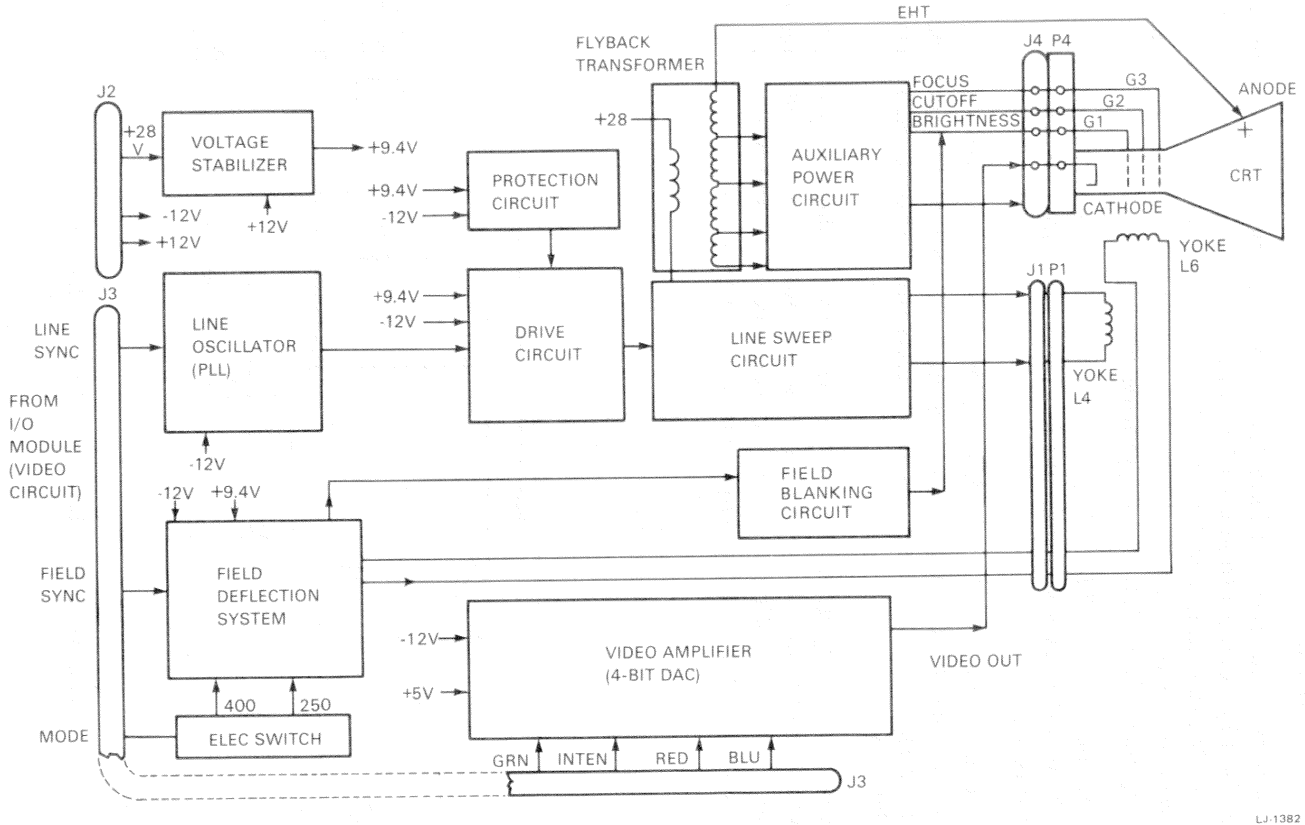


Figure 4-11 Monochrome Monitor Block Diagram

4.4.1 Line Oscillator

The monitor uses a phase-locked loop (PLL) line oscillator IC (E1). The circuit (Figure 4-12) operates from a −12 V supply, for ease in connecting to the drive circuit. The device has an internal shunt regulator so that all components between pin 6 and 2 are at the regulated voltage. R1 sets the current for the shunt regulator; R10, C1, and C2 provide decoupling.

The line sync pulse is at a TTL voltage level and is active low. R5 terminates the line, C3 provides level shifting, and R4 limits the current to the synchronizing input of E1.

The timing components for the oscillator are horizontal hold control R6, R7, and C6. R6, R7, and R8 determine the loop gain. C4, R9, and C5 determine the dynamic response of the loop. R8 also affects this response. R14 and C8 generate the ramp.

R14 is the external ramp generator for the PLL. R14 is connected to the high voltage flyback pulse, and acts as a current source for C8, thus producing a linear ramp. C7 is a coupling capacitor between the ramp and pin 4. R2 and R3 control the duty cycle of the output pulse and set the off time at 15 μs.

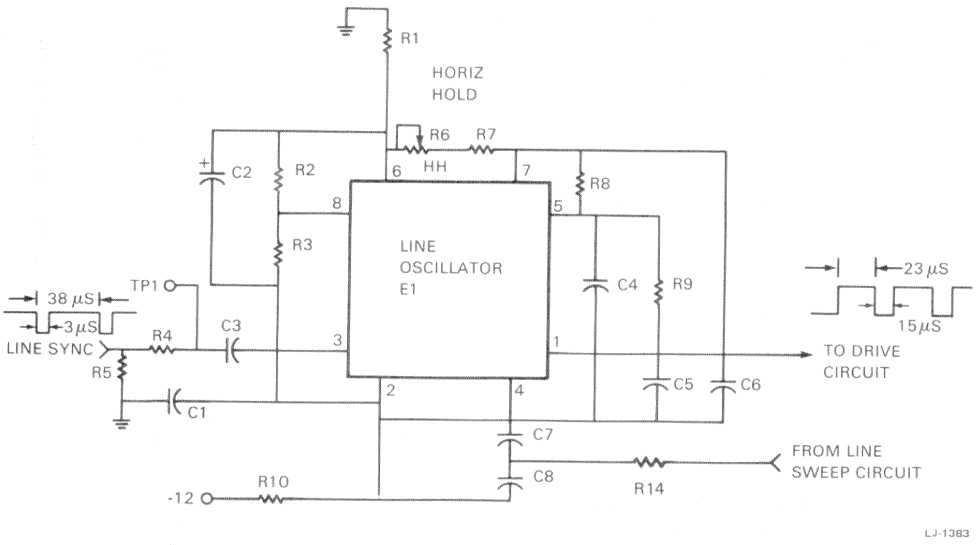


Figure 4-12 Line Oscillator Circuit

4.4.2 Drive Circuit

The purpose of the drive circuit is to properly switch Q6 in the line output stage. (Q6 is shown in Figure 4-13 for clarity.) The drive circuit uses the stable +9.4 V to drive the line sweep circuit. The line sweep circuit uses a push-pull transistor circuit for accuracy in setting drive current. This circuit is used instead of a transformer, which would have variations due to pulse width changes, inductance changes, or small voltage changes.

The base current necessary for Q6 saturation is 50 mA for about 23 μs. The reverse current to turn off Q6 is much larger, but this current lasts for a shorter duration. Worst case values are 1 A for 1 μs. Typical current pulses will be about 600 mA. Q3 is capable of handling this surge.

Assume the protection circuit with Q1 is on. When pin 1 of E1 is high, Q2 is on and receives base current from R11. R12 sets the drive current to the base of Q6. Because of the accuracy of this arrangement, the drive current can be close to an ideal value. This reduces overdrive, provides shorter storage time, and creates lower dissipation in Q6.

When E1 pin 1 goes low, Q2 turns off and Q3 turns on, pulling the Q6 base charge out very quickly because of the very low resistance path to the −12 V supply. At this time, the base of Q6 is a few volts below ground level.

Q1 and its associated circuitry provide protection for E1 and Q6, and act as a gate to remove drive power in case the +12 V or the −12 V supply is not working. If this circuit was not present when the −12 V supply was low or missing, Q6 (a Darlington transistor) would be turned on and draw excess power from the +28 V line. D2 sets the operating voltage for the gate. R16 sets the base current to Q1. R15 ensures that Q1 will stay off when the −12 V is low.

If the +12 V goes low, the drive would be removed, but the emitter base voltage of Q6 would exceed the specification. R17, in combination with R13, prevents excess reverse voltage across the base emitter of Q6. This is necessary if the +12 V line is low, or during turn on and turn off transient conditions. R13 also limits the peak current that E1 must sink.

R69 and R71, along with C46, decouple the +28 V line for the flyback transformer, and provide some regulation.

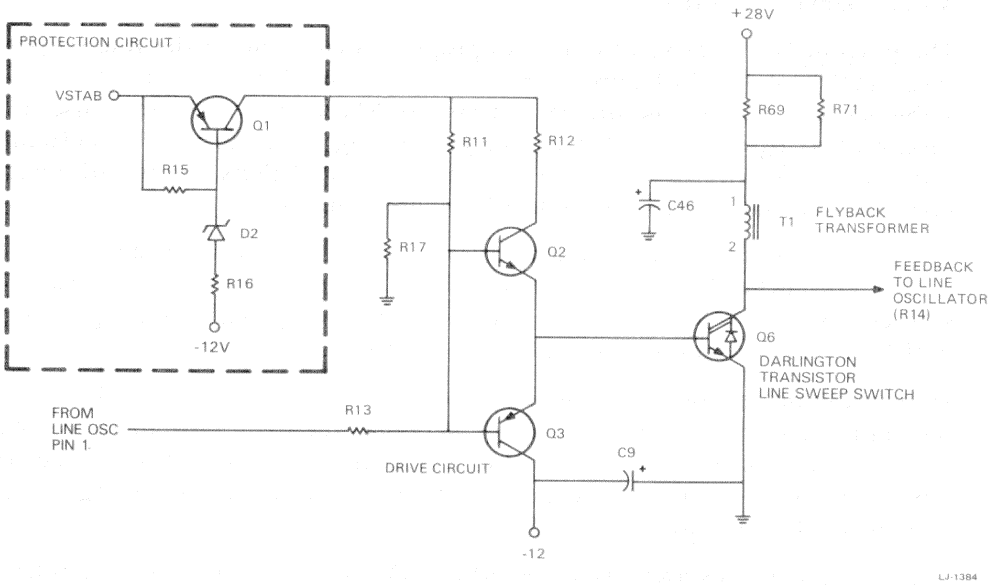


Figure 4-13 Drive Circuit

4.4.3 Line Sweep and Auxiliary Power Circuit

The line sweep circuit (Figure 4-14) is a conventional type that uses a third harmonic tuned flyback transformer (FBT). The main requirement of the line sweep circuit is to produce a 6 A (peak-to-peak) saw-tooth current in the deflection yoke (L4). The circuit's secondary requirement is to produce auxiliary voltages for the monitor.

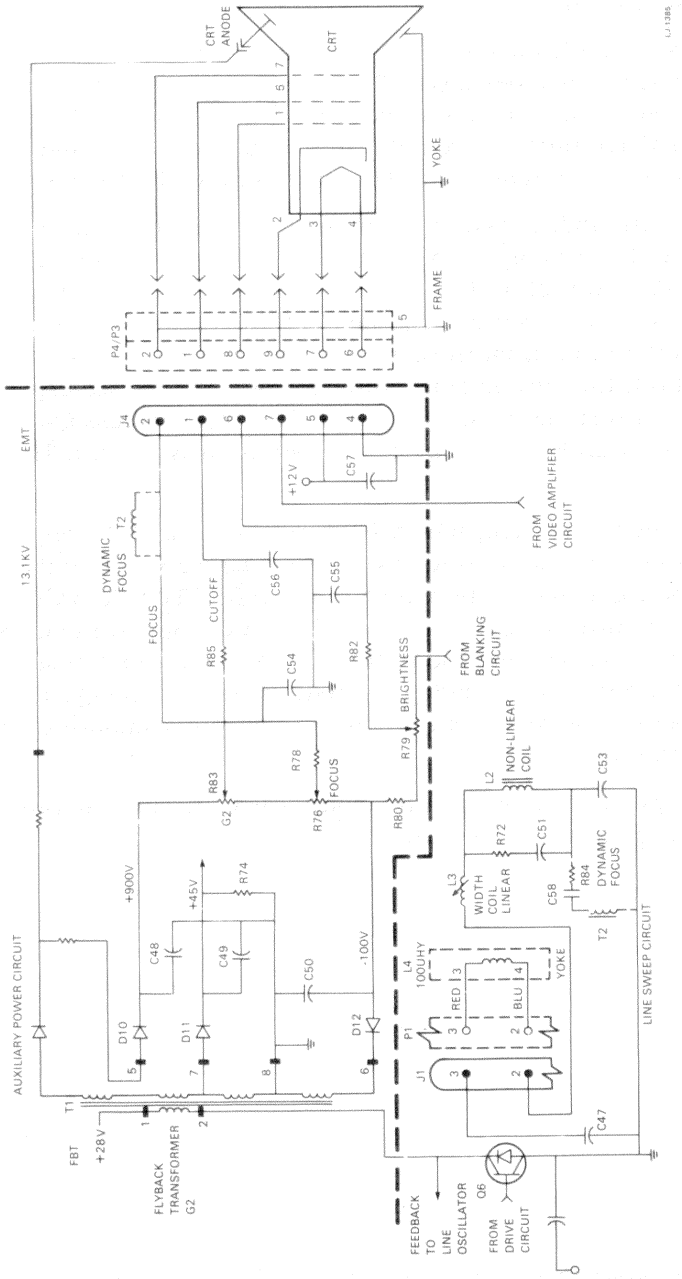


Figure 4-14 Line Sweep and Auxiliary Power Circuit

4.4.3.1 Line Sweep Circuit

The line sweep circuit's main switch is the Darlington* transistor (Q6), which includes an internal damper diode. This circuit has a retrace time of 6.8 μs at the ac zero point. This time gives adequate overscan of the active video, while keeping the flyback pulse at around 200 V. A nonlinear coil and an S-capacitor provide linearity correction. A conventional width coil provides width control.

Lt equals the total inductance of the yoke (L4), the width coil (L3), and the nonlinear coil (L2) (Figure 4-15). Assuming Q6 is on, current flows from C53 through Lt, Q6, and back to C53. Because the time constant is longer than the sweep time, the yoke receives a constant voltage, and produces a linear ramp, which moves the beam from the center of the screen to the right side. When Q6 is turned off, the current flows through C47, the retrace cap. The circuit resonates with a very short time constant. The voltage across Q6, its internal diode, and C47, builds up to a peak and then returns to zero. This is the flyback pulse.

During this time the current, which is phase shifted by 90 degrees, goes from its maximum positive value to its maximum negative value, and moves the beam from the right side of the screen to the left. When the voltage at the collector tries to turn negative, the diode in Q6 clamps it, the circuit returns to its long time constant, and the beam is moved from the left side toward the center. The current is now flowing through the diode, and Q6 can be turned on anytime before the center of the screen to ensure a smooth change from the diode to the transistor.

R72 and C51 provide damping of the nonlinear coil. This damping prevents ringing from appearing on the screen.

* New monitor boards may have a MOS FET instead of a Darlington transistor (or may have a diode connected to a winding on the flyback transformer) for faster response.

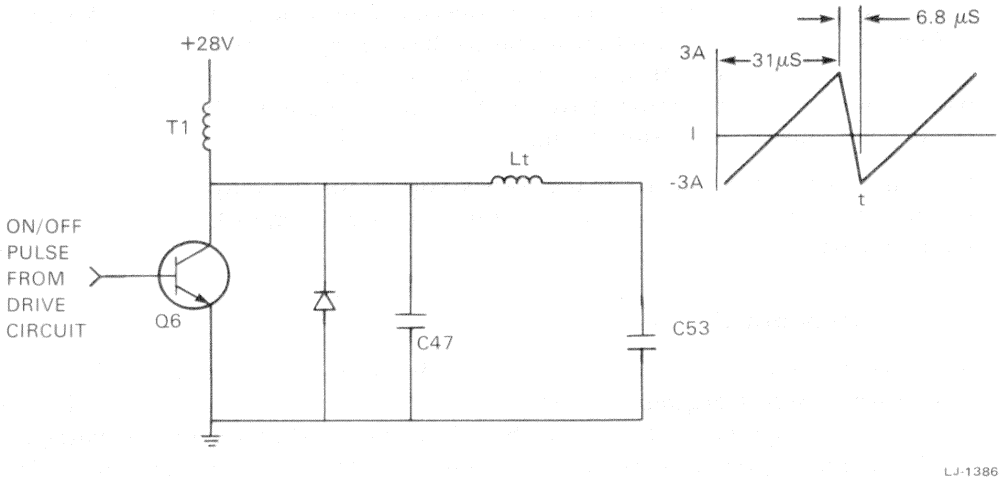


Figure 4-15 Simplified Line Sweep Circuit

4.4.3.2 Auxiliary Power Circuit

The flyback transformer produces auxiliary voltages as follows.

Voltage	Destination
+13.1 kV @85 µA max	CRT anode (EHT)
+950 V @200 µA	G2 and G3 (Cutoff and Focus grids)
+45 V @75 mA max	Video output
−100 V @1.2 mA	G1 (Brightness); G2 and G3

The flyback transformer includes the rectifier and the bleeder resister for the extremely high tension (EHT) lead. Also, there is a resistor in series with the EHT lead that helps suppress peak current when the CRT has a flashover.

D10 and C48 are the rectifier and filter for the +950 V supply, and D12 and C50 provide the same function for the −100 V supply. The 1000 V is divided in half by R83 and R76, which supply the bias voltage to the CRT for cutoff and focus. R78, R85, C54 and C56 provide decoupling and protection. (On new circuit boards, T2 adds dynamic focus.)

The divider for the brightness control consists of R86, R79, and R80. Assuming Q8 is saturated, the brightness control has a range from −13 V to −60 V. The −13 V allows a cutoff to be set for the tube, and the −60 is adequate to darken the tube at maximum drive level. This range allows the user to precisely adjust raster extinction by adjusting the brightness control.

D11 and C49 rectify and filter the +45 V supply for the output stage of the video amplifier. R74 is a bleeder resister, which discharges C49 primarily for safety reasons.

4.4.3.3 Dynamic Focus

New monitor boards have the provision for dynamic focus. Figure 4-16 shows a simplified circuit diagram of this circuit. The sawtooth current through C53 produces a voltage parabola across C53. T2 inverts and increases this voltage parabola, and applies it to G3 in series with the static focus control, R76. This focus control allows the fixed 300 V parabola to be moved between 0 V and 400 V. R84 damps any ringing from showing up on the display, and C58 blocks the dc component.

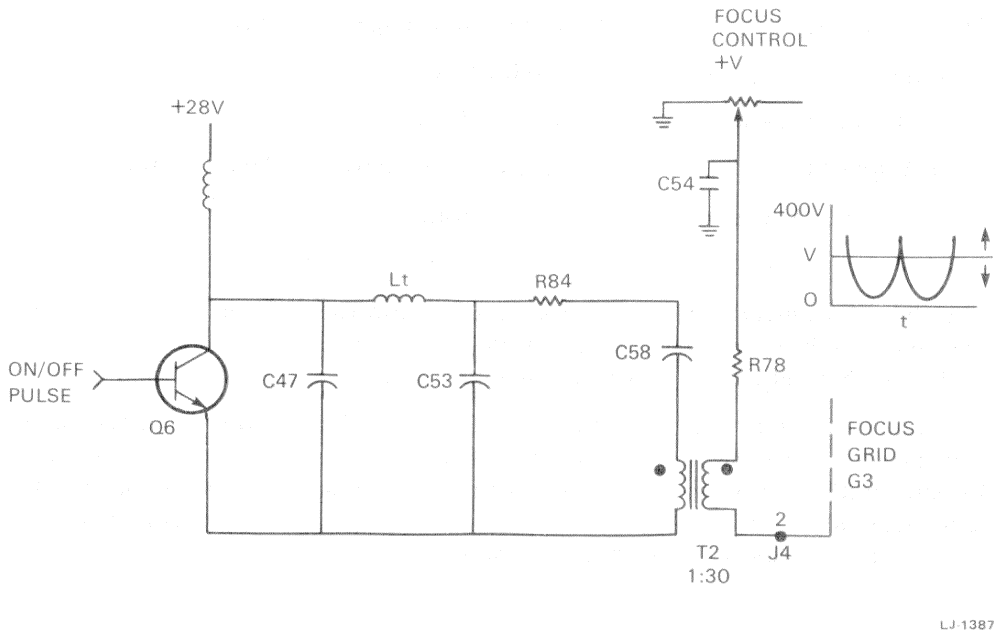


Figure 4-16 Simplified Dynamic Focus Circuit

4.4.3.4 Blanking Circuit

Q8 blanks the field retrace lines by negatively shifting the G1 grid by about 20 V. When Q8 is on, it shunts R81. A pulse from the field deflection circuit turns off Q8 and adds 47 K ohms to the G1 divider chain, thus moving G1 more negative, cutting off the CRT during field retrace. Because the cutoff control limits the maximum brightness to about 5 (ft-Lamberts), you cannot advance the brightness control far enough to make the retrace lines visible. (Specific components around Q8 change for new revision boards, but the function of the circuit remains unchanged. See Figure 4-17.)

4.4.3.5 New Blanking Circuit

When Q8 is off, the bottom of C59 is almost at ground. A pulse from the field deflection circuit turns Q8 on and pulls the bottom of C59 to −12 V. Because C59 is large, the top also moves 12 V and pulls G1 more negative by 12 V, blanking the screen during retrace. R81 keeps C59 near ground, and D14 protects the circuit during CRT flashover. C55 provides additional decoupling.

D14 prevents the base emitter junction of Q8 from being reversed biased. R82 and C55 provide decoupling and protection; however, the time constant is much shorter than the other grids, so the blanking pulse is not distorted.

All the bias voltages go to the CRT through J4, P4 and P3. J3 also contains spark gaps for protection.

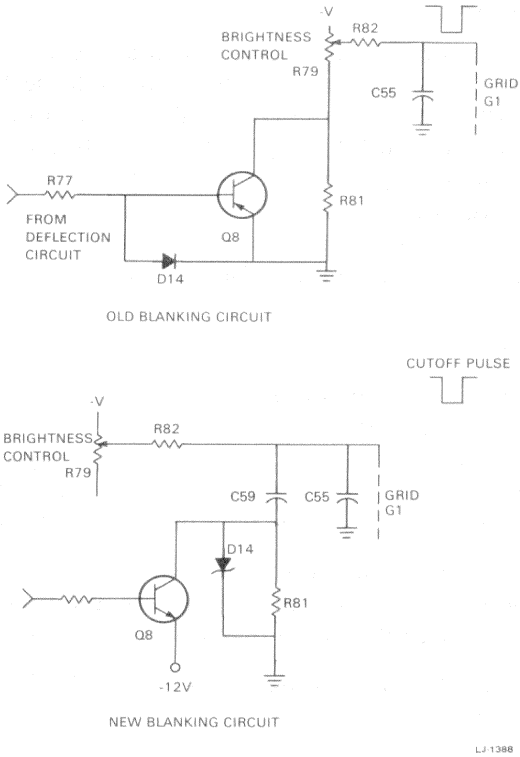


Figure 4-17 Blanking Circuit

4.4.4 Field Deflection

A specially packaged IC (E2, Figure 4-18) provides all operations for field deflection, including direct driving of the yoke. The device uses both the stable +9.4 V and the −12 V supply. The external components are used for setting bias, gain, linearity, and free run frequency.

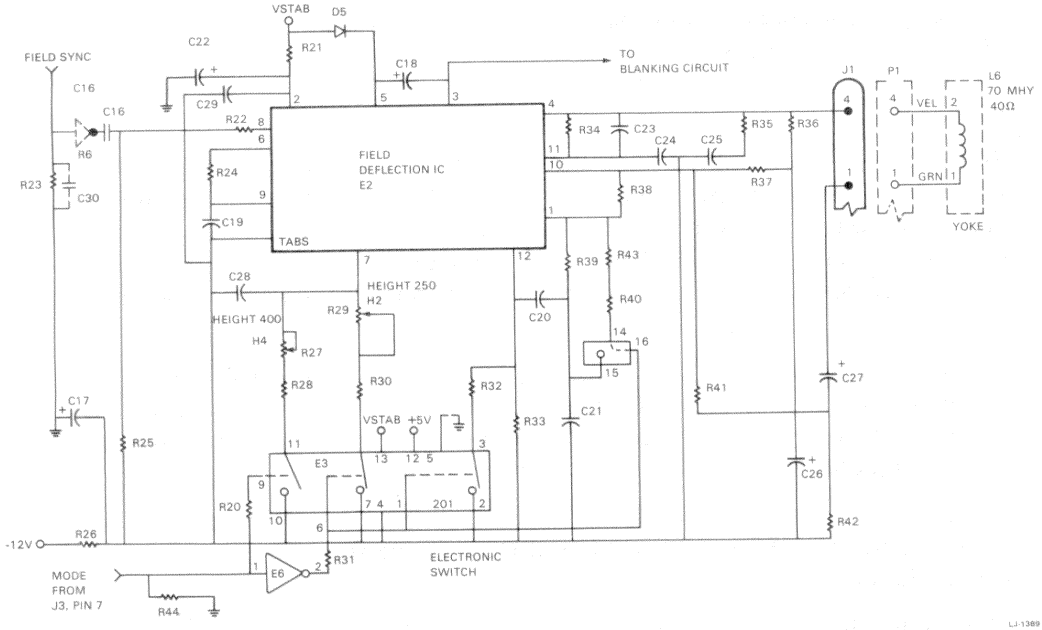


Figure 4-18 Field Deflection Circuit

In addition, the circuit has an electronic switch for software selection between 400 and 250 line video display modes. When the mode signal is on, the switch changes to another height control and corrects linearity. Adjustable resistor R27 (Height 400) controls the amplitude of the display in 400 line mode; R29 (Height 250) controls the amplitude of the display in 250 line mode. C28 decouples any noise coming from the height controls.

R24 and C19 control the internal oscillator frequency. Since the monitor operates at a refresh frequency of only 60 Hz, no adjustment control is necessary. The oscillator controls a ramp generator, which provides a linear ramp output (pin 12) and a buffered ramp (pin 1).

R33 gives the linear ramp a slight curve, which goes to the linearity capacitors C20 and C21 to produce a C curve. R39 adds this curve to the ramp at pin 1, which produces an S curve necessary for proper linearity on the CRT. R38 applies this S curve to the output stage. The 250 line mode switches R33 in parallel to R32 and switches R39 in parallel to R40 and R43 to ensure the correct linearity.

The output stage resembles a power operational amplifier (op-amp). The noninverting input connects internally to a 2.2 V reference. The inverting input is pin 10, and the output is pin 4. The main difference between this circuit and a conventional inverting op-amp circuit is that this circuit uses current feedback.

R42 samples the current through the yoke (L6) producing a voltage, which R41 (the summing point) applies to pin 10 of the op-amp. The op-amp compares this voltage to the other input at pin 10, which comes from pin 1 and the linearity circuit through R38. Thus, the feedback current controls the loop. These resistors are the primary means of setting the gain of the output stage.

A resistive divider made up of R36, R37, R41, and R42 controls the dc bias for the output stage. Bias at pin 4 is set around 300 mV, with respect to ground. C27 couples the signal to the output. C26 filters the ac signal at pin 4 for dc feedback and provides some linearity corrections.

Pin 3 connects to the base of Q8 for blanking. Pin 11 ensures stability of the circuit, with R34, R35, C23, C24, and C25 setting the amount of compensation.

The stable +9.4 V connects to pin 5 as the supply voltage for the output stage. D5 prevents the high voltage from the flyback generator from feeding back. C18 is the voltage doubler capacitor for the flyback generator within the IC, providing a faster retrace time.

The field sync signal is at TTL voltage levels. R23 terminates this signal. C16 provides level shifting of the synchronization signal to a −12 V level, and R22 provides current limiting. R25 provides a dc return path, as well as some noise immunity. R21, C22, R26, and C17 provide decoupling from the power supply. (New monitor boards have an inverter and a capacitor at the field sync input to reduce screen bounce while switching video modes.)

4.4.5 Video Amplifier

The video amplifier (Figure 4-19) consists of a power output stage and a four bit digital-to-analog converter (DAC) in one circuit. This arrangement provides accurate control of biasing and drive levels for the output transistor, as well as TTL interface and dc gain control for the video signals.

The DAC is a weighted-current, multiplying converter. It is built out of discrete transistors on two ICs, E4 and E5. Each bit contains an active current source and a differential switch. Each current source is set by a resistor and is adjustable by the contrast control.

R64, R63, R57, R56, and R54 set the maximum current for each bit. R63 and R64 are parallel, to reduce the power in the resistors. The maximum current for green, red, blue, and intensity is 40, 20, 10, and 5 mA respectively. R62 keeps the output stage conducting when there is no video signal.

E6 buffers and inverts the video signal, and controls the differential switch. When the input to E6 is high, indicating there should be light on the screen, the differential switch sinks current from Q10. The current also flows through L1 and R61, and generates the video voltage that goes to the cathode of the CRT. If the input to E6 is low, the switch sinks current from the +5 V supply.

R49 controls a dc voltage, which varies the current of each bit simultaneously, thus controlling contrast.

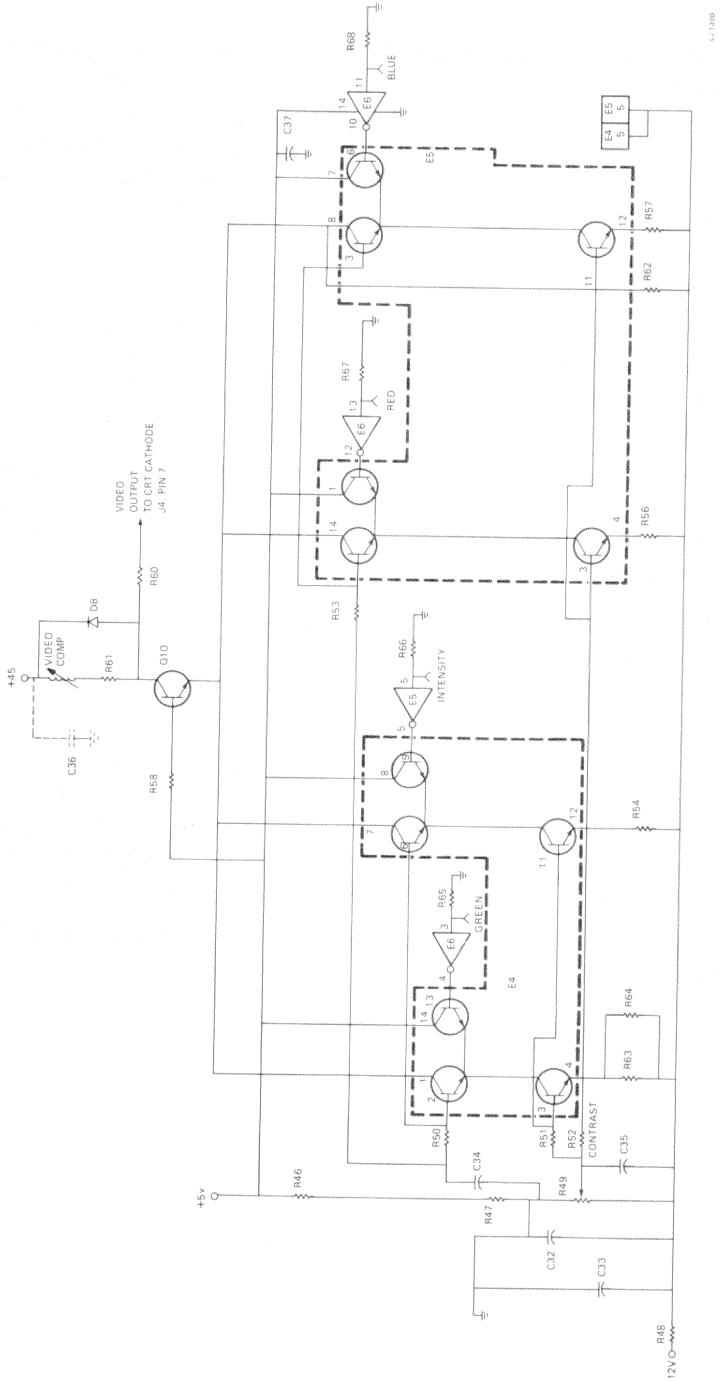


Figure 4-19 Video Amplifier Circuit

D8 and R60, on the collector of Q10, protect the monitor from any damage from a tube flashover. Video compensation L1, a variable inductor, compensates for the capacitance of the tube and its leads.

R46 and R47 eliminate glitches by setting the reference voltage on the differential switch to accommodate for the nonsymmetrical slew rate of E6.

R49 is the contrast control. R50, R51, R52, R53, and R58 are used to prevent high frequency oscillations. R65, R66, R67, and R68 terminate the TTL lines. R48, C33, C32, and (C36 on new boards) provide decoupling of the DAC.

The substrate of E4 and E5 connects to the −12 V supply.

4.4.6 Voltage Stabilizer

The stabilizer Q12 (Figure 4-20) and its associated circuitry use the +12 V line to provide a stable +9.4 voltage. This circuit is an emitter follower that uses a 10 V Zener diode (D15) as a reference. The current source for the Zener comes from the +28 V line. C60 and C61 provide decoupling.

The stabilizer output goes to the drive circuit and the field deflection circuit.

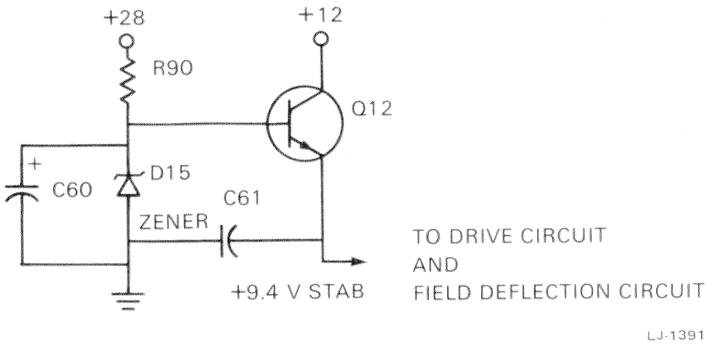


Figure 4-20 Voltage Stabilizer Circuit

Chapter 5
Diskette Drive Controller

5.1 Introduction

The diskette drive controller logic provides the interface between the VAXmate system bus and the VAXmate diskette drives. The controller converts binary data from the CPU module into modified frequency modulated (MFM) serial data that is transmitted to a diskette drive and recorded on the diskette. MFM is a magnetic recording method for diskette drives that encodes a clock signal into the MFM flux transitions recorded on the diskette. When data is read from the diskette, the controller recovers the clock and data signals by using a clock separator and data separator.

Figure 5-1 illustrates the controller position in the VAXmate system. The diskette drive controller logic contains a floppy disk controller (FDC), three internal registers, timing logic, address logic, data and control logic that connects to the diskette drive, and common logic that connects to the CPU module (Figure 5-2). The PC500 I/O board drawings on sheets 3 through 8 of the Engineering Print Set illustrate the diskette drive controller logic.

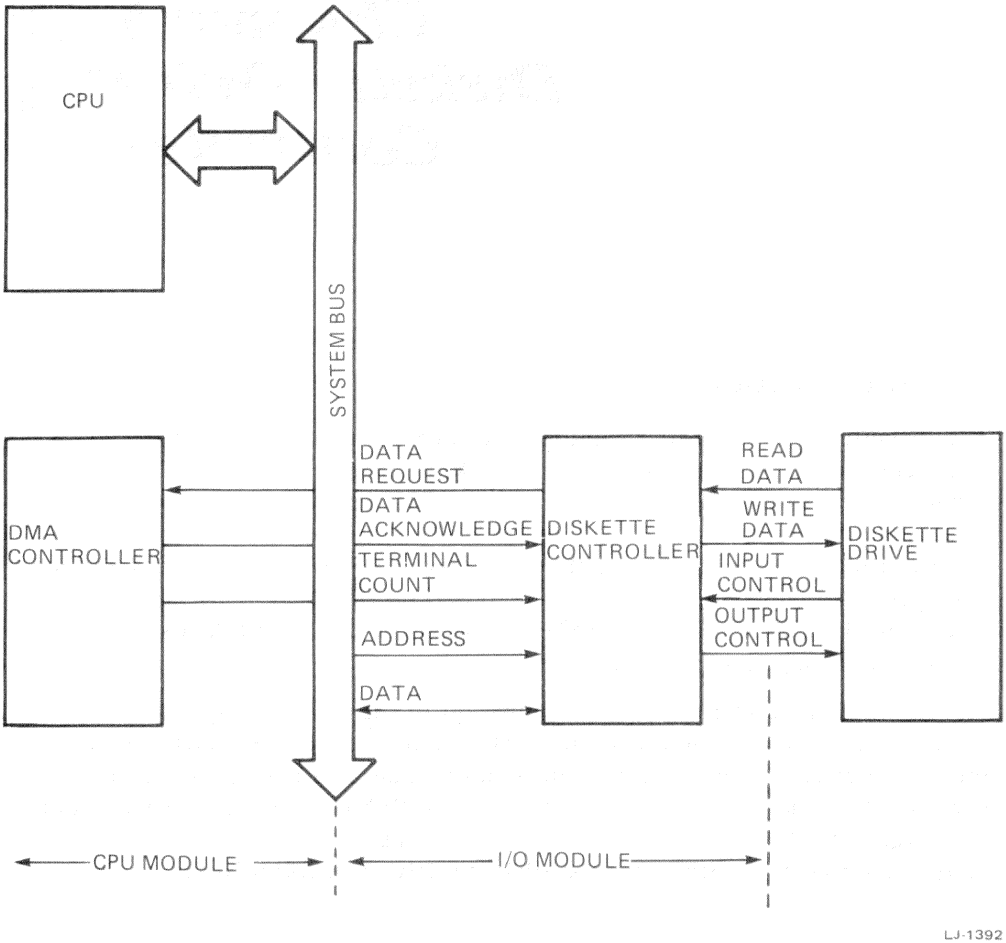


Figure 5-1 Diskette Controller – CPU Interconnect Block Diagram

5.2 Operation

The controller supports 5-1/4 inch, high-capacity diskette drives with standard (800 Kbyte) or high capacity (1.2 Mbyte) media. The diskette controller operates in either DMA or non-DMA mode. It uses DMA mode to transfer data to and from the system memory. In DMA mode, the processor issues the command to the diskette controller, and the diskette controller and system DMA

controller implement the data transfer. In non-DMA mode, the diskette controller generates interrupts to the processor each time the controller transfers a data byte.

5.2.1 Diskette Drive Controller Connector

The Diskette Drive Controller Connector (PC500 I/O Board in the Engineering Print Set, Sheet 4) connects the diskette drive controller to the diskette drive. The signals associated with the connector are used for motor control, reading data, and writing data. Table 5-1 lists the functions of these signals.

Table 5-1 Diskette Drive Connector Signals

Signal	Function
FD HD SEL 1 H	Selects diskette drive Head 1 or Head 0. Head 1=(1), Head 2=(0)
FPU H	The enable gate for control signals to the diskette drive.
FD WR EN H	Enables write data to the diskette drive.
WR DATA H	Data to be written on the diskette.
FD STEP H	Stepping pulses that step the head to the next or previous track based on FD DIRECTION H.
FD DIRECTION H	Provides the stepping direction of the read/write heads. When this signal is high, the heads step in (towards the center).
FD MOTOR A ON L	Selects diskette motor drive A.
FD MOTOR B ON L	Selects diskette motor drive B.
FD DRIVE B SEL L	Selects diskette drive B logic.
FD DRIVE A SEL L	Selects diskette drive A logic.
SEL 500 L	Provides data transfer rate as determined by SD0 and SD1.
FD DC H	Signal from drive logic indicating that the diskette drive door has been opened.
FD RAW DATA H	Data and clock information read from the diskette.
FD WR PROT H	Write protect status in read/write mode.
FD TRK0 H	Indicates that the read/write head is on track 0 (zero) of the diskette.
FD IDX H	Index pulse signal indicating the beginning of a track on the diskette.

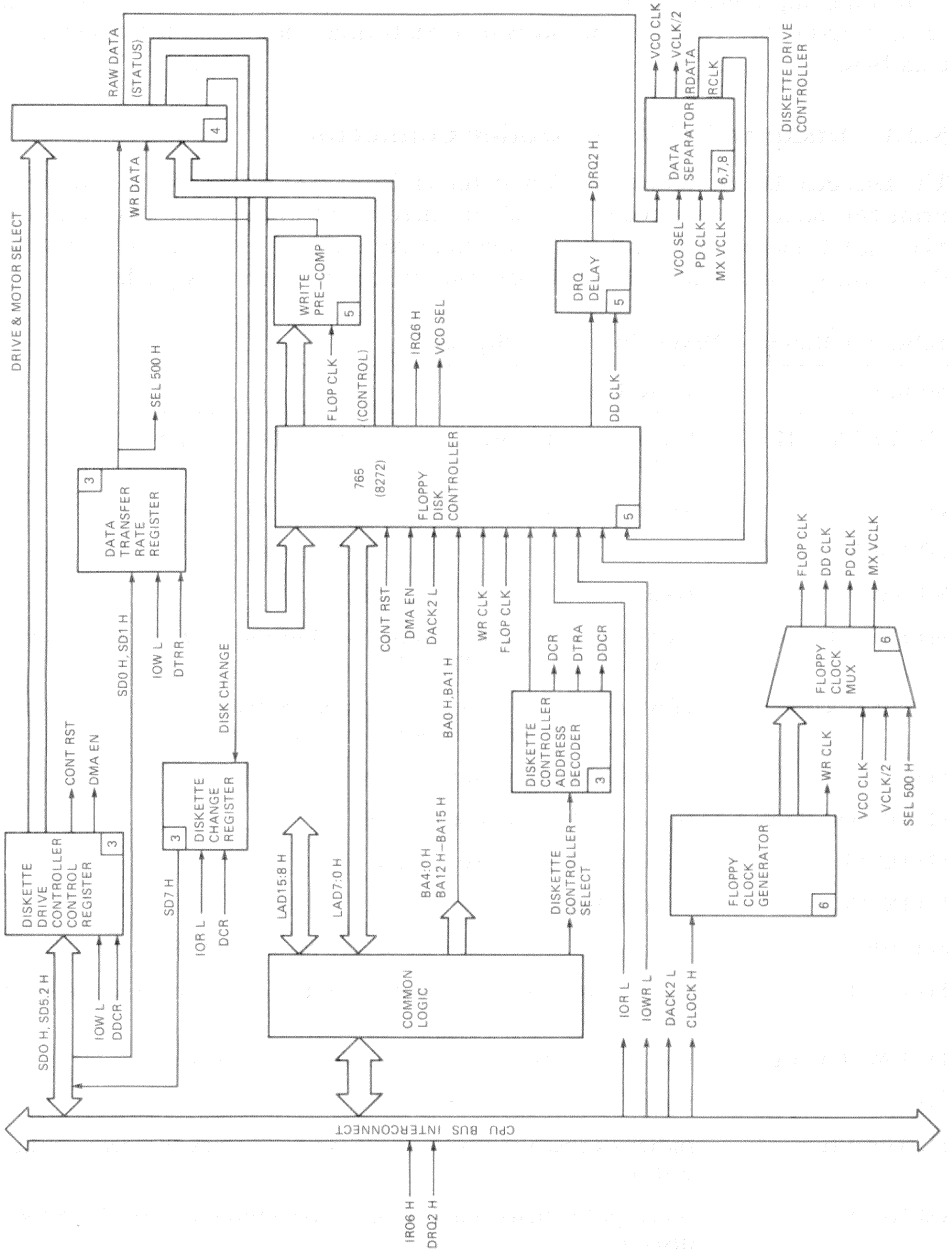


Figure 5-2 Diskette Drive Controller Block Diagram

5.2.2 Diskette Clock Generator

The 8 MHz clock signal from the VAXmate CPU timing logic is issued to the floppy clock generator (Sheet 6, E73), where the required timing signals for the diskette logic are generated. Outputs from the clock generator are fed to the floppy clock multiplexer (Sheet 6, E67).

5.2.3 Diskette Clock Multiplexer

Clock outputs from the floppy clock multiplexer select the clock signals required for timing by the data separator, DMA request logic, delay data logic, pre-compensation logic, and the floppy disk controller.

5.2.4 Address Decoder

The Buffered Address BA2-0 provides the address for the diskette drive controller. The DISK SEL command decodes the I/O address. The addresses are as follows.

BA2-0	Function
010	Select control register
100	Select floppy disk controller
101	Select floppy disk controller
111	Write: Data transfer rate register Read: Diskette change register

5.2.5 Floppy Disk Controller

The floppy disk controller (FDC) is a 40-pin LSI chip (Sheet 5, 8272A). The FDC provides the control functions and circuits to connect the RX33 diskette drives to the VAXmate CPU module. Write data (FD WR DATA H) is developed from data bus inputs (LAD7-0). Input control signals include track information, read and write commands, clock, chip select, and other parameters. Output signals include write data, write enable, step control, pre-compensation status (early, normal, late), and head select. A complete description of the 8272A can be found in the Intel data sheets.

5.2.6 Write Pre-Compensation Logic

MFM recording produces undesirable shifting of the peaks of adjacent flux transitions on the diskette. This causes the MFM flux transitions to move from where they had been written. MFM encoding causes write pre-compensation (pre-comp) logic to shift the write data in an opposite direction than expected by the peak shift of the the read voltage waveforms.

The write pre-comp circuit (Sheet 5) determines when the write data should be delayed. The delay determination is based on what diskette track is being written.

5.2.7 DRQ Delay

The DRQ delay logic (Sheet 5) compensates for timing mismatches within the controller logic. Data DMA request signal DRQ is clocked by the DRQ delay clock signal DRQ DLY CLK H, and is enabled onto the bus by the diskette DMA enable signal FD DMA EN L.

5.2.8 Data Separator

The purpose of the data separator is to extract the clock signal from the input data, and provide decoded data. It does this by taking the phase difference between the existing data and decreasing this phase relationship by increasing or decreasing the clock. A voltage is created as a function of this phase difference between data and clock. This voltage provides feedback to the voltage control oscillator in a closed loop system. The level of this voltage determines the frequency of the VCO clock, and in turn, the phase relationship of data and clock. (See Engineering Print Set (PC500 I/O Board, Sheet 8.))

5.2.9 Diskette Controller Registers

There are five 8-bit registers associated with the diskette controller. Three of the registers are contained in the diskette control logic, and two registers are inside the controller chip. The processor can access all these registers. The three control logic registers include the Control Register, Data Transfer Rate Register, and Change Register.

5.2.9.1 Control Register

The control register is a write only register that selects diskette drives, turns on the drive motors, enables and resets the diskette controller chip, enables diskette DMA mode, and enables interrupts to the system processor. The specified system data bus signals (SD 5-2,0) are latched in the register flip-flops (Sheet 3, E96). System reset (BRESET H) clears all control register bits. The control register bit descriptions are as follows.

Control Register (03F2H)

7	6	5	4	3	2	1	0
0	0	MOTOR B	MOTOR A	DMA ENABLE	RESET	0	DRIVE SELECT

Bit	Description
7-6	Not used
5	1 = Turn on motor of Drive B. 0 = Turn off motor of Drive B.
4	1 = Turn on motor of Drive A. 0 = Turn off motor of Drive A.
3	1 = Enable DMA request, DMA acknowledge, and interrupt request to system microprocessor.
2	1 = Enable FDC chip. 0 = Reset FDC chip.
1	Not used
0	0 = Select Drive A 1 = Select Drive B

5.2.9.2 Data Transfer Rate Register

As mentioned previously, the diskette controller supports a 5-1/4 inch diskette drive and media. The 5-1/4 inch drive has a data rate based on two different motor speeds (low and high). Low speed uses standard media, and operates at

a data transfer rate of 250 KBit. High speed mode requires high capacity media, and operates at a 500 KBit data transfer rate. System data bits SD0 and SD1, when written to the data transfer rate register, determine the data rate. The bit descriptions are as follows.

Data Transfer Rate Register (03F6H)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TRANSFER RATE	

BIT	DATA TRANSFER RATE
1 0	
0 0	500 KBit
0 1	250 KBit
1 1	Not used (default to 250)

NOTE
250 KBit is the power-up default data transfer rate.

5.2.9.3 Diskette Change Register

The change register is a read only register that provides the real time status of the diskette change input from the selected diskette drive. Bit 7 (SD 7, sheet 3) is set by FD DC H (from the drive logic) when the diskette door has been opened, indicating the diskette has possibly been removed or changed. The change register is as follows.

Change Register (03F6H)

7	6	5	4	3	2	1	0
CHANGE STATUS	0	0	0	0	0	0	0

Bit	Description
7	0 = no change 1 = door has been opened, diskette possibly removed or changed

5.2.10 FDC Chip Internal Registers

The FDC chip contains two registers: the main status register, and the data register. The main status registers holds FDC status and may be accessed at any time. Only the status register is used for the transfer of data between the processor and the diskette controller.

The data register consists of several stacked registers. Only one register has access to the data bus at a time. This register stores data, commands, parameters, and diskette drive status information. The information written into, or read from, this register is used to program or obtain results after a specific command.

5.2.10.1 Main Status Register

This register contains the diskette controller status. The CPU may access this register at any time to transfer data between the CPU and controller.

Main Status Register (03F4H)

7	6	5	4	3	2	1	0
REQUEST FOR MASTER	DATA I/O DIR	NON-DMA MODE	CONTROL BUSY	DRIVE 3 BUSY	DRIVE 2 BUSY	DRIVE 1 BUSY	DRIVE 0 BUSY

Bit	Description
7	When set, this bit indicates that the data register is ready to send data to or receive data from the processor.
6	Indicates direction of the data transfer. 1 = data transfer from data register to processor. 0 = data transfer from processor to data register.
5	1 = execution phase during non-DMA mode. 0 = execution phase ended; result phase has started.
4	When set, this bit indicates that a read or write command is in process, and the controller will not accept any other command.
3-0	Disk drive n is in seek mode; the controller will not accept a read or write command.

5.2.10.2 Data Register

This register stores data, commands, parameters, and disk drive status. It consists of several registers arranged in a stack, with only one register at a time presented to the data bus.

Data Register (03F5H)

7	6	5	4	3	2	1	0
STATUS OR DATA							

Bit	Description
7-0	Data

5.2.10.3 Status Registers

The following four registers store status information after a command has been executed. The storage occurs during the result phase, and is relevant to the specific command.

Internal Register - Status Register 0

7	6	5	4	3	2	1	0
INTERRUPT CODE		SEEK END	EC	NOT READY	HEAD ADDRESS	UNIT SELECT	

Bit	Description
7-6	0 0 = Command was completed and terminated properly. 0 1 = Command was started but was unsuccessful. 1 0 = Command issued was never started. 1 1 = Abnormal termination: the disk drive ready signal changed state during command execution.

Internal Register - Status Register 1

7	6	5	4	3	2	1	0
EN	0	DATA ERROR	OVERRUN	0	NO DATA	NW	MISSING ADDRESS MARK

Bit	Description
7	Set when the controller attempts to access a sector beyond the last sector of a cylinder.
6	Not used, always zero.
5	Set when the controller detects a cycle redundancy check (CRC) error.
4	Set when the processor does not service the controller within a certain time interval during data transfers.
3	Not used, always zero.
2	Set when the following conditions occur. a. The controller cannot find the specified sector during execution of a read data, a write-deleted data, or a scan command. b. The controller cannot read the ID field without an error during execution of the read ID command. c. The starting sector cannot be found during execution of the Read A cylinder command.
1	Set when the controller detects a write-protect signal from the disk drive during a write data, write-deleted data, or format cylinder command.
0	Set under the following conditions. a. The controller does not detect the ID address mark after seeing the index hole twice. b. The controller cannot detect the data address mark or the deleted data address mark. This bit also sets the missing address mark bit in data field (Status Register 2, bit 0).

Internal Register - Status Register 2

7	6	5	4	3	2	1	0
0	CONTROL MARK	DATA ERROR IN DATA FIELD	WC	SCAN HIT EQUAL	SN	BC	MD

Bit	Description
7	Not used, always zero.
6	Set when the controller finds a deleted address mark during a read data or scan command.
5	Data error in error field. Set when the controller detects a cycle redundancy check error (CRC) in the data field.
4	Set when the contents of the current cylinder differs from the contents stored in the data register.
3	Set when the "equal" condition is satisfied during execution of a scan command.
2	Set if the controller cannot find a sector on the cylinder that meets the condition during a scan command.
1	Set when the cylinder contents is different than the contents stored in the data register, and the cylinder contents is FF(HEX).
0	Set when the controller cannot find a data address mark or deleted data address mark during a read operation.

Internal Register - Status Register 3

7	6	5	4	3	2	1	0
FAULT	WRITE PROTECT	READY	TRACK 0	TWO SIDE	HEAD ADDRESS	UNIT SELECT	

Bit	Description
7	Indicates the fault signal status from the diskette drive.
6	Indicates the write protected signal status from the diskette drive.
5	Indicates the ready signal status from the diskette drive.
4	Indicates the Track 0 signal status from the diskette drive.
3	Indicates the two side signal status from the diskette drive.
2	Indicates the side select signal status for the diskette drive.
1	Indicates the unit select 1 signal status for the diskette drive.
0	Indicates the unit select 0 signal status for the diskette drive.

Chapter 6
Hard Disk Controller

6.1 Introduction

The VAXmate hard disk controller connects the VAXmate CPU to an RD31-A (or equivalent) hard disk drive. The controller subsystem, including the hard disk drive, is located in the RCD31 expansion box (Figure 6-1). It consists of a WD1003-WAH controller module with cabling to connect it to the hard disk drive. This chapter describes only the hard disk controller. The hard disk drive technical description (*RD31-A Disk Drive Manual*, EK-RD31A-TD) contains details of the RD31-A.

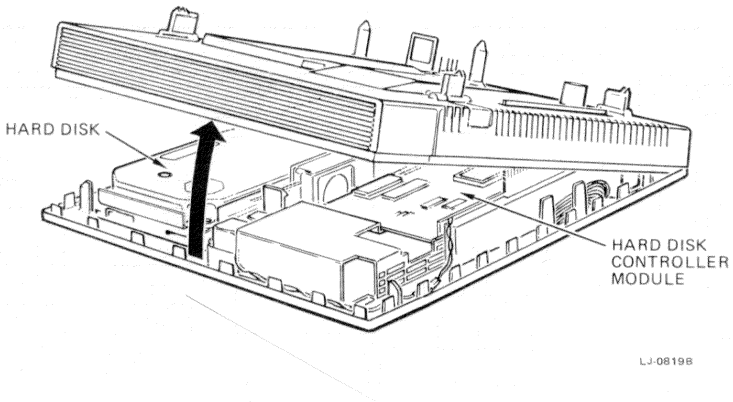


Figure 6-1 Hard Disk Subsystem Location

6.2 General Description

The VAXmate hard disk subsystem expands the on-line storage capacity of the system with an additional 20 megabytes of Modified Frequency Modulated (MFM) formatted data.

The controller module plugs into a 62-pin and a 36-pin connector on the expansion box backplane, and is connected to the hard disk drive by 34-pin and 20-pin cables. The 34-pin cable provides connections for two drives. There is also a 20-pin cable connection for each installed drive.

6.3 Physical Description

The hard disk controller module is a 25.4 centimeter (10 inch) long by 10.8 centimeter (4.25 inch) wide multilayer printed circuit board. It has two edge connectors (fingers on both sides of the board), three right-angle male plug connectors (J1, J2, and J3), and six sets of jumper pins, all on the component side of the board (Figure 6-2).

There are five major chip circuits on the board. They are a WD201A disk controller, WD10C20 read/write channel device, RAM sector buffer (1K × 8), WD1015 buffer manager control processor, and a WD11C00A host bus interface/buffer manager.

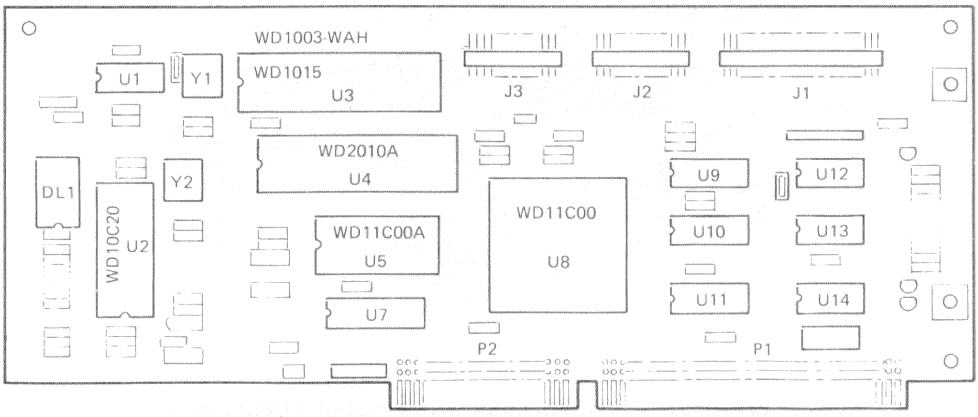


Figure 6-2 Hard Disk Controller Module – Component Side

6.3.1 Module Cabling

Three cables connect the hard disk drive to the VAXmate disk controller module. Two cables connect to the WD1003 controller board (Figure 6-3), and a single 4-pin cable connects to the expansion box power supply module (Figure 6-4). Figure 6-5 shows the hard disk subsystem interconnections.

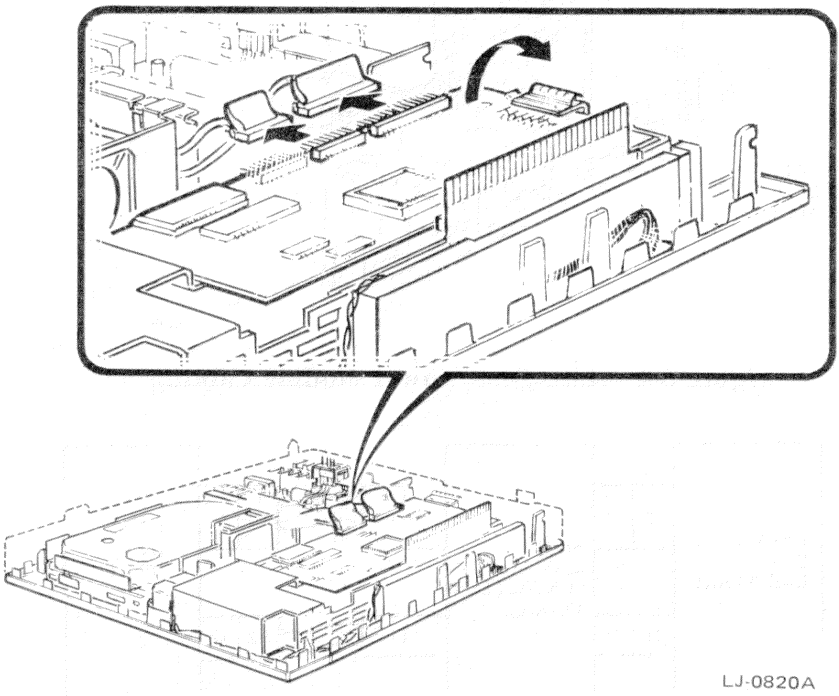


Figure 6-3 Hard Disk/Control Module Cabling

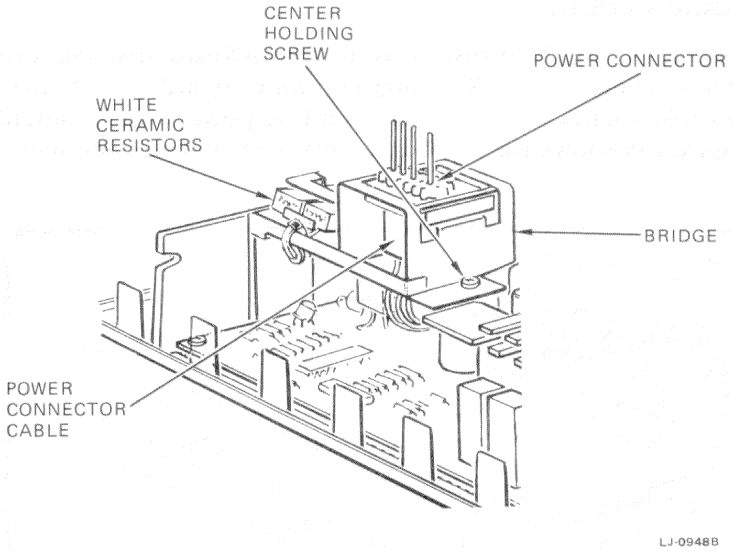


Figure 6-4 Hard Disk/Power Module Cabling

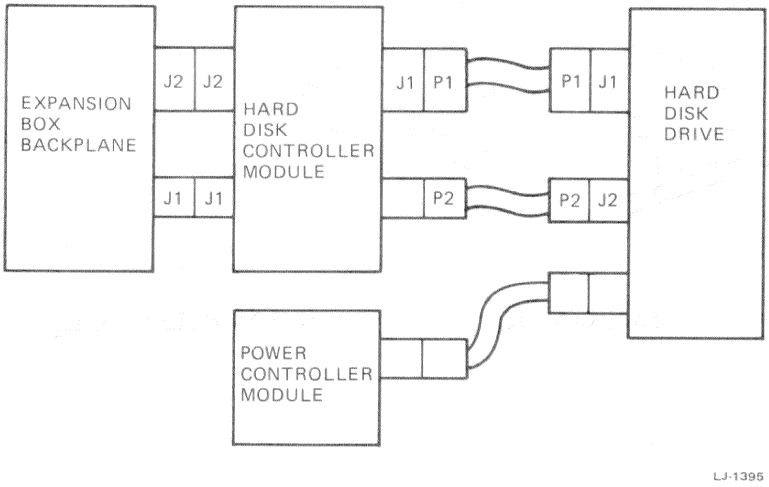


Figure 6-5 Hard Disk Subsystem Interconnections

Appendix B lists the edge connector signals. The pin references are as follows.

1. P1 – 62-pin card edge connector

   Component side – pins A1 through A31

   Conductor side – pins B1 through B31

2. P2 – 36-pin card edge connector

   Component side – pins C1 through C18

   Conductor side – pins D1 through D18

6.3.2 Module Jumper Settings

Table 6-1 lists the module jumper settings.

Table 6-1 WD1003-WAH Jumper Settings

Jumper	Position	Function
W1	no jumper*	Status read is not latched. Dynamic drive select (select=drive busy)
	jumper	Status read latched. Static drive select (select asserted except during reset)
W2	no jumper*	Primary addresses selected
	jumper	Secondary addresses selected
W3	not used*	No jumper pins installed on board
W4	Jumper 2-3*	Ties firmware sense bit high
	Jumper 1-2	Supports two head, 612 cyclinder second drive, with standard system Set-Up for four head, 306 cylinder drive.
W5	Jumper 1-2*	Standard configuration
	Jumper 2-3	Internal power-up circuit signal
W6	Jumper 2-3*	Ties input high. The 35 μs step rate is selected (step rate 0).
	Jumper 2-3	Ties input low. The 16 μs step rate is selected (step rate 15).

* These positions are normal jumper settings.

6.4 Functional Description

The WD1003-WAH hard disk controller is a PC-AT bus compatible printed circuit module that connects a hard disk drive to the 80286 host processor. The hard disk controller includes the following logic.

- WD11C00A-22 host interface device
- 2K × 8 RAM sector buffer memory
- WD1015 buffer manager control processor
- WD2010 Winchester disk controller
- WD10C20 read/write channel device
- Read data separation logic
- Write pre-compensation logic

Figure 6-6 is a basic block diagram of the controller. The following paragraphs briefly describe the major sections of the controller.

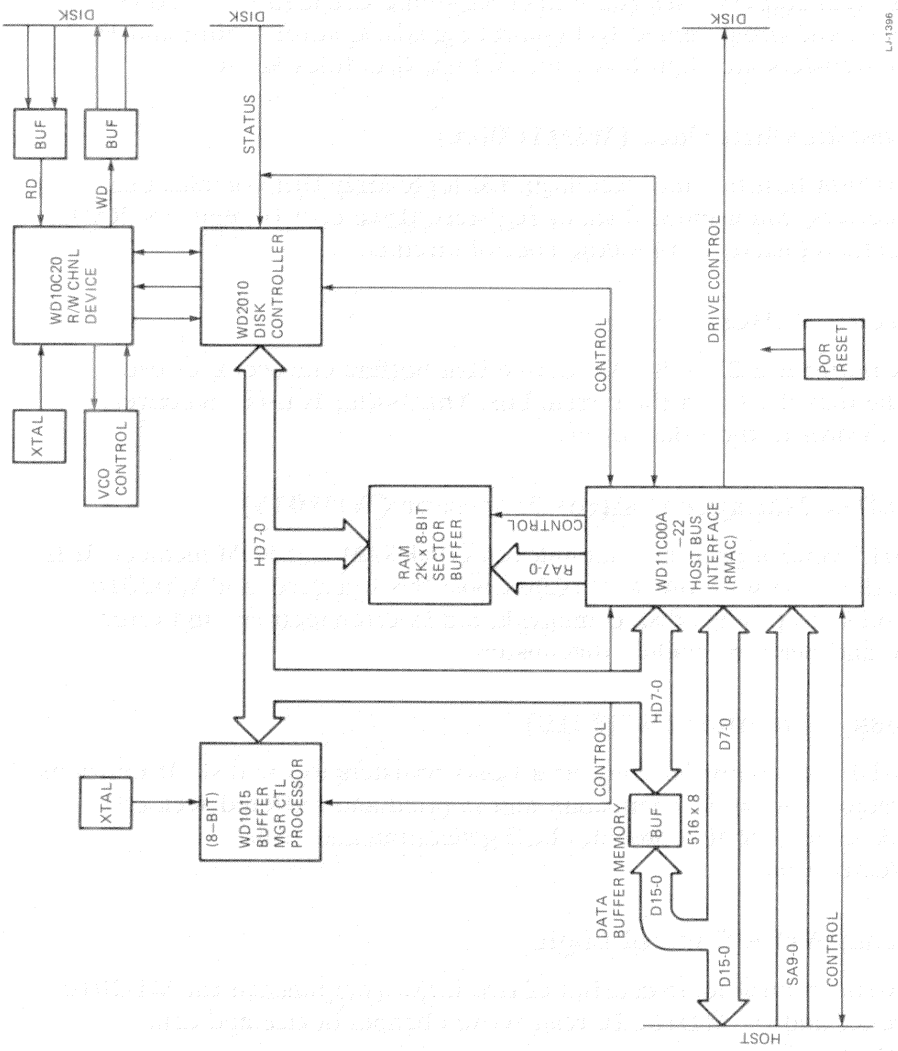


Figure 6-6 Hard Disk Controller Block Diagram

6.4.1 System Bus Interface

The controller is connected to the host CPU through the system data bus (SD7-0), system address lines (only lines SA9-0 are decoded to access controller registers), and programmed I/O control signals. Control, status, and ECC check byte transfers are eight bits wide and use data lines SD7-0.

6.4.2 Host Bus Interface (WD11C00A)

The WD11C00A host bus interface is an LSI logic array that contains bus drivers/receivers, command and status registers, drive control registers, RAM buffer address registers, and module control circuits.

6.4.3 Sector Buffer

The sector buffer is a 2K × 8 RAM device that buffers one sector of data between the disk drive and the system bus. This buffer is used to convert 16-bit data words to 8-bit data bytes.

6.4.4 Buffer Manager Control Processor (WD1015)

The WD1015 control processor includes internal RAM and ROM memory. It is used in conjunction with the WD11C00A host bus interface, and WD2010 disk controller, to process disk commands, aid in error recovery and error correction, and perform module diagnostics.

6.4.5 Disk Controller (WD2010)

The WD2010 disk controller controls all data transfers to the disk. It performs multiple sector read/write commands, and implied and buffered seek commands. This controller also provides ECC generation and error detection/correction.

6.4.6 Read/Write Control Logic

The read/write control logic consists of two major components: the WD2010 disk controller and the WD10C20 read/write channel device and data separator (Figure 6-7).

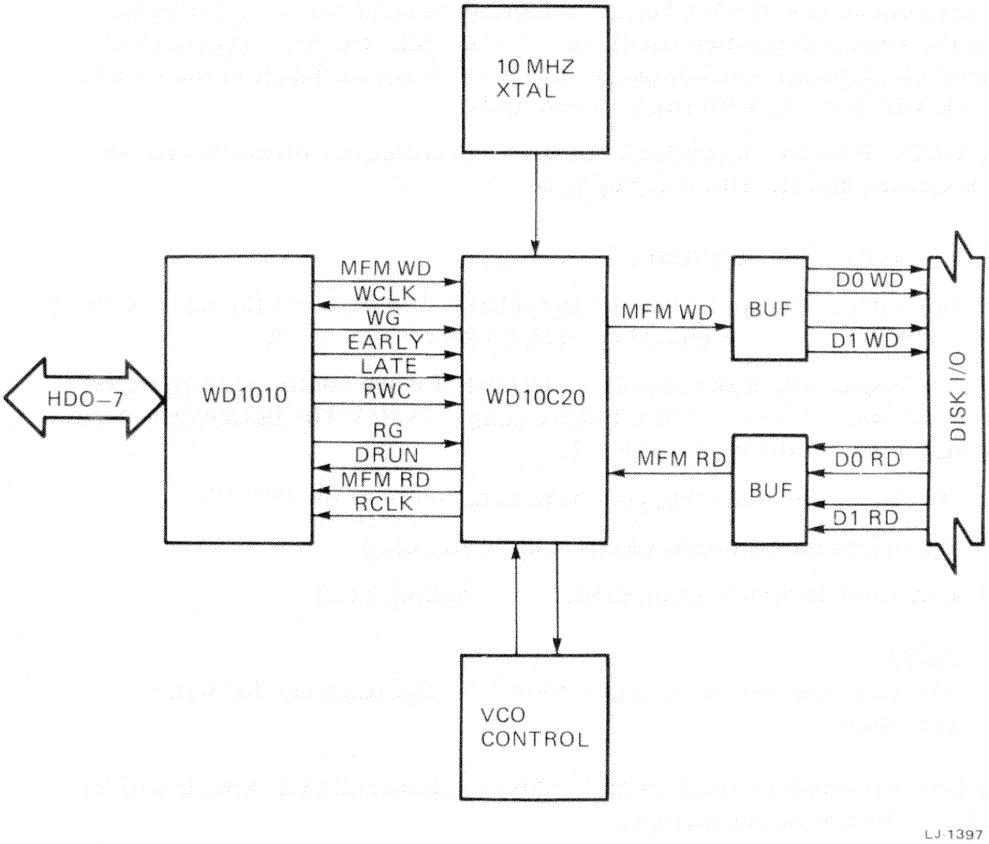


Figure 6-7 Controller Read/Write Logic – Block Diagram

The WD10C20 performs write data pre-compensation, and read data separation (phase-locked loop data synchronization). The disk controller converts 8-bit parallel data bytes into modified frequency modulated (MFM) pulse serial data, for storage on the disk surface. Early/late pre-compensation control signals are provided by the controller.

For read operations, the WD10C20 synchronizes MFM read data (MFM RD) with the voltage controlled oscillator (VCO) clock. The VCO generates reformed clock pulses synchronous to RCLK clock signal. RCLK defines a data bit cell which tracks with shifts in data pulses.

The WD2010 locates sector/data IDs when a continuous stream of ones or zeros occurs, and the DRUN signal is active.

6.4.7 Command Sequence

The following paragraphs illustrate the relationship between the major controller components during a typical command execution sequence.

In the idle state, the disk controller (WD2010) drive control signals are off. Controller status is ready, and the drive status is valid. The buffer manager is idle and monitors the wakeup signal.

The CPU issues the following command parameters to the task file.

- the operation command (seek, read, write, etc.)
- command attributes (long mode, retry control, etc.)

> ***NOTE***
> The CPU also issues the sector format or data sequence for write operations.

The host bus interface receives and holds the command byte, which will be used later by the buffer manager.

If a read operation is specified, the read command sets the module wakeup latch, which causes the controller status to go busy, and asserts the WD1015 wakeup signal. Write and format commands set the data request status signal (DRQ), which initiates the host data transfer. When the data transfer is completed, the wakeup signal and busy status are set.

The buffer manager examines the command, verifies the command parameters, and passes the command to the disk controller (WD2010A) for execution.

The disk controller executes the command by issuing the drive data, asserting drive control signals, and determining status.

When the command is completed, the disk controller interrupts the buffer manager, which then inspects the command, status, and other parameters for additional requirements. If completion is required, the buffer manager sets controller status to ready, and interrupts the host.

The WD1003-WAH returns to idle, and the host can examine controller and drive status, read input data, and other parameters to complete the operation.

6.4.8 Data Registers

All system bus data transactions between the system CPU and the hard disk controller are in 16-bit word transfer bus mode. The controller reserves system I/O address 1F0 (hex) for the programmed data transfers. The controller module logic has an 8-bit RAM sector buffer and a byte register, to place the 16-bit system data bus words on the controller 8-bit local data bus (Figure 6-8).

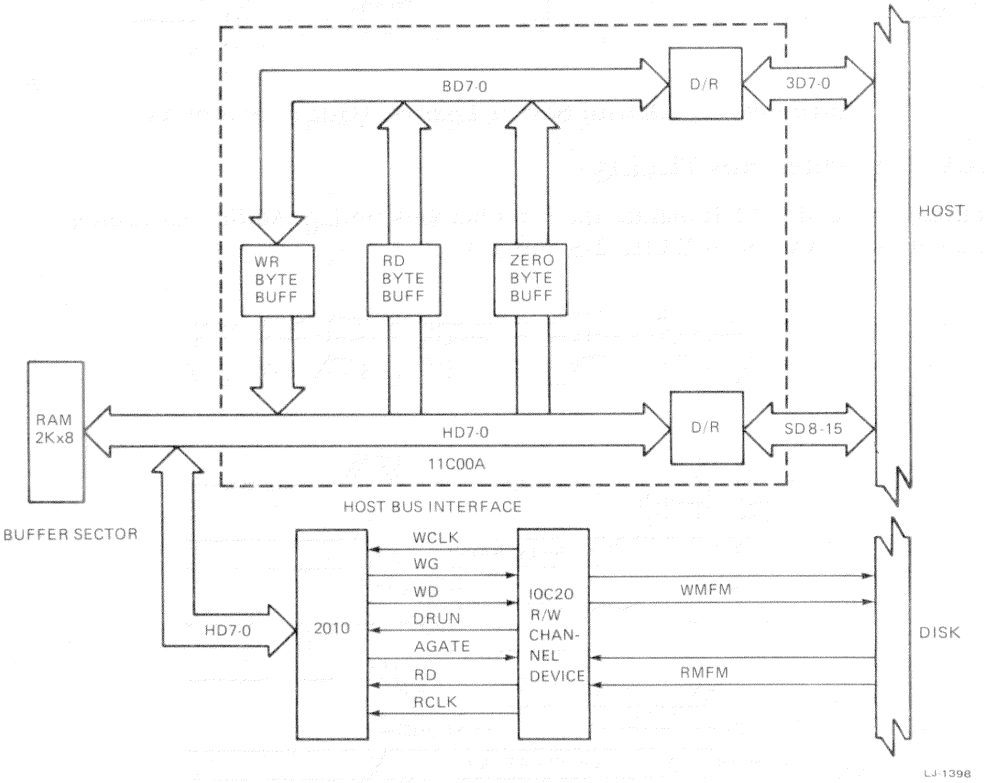


Figure 6-8 Read/Write Data Transfer Path

Figure 6-9 shows the disk track and sector format.

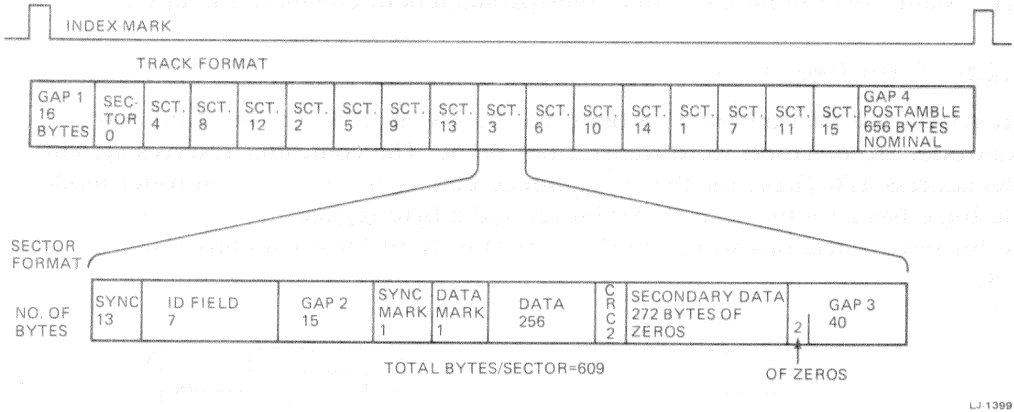


Figure 6-9 Track and Sector Format (Interleave of 4)

6.4.9 Interface Bus Timing

Figures 6-10 and 6-11 illustrate the interface bus timing. Additional timing parameters are shown in Tables 2-3 and 2-4.

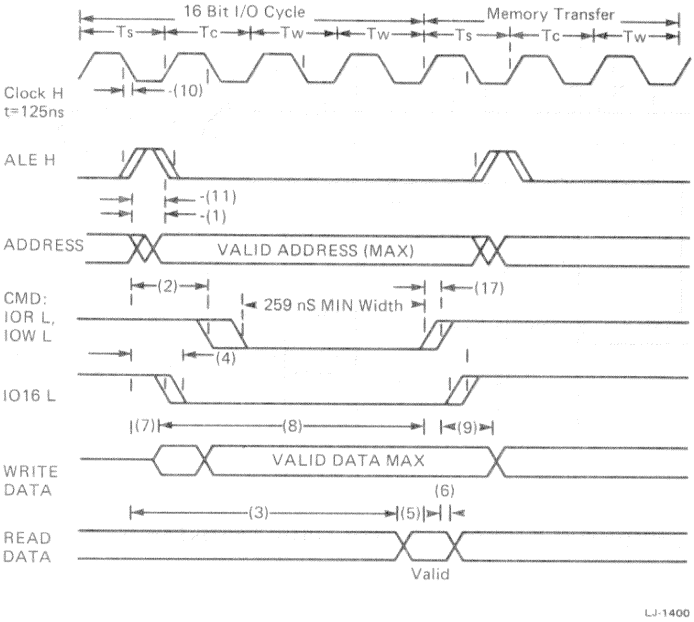


Figure 6-10 16-Bit I/O Cycle Timing – Transfer Data Mode

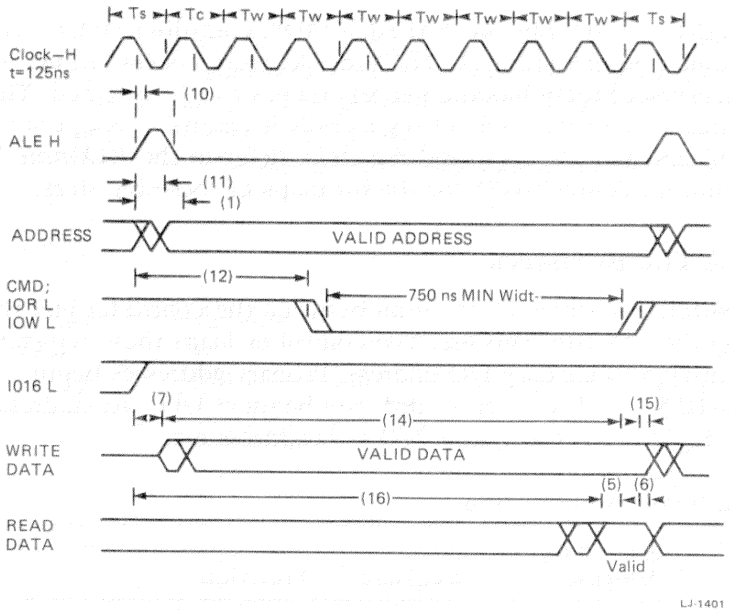


Figure 6-11 8-Bit I/O Cycle Timing – Transfer Data Mode

6.5 Software Operation

Control and data transfers between the hard disk controller and system CPU use programmed input/output (I/O). Direct Memory Access (DMA) is not supported. Primary/secondary module address ranges can be selected. The hard disk controller contains two sets of registers that control disk operations: the task file registers, and the command registers. Refer to the *VAXmate Technical Reference Manual* (Q6ZCS-GZ) for the bit maps of these registers.

6.5.1 Task File Registers

All data, control, and status information between the controller and the system pass through the task file registers. The controller maps these registers into either a primary or secondary I/O address. Primary addresses begin at I/O base address 1F0(HEX), and secondary addresses begin at I/O base address 170(HEX). Table 6-2 is the system I/O port address map.

Table 6-2 I/O Port Address Map

Primary Address	Secondary Address	Register	Function
1F0 (R/W)	170	DTR	Hard disk data register, 16 bits
1F1 (WO)	171	WPC	Write Precompensation Cylinder
1F1 (RO)	171	ERR	Error Register
1F2 (R/W)	172	SCT	Sector Count
1F3 (R/W)	173	SN	Sector Number
1F4 (R/W)	174	CLL	Cylinder Number, Low Byte
1F5 (R/W)	175	CLH	Cylinder Number, High Byte
1F6 (R/W)	176	SDH	Sector Size, Drive Head Select
1F7 (WO)	177	CMD	Command Register
1F7 (RO)	177	ST	Status Register
3F6 (WO)	376	FDR	Fixed Disk Register
3F6 (RO)	376	ASR	Alternate Status Register
3F7 (RO)	377	DIR	Digital Input Register

Data transfers are word-length transfers, except for ECC bytes during Read Long and Write Long commands (ECC bytes are transferred in byte mode). There are eight task file registers, six of which have read/write capability. The remaining two registers have different definitions for read and write operations. Table 6-3 provides a summary of these registers.

Table 6-3 Task File Register Summary

Register	7	6	5	4	3	2	1	0
WPC	Cylinder number/4							
ERR	BBD	ECC	0	INF	0	ACD	TKO	DNF
SCT	Number of sectors							
SN	Sector number							
CLL	Cylinder number low							
CLH	0	0	0	0	0	0	Cylinder number high	
SDH	ECC/ CRC	0	512/ 256	DS	HS3	HS2	HS1	HS0
CMD	Command							
ST	BSY	RDY	WFT	SKC	DRQ	CRD	IDX	ERR

6.5.1.1 Data Register (1F0/170)

This read/write register provides a 16-bit data path to the sector buffer for normal read and write commands in the programmed I/O mode. Access this register only while executing a read or write command. After a Read Long or Write Long command is issued, four ECC bytes are transferred byte-by-byte, with at least 1.6 microseconds between transfers. The Data Request status bit (DRQ, bit 3 of the Status Register) must be valid before transferring each ECC byte.

6.5.1.2 Write Pre-compensation Register (1F1/171)

The write pre-compensation register is a write only register that contains the starting cylinder number that needs pre-compensation. This number is the value of the cylinder divided by four.

6.5.1.3 Error Register (1F1/171)

This register contains specific error status information that may appear after a command is completed. The data is valid when the error bit is set in the Status Register, unless the previous command was the diagnose command. The controller automatically executes the diagnose command upon power-up, and the Error Register is polled to check hardware status. In each case (diagnostic mode and powerup), the Error Register is polled, regardless of the error bit indication in the Status Register. At power-up, or in diagnostic mode, the Error Register returns the bit values shown in the *VAXmate Technical Reference Manual* (Q6ZCS-GZ).

6.5.1.4 Sector Count Register (1F2/172)

This read/write register contains the number of sectors to be transferred to the sector buffer during a Read, Write, Read Verify, or Format Track command. During a multiple sector transfer, after each sector is transferred to the sector buffer, the controller decrements the sector count, and increments the sector number. Loading the register with 00 causes a 256 sector transfer.

6.5.1.5 Sector Number Register (1F3/173)

The sector number register holds a sector number anywhere from 0 to 255. During a multiple sector command, the number in the register specifies the first sector in the transfer. The controller increments this number after each full sector data transfer to the sector buffer.

6.5.1.6 Cylinder Number Low Register (1F4/174)

This register holds the eight least significant bits of the 10-bit cylinder number. The Cylinder Number High register provides the two most significant bits of the number.

6.5.1.7 Cylinder Number High Register (1F5/175)

The cylinder number high register is a read/write register that holds the two most significant bits of the desired cylinder number. The Cylinder Number Low register holds the eight least significant bits of the number.

6.5.1.8 Fixed Size/Drive/Head Register (1F6/176)

The data in this register selects the drive parameters.

6.5.1.9 Status Register (1F7/177)

This register indicates the result of a previous operation. The program must read the register to determine the result. If Write Fault or Error is active, or Seek Complete or Ready is inactive, a multiple sector operation is aborted.

6.5.2 Command Register (1F7/177)

This write-only register begins command execution immediately upon receipt of macro commands from the system. The system loads the Command Register with the information required for the command. The Command Register should not be written to while the controller is busy. If Write Fault is active, or Drive Ready or Seek Complete are inactive, the controller does not execute any command, and an Aborted Command Error results. Also, any illegal command results in an Aborted Command Error. When any command is written to this register, the controller interrupt is reset.

6.5.2.1 Restore Command (10-1F)

The restore command moves the read/write heads to the outermost track position (track 000). This command is usually used during a power-up condition. The controller issues step pulses to the selected drive until the Track 00 signal from the drive becomes true. The drive Seek Complete signal governs the step rate. If the Track 00 signal is not asserted after 2047 step pulses, the command aborts with the error bit set in the Status Register, and TK 00 Error set in the Error Register. This command sets the implied seek step rate. The lower four bits of the command select one of 16 possible step rates. The command terminates when Drive Ready is deasserted, or Write Fault is asserted. When these conditions occur, the error bit in the Status Register sets, and the Error Register reports an aborted command.

6.5.2.2 Seek Command (70-7F)

The Seek Command moves the read/write heads to the cylinder specified in the task file cylinder select registers. The four low order bits set the implied seek rate. At the completion of this command, the controller generates an interrupt. If Drive Ready is inactive, or Write Fault is active, the command terminates, the error bit in the Status Register is set, and the Error Register shows an aborted command.

6.5.2.3 Read Sector Command (20-23)

The Read Sector command transfers the specified number of sectors (1 to 256) from the selected drive. The sector count is contained in the Sector Count Register (SCT) of the Task File Register. If the heads are not positioned at the specified cylinder, the controller performs an implied seek to the proper cylinder. The step rate used is determined by the most recently executed Restore or Seek command. Multiple sector reads may cross head and cylinder boundaries. If Drive Ready is inactive, or Write Fault is active, the command terminates, and the error bit sets in the Status Register.

6.5.2.4 Write Sector Command (30-32)

The Write Sector command writes the number of sectors specified in the Sector Count Register to the selected drive. If the heads are not positioned at the cylinder specified in the Task File Registers, the controller performs an implied seek to the proper cylinder. The step rate used is determined by the most recently executed Restore or Seek command. Multiple sector writes can cross head and cylinder boundaries. If Drive Ready is inactive, and Write Fault is active, the command terminates, and the error bit is set in the Status Register. The controller interrupts as each sector except the first transfers, and at the end of the command. The first sector can be written to the buffer immediately after the controller sends the command, and the Data Request (DRQ) bit is on.

6.5.2.5. Format Track Command (50)

This command formats one track using the Task File Register and the sector buffer. The sector buffer is used for additional parameter information instead of sector data. The controller formats the track specified by the task file register with ID and data fields, and references an interleave table transferred to the buffer. The interleave table for an interleave factor of two is shown in the *VAXmate Technical Reference Manual* (Q6ZCS-GZ).

6.5.2.6 Read Verify Command (40-41)

Read Verify functions similar to a normal Read Command, except that data is not output to the system processor. The controller reads the number of sectors specified in the Task File Registers from the selected drive, and checks the ECC bytes for data verification. If the heads are not positioned at a cylinder specified by the task file registers, an implied seek to the proper cylinder is performed to position the heads. The step rate to be used is determined by the

most recently used Restore or Seek command. Multiple sector reads may cross head and cylinder boundaries. If the Drive Ready signal is inactive, or Write Fault is active, the command terminates, and the error bit is set in the Status Register. This command continuously monitors these signals. The controller interrupts upon completion of the command or when an error occurs.

6.5.2.7 Diagnose Command (90)

This command allows the controller to execute self tests, and if a problem exits, to report the results. Tests are run on internal ROM and RAM, ECC circuitry, and data path circuitry. When a failure occurs, the controller loads the appropriate error code into the Error Register. An interrupt is generated upon completion of this command.

6.5.2.8 Set Parameters Command (91)

This command sets the drive parameters for the maximum number of heads per drive and sectors per track. Prior to issuing this command, the drive selection must be specified in the Sector Size/Drive Select/Head Select task register, and the Sector Count Register must be set. This command must be issued before any multiple sector operations are performed. An interrupt is generated upon completion of this command.

6.5.3 Control and Status Registers

6.5.3.1 Alternate Status Register (3F6)

This register is a duplicate of the Task File Status Register.

6.5.3.2 Fixed Disk Register (3F6)

This register resets the controller under program control, and enables and disables the controller interrupt.

6.5.3.3 Digital Input Register (3F7)

The digital input register contains the complemented current state of the Write Gate, Head Select, and Drive Select signals.

Chapter 7
Expansion Box

7.1 Introduction

The expansion box (Figure 7-1) converts the VAXmate workstation into a Digital network server. The expansion box has a hard disk storage device and a bus interface. The hard disk uses the MS-DOS operating system and MS-Windows application programs. The expansion box attaches to the bottom of the VAXmate workstation.

The expansion box is available in the following configurations:

RCD32-FA	40 Mbyte VAXmate Expansion Box (non-U.S.A. version)
RCD32-FC	40 Mbyte VAXmate Expansion Box (U.S.A. version)
RCD31-FA	20 Mbyte VAXmate Expansion Box (non-U.S.A. version)
RCD31-FC	20 Mbyte VAXmate Expansion Box (U.S.A. version)

The expansion box has the following components.

1. A power regulator
2. A lithium battery backup for real-time clock
3. A hard disk drive
4. A dc fan (The dc fan is not in early RCD31-EA and -EC models of the expansion box.)
5. A card cage with backplane for
   a. Option slot – 1
   b. Option slot – 2
   c. Hard disk controller

Each option slot is compatible with the industry-standard 8-bit bus and 16-bit bus to accept hardware options. The backplane has a maximum 9.5 watt per slot maximum power capacity. A CPU clock signal of 8 MHz is available for the backplane.

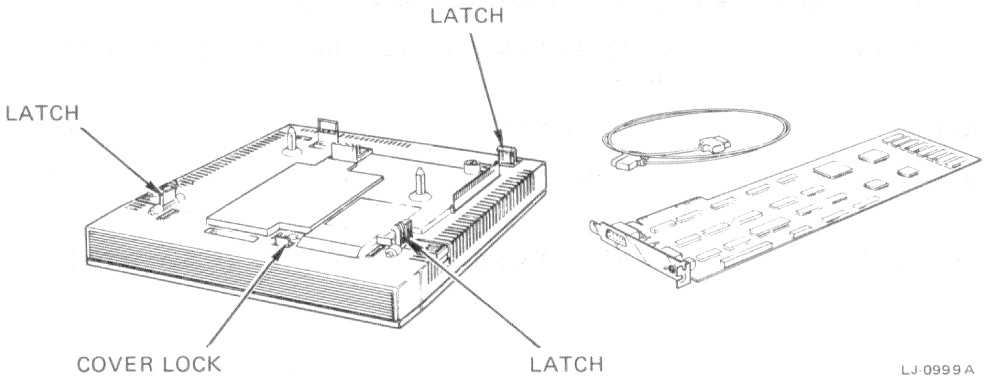


Figure 7-1 VAXmate Expansion Box

7.2 Expansion Box Battery

The expansion box battery provides power for the VAXmate workstation time of day clock and event timer. For the VAXmate workstation to recognize the presence of the battery, toggle the power switch to reset a bit in a register in the VAXmate workstation. Then, run the extended self-test to configure the system and see if the battery, hard disk, and expansion box are displayed in the configuration list.

Run the Extended Self-Test as follows.

1. Turn the power on and let the power-up test complete.
2. Turn the power off and wait 15 seconds for the drive to spin down. Turn the power on again to clear the power fail bit in the event timer, and allow the power-up test to complete. The power fail bit indicates if the battery is present in the expansion box.
3. Observe the configuration list upon completion of the Extended Self-Test to determine that Li (lithium battery), RD (hard disk), and BA500 (expansion box) appear in the configuration list. This verifies that battery backup is available, the hard disk is connected to the hard disk controller, and the expansion box connection is good.
4. If error numbers 83 or 87 are displayed during the Extended Self-Test, disk drive 0 or 1 (identified as C or D) has not been formatted. One of the disk drives must be formatted before completing the test using specific formatting software. See the *VAXmate Expansion Box Installation Guide and Owner's Manual* (EK-RCD31-OM) for instructions.

7.3 Accessing Expansion Box Components

To access the expansion box card cage for option installation, remove the expansion box cover as follows.

1. Remove all external cables.
2. Separate the expansion box from the system unit by pressing three latches and lifting from the front of the expansion box (Figure 7-1).
3. Release the cover lock and lift up the front edge of the cover. Then, lift the cover straight up (Figure 7-2). Figure 7-3 shows the location of the expansion box components.

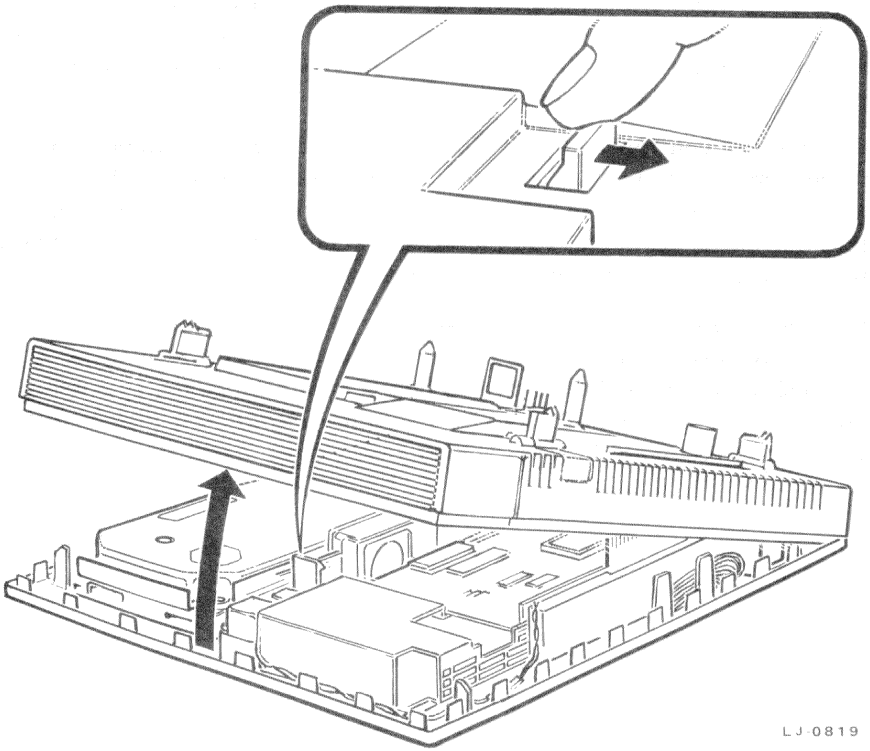


Figure 7-2 Expansion Box Cover Removal

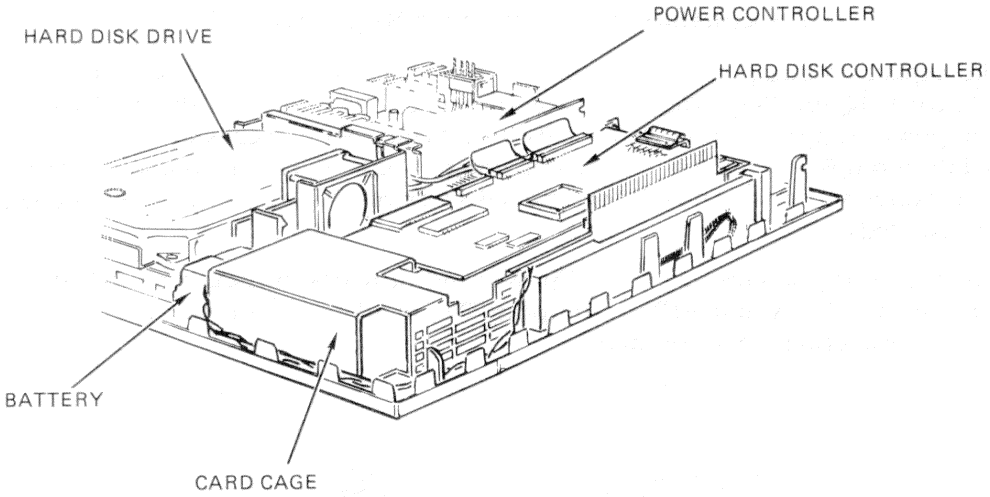


Figure 7-3 Expansion Box Components

7.4 Expansion Box Functional Description

Figure 7-4 is a block diagram of the expansion box components. The remainder of this chapter features a hardware technical description of these components, except for the hard disk drive and hard disk controller, which are described in Chapter 6.

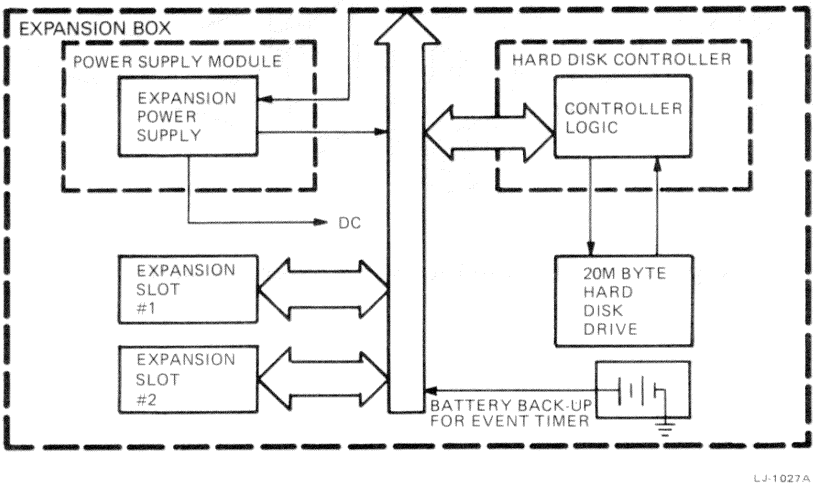


Figure 7-4 Expansion Box Block Diagram

7.4.1 H7271 Expansion Box Power Regulator Module

The expansion box power regulator (54-16843-01) is assembled on a single PC board (Figure 7-5). The expansion box uses 300 volts from the workstation power supply. It has a green LED to indicate that power is on, which is visible through the louvers on the left side of the box. The regulator has hard wire cables and connectors for the hard disk drive, the backplane, and a dc fan (if installed).

The regulator provides 72 watts of power and provides over-current protection for the +5.1 V and +12.1 V outputs. The regulator also provides short-circuit protection for all outputs.

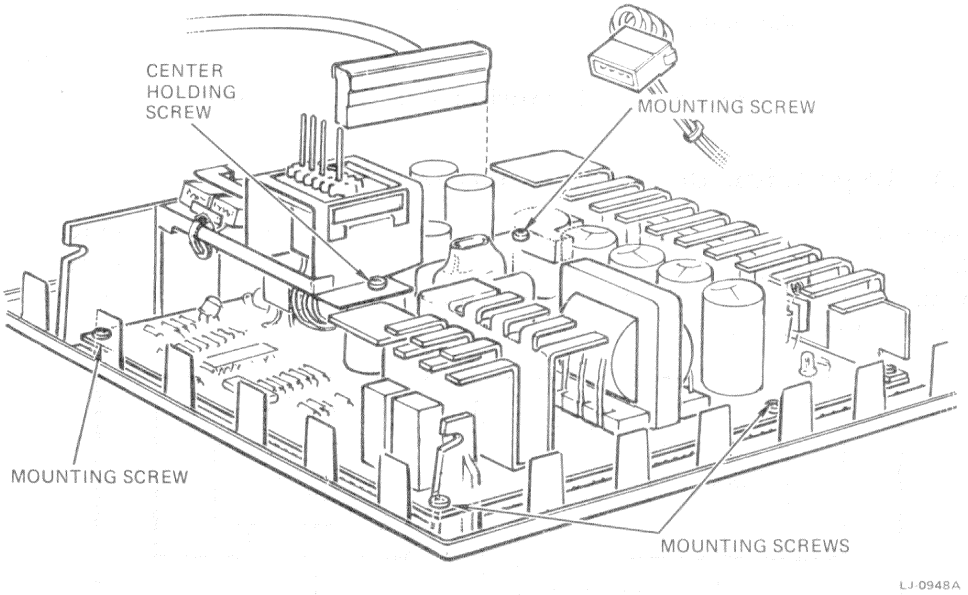


Figure 7-5 Expansion Box Power Regulator

7.4.2 Power Regulator Functional Description

Figure 7-6 is a block diagram of the expansion box power regulator. The power regulator receives unregulated ±150 Vdc input from the workstation The input pin assignments are as follows.

Pin	Voltage
1	+150 Vdc
2	Key
3	Safety Ground
4	NC
5	−150 Vdc

The high voltage dc input goes to line filter L1. E4 control pulse width modulator and E3 CMOS timer turn the Q1 Field Effect Transistor on and off at a 100 kHz rate, to switch the voltage across the primary side of the T1 transformer.

The transformer output is rectified, filtered, and regulated to produce four dc output voltages (+5.1 V, +12.1 V, −5 V, and −12 V) for the hard disk drive, the option backplane, and the fan.

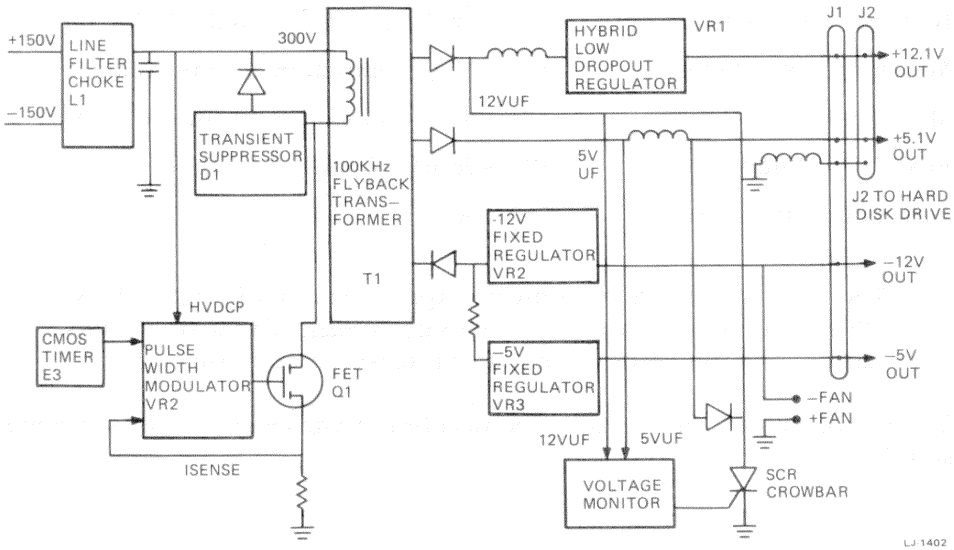


Figure 7-6 Expansion Box Power Regulator Block Diagram

VR1 in the 12.1 V output circuit is a hybrid, low-dropout voltage regulator. During start-up time for the hard disk, this regulator minimizes the power loss, while maintaining the 12.1 V output. VR2 is a −12 V fixed voltage regulator. VR3 is a −5 V fixed voltage regulator.

The D21 crowbar silicon controlled rectifier (SCR) monitors the +5.1 V and the +12.1 V for an over-voltage condition, and provides protection against this condition. The +5.1 V signal and the +12VUF sense signal provide the voltage levels to the SCR. When an over-voltage occurs, the SCR shorts these voltages to ground.

A voltage monitor senses the transformer output for sufficient power for normal power regulator operation. The voltage monitor uses operational amplifiers (E1) as voltage comparators. If an over-voltage condition occurs, the Q4 transistor turns on and shorts the +5.1 V and +12.1 V outputs, which then trips the SCR primary shutdown circuit.

7.4.3 Power Regulator Specifications

The paragraphs that follow provide the input and output specifications for the expansion box power regulator.

7.4.3.1 Power Regulator Input

Nominal Input Voltage	300 Vdc (from +150 V and −150 V input)
Minimum Input Voltage	245 Vdc (at minimum ac line voltage)
Maximum Input Voltage	375 Vdc (at maximum ac line voltage)
Peak Input Voltage	424 Vdc maximum for 1 sec
Maximum Input Current	500 mA

NOTE

The power regulator must meet output regulation specifications with input voltages as low as 180 Vdc, to ensure that all outputs remain a minimum of 0.5 ms after removal of ac power.

Safety protection is provided by the fuse in the VAXmate workstation power supply.

7.4.3.2 Expansion Box Power Supply Output

The VAXmate workstation power supply and the expansion box power regulator provide a total of 28.5 watts of power to the expansion box card cage (9.5 watts per option slot). The hard disk controller occupies the top option slot. A total of 19 watts is available for any industry-standard options you install in the remaining two slots.

> ***CAUTION***
> Never install option boards that exceed the available expansion box wattage. A single option or a combination of options that needs more than 19 watts can damage the expansion box circuitry, blow the fuse in the workstation, or damage the VAXmate workstation power supply. See your option documentation or sales representative to determine the wattage requirements for the industry-standard options you wish to install.

Table 7-1 is a summary of the output voltage and current ranges to be considered when you design a module for the option backplane.

Table 7-1 Output Voltage Summary

Output	Voltage (min)	Voltage (max)	Current (min)	Current (max)	Ripple (max pk-pk)
+5.1 V	+4.85 V	+5.35 V	0.8 A	4.5 A	75 mV
+12.1 V	+11.5 V	+12.7 V	0.6 A	1.2 A	50 mV
−12 V	−10.8 V	−13.2 V	0.0 A	0.2 A	100 mV
−5.0 V	−4.5 V	−5.5 V	0.0 A	0.2 A	100 mV
Fan −12V				0.25 A	

7.5 Expansion Box Backplane

Figure 7-7 is the expansion box backplane. The slots labeled J1 and J2 are available for installion of industry-standard options. The top slot, J3, is reserved for the hard disk controller.

The expansion backplane has two buses: an 8-bit bus and a 16-bit bus. These buses are available for use with industry-standard options. See Appendix B for the signals on these buses.

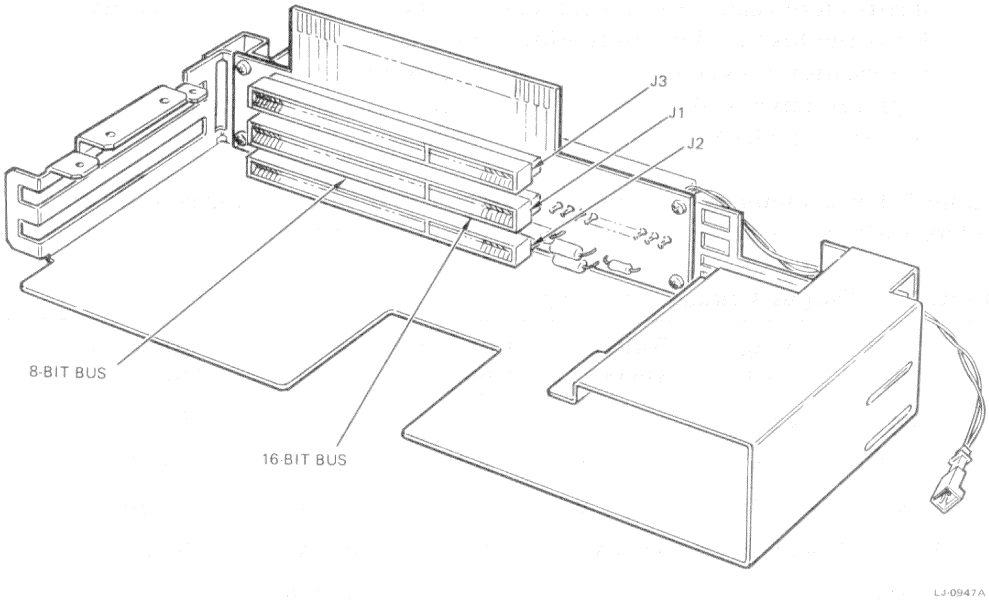


Figure 7-7 Expansion Box Backplane

7.5.1 Installing Options in the Backplane

Use the following procedure to install industry-standard options in the backplane.

1. Remove the expansion box cover (Section 7.3).
2. Disconnect the hard disk drive cables from the controller board, and tip the card cage on its back (Figure 7-8).

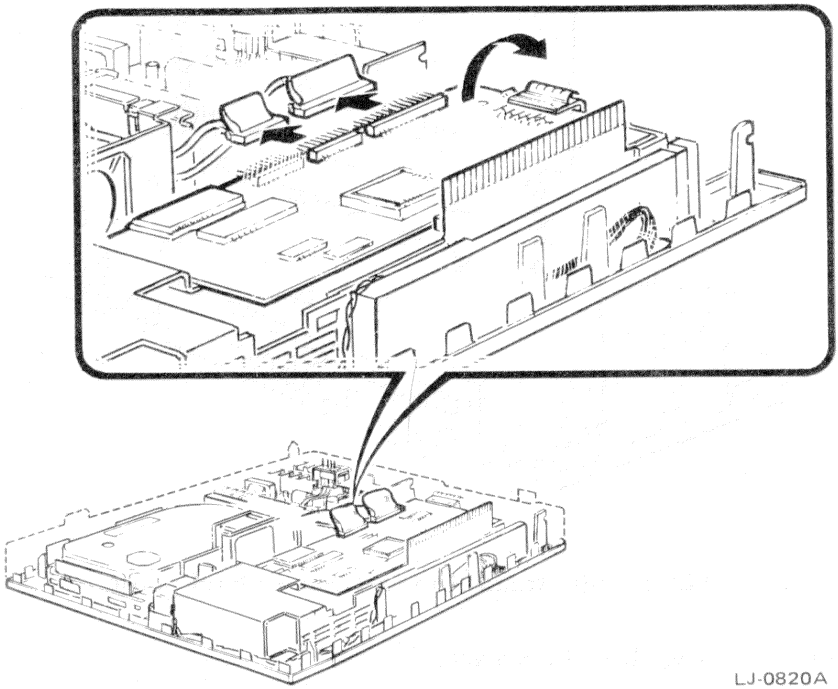


Figure 7-8 Accessing Option Slots in Backplane

3. Install the industry-standard option board into either option slot (Figure 7-9). Use the bottom slot if you have one board mounted on top of another board.
4. Make sure the option connectors are firmly installed.

5. Secure the option with the grounding screw, as shown in Figure 7-9.

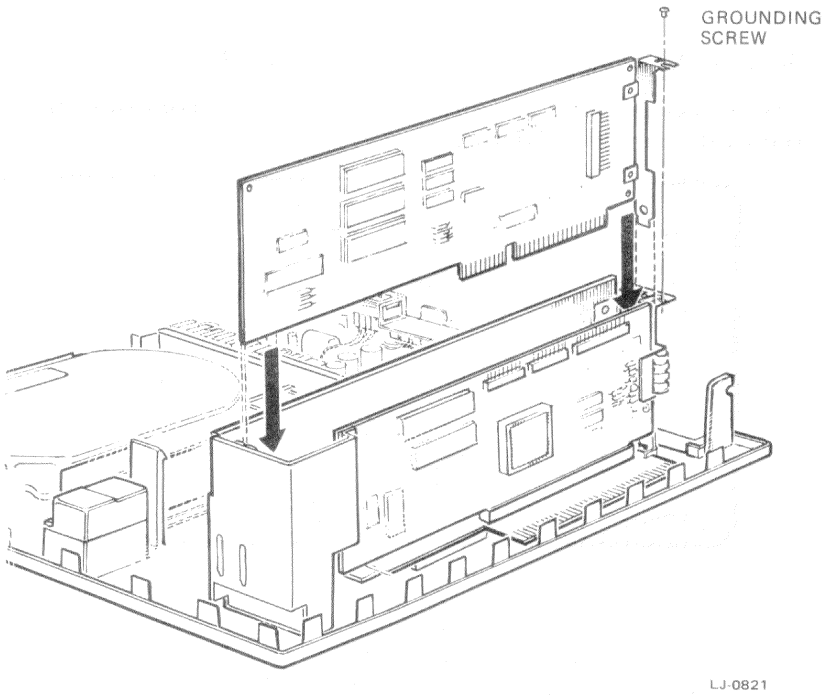


Figure 7-9 Installing Options in Backplane

6. Tip the card cage back into place.
7. Connect the hard disk drive cables to the controller board.
8. Make sure the cable connectors are seated correctly on the pins.

9. Connect the cable for your option, if present (Figure 7-10). Follow the instructions provided with your option to install the cable and any peripheral device.

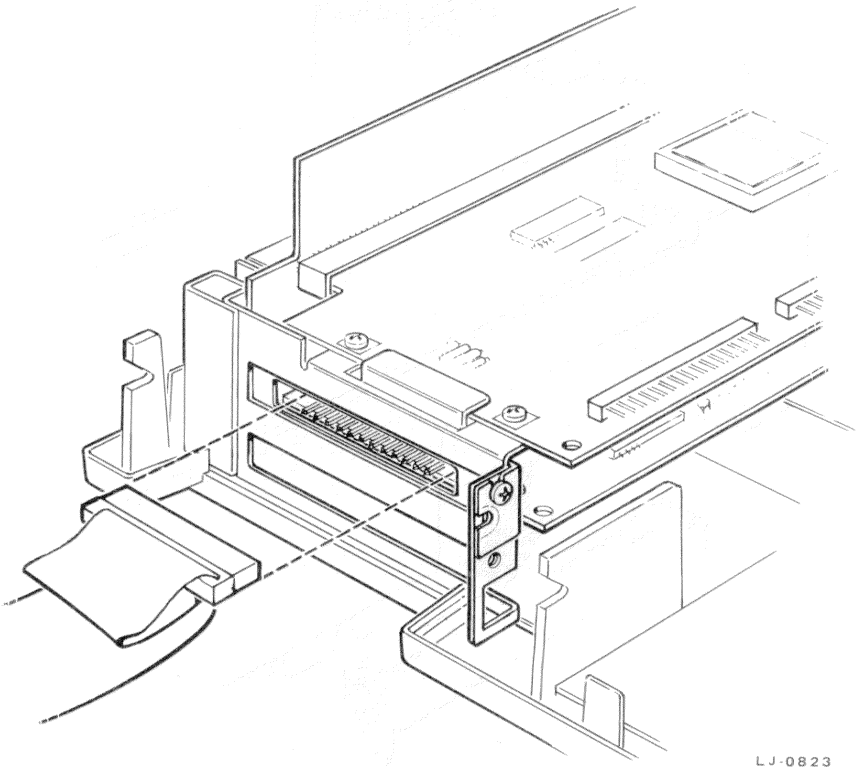


Figure 7-10 Connecting Cable to Option in Backplane

10. If you installed an option cable, remove the cable access plate from the top cover (Figure 7-11).

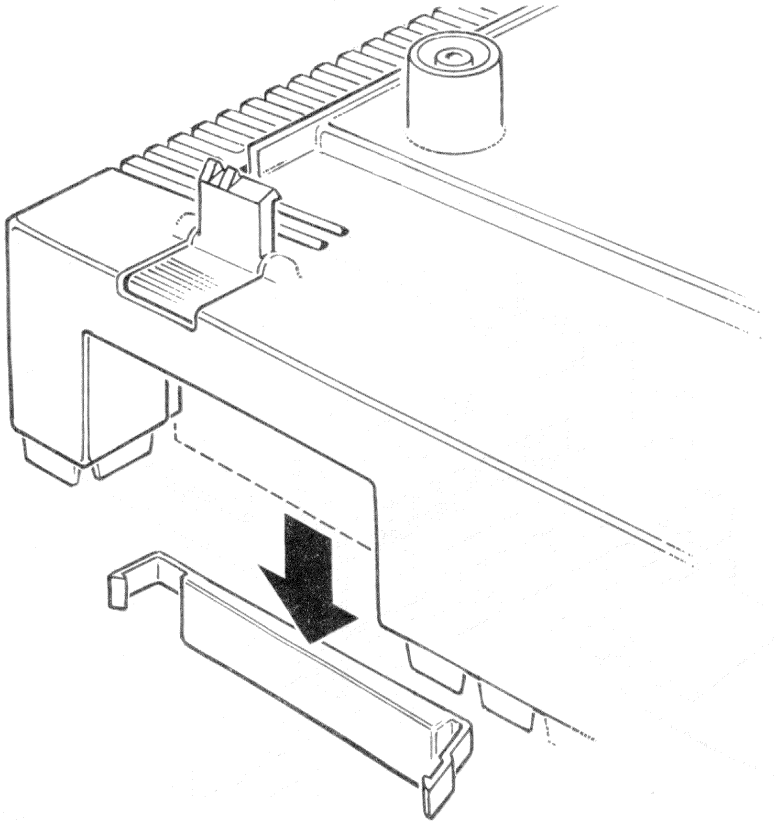


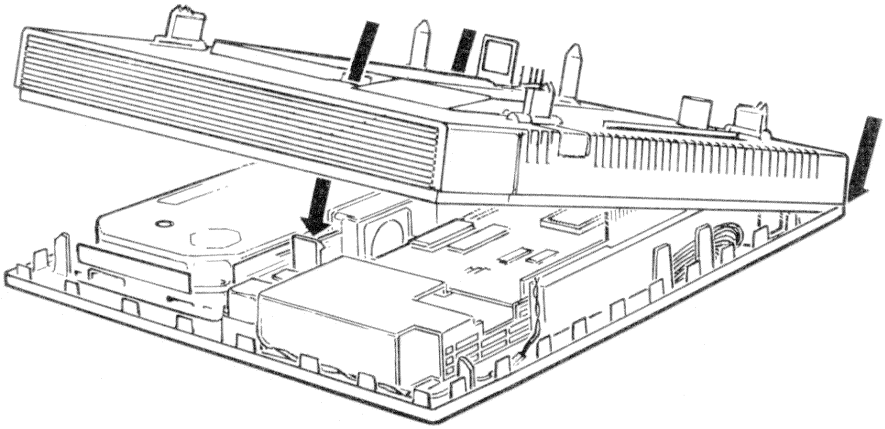
Figure 7-11 Removing Cable Access Plate

11. Replace the expansion box cover as follows.

    a. Lower the back corners of the cover into the groove on the back of the base.

    b. Make sure that the corners are seated correctly, and that all wires are inside the tabs on the perimeter of the base, so they do not interfere with closing the cover.

    c. Lower the cover into place and make sure the cover lock latches (Figure 7-12).



LJ-0819A

Figure 7-12 Replacing Expansion Box Cover

Chapter 8
Keyboard and Keyboard Controller

8.1 Introduction

This chapter describes the LK250 keyboard and the keyboard controller located on the VAXmate CPU board. The keyboard is the user interface to the system with its own internal controller, an 8051. The 8051 controller detects and encodes keystrokes, and transmits the information to the keyboard interface controller, an 8042 on the CPU board. The 8042 sends the information to the central processor. The keyboard also receives information from the central processor through the keyboard interface controller. The keyboard supports both industry-standard applications and Digital-developed applications on the VAXmate network.

The LK250 keyboard supports host control of keyboard LEDs, keyclicks, autorepeat, and two scan code modes for identifying the keys. These modes are

1. VAXmate workstation mode
2. Industry-standard AT-compatible mode.

8.2 Keyboard Physical Description

The keyboard (Figure 8-1) has 105 keys arranged in the following groups.

- Main keypad (57 keys)
- Editing keypad (18 keys)
- Special function keypad (20 keys)
- Arrow keypad (10 keys)

The keyboard circuitry is contained within a low-profile plastic shell that you can open with a hex-nut driver. Keycaps require a special tool for removal.

The keyboard has a label strip holder and four LEDs located along the top edge of the keyboard above the special function keys. The label strips are used to identify these keys and the LEDs for different application programs.

A coiled cable, with a 6-pin modular connector on one end and a 6-pin rectangular connector on the other, connects the keyboard to the workstation. The modular connector fits into J4, the keyboard jack. You can route the cable in the slot in the bottom of the keyboard to extend out of either side of the keyboard.

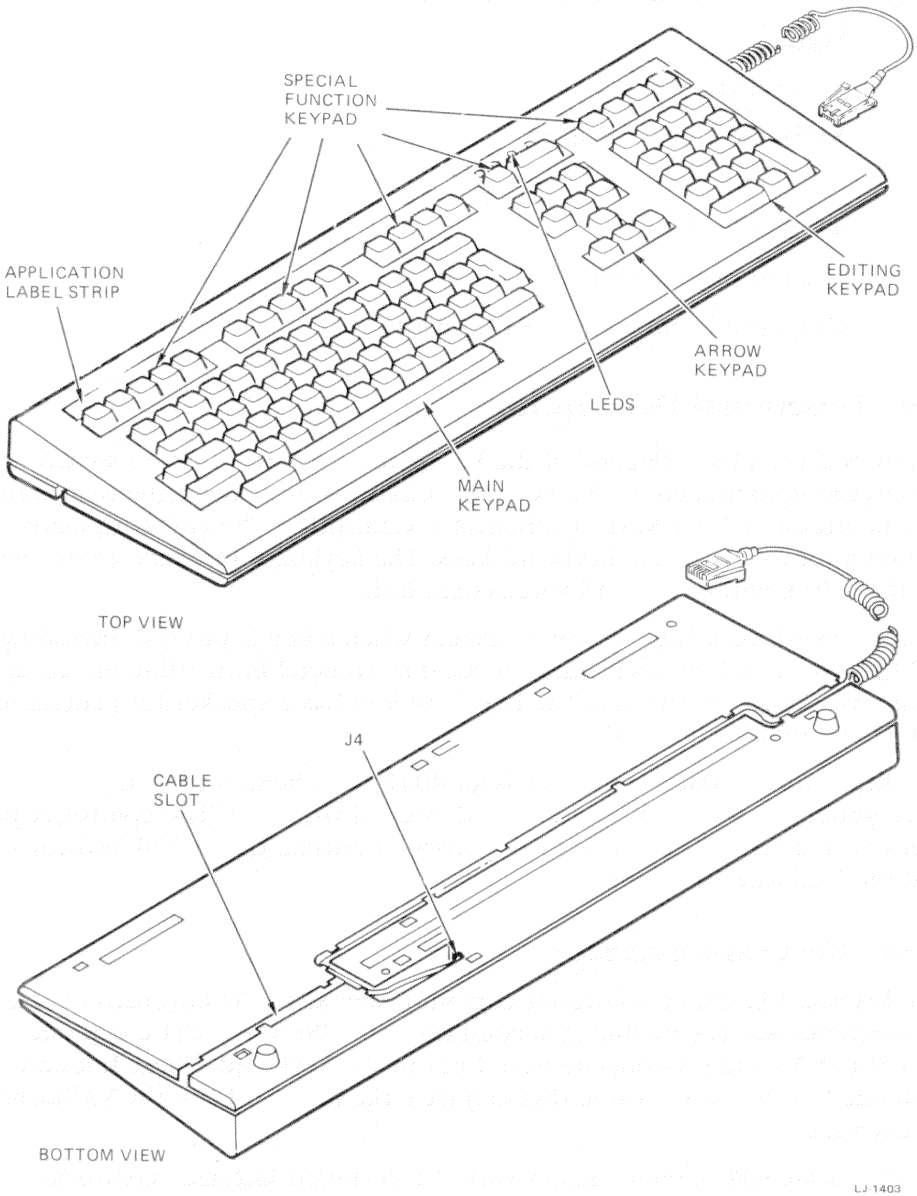


Figure 8-1 LK250 Keyboard

The signals on the keyboard cable are as follows.

Pin	Signal
1	Ground (connected to pin 5)
2	Keyboard clock / Request L
3	Keyboard data
4	+5 V to keyboard
5	Ground to keyboard
6	CTRL (no connection in CPU board)

8.3 Functional Description

Figure 8-2 is a block diagram of the keyboard circuitry. All logic shown in this figure is contained on the keyboard circuit board except the Keyboard Matrix circuit and the Keyboard Interface Controller. The keyboard matrix circuit appears below the keyboard keys. The keyboard interface controller is on the CPU board in the VAXmate system unit.

The keyboard has a logic matrix to detect when a key is pressed, including a 7.373 MHz crystal, an 8051 microprocessor, an octal buffer/line driver, and a binary-to-decimal decoder. The keyboard also has a speaker for generating key clicks and a bell sound.

The keyboard interface controller is an 8042 peripheral interface microprocessor with Digital-developed internal firmware. The controller provides both a physical and a logical interface between the LK250 keyboard and the VAXmate CPU module.

8.3.1 Keyboard Interface

The keyboard interface controller communicates with the keyboard over a bidirectional serial data line. A second line provides the serial clock rate. Power (+5 V) and ground also have lines to the keyboard. These lines are contained in the coiled cable that connects the keyboard and the VAXmate workstation.

The VAXmate CPU communicates with the keyboard interface controller through bidirectional, 8-bit, parallel I/O data lines (IOD7-0 H).

The interface at J6 provides standard TTL signal levels and communicates with the keyboard using bidirectional protocol. The interface transfers character information in groups of 8-bit patterns.

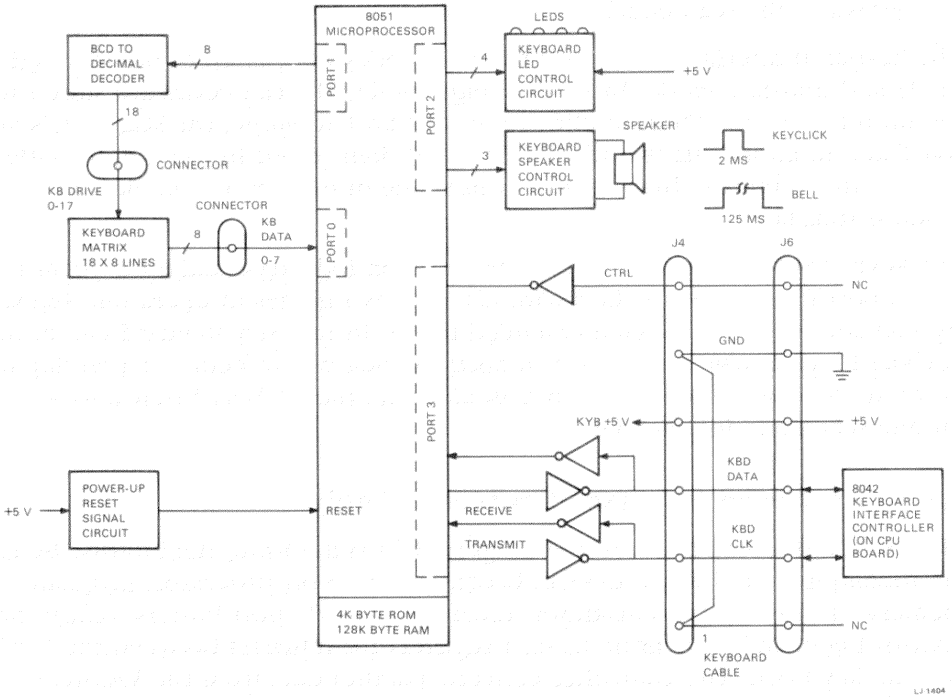


Figure 8-2 Keyboard Block Diagram

8.3.2 Logical Interface

The logical interface on the 8051 generates scan codes to send to the 8042. The term scan code means a stream of one or more byte values that represents the pressed or released state of a key. The act of pressing or releasing a key generates the scan code.

The keyboard interface controller has two modes of operation: pass-through mode and translate mode. In pass-through mode, all scan codes are stored in the output buffer without modification. In translate mode, the scan codes are translated to an industry-standard value, and then stored in the output buffer. Bit 6 of the command byte controls this mode of operation. The default mode is translate.

The keyboard has keys that are not available on industry-standard keyboards. To support these keys, the keyboard also has two modes of operation: industry-standard mode and Digital-extended mode. In industry-standard mode, the keyboard may transmit a series of industry-standard scan codes, depending on other modes that are in effect. In Digital mode, the keyboard transmits a unique scan code for each key.

8.3.3 Keyboard Interface Controller Logic

The keyboard interface controller (Figure 8-3) is a 40-pin, dual-in-line 8042 microcomputer peripheral device. It contains an 8-bit processor, program memory, data memory, transmitter, receiver, two I/O port buffers, read/write control logic, and asynchronous data registers for transfers between the CPU and the keyboard. The controller converts parallel data from the VAXmate CPU (IOD7-0 H) into serial data for transmission to the keyboard (KBD DATA). It also converts serial data from the keyboard, as Test 1 input to the controller, into parallel data that goes back to the CPU. When the processor in the controller is ready, it generates an interrupt request (IRQ1 H) to signal the VAXmate CPU that data is ready in its internal data register.

The keyboard interface controller also provides several hardware control functions that are unrelated to the keyboard. (See Section 8.3.5.)

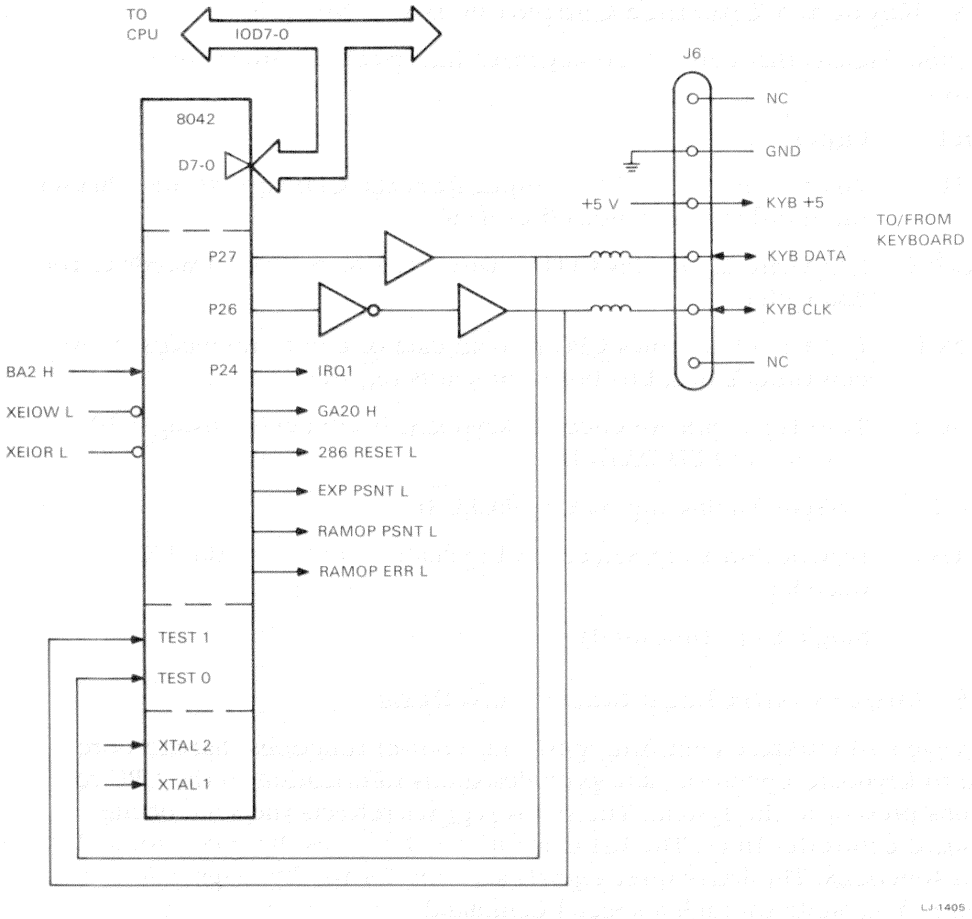


Figure 8-3 Keyboard Controller Block Diagram

8.3.4 Keyboard Interface Controller Input Signals

The input signals that control the keyboard interface controller are as follows.

Signal	Function
BA2 H	Bus Address 2 H: Address input from the CPU to indicate whether the transfer is a command or data
XEIOW L	I/O Write L: Enables CPU to write data or command words to the controller
XEIOR L	I/O Read L: Enables CPU to read data or command words in the controller's data bus buffer or status register
TEST 0,1	Test: Input pins to check if keyboard is connected using KBD CLK H and KBD DATA H
XTAL 1,2	Crystal: Timing inputs for DPCLK H
IOP CS L	In/Out Port Chip Select L: Chip select input from the I/O decoder
SS L	Single Step: (not used)

8.3.5 Other Control and Status Functions

The keyboard interface controller performs control functions that are unrelated to keyboard operation, and provides status information to the CPU for options present in the system. The status register reflects the state of the keyboard controller lines. The list that follows describes these control and status functions. The latter three signals are only for use by diagnostics, and are only accessible through a special command.

Signal	Function
286 RESET L	286 Reset L: Reset the VAXmate 80286 CPU
GA20 H	Gate 20 H: Gate address line 20
EXP PSNT L	Expansion Box Present L: VAXmate expansion box present
RAMOP PSNT L	RAM Option Present L: Expansion memory option present
RAMOP ERR L	RAM Option Error L: Expansion memory error

8.4 LK250 Keyboard Logic

The following paragraphs describe the logic on the keyboard circuit board.

8.4.1 Keyboard Matrix Scanning

The key locations have an 18 × 8 line matrix. Each key switch connects across a matrix intersection. This gives a fixed position for each key in the matrix. The matrix accommodates all 105 keys on the keyboard.

Figure 8-4 is a simplified block diagram of the matrix scanning circuit. Eight lines from port 1 of the 8051 microprocessor go to the input lines of two 74LS145 BCD-to-decimal decoders. Ten outputs from one decoder and eight outputs from the other decoder provide the drive lines (KB DRIVE 17-0) for the matrix.

The other axis of the matrix consist of eight lines at +5 V through pull-up resistors. These lines (KB DATA 7-0) go to port 0 of the 8051 microprocessor.

The 8051 scans the 18 drive lines and reads the 8 data lines for key closures. After verifying that the key closure occurred by scanning the lines again, the 8051 firmware translates the position information into a scan code, and transmits it to the system central processor through the keyboard interface controller.

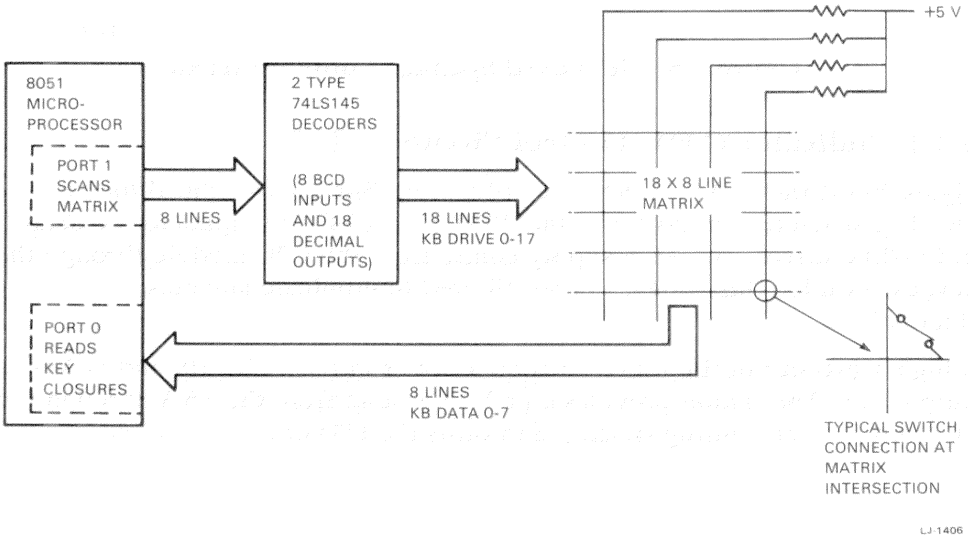


Figure 8-4 Matrix Scanning Circuit Block Diagram

8.4.2 Keyboard Speaker Control Circuit

Figure 8-5 is the speaker control circuit. The 8051 microprocessor controls three output lines to an octal buffer/line driver (74LS240), which drive the base of the drive transistor. The 8051 sets up the three lines by adding one of eight binary combinations to the input to the octal buffer/line driver. The firmware in the 8051 generates a tone by applying a square wave to the speaker through the drive transistor. The time that the tone is on determines if a bell or click sound is used. The number of buffer/line drivers used determines the volume.

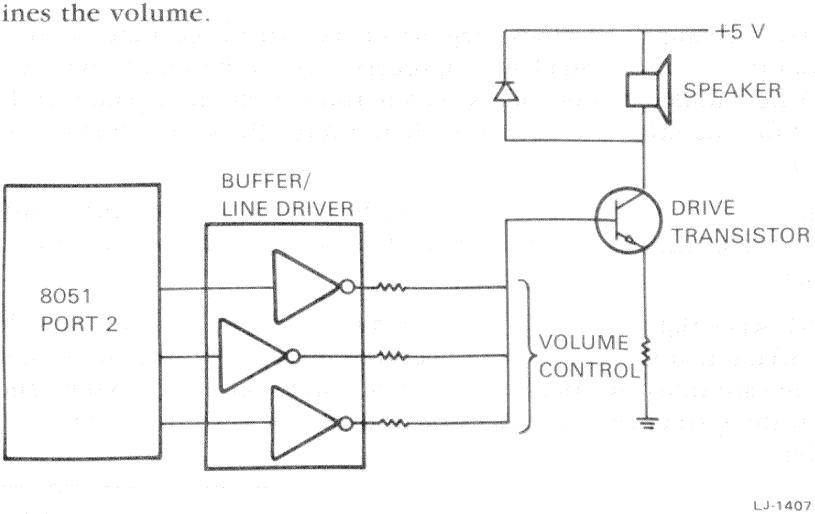


Figure 8-5 Keyboard Speaker Control Circuit

8.4.3 Indicator (LED) Control Circuit

Figure 8-6 is the LED indicator control circuit. The control signal for each LED is generated from port 2 of the 8051 to one of four inputs to the octal buffer/line driver. The +5 V supply comes from the CPU module through the keyboard cable. This voltage is then filtered to eliminate any noise fluctuations.

A high signal out of the 8051 turns on a driver in the 74LS240, and makes its output low. This action provides a path to ground from the +5 V through the LED and current limiting resistor, and turns the LED on.

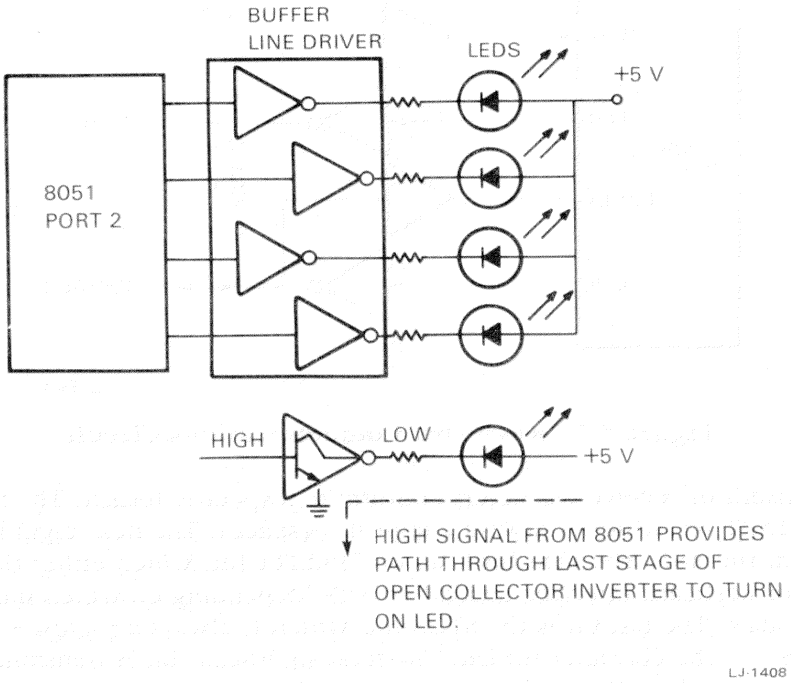


Figure 8-6 Keyboard Indicator Control Circuit

8.4.4 Keyboard Communications Circuit

The keyboard scan codes and other special codes go from the 8051, through 74LS05 line drivers and the keyboard cable to the keyboard interface controller on the CPU board (Figure 8-7). The lines are bidirectional, meaning that either the system or the keyboard can drive the lines.

The 8051 firmware contains features that the system central processor can enable, such as keyboard transmission characteristics and control signals for the LED indicators and the speaker. These commands come from the CPU, through the keyboard interface controller on the DATA and CLOCK/REQ lines. A 74LS05 line receiver inverts the signal and places it at the port 3 input to the 8051.

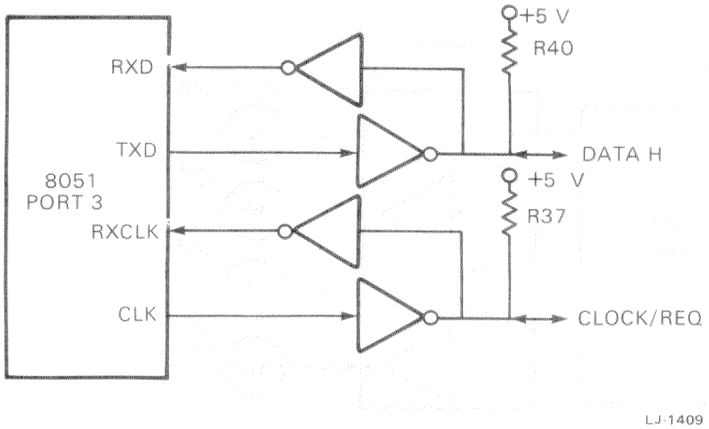


Figure 8-7 Keyboard Communications Circuit

The transmit or receive characters conform to a specific format. The first bit is the START bit, which is always a logical 0 (space). The next eight bits represent the data. The next bit is an odd PARITY bit, which either the LK250 or keyboard interface controller adds, depending on which module is sending data. The last bit is the STOP bit, which is always a logical 1 (mark). Figure 8-8 is the character format. The least significant bit is transmitted first. Separate clock line signals synchronize the data. (See Keyboard Protocol, Section 8.6.)

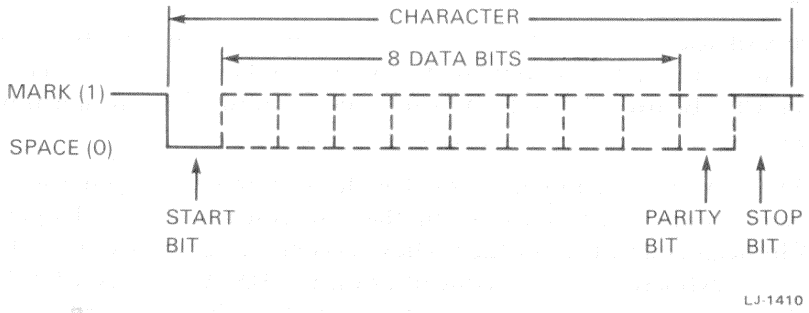


Figure 8-8 Keyboard Transmit and Receive Character Format

8.4.5 Keyboard Reset Signal

Whenever you turn the system on, the 8051 in the keyboard is reset to allow it to start operating. A reset generator turns on and applies +5 V to the reset input to the 8051. The generator holds this input high long enough for the 8051 to complete the reset process; then, the reset generator shuts off.

8.5 Keyboard Controller Diagnostics

At power-up, the keyboard controller executes a diagnostic test. The test verifies the keyboard controller's ROM and RAM. If an error occurs during power-up testing, the keyboard controller will not respond to any input and must be reset (powered-down).

The keyboard controller completes the test within 200 ms after power-up. During the power-up test, the controller ignores inputs from the keyboard keys. At the completion of testing, the diagnostic sends an error or ok indication to the keyboard interface controller, if possible. The error indication is ERROR; the O.K. indication is AAH.

8.6 Keyboard Protocol

Because the keyboard has two modes, and both the keyboard interface controller on the CPU board and the 8051 microprocessor in the keyboard can control the data and clock lines, the keyboard needs some protocol to exchange data. The protocol is as follows.

1. The keyboard always supplies clock signal during data transfers.
2. The system can override the keyboard any time, except during the stop bit.
3. The system must request use of the data line.
4. An error automatically results in a Resend.
5. Other command specific protocol conditions may apply.

8.6.1 VAXmate and Industry-Standard AT-Compatible Protocol

Normally, both the KBD DATA and the KBD CLOCK lines are high, and the driving circuit pulls them low. As you press a key, the 8051 pulls the clock and the data circuit low, and sends the data to the keyboard controller. If the keyboard interface controller holds the clock line low, it aborts any output

from the keyboard (except during a stop bit). The keyboard interface controller uses this Inhibit signal to stop any additional transmission from the keyboard until the keyboard interface controller processes the current data. If the keyboard interface controller detects an error in transmission from the keyboard, the keyboard interface controller turns the inhibit signal into Request to Send and Resend commands to the keyboard. If the keyboard interface controller receives data for the CPU, it holds the keyboard disabled, interrupts the CPU (IRQ1 H), and waits for the CPU to acknowledge the interrupt and read the data, before enabling the keyboard.

The keyboard must complete sending a data byte within 2 ms, or a timeout error will occur. The keyboard must respond to a keyboard interface controller command within 20 ms.

8.6.2 Keyboard Interface Controller to Keyboard Transmission

The keyboard interface controller commands and values are similar to those that the keyboard transmits, except they have a 90 degree phase shift between the clock and data pulses. This phase shift occurs because the keyboard generates the clock pulses for the keyboard interface controller. The keyboard interface controller must request the keyboard to provide the clock using the following protocol.

1. The keyboard interface controller lowers the clock line, thus disabling keyboard.
2. The keyboard interface controller lowers the data line.
3. After 60 μs (min), the keyboard interface controller releases the clock line.
4. The keyboard interface controller waits for the keyboard to drive the clock line.

After the keyboard interface controller sends the parity bit, the keyboard sends the stop bit, which notifies the keyboard interface controller that the keyboard received the data.

8.7 Keyboard Scan Codes

When a key is pressed, the keyboard sends a scan code that identifies the key. If the key is held down for a time that exceeds the auto-repeat delay time, the scan code is sent repeatedly at the auto-repeat rate. When a key is released, a release code of F0H is sent, followed by the scan code of the released key.

If bit 6 of the keyboard interface controller command byte is set, the keyboard interface controller converts the keyboard scan code value to an industry-standard one byte value. With this value, a released key is indicated by adding 80H to the one byte value of the pressed key.

No conversion is performed if bit 6 of the keyboard interface controller command byte is clear. This is the default value at power-up. The power-up firmware changes the value so the default is Translate.

See the *VAXmate Technical Reference Manual* (Q6ZCS-GZ) for the LK250 scan codes.

Chapter 9
VAXmate Workstation Power Supply (H7270)

9.1 Introduction

The VAXmate power supply receives ac input (either 100 to 120 Vac or 200 to 240 Vac), and generates five regulated output dc voltages, an unregulated 300 V (±150 Vdc) output for the VAXmate expansion box, and a system control signal indicating that there is sufficient energy to allow system operation. To provide the required efficiency, the power supply operates in a switching mode at 100 kHz. To protect against overvoltage and overcurrent conditions, the power supply has a sensing circuit. To protect against electrical hazards, the power supply has an externally-replaceable fuse.

The power supply is on a single printed circuit board within the system box. A board-mounted jumper plug sets the input voltage range, with the following option number variations.

Option	Input Voltage	Output Power
H7270-AA	100 – 120 Vac rms nominal	90 watts*
H7270-AB	220 – 240 Vac rms nominal	90 watts*

* Output power does not include the 300 V power for the expansion box, which is 111 W (maximum).

Line Voltage and Current

H7270-AA

Voltage – 100 to 120 Vac nominal, single-phase, two wire plus safety earth ground, 90 V rms to 128 V rms (255 V to 362 V, peak to peak).

Current – 4.4 A (rms) maximum at 88 Vac input. Nominal is 3.9 A at 100 Vac, 2.6 A at 120 Vac.

H7270-AB

Voltage – 220 to 240 Vac nominal, single-phase, two wire plus safety earth ground, 180 V rms to 256 V rms (509 V to 724 V, peak to peak).

Current – 2.2 A (rms) maximum at 176 Vac input. Nominal is 1.8 A at 220 Vac, 1.6 A at 240 Vac.

Line Frequency

The line frequency can be 47 Hz minimum to 63 Hz maximum.

Fuse

An externally replaceable fuse protects the input wiring. The fuse is either of the following:

- 6A, 250 V AGC normal blow fuse for 100 – 120 Vac
- 3A, 250 V UL-approved for 220 – 240 Vac

Real Input Power

The input maximum real power is 236 watts at full-rated, regulated dc output load of 89 watts, plus 111 watts to the auxiliary power converter for the VAXmate expansion box.

Power Supply Connectors – The power supply board, which receives ac voltage on input connector J1, has the pin outputs shown in Table 9-1.

Table 9-1 Power Supply Output

Pin No.	Output	Connects To
1	+HV DC (left pin on component side)	J2 HV DC (300 V) to the expansion box
2	Key	
3	Safety ground	
4	NC	
5	–HV DC	
1	+12 V	J3 to the disk drives
2	Return	
3	Return	
4	+5 V	
1	Key	J4 to the monitor
2	+28 V	
3	Return	
4	–12 V	
5	Return	
6	+12.1 V	
7	Return	
8	Key	

Table 9-1 Power Supply Output *(cont.)*

Pin No.	Output	Connects To
1	AC OK H	J5 to the CPU board
2	Key	
3	−12 V	
4	Return	
5	+12 V	
6	Return	
7	+5 V	
8	+5 V	
9	+5 V	
10	+5 V	
11–14	Return	
15	−9 V	
16	−9 V return	

9.2 Physical Layout

Figure 9-1 is the layout of the major components on the power supply board.

WARNING
The heat sink for transistor Q1 carries hazardous voltage. It is connected to the 300 V (+HV DC).

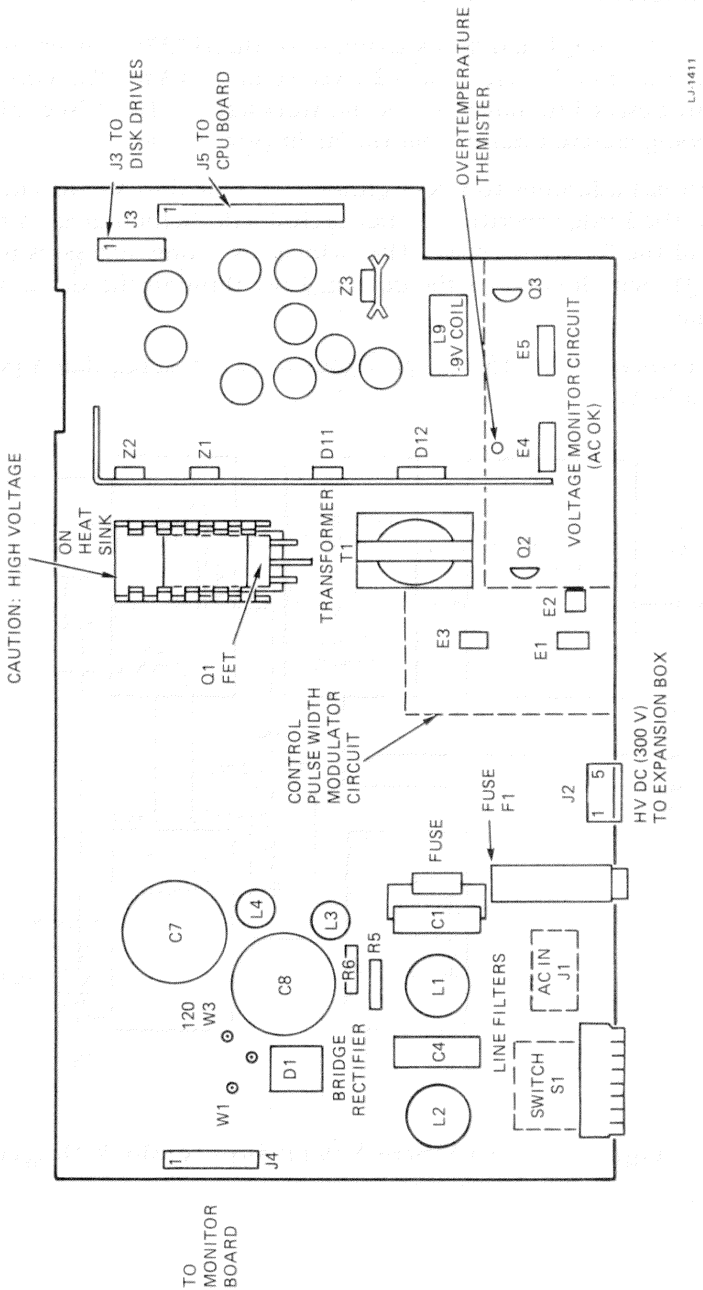


Figure 9-1 VAXmate Power Supply

9.3 Functional Description

Figure 9-2 is a simplified block diagram of the H7270 power supply. The line voltage comes in at J1, either at 120 Vac or at 240 Vac. The emi line filters keep main power line noise out of the workstation. The filters also prevent workstation-generated noise from the main power line.

The board has a jumper to select either 120 V or 240 Vac input. With either selection, the bridge rectifier output is 300 Vdc, which goes to the primary winding of the T1 transformer. The primary winding also goes to an electronic switch, Q1, which controls the current flow through the primary of the transformer.

This high voltage dc (±150 V) also goes to J2 for unregulated power to the expansion box.

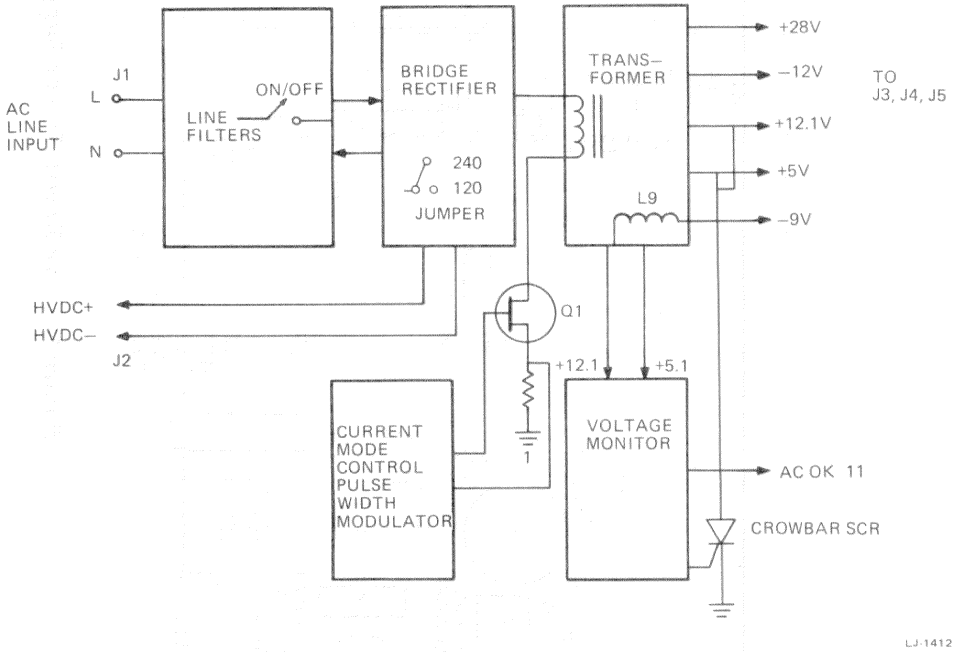


Figure 9-2 VAXmate Power Supply Block Diagram

A current-mode control pulse width modulator turns Q1 off and on at a 100 kHz rate, to switch the voltage across the primary side of the transformer.

The transformer has four secondary windings that produce the required voltages for the CPU board, the disk drives, and the monitor. They are +5.1 V, +12.1 V, −12 V, and +28 V. The isolated −9 V for the network interface comes from the L9 inductor.

A voltage monitor senses the transformer output and generates the AC OK H signal to let the CPU processor know that sufficient power is present for normal power supply operations.

9.4 Power Supply Circuit

Figure 9-3 is a simplified illustration of the power supply circuit. The ac line input goes to J1. One side of the ac line (phase) goes to the fuse, emi line filters, and an on/off switch. The ac voltage goes to a full-wave bridge rectifier (D1) that converts the ac voltage into dc voltage.

The other side of the ac input line (neutral) connects to the emi filters, the on/off switch, and a board-mounted plug selectable jumper for ac input voltage range selection. If the pin labeled 120 on the etch is connected, the ac voltage uses a voltage doubler circuit. If the other pin is connected, the 240 Vac circuit is a full-wave bridge rectifier. The bridge rectifier output is the same ±150 Vdc), and goes to the primary winding of the T1 transformer, regardless of the ac line selected.

When the input voltage is applied, the specified peak current is reached every half cycle. Following this inrush of current, there may be repetitive peaks for up to ten cycles before a steady state of operation is reached. The L1 and L2 inductors provide line filtering, using opposite phased voltages to impede the transmission of emi spikes and noise, both from the main power line to the workstation, and from workstation to the main power line.

The secondary of the transformer has four separate windings for each of the dc voltages. They are +5.1 V, +12.1 V, −12 V, and +28 V. The −9 Vdc output is generated from the L9 forward inductor. Filtering of common-mode switching noise on this output is affected by the L10 inductor. Diodes in each circuit provide half-wave rectifying, filtering, and shunt regulation. The 7912 is a −12 V, three terminal, linear regulator. The LM317 is an adjustable positive voltage regulator set for +28 V.

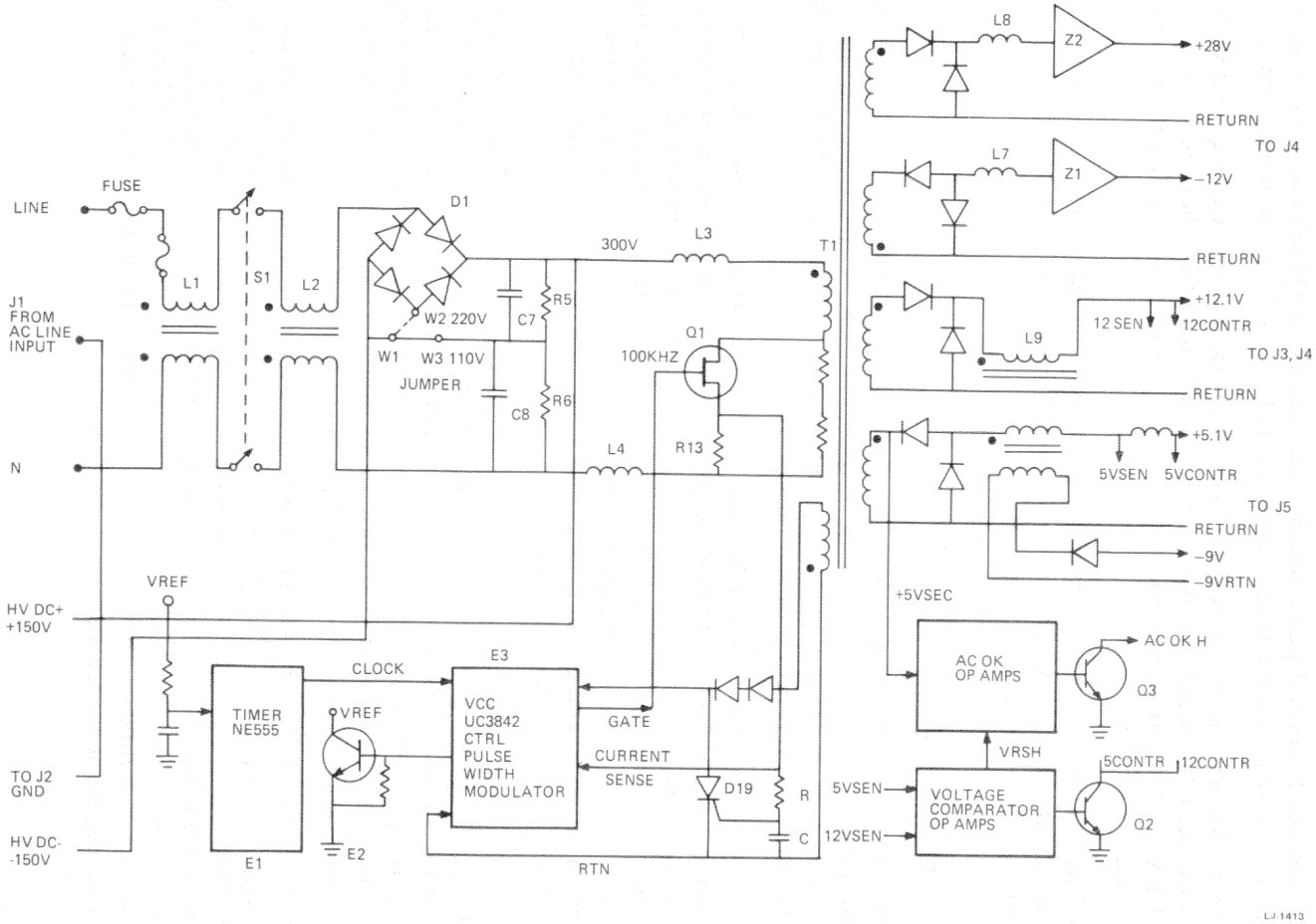


Figure 9-3 VAXmate Power Supply Simplified Circuit Diagram

9.4.1 Control Pulse Width Modulator Circuit

The Control Pulse Width Modulator circuit uses an NE555 timer. An RC circuit at its input sets the output pulses for whatever frequency you need. In this circuit, it is set for 100 kHz. The output of the timer goes to the clock input on the UC3842, a current-mode control pulse width modulator.

E2 (H11AV1A) is an opto-coupler that senses current and is used in the feedback loop. The current that goes through this device generates a current in the primary side of the power supply. This current is used to set the current in the switching transformer.

E3 determines the time that the switching transistor Q1 is on. Bias voltage for E3 during power up comes through resistors R9 and R10. Once transformer T1 is in operation, a primary winding (pins 1 and 2), operated in flyback mode, provides the bias voltage to the pulse width modulator. The output of E3 goes to the gate input on the switching transistor. Q1 is a metal oxide semiconductor field-effect transistor (MOSFET). Q1 turns on and off, sets the current in the primary of the transformer, and switches the 300 V across the transformer at 100 kHz.

9.4.2 Voltage Monitor

The voltage monitor has two circuits: a voltage comparator crowbar circuit for turning off the power supply if an over-voltage occurs, and an AC OK circuit to let the CPU processor know that sufficient mains power is present for normal power supply operation.

9.4.2.1 Crowbar Circuit

The crowbar circuit senses overvoltage conditions, and it provides protection against this condition. R13, a current sense resistor, monitors the current through the T1 transformer and Q1, the power switch field effect transistor. When R13 detects an overcurrent condition, a silicon controlled rectifier (SCR) D19 fires, shutting down the power supply. Toggling the on/off switch restores normal operation.

The 5 V sense signal (5VCONTR) on the +5 Vdc line, and the 12 V sense signal (12 VSEN) on the +12.1 V line from the secondaries of the transformer, monitor the voltage levels. These signals go to the operational amplifier, E4 (324), which is used as a comparator. It sends the error through an opto-coupler H11AV1A to feed this error back to the primary side of the pulse width modulator for voltage regulation.

When the E4 comparator detects an overvoltage condition, or an over temperature condition through temperature resistor R62, transistor Q2 shorts the +5 V and +12 V outputs. This creates an overcurrent condition, which then trips D19, the silicon-controlled rectifier primary shutdown circuit. In the event that the tolerance of either +5.1 V or +12.1 is exceeded, the power supply shuts down. Again, toggling the on/off switch restores normal operation.

9.4.2.2 AC OK Circuit

The AC OK circuit uses operational amplifiers (op-amps) as comparators.

AC OK H, when asserted, indicates to the CPU processor that sufficient mains power is present, and implies that the workstation and expansion box power supplies are ready for normal operation. AC OK H goes high between 0.35 and 1.15 seconds after detection of the mains power. This signal stays high a minimum of 0.5 ms before dc output voltages go out of specification following a mains failure or simply switching the system unit off (Figure 9-4).

The rise time (10% to 90%) and fall time (90% to 10%) is 1.0 ms (maximum).

The CPU processor may use AC OK H either as an asynchronous system reset at power up, or as a 0.5 ms (minimum) warning that the power supply outputs are about to go out of specification due to the removal of the main power. Note that under the condition of a load fault (for example, a short circuit) or power supply failure (for example, a component failure), this circuit does not guarantee that AC OK H will provide any warning of the power supply outputs going out of specification.

Table 9-2 shows the characteristics of the AC OK H output.

Table 9-2 AC OK H Signal Characteristics

State (AC OK)	Voltage Output (VOL)	Current Output (IOL)
Low (negated)	<0.4	+10.0 mA
High (asserted)	5.0	<+20.0 μA

AC OK H remains asserted when

- AC input voltage > or = nominal line voltage for at least 200 ms (see Section 9.5.1)
- Input power is removed for one half cycle (at 50 or 60 Hz at an arbitrary point in the waveform)

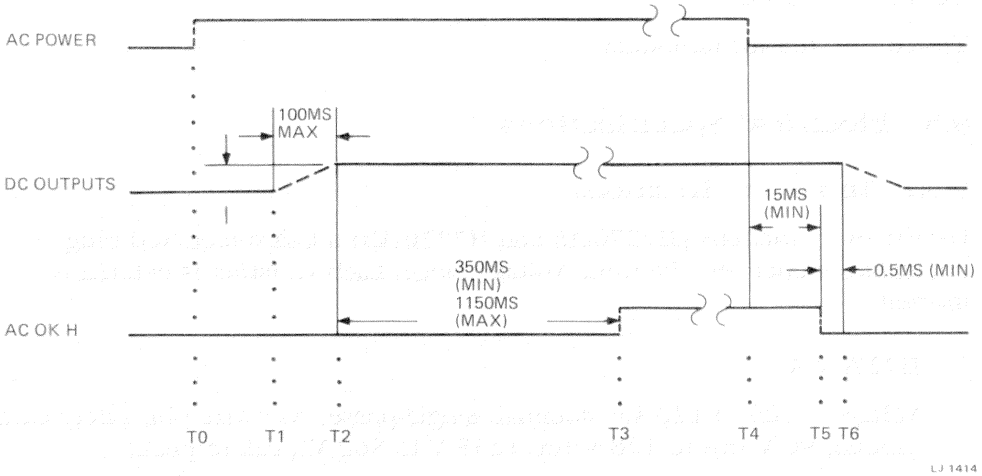


Figure 9-4 AC OK H Timing Diagram

Event	Definition
T0	AC power applied
T1	DC output voltages begin to rise
T2	DC output voltages in regulation
T3	AC OK H asserted
T4	AC power removed
T5	AC OK H negated immediately upon detection of no ac power
T6	DC output voltage regulation guaranteed until this time

Interval	Duration Specification
T0–T1	Not specified
T1–T2	100 ms maximum (5.1 V output only)
T2–T3	350 ms minimum, 1150 ms maximum
T4–T5	15 ms minimum
T5–T6	0.5 ms minimum

9.5 Electrical Specifications

9.5.1 Input Specifications

For the two variations (H7270-AA and H7270-AB) a board-mounted plug selectable jumper sets the input voltage range. Each variation is externally marked.

H7270-AA

Voltage – 100 to 120 Vac nominal, single-phase, two wire plus safety earth ground, 90 V rms to 128 V rms (255 V to 362 V, peak to peak).

Current – 4.4 A (rms) maximum at 88 Vac input. Nominal is 3.9 A at 100 Vac, 2.6 A at 120 Vac.

H7270-AB

Voltage – 220 to 240 Vac nominal, single-phase, two wire plus safety earth ground, 180 V rms to 256 V rms (509 V to 724 V, peak to peak).

Current – 2.2 A (rms) maximum at 176 Vac input. Nominal is 1.8 A at 220 Vac, 1.6 A at 240 Vac.

Line Frequency

The line frequency can be 47 Hz minimum to 63 Hz maximum.

Fuse

An externally replaceable fuse protects the input wiring. The fuse is either of the following:

- 6A, 250 V AGC normal blow fuse for 100 to 120 Vac
- 3A, 250 V UL-approved for 220 to 240 Vac

Real Input Power

The input maximum real power is 236 watts at full-rated, regulated dc output load of 89 watts, plus 111 watts to the auxiliary power converter for the VAXmate expansion box.

9.5.2 Output Specifications

Table 9-3 summarizes the output voltage and current ranges.

Table 9-3 Output Voltage Summary

Output (V)	Voltage (min)	Voltage (max)	Current (A min)	Current (A max)	Ripple (max pk-pk)
+ 5.1	+ 4.85	+ 5.35	6.40	10.24	100 mV
+ 12.1	+ 11.50	+ 12.70	0.17	1.37	100 mV
- 12.0	- 11.40	- 12.60	0.12	0.33	50 mV @ < 500 Hz; 100 mV @ > 500 Hz.
+ 28.0	+ 26.60	+ 29.40	0.45	0.55	50 mV @ < 500 Hz; 100 mV @ > 500 Hz.
- 9.0	- 8.55	- 9.45	0.18	0.20	100 mV
300.0	240.00	375.00	0.00	0.46	

NOTE

The –9 V output is nominally isolated from both primary and secondary windings of the power supply. A small value of conductance is included between the returns of the –9 V output and the power supply secondary return, to keep the –9 V portion of the system circuit from acquiring a significant static charge.

9.5.3 Temperature

System ambient temperature is 15 – 32° C (59 – 90° F). System shutdown occurs for temperatures above 32° C (90° F).

9.5.4 Safety

The power supply specified is Underwriters Laboratories (UL) recognized, Canadian Standards Association (CSA) certified, and in compliance with International Electrotechnical Commission IEC 380 and IEC 435 (verified by an independent testing firm). The system is an IEC Class One product.

Appendix A
VAXmate
Workstation Specifications

VAXmate Workstation

The VAXmate workstation consists of a base system unit that includes a CPU, I/O video module, power supply and diskette drive, a keyboard, and a mouse.

System Unit

Physical Dimensions

Height	28.57 cm (11.25 in) (at highest point)
Width	40.64 cm (16 in) (at widest point)
Depth	38.1 cm (15 in)
Footprint	609.6 sq cm (240 sq in)
Weight	15 kg (35 lbs)

CPU

Processor	80286 processor
Memory	1 Mbyte RAM

Power Supply

Type	100 KHz
AC input (120 V or 220 V)	
120 V (nominal)	90 to 128 V rms
220 V (nominal)	180 to 256 V rms

Line current	
120 V (nominal)	±2.7 Vac nominal
220 V (nominal)	±1.8 Vac nominal
AC power consumption	312 watts nominal
Regulated voltages	+5.1, +12.1, −12, +28 and −9 Vdc
Unregulated voltages	±150 Vdc
Circuit protection	fuse
Over-temperature protection	thermister control

Environment – Class A

Ambient operating temperature	15°C (59°F) to 32°C (90°F)
Relative humidity	8% to 80%
Maximum wet bulb (non-condensing)	25°C (77°F)
Altitude (maximum)	
Operating	up to 8,000 feet
Non-operating	up to 30,000 feet

Workstation System Expansion

PC50X-AA memory	2 Mbytes customer-installable card
FP287 math coprocessor	80287 numeric data coprocessor for floating point operations
Expansion box	20- or 40-Mbyte hard disk drive and two industry standard option slots (See Chapter 7.)
PC50X-MA integral modem (North America)	Hayes compatible 300/1200/2400 baud

Monitor

The following are specifications for the monochrome monitor on the VAXmate workstation.

CRT	340 mm (14 in.) diagonal, 13-inch viewable, amber or green phosphor; 20 mm (0.788 in) neck diameter; 90 degree deflection 770 mm (30 in) front curvature.
Active Display	240 mm horizontal by 150 mm vertical (9.5 × 6 in)
Resolution	640 pixels horizontal by 400 pixels vertical 800 pixels horizontal by 250 pixels vertical
Horizontal scan rate (Line sync)	26.40 kHz (640 × 400) / 26.49 kHz (800 × 250)
Vertical scan rate (Field sync)	60 Hz noninterlaced
Video pixel clock	22.384 MHz (640 × 400) 27.984 MHz (800 × 250)
Average power	16 W

I/O-Video Module

Text display:	
Soft font (loadable)	256 characters
Soft font (matrix)	8 pixels horizontal by 16 pixels vertical
Video input	4-bit TTL, 16 intensity levels
CGA-compatible modes	80 column × 25 row text 40 column × 25 row text 640 × 200 × 2 color bit map graphics 320 × 200 × 4 color bit map graphics
Additional modes	640 × 400 × 2 color bit map graphics 640 × 400 × 4 color bit map graphics 800 × 250 × 4 color bit map graphics 320 × 200 × 16 color bit map graphics

Diskette Drive Read/Write Capability

Read/Write	1.2 Mbytes IBM PC-AT 5-1/4 diskettes
Read/Write	0.4 Mbytes Digital RX50 5-1/4 diskettes
Read-only	0.36 Mbytes IBM PC-XT 5-1/4 diskettes

Keyboard

Physical Description (Low-profile, detachable)

Height	5 cm (2 in) at highest point
Length	53.3 cm (21 in)
Width	17.1 cm (6.75 in)
Weight	2 kg (4.5 lbs)
Audio and visual indicators	4 lights and bell tone generator
Cord	1.9 m (6 ft) coiled cord; 6 pin, modular connector on keyboard end; 6 pin, shielded connector on workstation end; plugs into right side of workstation
Keypad	Sculptured key array
Home row key height	3 cm (1.2 in) above desktop
Power	+5 V ±5% @ 275 mA, 1.4 W maximum

Mouse

Physical Description

Size	8.8 cm (3.5 in) diameter, 4.0 cm (1.6 in) high
Weight	170 grams (6 oz) including cable
Switches	Three tactile feel switches actuating force 0.8 newtons (3 oz) ±25%
Cable	1.5 m (5 ft) round, .375 cm (0.15 in) diameter, six conductor, #26 stranded, shielded, flexible cable
Connector	7-pin miniature circular type (male)

Electrical Specifications

Power	+5 volts ±5 % at 130 mA, −8 to −13 volts at 20 mA (RS-232 mode)
Interface	Digital ThinWire
Ethernet Port	Includes a T-connector, terminator, and 3.6 m (12 ft) cable
Serial Communications Port	Includes a modem control
Serial Printer Port	6-pin modular jack

Table A-1 lists the power consumption of the VAXmate system unit.

Table A-1 System Unit Power Comsumption (Maximum Amps and Power)

Component	+5.1 V	+12.1 V	−12.0 V	+28.0 V	−9.0 V	Watts
CPU board (max)	Amps 4.486	Amps 0.013	Amps 0.013	Amps 0.000	Amps 0.000	23.192
I/O-video board	3.100	0.060	0.039	0.000	0.200	18.806
Monitor board (max)	0.200	0.250	0.250	0.550	0.000	22.445
RX33						
Start-up (400 ms)	0.630	1.000	0.000	0.000	0.000	15.313
Read/write	0.550	0.600	0.000	0.000	0.000	10.065
2 Mbyte memory	0.600	0.000	0.000	0.000	0.000	3.060
Integral modem	0.750	0.040	0.030	0.000	0.000	4.669
LK250 (external)	0.220	0.000	0.000	0.000	0.000	1.122
Mouse (external)	0.250	0.000	0.000	0.000	0.000	1.275
TOTAL						
steady-state	10.156	0.963	0.332	0.550	0.200	84.633
peak	10.236	1.363	0.332	0.550	0.200	89.881

The VAXmate workstation power supply and the expansion box power regulator provide a total of 28.5 watts of power to the expansion box card cage (9.5 watts per option slot). The hard disk controller occupies the top option slot

(when installed). A total of 19 watts is available for any industry-standard options in the remaining two slots. Each option slot accepts options that use an 8-bit and/or 16-bit industry-standard bus and a clock frequency of 8 Mhz.

Table A-2 lists power consumption in the expansion box.

Table A-2 Expansion Box Power Consumption (Maximum)

Component	+5.1 V	+12.1 V	−12.0 V	−5.0 V	Fan	Watts
RD31 (max)	Amps	Amps	Amps	Amps	Amps	38.80
Start-up (20 sec)	1.2	2.600	0.0	0.0		
Operating:						
idle	0.6	0.900	0.0	0.0		15.50
random seek	0.6	1.100	0.0	0.0		17.50
RD32 (max)						
Start-up (20 sec)	1.3	2.000	0.0	0.0		32.00
Operating:						
idle	1.2	0.510	0.0	0.0		12.73
random seek	1.3	1.800	0.0	0.0		29.50
RCD31/32 controller	1.0	0.001	0.0	0.0		5.26
Option-1	1.3	0.100	0.1	0.1		9.54
Option-2	1.3	0.100	0.1	0.1		9.54
TOTAL						
RCD31-EA, -EC						
steady-state	4.3	1.300	0.2	0.2		41.44
peak	4.8	2.800	0.2	0.2		63.14
RCD31-FA, -FC						
steady-state	4.3	1.300	0.2	0.2	0.25	44.44
peak	4.8	2.800	0.2	0.2	0.25	66.14
RCD32-FA, -FC						
steady-state	4.9	2.000	0.2	0.2	0.25	53.84
peak	4.9	2.200	0.2	0.2	0.25	59.34

CAUTION

Never install option boards that exceed the available expansion box wattage. A single option or a combination of options that needs more then 19 watts can damage the expansion box circuitry, blow a fuse in the workstation, or damage the VAXmate workstation power supply.

Appendix B
Expansion Box
Bus Connectors

Figure B-1 is the Expansion Box bus connectors. Figure B-2 shows the signals on these connectors.

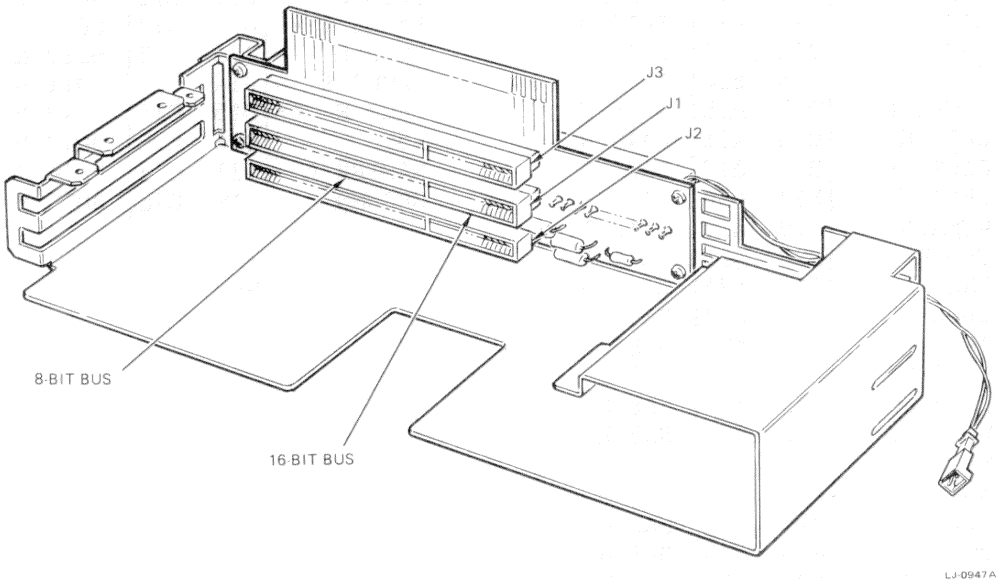


Figure B-1 Expansion Box Backplane

8-Bit Bus Connector

GROUND	B1	A1	I/O CHK L
RESET H	B2	A2	SD7 H
+5V	B3	A3	SD6 H
IRQ9 H	B4	A4	SD5 H
-5V	B5	A5	SD4 H
DRQ2 H	B6	A6	SD3 H
-12V	B7	A7	SD2 H
OWS L	B8	A8	SD1 H
+12V	B9	A9	SD0 H
GROUND	B10	A10	I/O RDY H
MEMW L	B11	A11	AEN H
MEMR L	B12	A12	SA19 H
IOW L	B13	A13	SA18 H
IOR L	B14	A14	SA17 H
DACK3 L	B15	A15	SA16 H
DRQ3 H	B16	A16	SA15 H
DACK1 L	B17	A17	SA14 H
DRQ1 H	B18	A18	SA13 H
REFRESH L	B19	A19	SA12 H
CLOCK H	B20	A20	SA11 H
IRQ7 H	B21	A21	SA10 H
IRQ6 H	B22	A22	SA9 H
IRQ5 H	B23	A23	SA8 H
IRQ4 H	B24	A24	SA7 H
IRQ3 H	B25	A25	SA6 H
DACK2 L	B26	A26	SA5 H
T/C H	B27	A27	SA4 H
ALE H	B28	A28	SA3 H
+5V	B29	A29	SA2 H
OSC H	B30	A30	SA1 H
GROUND	B31	A31	SA0 H

16-Bit Bus Connector

MEM16 L	D1	C1	SBHE L
I/O16 L	D2	C2	UA23 H
IRQ10 H	D3	C3	UA22 H
IRQ11 H	D4	C4	UA21 H
IRQ12 H	D5	C5	UA20 H
IRQ15 H	D6	C6	UA19 H
IRQ14 H	D7	C7	UA18 H
DACK0 L	D8	C8	UA17 H
DRQ0 H	D9	C9	EMEMR L
DACK5 L **	D10	C10	EMEMW L
DRQ5 H **	D11	C11	SD08 H
DACK6 L **	D12	C12	SD09 H
DRQ6 H **	D13	C13	SD10 H
DACK7 L **	D14	C14	SD11 H
DRQ7 H **	D15	C15	SD12 H
+5V	D16	C16	SD13 H
MASTER L	D17	C17	SD14 H
GROUND	D18	C18	SD15 H

** Not Implmented

LJ-1389-P

Figure B-2 Expansion Box Backplane Connector Signals

Appendix C
VAXmate CPU Module Block Diagram

Figure C-1 is the VAXmate CPU block diagram.

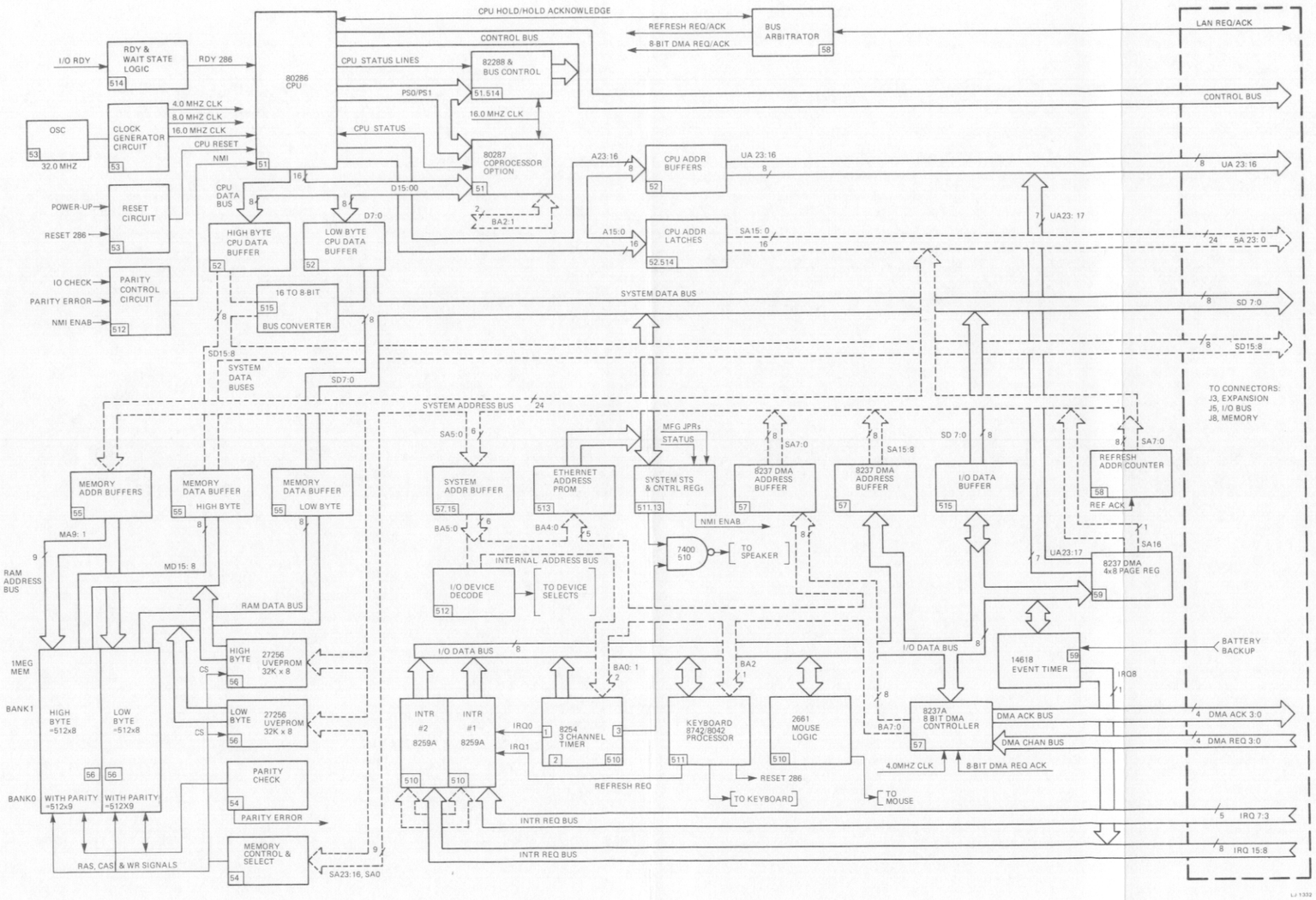
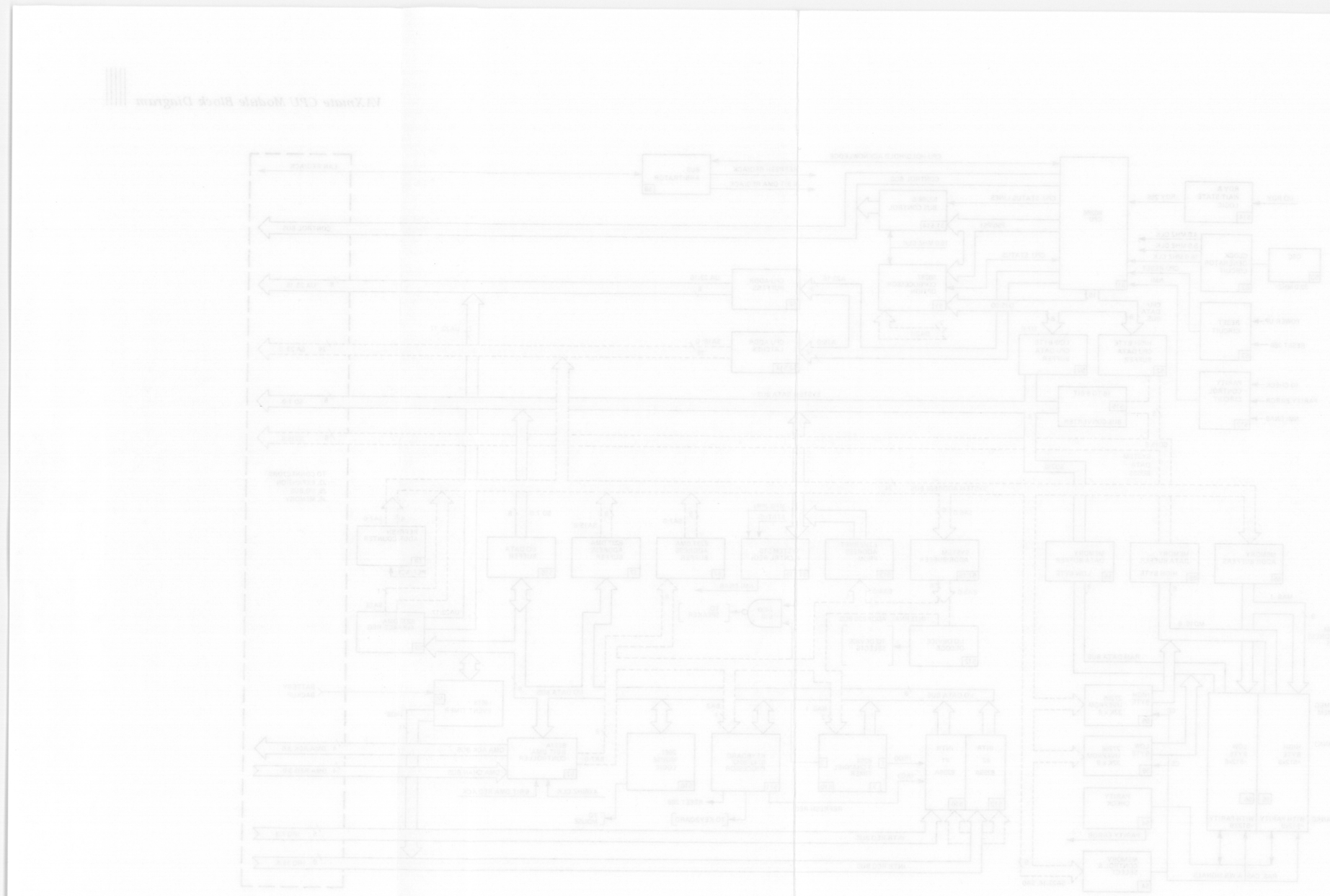


Figure C-1 VAXmate CPU Block Diagram



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