EK-UDA50-UG-003

UDA50 User Guide

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UDA50 User Guide

Prepared by Educational Services
of
Digital Equipment Corporation

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PDP	DIBOL	RSX
UNIBUS	EduSystem	VMS
VAX	IAS	VT
UDA50	MASSBUS	RA80
HSC50	RA60	RA81

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INTRODUCTION

1.1 UDA50 DISK CONTROLLER

The UDA50 is an intelligent controller which interfaces up to four, 16-bit, RA series disk drives to any UNIBUS system. Two hex-height modules, the Standard Disk Interconnect (SDI) module and the processor module, make up the UDA.

The UDA50 uses a radial bus configuration instead of the conventional daisy-chain (serial) method. Radial configuration means there is a separate I/O cable going to each disk drive (see Figure 1-1).

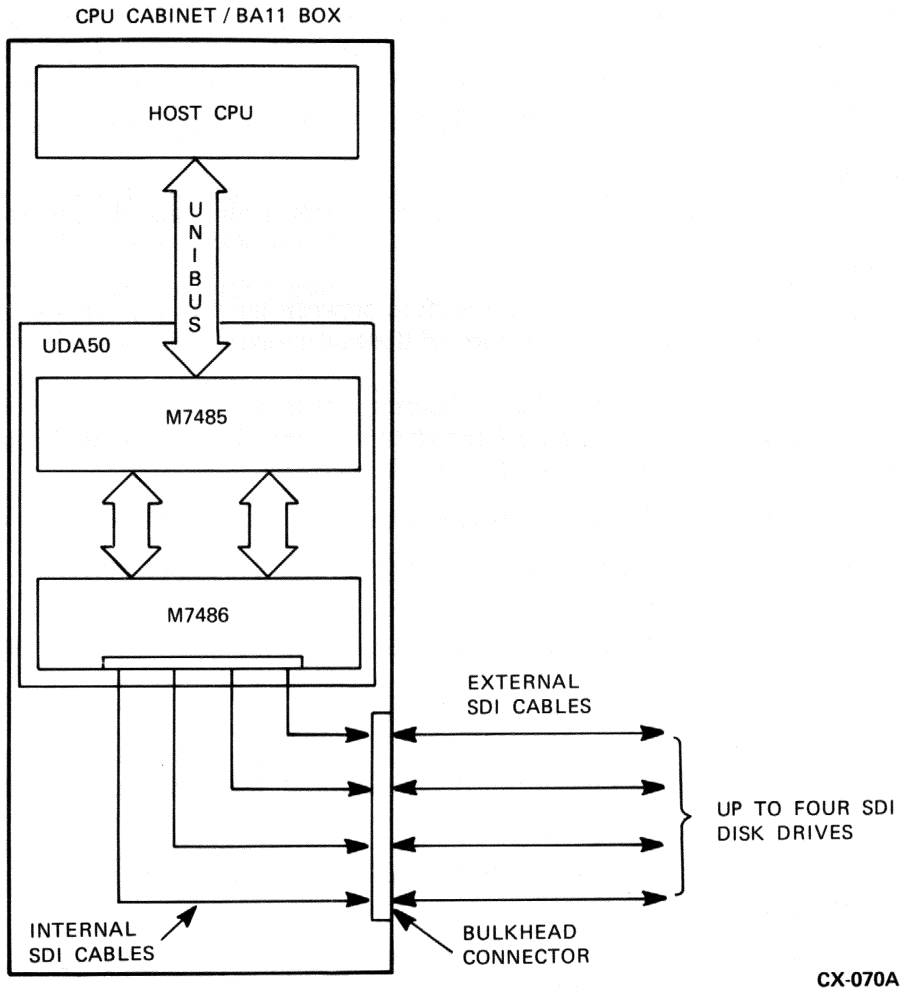

Figure 1-1 UDA50 Disk Subsystem Configuration

1.2 DIGITAL STORAGE ARCHITECTURE (DSA)

The UDA50 belongs to the family of DSA products which implements the Standard Disk Interconnect (SDI). DSA defines the operating rules of mass storage subsystems and how the subsystems interface with the host computer. Some of the characteristics of DSA are listed below:

- I/O is managed by the controller instead of the host.
- The host views the disk subsystem as one contiguous string of sectors known as logical blocks. A logical block contains 512 bytes of information.
- The host is not concerned with disk geometry such as cylinder, track, sector, etc.
- The host and subsystem exchange messages using the Mass Storage Control Protocol (MSCP).

1.3 MASS STORAGE CONTROL PROTOCOL

The UDA50 Disk Controller is a Mass Storage Control Protocol (MSCP) device. MSCP is a communication protocol used with intelligent mass storage controllers. MSCP hides device-dependent requirements such as disk geometry and error recovery strategies from the host. It thus enables several different device drivers to be replaced by one class driver.

To request an I/O operation, the host constructs an MSCP message and sends it to the controller. The MSCP message contains the drive address, the function to be performed, the starting logical block number and the amount of data requested. (Because MSCP hides device dependent requirements, the message does not contain drive geometry information.) When the subsystem receives the request, it performs all drive management and data movement as well as any necessary recovery independently. Upon completion, the subsystem sends the host an MSCP response message giving status information. This flow differs from conventional subsystems where host computer resources are used to control the drive.

1.4 UDA50 MODULES

The following paragraphs describe the hardware on both the SDI module and the processor module:

1.4.1 The SDI Module

The SDI module (M7486) is the communication interface between the UDA microprocessor module and the disk drives. Some of the circuitry and functions of the SDI module are listed below:

- Contains a 32K byte high speed buffer used during data transfers. The buffer allows controller-to-drive tranfers at a higher rate than controller-to-host transfers; this improves performance by minimizing missed disk revolutions due to a buffer full condition.
- Converts the UDA50 buffer format (parallel) to SDI format (serial) and vice versa.
- Generates Real-time Error Correction Code (ECC). This code has a correction capability of up to 8 10-bit error bursts per block (sector).
- Implements the real-time and electrical interface to the SDI, including error detection on the SDI and RAM.

1.4.2 The Processor Module

The processor module is the control portion of the UDA. Some of the circuitry and functions of the processor module are listed below:

- Performs all UDA50 interaction with the UNIBUS via two UNIBUS registers. A switch pack is used to set the I/O page register address.
- Contains a mount for a standard UNIBUS interrupt priority plug. Host software defines the interrupt vector address during UDA50 initialization, so no hardware means of setting the address is required.

- Reports microcode detected errors through the 4 LED indicators on the processor modules and the 4 LED indicators on the SDI module. The error code generated indicates which part to replace.
- Also located on the processor module is a dual microprocessor made up of two 12-bit microprogram sequencers sharing a common 16-bit ALU. The combination of the sequencers and the shared ALU creates a dual microprocessor capable of executing two independent microprograms (from Read Only Memory) at the same time. One of the sequencers controls the UDA to host interaction and the other controls the UDA to disk drive interaction. For greater efficiency, one sequencer fetches an instruction while the other executes an instruction.

1.5 UDA50 FUNCTIONAL MICROCODE

The functional microcode can be divided into two functional flows or streams: the UNIBUS control stream which controls the controller to host interface and the drive control stream which controls the controller to disk drive interface.

1.5.1 UNIBUS Control Stream

Some of the functions the UNIBUS Control Stream performs are listed below:

- The UNIBUS Control Stream goes to the appropriate handling routine in the microcode when the host has a command to send to the UDA or the UDA has a response to send to the host.
- Exchanges (information) packets with the host.
- Validates each packet from the host.
- Constructs the UDA response packets for transmission to the host.
- Analyzes the drive packets and performs the functions listed below.
    - Decodes the logical block number (LBN) to cylinder, group, track, and sector information.
    - Optimizes seek selection from the outstanding commands.
    - Allocates data buffer space.
    - Computes and stores parameters for each sector transfer.
    - Performs packet error detection.
    - Transfers data to or from the host.
- Performs ECC error correction.
- Polls the host at the completion of each command.
- Monitors host activity.
- Performs initialization.
- Initiates Drive Control Stream packet executions.

1.5.2 Drive Control Stream

Some of the functions the Drive Control Stream performs are listed below:

- Monitors "attention" from the drives. When attention has been detected, the Drive Control Stream gets the drive status, compares it with the previous status and takes the appropriate action.
- Constructs and sends packets to the disk drives. The packets may be the result of a host request (read, write, replace, etc.) or in response to a drive attention condition.
- Receives and validates packets from the drives.

- Monitors the drive status flags from the UNIBUS Control Stream. The drive status flags are used for communication between the UNIBUS control stream and the Drive Control Stream.
- Performs tasks as required by the drive status flags. Some of these tasks are listed below:
  - Initiates read, write, seek, and head select packets to the drive.
  - Reads and verifies the block (sector) header.
  - Performs data transfers between internal RAM and disk drive.
  - Updates drive status and buffer use flags.
  - Performs data error analysis and recovery.
  - Performs bad block revectoring.

1.6 UDA50 SPECIFICATIONS

The UDA50 Disk Controller Specifications are described in Table 1-1.

Table 1-1 UDA50 Specifications

Characteristics	Specifications
Physical components	UDA module 1 (M7485) UDA module 2 (M7486) 50-pin flat cable assembly 40-pin flat cable assembly SDI cable assembly I/O bulkhead assembly
Power consumption	84 watts nominal
Heat dissipation	Approximately 295 Btu/hour
Electrical voltage and current requirements	12 amps at +5 volts, 100 milliamps at +15 volts and 1.4 amps at −15 volts
Operating temperature, range	10° C to 40° C (50° F to 104° F) with a temperature gradient of 20° C/hour (36° F/hour)
Operating relative humidity range	10% to 90% with a wet bulb temperature of 28° C (82° F) and a minimum dew point of 2° C (36° F)
Operating altitude range	Sea level to 2438 meters (8000 ft). Derate the maximum allowable operating temperature by 1.8° C/1000 meters (1° F/1000 feet) for operation above sea level
Mounting restrictions	Mounts in two hex-height UNIBUS SPC slots in the following UNIBUS and VAX mounting boxes: BA11-A BA11-K BA11-L

1.7 RELATED DOCUMENTATION

Digital customers may order the following list of UDA50 related manuals from the Peripherals and Supplies Group:

- *UDA50 USER GUIDE* (EK-UDA50-UG)
- *UDA50 SERVICE MANUAL* (EK-UDA50-SV)
- *UDA50 MAINTENANCE GUIDE* (AA-M185A-TC)
- *UDA50 FIELD MAINTENANCE PRINT SET* (MP-01331)
- *DSA CONTROLLER DOCUMENTATION KIT* (QP906-GZ)*
- *DSA DRIVES DOCUMENTATION KIT* (QP907-GZ)*

* The DSA Controller kit consists of a small looseleaf binder, *UDA50 Maintenance Guide* and *HSC50 Maintenance Guide*. The DSA Drives Kit consists of the two small binders containing the current maintenance guides for disks that operate on the UDA50 and HSC50 controllers.

Within the United States, Digital Customers may order the above manuals from the Peripherals and Supplies Group over a toll free number (800-258-1710). Orders by mail should be addressed to one of the following primary distribution centers.

Northeast/Mid-Atlantic Region

Accessories & Supplies Group
Cotton Road
Nashua, NH. 03060
Tel: 603-884-5111

Central Region

Peripherals and Supplies Group
1050 E. Remington Road
Schaumberg, Illinois 60195
Tel: 312-640-5612

Western Region

Peripherals and Supplies Group
Moffett Park Warehouse
632 East Caribbean Drive
Sunnyvale, CA 94086
Tel: 408-734-9125

Outside the United States, consult local Digital offices.

Internal Digital Equipment Corporation customers can order the *UDA50 User Guide*, the *UDA50 Service Manual*, and the UDA50 Field Maintenance Print Set directly from Printing and Circulation Services, 444 Whitney Street, Northboro, Masschussetts 01532.

The *UDA50 Maintenance Guide*, the Maintenance Guide Looseleaf Binder, and the DSA Controllers Documentation Kit, can be ordered from the Software Distribution Center, Order Administration/Processing, 20 Forbes Road, Northboro, Massachusetts 01532.

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

The installation procedure for the UDA50 Disk Controller requires the insertion of two hex-height modules into a UNIBUS backplane. If the UDA50 Disk Controller is to control disk drives located outside the cabinet it is in, then an input/output (I/O) bulkhead assembly must be mounted on the rear of the CPU cabinet. SDI cables must be connected between the UDA50 Disk Controller and the I/O bulkhead assembly and from the I/O bulkhead to each disk drive. Figure 2-1 gives an illustrated parts breakdown of the UDA50 assembly.

Use the following checklist to perform the UDA50 installation. The list indicates the paragraph number where each procedure is described.

- Check the I/O page address switches and jumpers (2.2.1) _____
- Check the UDA50 priority plug (2.2.3) _____
- Insert and clamp the SDI cable to J4 (2.2.8) _____
- Select the backplane slot (2.2.4) _____
- Prepare the backplane slot (2.2.5) _____
- Insert the UDA50 modules (2.2.6) _____
- Install two flat ribbon cables (2.2.7) _____
- Install the I/O bulkhead connector (2.2.9) _____
- Install the internal SDI cable to the I/O bulkhead (2.2.10.1) _____
- Install the external SDI cable to the I/O bulkhead (2.2.10.2) _____
- Alternate SDI cable installation (2.2.10.3) _____
- Install the bootstrap ROM (2.3) _____
- Perform the field acceptance test (2.4) _____

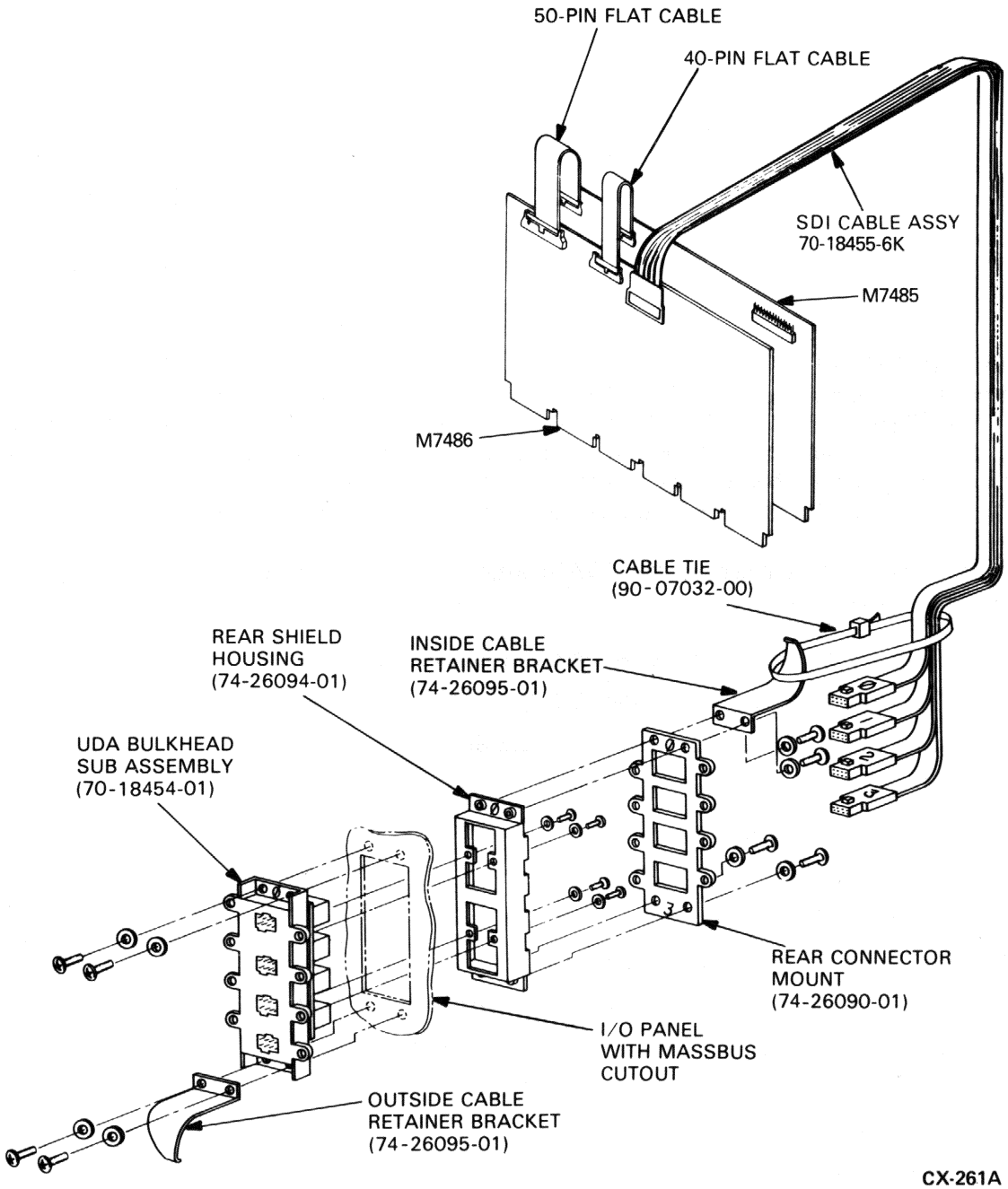

Figure 2-1 UDA50 Illustrated Parts

2.2 MODULE PREPARATION AND INSTALLATION

The following paragraphs describe how to install the UDA50 modules, I/O bulkhead and cables once the CPU and disk drive cabinets have been set up.

2.2.1 I/O Page Address Switches And Jumpers

The UDA50 Disk Controller contains two registers visible in the I/O page. They are the initializing and polling (IP) register and the status and address (SA) register. The IP and SA registers are assigned an octal UNIBUS address of 772150 and 772152, respectively.

The UNIBUS address selector switches and a jumper plug W13 are used to set the UNIBUS address for the IP register. The location of these switches and jumper plug on UDA50 module M7485 is shown in Figure 2-2. Set the UNIBUS address switches and jumpers to the positions shown in Figure 2-3 to select UNIBUS address 772150. If 772150 (default address shipped with the UDA) cannot be used, alternate addresses are: 1760334 and 1760340.

NOTE

The UNIBUS address switches and jumpers should be set for a floating address when a second DSA Controller is installed on a system. Check the system configuration and UNIBUS addresses of all devices already installed. Common floating addresses are: 760340 and 760330.

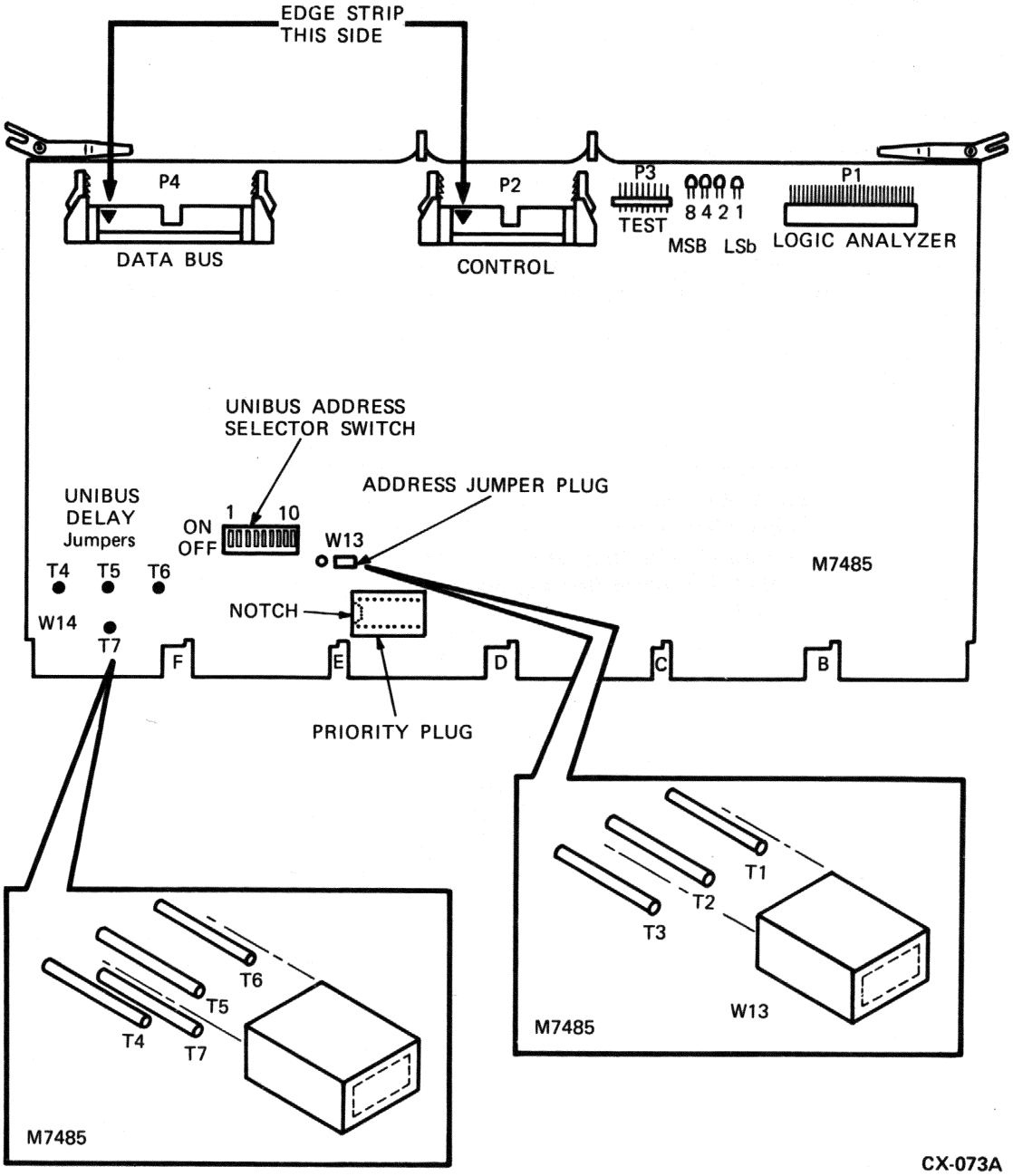

Figure 2-2 M7485 UNIBUS Address switch and Jumper Locations

7 6 0 3 3 4

111 110 000 011 011 100

UNIBUS ADDRESS BITS	17 16 15	14 13 12	11 10 9	8 7 6	5 4 3	2 1 0
OCTAL CODE	7	7	2	1	5	0
BINARY CODE	1 1 1	1 1 1	0 1 0	0 0 1	1 0 1	0 0 0
UDA50 SWITCH SETTING	1 1 1	1 1 S10 (ON)	S9 S8 S7 OFF ON OFF	S6 S5 S4 OFF OFF ON	S3 S2 S1 ON OFF ON	W13 0 0 (T1,T2)
	ALWAYS ONES					ALWAYS ZEROS

NOTE

The UNIBUS address switches and jumpers should be set for a floating address when a second UDA50 is installed on a system. Check the system configuration and UNIBUS addresses of all devices

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Figure 2-3 UDA50 Switch Setting for Address 772150

In past disk products, a vector address was also physically selectable. This is not true with the UDA50 Disk Controller. A vector address, typically 154 (octal), will be supplied by the software.

2.2.2 UNIBUS Tuning

A UNIBUS system may experience data late conditions that can be remedied by tuning the UNIBUS. This process involves changing the relative positions of the nonprocessor request (NPR) devices on the bus. The device at the front of the bus (near the host) has the highest priority. The device at the end of the bus has the lowest priority.

2.2.2.1 UNIBUS Device Positions – The UDA should be placed at the end of the UNIBUS (lowest NPR priority) because it is heavily buffered. Other NPR devices should be placed along the UNIBUS depending on their buffering. The NPR devices with the least amount of buffering should be placed at the front of the UNIBUS.

2.2.2.2 UDA NPR Priority Jumper – A jumper has been inserted on the M7485 module to help tune the UNIBUS system. The jumper changes the average number of UDA NPR requests over a given amount of time by delaying the request for 0, 6.2, or 10 microseconds. Table 2-1 shows the amount of delay and jumper configuration.

Table 2-1 UNIBUS Delay

Amount of Delay	Jumper Configuration
0 microseconds	T4-T6
6.2 microseconds	T5-T6
10 microseconds	T6-T7

On some systems it is not possible to remedy data late errors by changing the UDA NPR Priority Jumper. The following is a list of systems that cannot use a UDA and a list of rules on how many UDAs can be installed on a system:

- The UDA/RK07/DMR11 configuration (on an 11/70 only) gives data late errors from the RK07 regardless of the UDA's jumper setting. Either an RK07 or a UDA, but not both, can be configured on the 11/70 when a (1 megabit per second) DMR11 is present.
- On both PDP-11 and VAX systems, no more than two UDAs may be installed on a UNIBUS with nonbuffered UNIBUS peripheral devices.

NOTE
If a bus repeater is used, a greater possibility of data late errors exists. In general, the longer the UNIBUS, the greater the possibility of data late errors.

2.2.2.3 UDA Burst Parameter – The UDA burst parameter is a host software value that indicates how many long words (32 bits) the UDA will attempt to transfer when it accesses the UNIBUS. The default for this parameter is 1, but can range from 1 to 32.

Increasing the UDA burst parameter to a number greater than 1, increases overall system efficiency. However, data late conditions are more likely to exist.

2.2.3 UDA50 Priority Plug

All UDA50 M7485 modules are shipped with a level 5 priority plug. This is the recommended priority level for UDA50 Disk subsystems and the plug need not be changed for the majority of installations. If another priority level is required in some special circumstance, the current priority plug must be removed and the new one inserted. The location of the priority plug is shown in Figure 2-2. It should be inserted so the notch on the priority plug aligns with the hole on the module socket.

2.2.4 UNIBUS Backplane SPC Slots

The UDA50 Disk Controller will operate in either the standard UNIBUS or modified UNIBUS hex-height small peripheral connector (SPC) slots. Locate two adjacent empty SPC slots for the two UDA50 modules. Illustrations of the UNIBUS backplanes and pin assignments are shown in Figures 2-4 and 2-5, respectively.

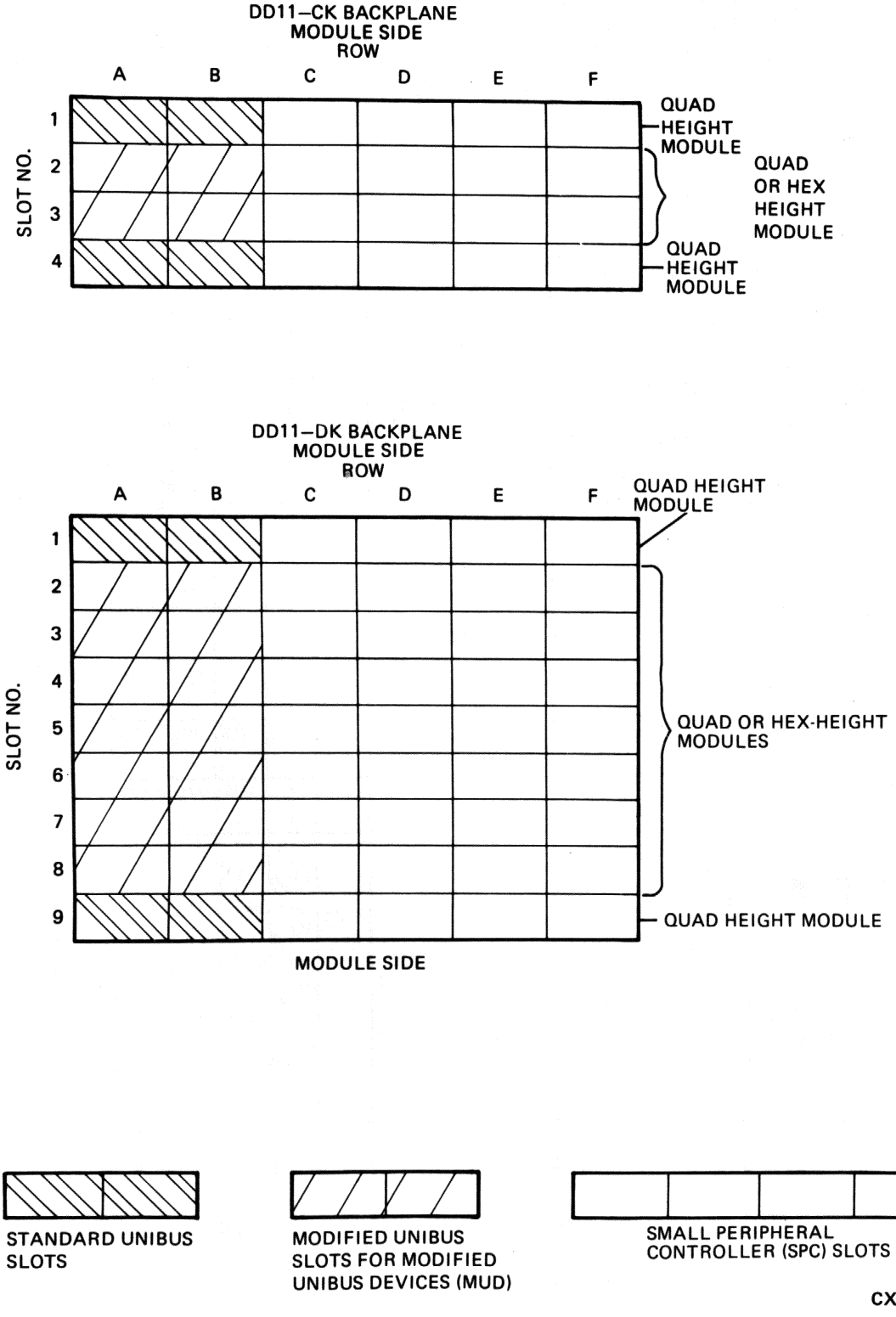

Figure 2-4 Optional Backplane Slot Assignments

STANDARD UNIBUS PIN DESIGNATIONS

Side / Pin	ROW A 1	ROW A 2	ROW B 1	ROW B 2
A	INIT L	+5V	BG6 H	+5V
B	INTR L	GND	BG5 H	GND
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	GND	BR4 L
E	D04 L	D03 L	GND	BG4 H
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	GND	PB L	A11 L	A10 L
P	GND	BBSY L	A13 L	A12 L
R	GND	SACK L	A15 L	A14 L
S	GND	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	NPG H	BR6 L	SSYN L	C0 L
V	BG7 SO	GND	MSYN L	GND

MODIFIED UNIBUS PIN DESIGNATIONS

SIDE / PIN	ROW A 1	ROW A 2	ROW B 1	ROW B 2
A	INIT L	+5V	RESV PIN	+5V
B	INTR L	TP	RESV PIN	TP
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	+5 BAT	BR4 L
E	D04 L	D03 L	INT SSYN	PAR DET
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	PAR P1	PB L	A11 L	A10 L
P	PAR P0	BBSY L	A13 L	A12 L
R	+15 BAT	SACK L	A15 L	A14 L
S	-15 BAT	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	+20 (CORE)	BR6 L	SSYN L	C0 L
V	+20 (CORE)	+20 (CORE)	MSYN L	-5 (CORE)

NOTE: INDICATES A REDESIGNATED PIN.

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Figure 2-5 Standard and Modified Backplane Pin Assignments

The early SPCs did not utilize direct memory access (DMA) data transfers to and from memory; therefore, the signals now used for this purpose are not part of the original SPC pin assignments. Newer options, such as the UDA50 Disk Controller, do utilize DMA transfers. A new pin assignment called SPC PRIME includes these signals. Refer to Figure 2-6. If the UDA50 Disk Controller is used in an older (non-SPC PRIME) slot, it is necessary to ensure the signals shown in Table 2-2 are wired on the backplane.

	ROW C		ROW D		ROW E		ROW F	
SIDE / PIN	1	2	1	2	1	2	1	2
A	NPG (IN)	+5V	TP	+5V	GND A	+5V	ABG OUT	+5V
B	NPG (OUT)	-15V	TP	-15V	ASSYN IN H	-15V	ABG IN	-15V
C	PA L	GND	A SEL 6	GND	A12 L	GND	SSYN L	GND
D	LTC	D15 L	A OUT LOW	BR7 L	A17 L	A15 L	BBSY L	FO1 N1
E	TP	D14 L	A SEL 4	BR6 L	MSYN L	A16 L	FO1 V2	D02 L
F	TP	D13 L	A SEL 0	BR5 L	A02 L	C1 L	D05 L	D06 L
H	D11 L	D12 L	A IN	BR4 L	A01 L	A00 L	D07 L	A INT ENB B
J	A INT B	D10 L	A SEL 2	A BR OUT	SSYN L	C0 L	NPR L	GND A
K	TP	D09 L	A OUT	BG7 SO	A14 L	A13 L	D08 L	A INT B
L	A INT ENBB	D08 L	INIT L	BG7 OUT	A11 L	TP	D03 L	FO1 L2
M	TP	D07 L	AINT ENBA	BG6 SO	AIN	AOUT HIGH	INTR L	FO1 M2
N	DC LO	D04 L	A INT A	BG6 OUT	A OUT LOW	A08 L	FO1 N1	D04 L
P	HALT REQ	D05 L	TP	BG5 S0	A10 L	A07 L	ABR OUT	FO1 P2
R	HALT GRT	D01 L	TP	BG5 OUT	A09 L	ASEL 4	FO1 L2	FO1 N1
S	PB L	D00 L	TP	BG4 S0	ASEL 6	ASEL 0	FO1 M2	FO1 P2
T	GND	D03 L	GND	BG4 OUT	GND	ASEL 2	GND	SACK L
U	+15	D02 L	TP	ABG IN	A06 L	A04 L	A INT A	ABR OUT
V	AC LO	D06 L	ASSYN IN H	ABG OUT	A05 L	A03 L	A INT ENB A	FO1 FO1

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Figure 2-6 SPC PRIME Backplane Pin Assignments

Table 2-2 Backplane Signal Checks

Backplane Pins	Signal Names	Used On
Pin CA1	NPG IN	M7485
Pin CB1	NPG OUT	M7485
Pin FJ1	NPR	M7485
Pin CV1	AC LO1	M7485
Pin CU1	+15V	M7486

2.2.5 UNIBUS Backplane Slot Preparation

If the slot has SPC PRIME pinning, the NPG jumper will have to be removed. The NPG line is the UNIBUS grant line for devices that perform data transfers without processor intervention. Continuity of the NPG line is provided by wire-wrap jumpers on the backplane. When an NPR device is placed in a slot, the corresponding jumper wire from pin CA1 to pin CB1 of that slot must be removed. The routing of the NPG signal through the backplane is shown in Figure 2-7. Grant priority decreases from slot 1 to slot 9.

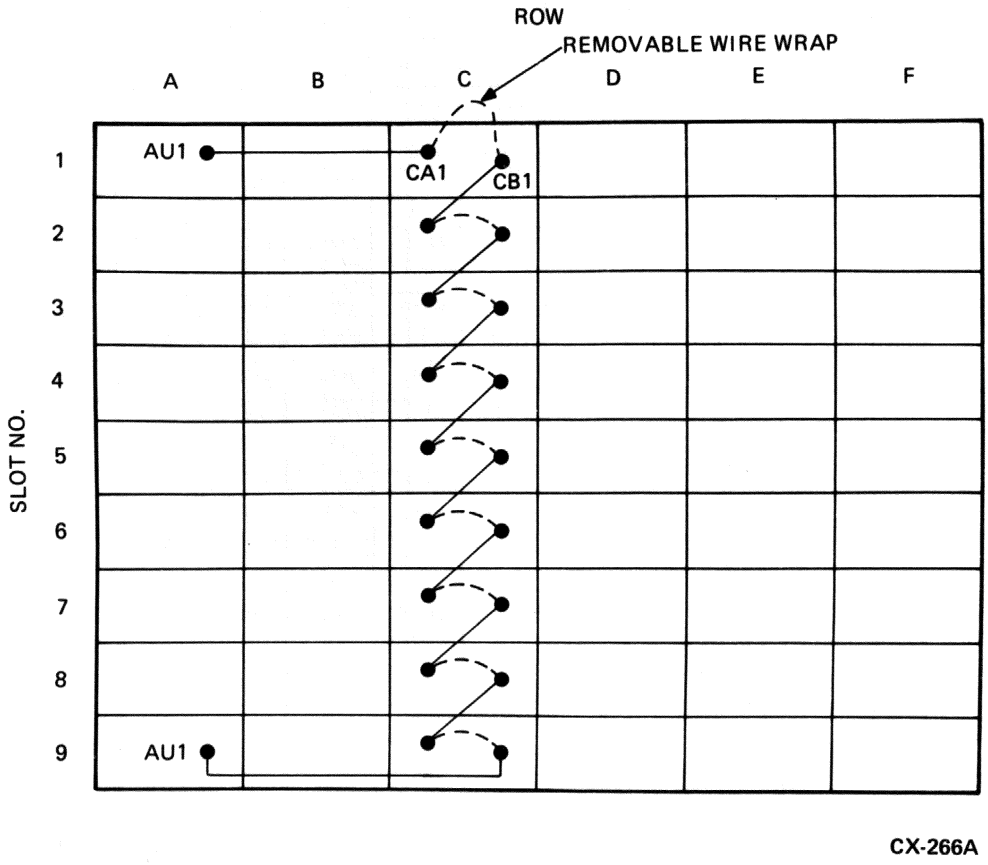

Figure 2-7 NPG Jumper Lead Routing

The NPG jumper must be removed from the slot that will be occupied by UDA50 module M7485. Module M7485 will not operate with the NPG jumper in place. The NPG jumper may also be removed from the slot occupied by the second UDA50 module M7486, since the module will provide continuity on the NPG line. Module M7486 will operate whether or not the NPG jumper is in place. If both NPG jumpers are removed from these two module slots, the module location can be interchanged and the UDA50 will still operate.

CAUTION

The NPG continuity line will be interrupted whenever module M7486 is removed.

NOTE

If an NPR device is removed from a slot, the jumper wire from pin CA1 to pin CB1 must be reconnected.

The bus grant lines (BG4 through BG7) for devices requiring processor intervention during data transfers are routed through each small peripheral control section in slot D. Each of the four grant signals is routed on a separate line. Grant priority for each level decreases from slot 1 to slot 9.

A bus grant jumper card (G727, G7270, or G7271) must be placed in connector D of any unoccupied SPC section. If an SPC section is left open, bus grant continuity will be lost.

2.2.6 UDA50 Module Insertion

Insert the two UDA50 modules into the two adjacent SPC slots prepared for them. The two modules may be inserted in any order if the NPG jumpers have been removed from both SPC slots. Otherwise, ensure module M7485 is in the SPC slot without the NPG jumper.

2.2.7 Flat Ribbon Cable Installation

The two UDA50 hex-height modules must be interconnected by two 4 inch long flat ribbon cables as shown in Figure 2-8. The outer cable is a 50-conductor flat ribbon cable which connects M7486 (P1) to M7485 (P4). The inner cable is a 40-conductor flat ribbon cable which connects M7486 (P3) to M7485 (P2).

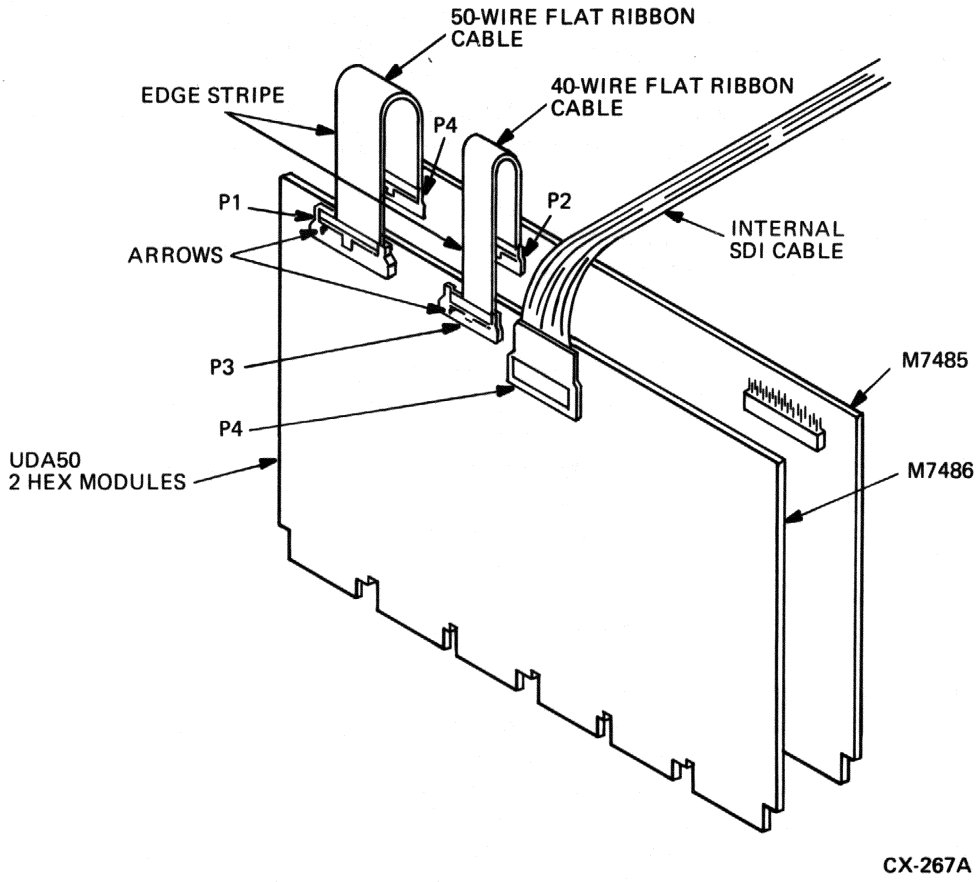

Figure 2-8 UDA50 Intermodule Flat Ribbon Cables

Install the cables so the arrows on the plugs align with the sockets. The edge stripe on the cables is on the same edge as the arrow. It does not matter which UDA50 module is inserted first.

2.2.8 SDI Cable Installation

Insert plug P4 of the internal SDI cable assembly into connector J4 on UDA50 module M7486 as shown in Figure 2-9. Slide the cable retainer over connector J4 until the connector protrudes through the plastic cutout. The cable retainer should lock the SDI cable in place.

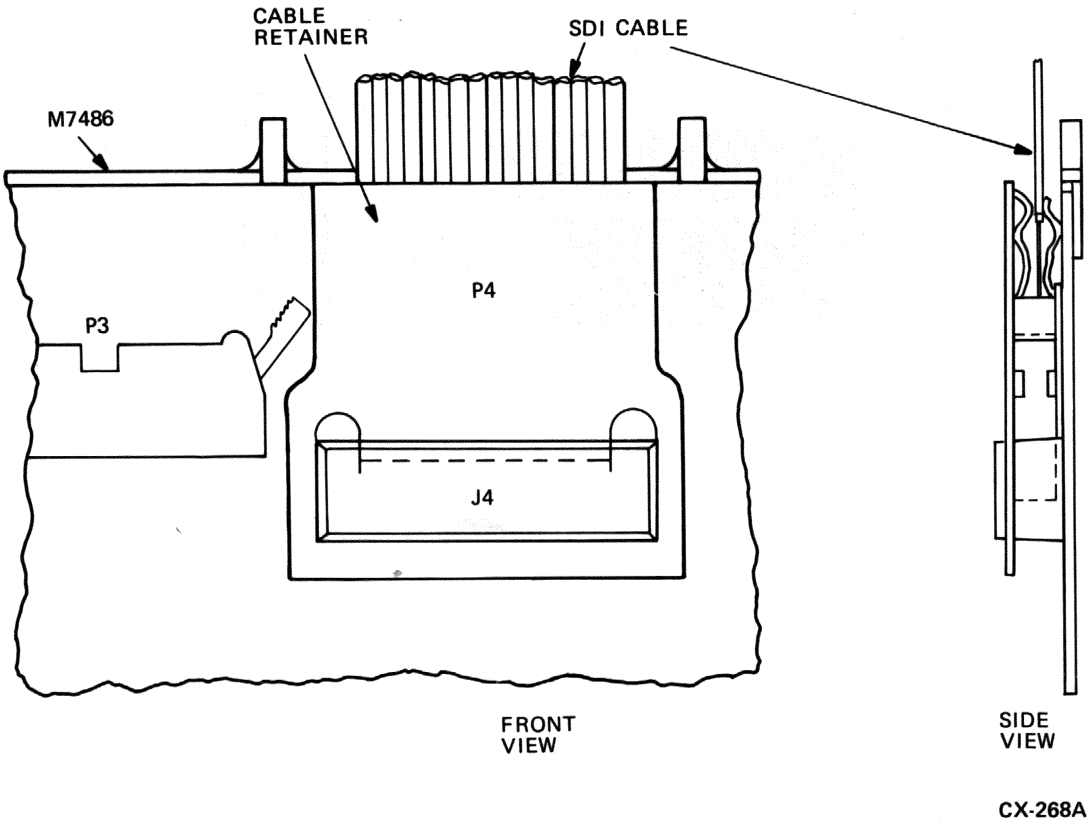

Figure 2-9 M7486 SDI Cable Assembly Installation

2.2.9 I/O Bulkhead Connector Installation

An I/O bulkhead connector must be installed on the I/O panel at the rear of the CPU cabinet. The I/O bulkhead provides a feed-through connection for all SDI cables leaving the CPU cabinet. Figure 2-10 shows the location of the I/O panel on a PDP-11/44 cabinet. Other CPU cabinets use this same I/O panel. If no I/O panel is available, refer to Paragraph 2.2.11.3 (Alternate SDI Cable Installation).

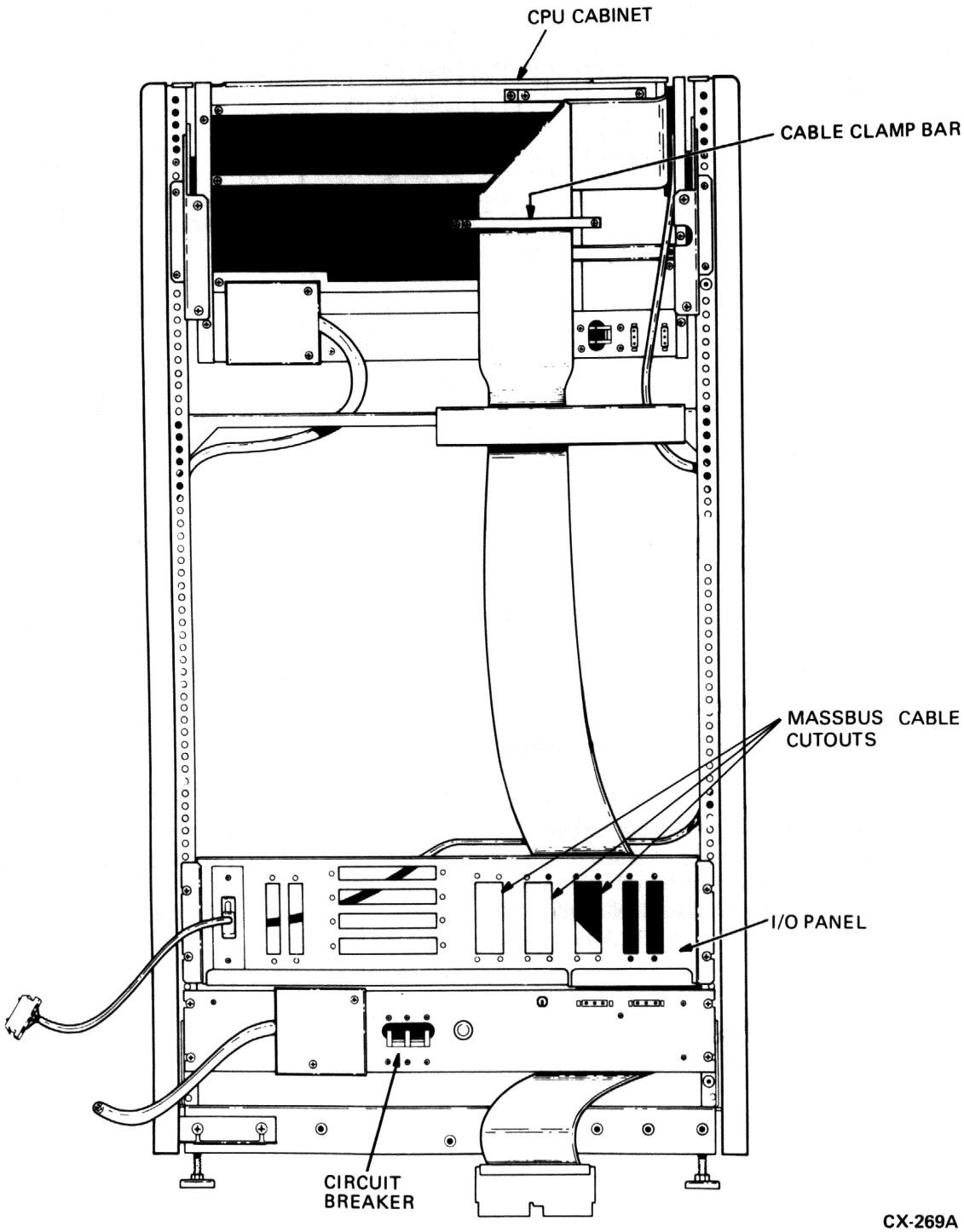

Figure 2-10 I/O Panel and MASSBUS Cable Slot Locations

On the I/O panel are three wide cutouts intended for MASSBUS cable use. The location of these three MASSBUS cable cutouts is also shown in Figure 2-10. Select any empty MASSBUS cable cutout to mount the I/O bulkhead connector. Once an empty MASSBUS cable cutout is found, use the following procedure to install the I/O bulkhead:

1. Install the UDA bulkhead subassembly and its outside cable retainer bracket as shown in Figure 2-11. Connector number 0 on the bulkhead should be on the top. Four screws and lock washers are used for mounting.
2. Install the rear shield housing next. Connector number 0 should be on the top. Four screws and lock washers are used for mounting.
3. Install the rear connector mount and the inside cable retainer bracket next. Again, connector number 0 should be on the top.

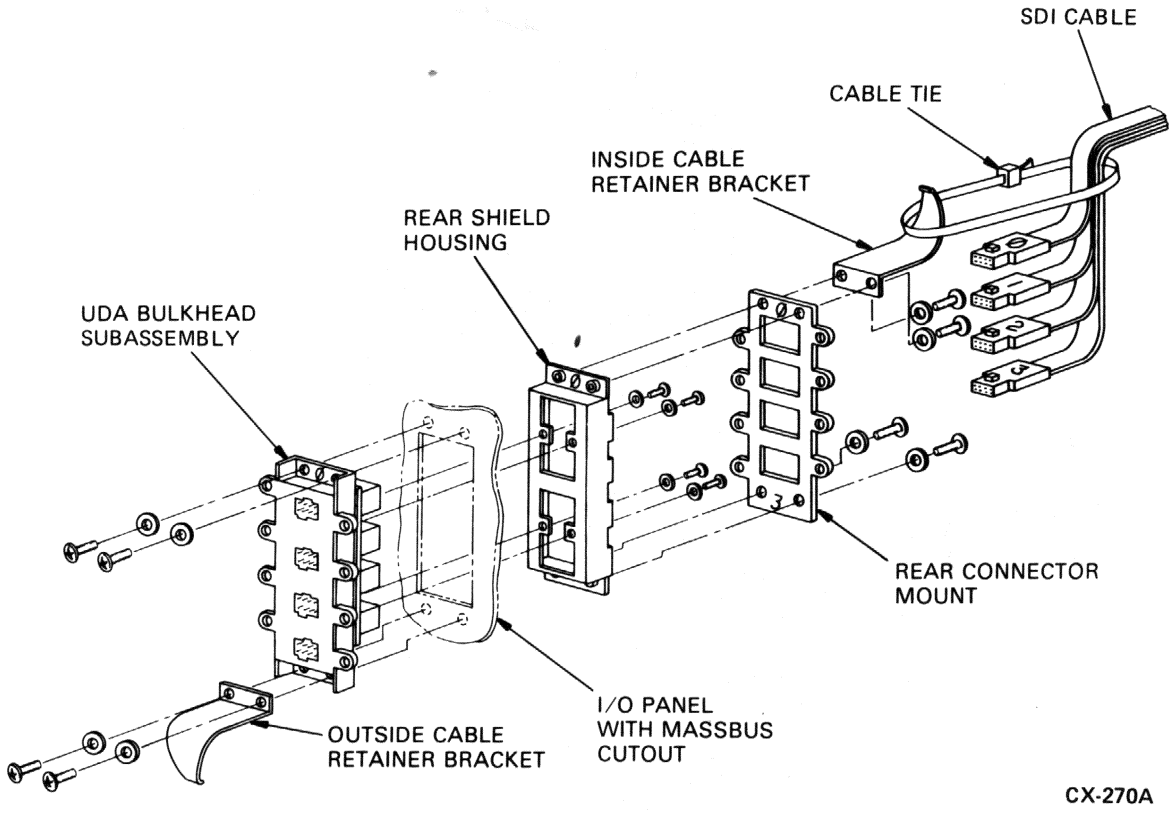

Figure 2-11 I/O Bulkhead Installation

2.2.10 SDI Cabling Procedures

Standard Disk Interconnect (SDI) cables must be installed both inside and outside the CPU cabinet. The internal SDI cabling procedure is described first.

2.2.10.1 Internal SDI Cables – One end of the internal SDI cable is already connected to UDA50 Module M7486. This is described in paragraph 2.2.9. The other end of the SDI cable assembly must be plugged into the I/O bulkhead on the I/O panel at the rear of the CPU cabinet. Use the following procedure to install this cable:

1. Bring the SDI cable assembly out of the CPU UNIBUS BA-11 box through the cable trough shown in Figure 2-12.

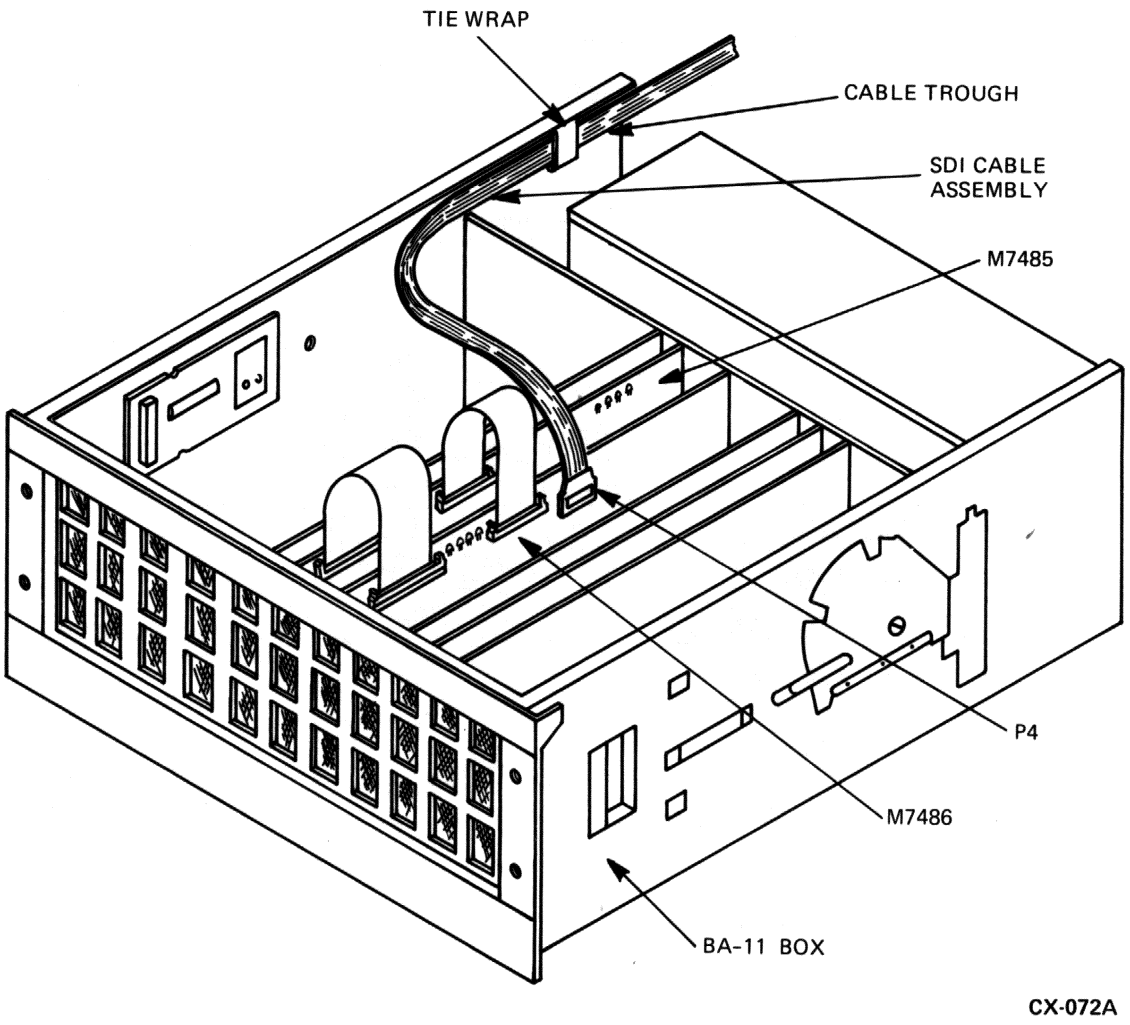

Figure 2-12 SDI Cable Routing Inside BA-11 Box

2. Install a tie wrap on the SDI cable assembly approximately where it passes through the cable trough. Refer to Figures 2-12 and 2-13.

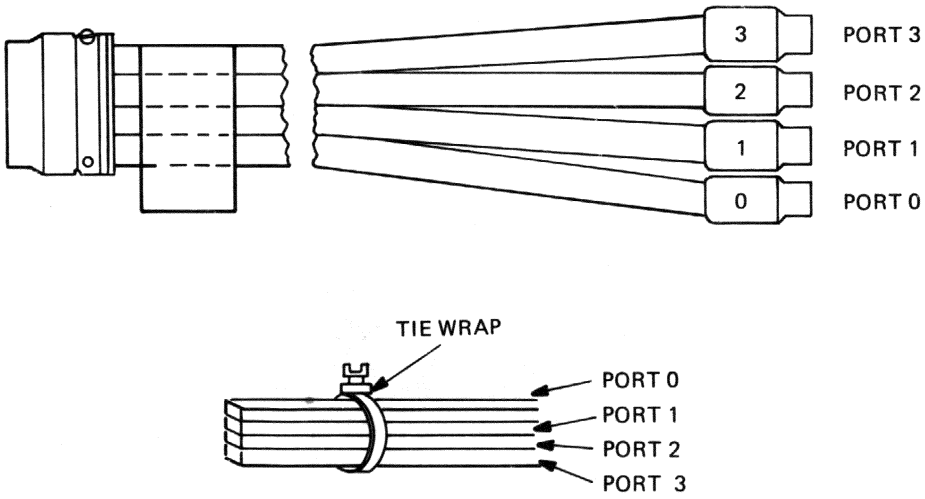

Figure 2-13 SDI Cable Assembly with Tie Wrap

3. Tie wrap the SDI cable at point A where it exits the rear of the BA-11 box. Refer to Figure 2-14.

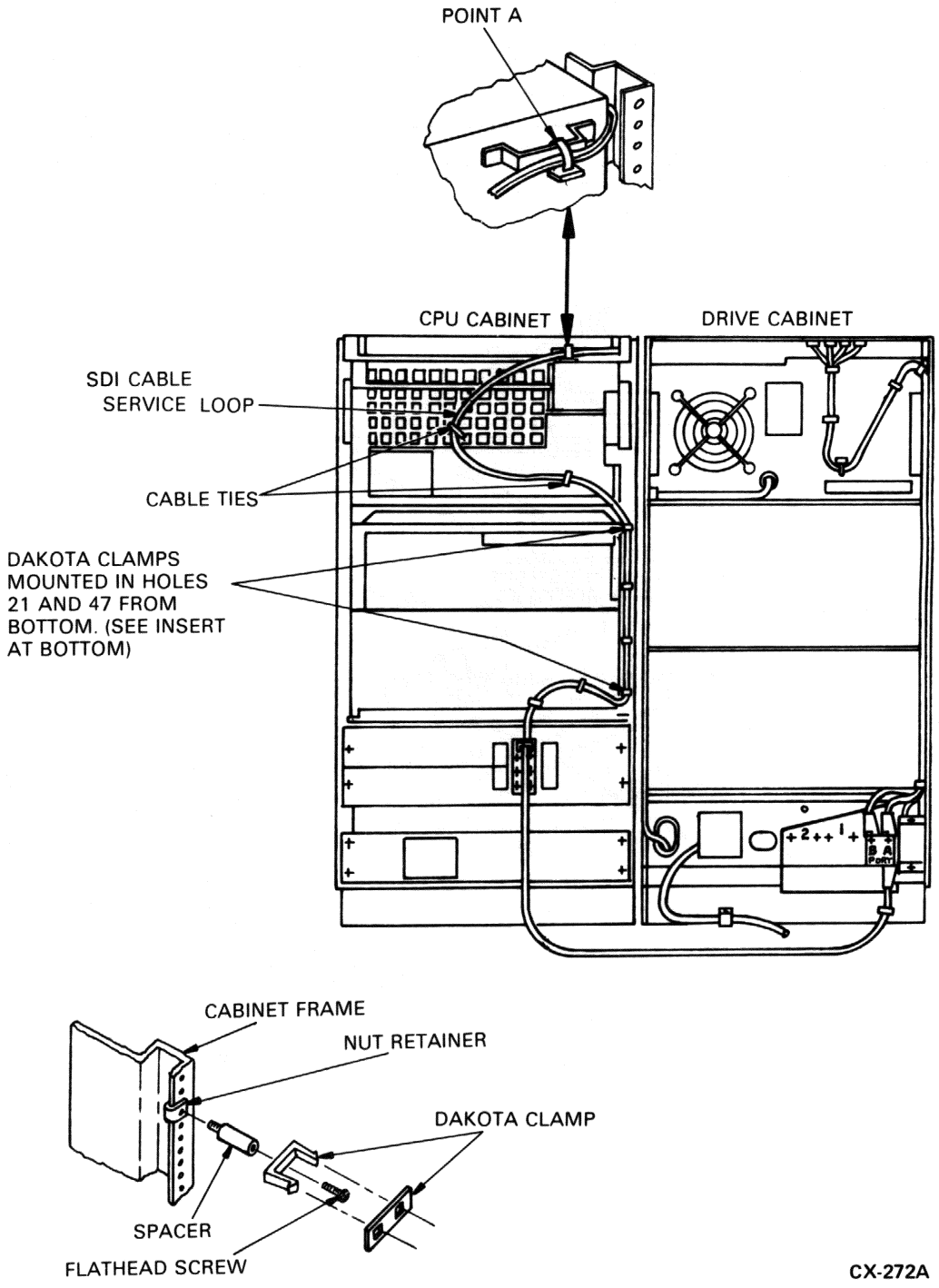

Figure 2-14 SDI Cable Assembly Installation

4. Install the two Dakota clamps as shown in Figure 2-14 and insert the SDI cable assembly in them.
5. Install the remaining seven cable ties on the SDI cable assembly as shown in Figure 2-14. The seventh cable tie is hidden behind the bottom I/O panel.
6. Insert the SDI cable plugs into the I/O bulkhead with the port 0 cable in the top connector. The I/O bulkhead connectors are numbered 0, 1, 2, and 3 from the top. Clamp the SDI cables to the retainer bracket. Refer to Figure 2-15.

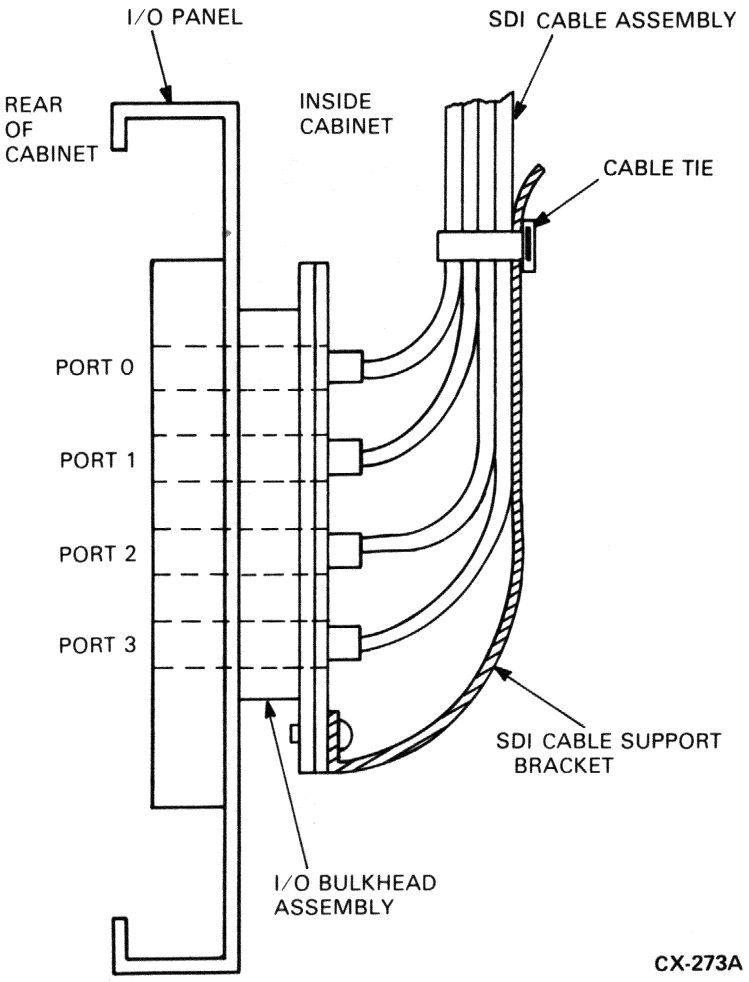

Figure 2-15 SDI Cable Retainer Bracket

2.2.10.2 External SDI Cables – The external SDI cables are shielded cables that must be grounded to the I/O bulkhead by mounting the shield terminators with screws. Use the following procedure to install these cables:

1. Plug the first SDI cable into the bottom I/O bulkhead connector.
2. Screw the SDI cable shield terminator to the I/O bulkhead as shown in Figure 2-16.

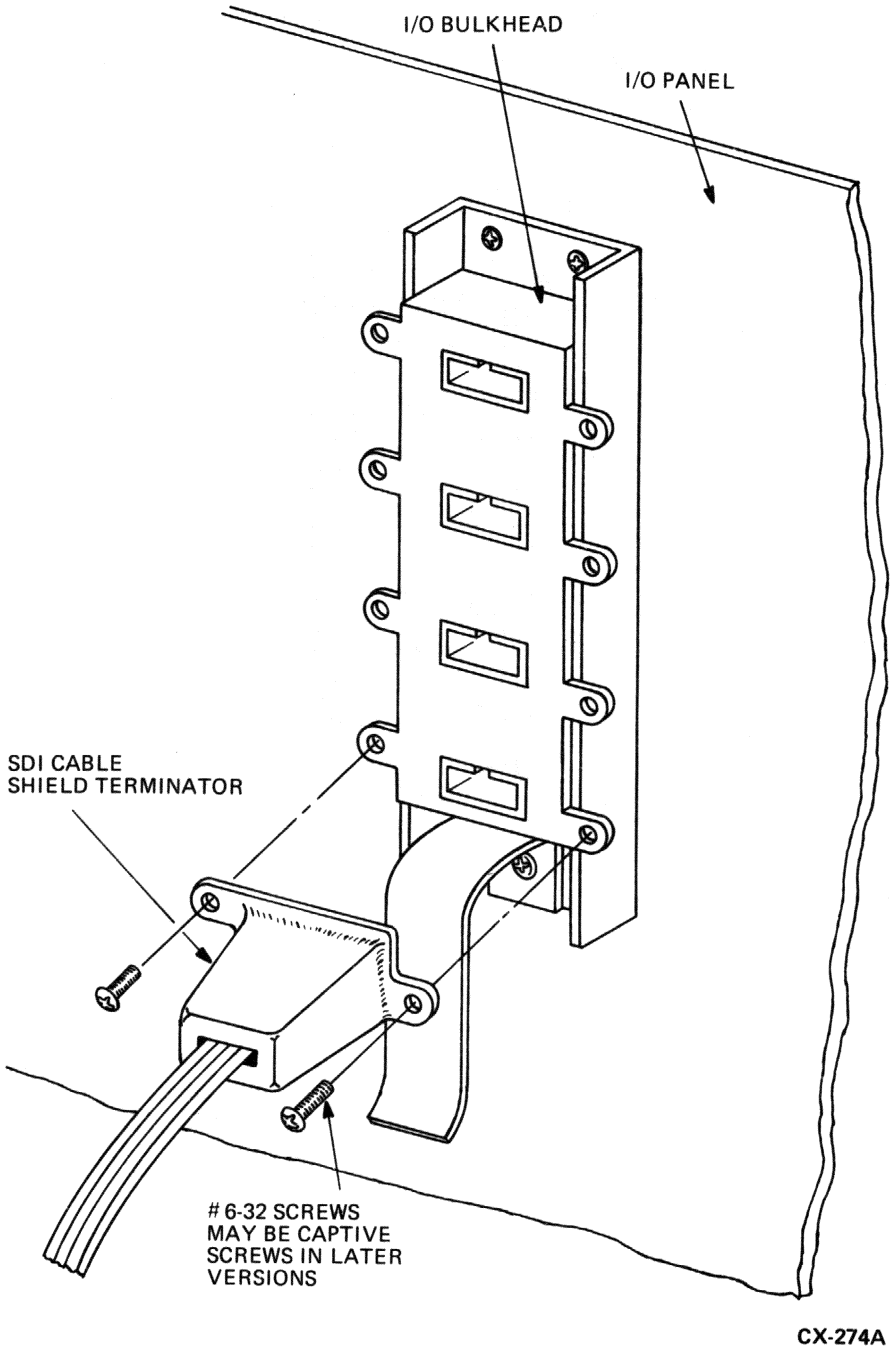

Figure 2-16 SDI Cable Shield Terminator Installation

3. Install an SDI cable for each disk drive, starting at I/O bulkhead connector 3 and going up sequentially to 0.

NOTE

Connecting drive 0 to UDA port 0 and drive 1 to UDA port 1 etc., is a useful practice. However, it actually does not matter which drive connects to which UDA port because the UDA treats each port equally and gets the unit number for each drive from that drive.

4. Secure the SDI cables to the SDI cable retainer bracket shown in Figure 2-17.

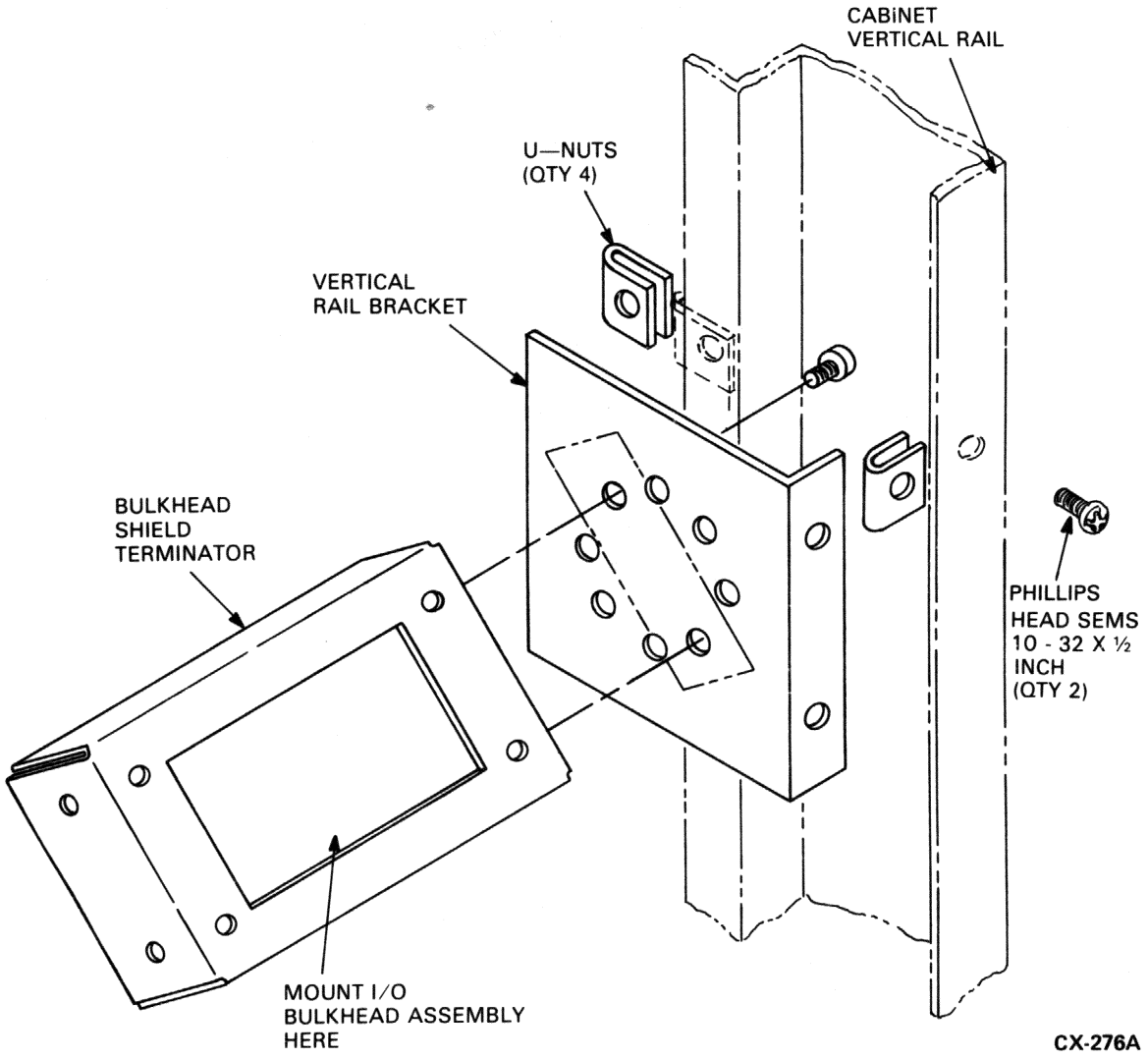

Figure 2-17 Clamping the SDI Cables to the Support Bracket

5. Install the drive end of the SDI cables into the drive I/O bulkhead connectors as described in the disk drive user guide.

2.2.10.3 Alternate SDI Cable Installation – The SDI cable installation procedures described in paragraph 2.2.10.1 and 2.2.10.2 should be used whenever an I/O panel is available and room permits. When an I/O panel is not present, an alternate means of SDI cable installation is provided. This alternate procedure requires the parts shown in Figure 2-18. Use Figure 2-18 as a reference and perform the following steps:

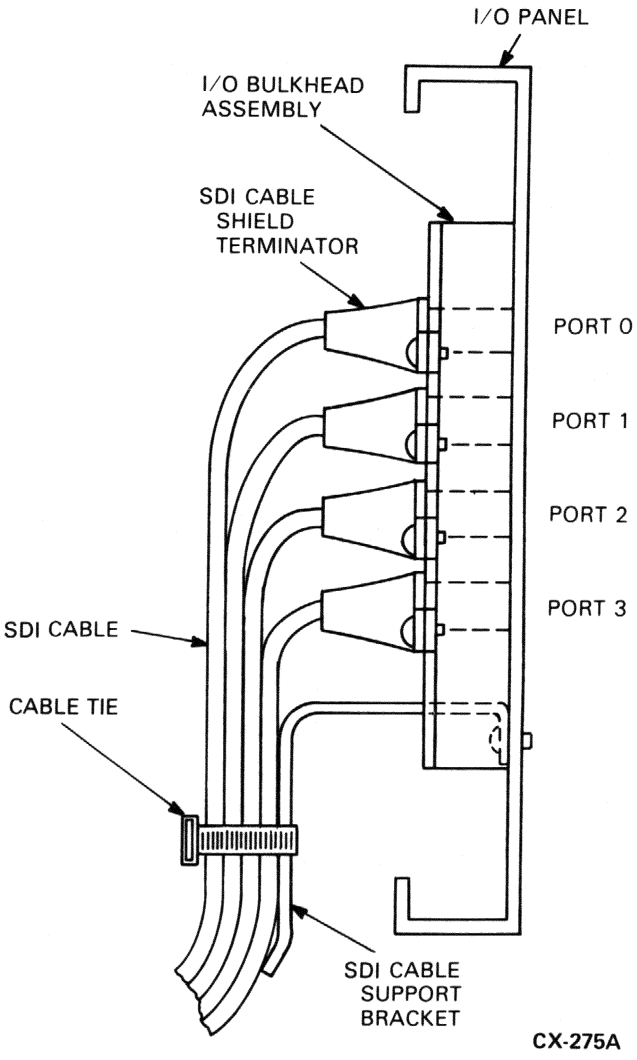

Figure 2-18 Alternate SDI Cable Installation

1. Select a suitable location on either rear vertical cabinet rail where this alternate I/O bulkhead can be mounted without interfering with existing equipment. Choose the lowest available location in the cabinet.
2. Push on the four u-nuts to align with the holes in the vertical rail bracket.
3. Select the best angle and mount the bulkhead shield terminator onto the vertical rail bracket with two Phillips head sems (10-32 x 1/2 inch).
4. Mount the vertical rail bracket onto the vertical cabinet rail with the four Phillips head sems (10-32 x 1/2 inch).
5. Install the I/O bulkhead connector onto the bulkhead shield terminator. Mount the I/O bulkhead so connector number 0 is towards the right.

2.3 INSTALLATION OF BOOTSTRAP ROM

The proper bootstrap ROMs are shipped with the UDA50. Bootstrap ROM 23-767A9-00 must be installed on the PDP-11 bootstrap ROM module M9312. Bootstrap ROM 23-990A9-00 must be installed on the VAX 11/750.

2.4 FIELD ACCEPTANCE TEST PROCEDURE

The field acceptance and test procedure for the UDA50 Disk Subsystem has three parts:

1. Run the UDA50 Disk Controller resident diagnostic test.
2. Run the disk drive field acceptance test found in the disk drive user guide.
3. Run the UDA50 host-resident diagnostics after each subsystem device has been tested separately.

2.4.1 UDA50-Resident Diagnostics

The UDA50-resident diagnostics are initiated when power is applied to the UDA50 Disk Controller. The CPU should be halted during this test. The four LED indicators on each UDA50 module should display a cycling pattern in the LEDs. The cycling pattern in the LEDs signifies the completion of a successful UDA50 diagnostic test. Figure 2-19 shows the location of the four LEDs on each UDA50 module.

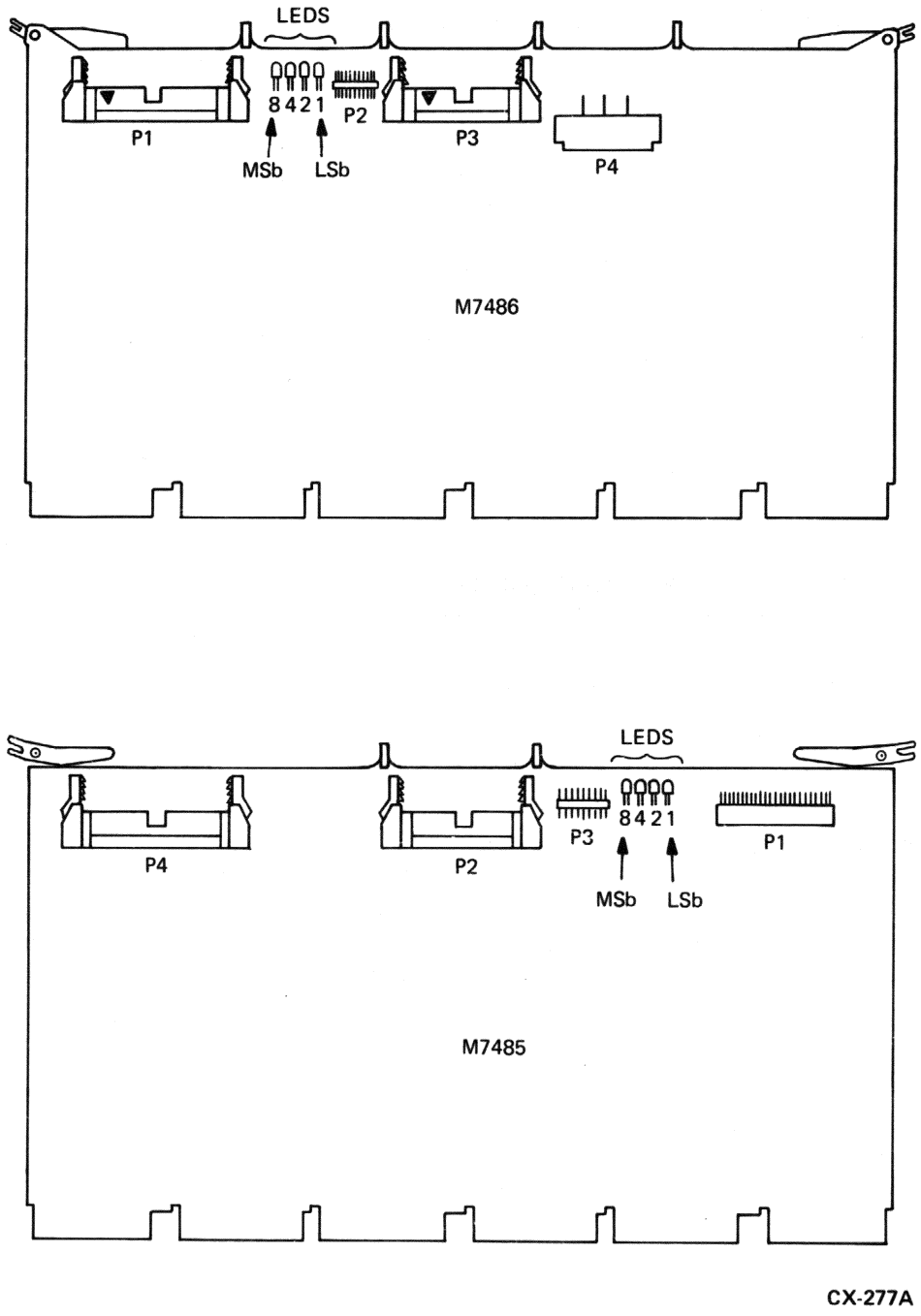

Figure 2-19 Diagnostic LED Locations on UDA50 Modules

If the UDA50 LEDs do not display the cycling pattern after power is applied, look up the LED code in Table 2-3 to locate the problem.

Table 2-3 LED Error and Symptom Codes

M7485 LEDs 8 4 2 1	M7486 LEDs 8 4 2 1	Error Symptoms	Most Likely Failure
0 0 0 1	x x x x	Hex 1; undefined	Undefined
0 0 1 0	0 0 0 0	Hex 2; microcode stuck in init step 2	M7485 or software
0 0 1 1	0 0 0 0	Hex 3; microcode stuck in init step 3	M7485 or software
0 1 0 0	0 0 0 0	Hex 4; microcode stuck in init step 4 or UNIBUS timeout error	M7485 or host inactive
B L 0 1 0 I N K	0 0 0 0	Hex 4/5; test complete UDA50 communicating with host software	No problem
0 1 1 0 x x x x	x x x x 0 1 1 0	Hex 6; undefined	Undefined
0 1 1 1 x x x x	x x x x 0 1 1 1	Hex 7; undefined	Undefined
1 0 0 0	0 0 0 0	Hex 8; wrap bit 14 set in SA register	M7485 or software
1 0 0 1 0 0 0 0	0 0 0 0 1 0 0 1	Hex 9; board one error	M7485
1 0 1 0 1 0 1 0	0 0 0 0 1 0 1 0	Hex A; board two error	M7486
1 0 1 1 x x x x	x x x x 1 0 1 1	Hex B; undefined	Undefined
x x x x 1 1 0 0	1 1 0 0 x x x x	Hex C; Timeout error, check error code in SA register	Many causes
1 1 0 1 x x x x	x x x x 1 1 0 1	Hex D; RAM parity error	M7486
1 1 1 0 x x x x	x x x x 1 1 1 0	Hex E; ROM parity error	M7485
1 1 1 1	1 1 1 1	Hex F; sequencer error	M7485
Cycling pattern	Cycling pattern	None	No problem *
		The cycling pattern continues beyond the start of the host software initialization process. The UDA50 is not responding to the host CPU.	M7485

* The LEDs normally cycle while the UDA50 is waiting for the host to start the initialization process. At that time, it responds to the initialization and the cycling pattern stops. This normally occurs in about two seconds.

Note: 1 = LED ON 0 = LED OFF x = May be ON or OFF

When two codes are given for the same error, both indicate the same failure.

2.4.2 Drive-Resident Diagnostics

Each disk drive should be tested separately by running the drive-resident diagnostics. The procedure for running the resident diagnostics is found in the installation chapter of the disk drive user guide. Perform the drive field acceptance tests found in the installation chapter and then go to Paragraph 2.4.3 for the subsystem diagnostic procedures.

2.4.3 Subsystem Diagnostics

The subsystem diagnostic procedures for the UDA50 controller are different, depending on whether they are used on a PDP-11 CPU or a VAX CPU. The following paragraphs first cover the PDP-11 diagnostics and secondly, the VAX diagnostics.

NOTE
If the diagnostic program reports errors, refer to the UDA50 Service Manual or Maintenance Guide.

2.4.3.1 PDP-11 Subsystem Diagnostics –

- CZUDE (UDA disk formatter)

  CZUDE is not a diagnostic. Do not run it unless specifically instructed to.

- CZUDC (UDA and disk drive diagnostic)

  This diagnostic consists of the following four tests:

  - Test 1 – UNIBUS Addressing Test
  - Test 2 – Disk-Resident Diagnostic Test
  - Test 3 – Disk Functional Test
  - Test 4 – Disk Exerciser Test

The hardware and software questions asked by this diagnostic are shown in the following two samples along with their default answer <X>.

NOTE
Refer to the software documentation for detailed description, error messages, etc.

Sample hardware questions:

```
CHANGE HW (L)    ? Y

 UNITS (D)  ? 1

UNIT 0

UNIBUS ADDRESS OF UDA (0) 172150?

VECTOR (0) 154?

BR LEVEL (D) 5 ?

UNIBUS BURST RATE (D) 0?

DRIVE NUMBER (D) 0?

EXERCISE ON CUSTOMER DATA AREA IN TEST 4 (L) N ?N
```

Sample software questions:

```
CHANGE SW (L)    ? Y

ENTER MANUAL INTERVENTION MODE FOR SPECIAL DIAGNOSIS (L) Y ? N

REMAINING SOFTWARE QUESTIONS APPLY TO TEST 4 ONLY

ERROR LIMIT (D) 32 ?

READ TRANSFER LIMIT IN MEGABYTES - 0 FOR NO LIMIT (D) 0 ?

SUPPRESS PRINTING SOFT ERRORS (L)  Y ?

DO INITIAL WRITE ON START (L)  Y ?

ENABLE ERROR LOG (L)  N ?
```

2.4.3.2 VAX Subsystem Diagnostics –

- ZZ-EVRLB (UDA50 disk formatter)

  ZZ-EVRLB not a diagnostic. Do not run it unless specifically instructed to.

- ZZ-EVRLA (UDA50 disk subsystem diagnostic)

  The VAX UDA host-resident diagnostic contains the following four tests.

  - Test 1 – UNIBUS addressing test
  - Test 2 – Disk-resident diagnostic test
  - Test 3 – Disk functional test
  - Test 4 – Disk exerciser test

  Use the verify section of this diagnostic for system installation.

- ZZ-EVRLC (Generic disk drive exerciser)

  This program tests the read and write ability of any SDI type disk drive from a UDA50, and will display differences in the read and write data to the operator.

NOTE

Refer to the software documentation for detailed descriptions, error messages, etc.

CHAPTER 3
UDA50 PROGRAMMER INFORMATION

3.1 UDA50-SPECIFIC PROGRAMMING INFORMATION

The following information is UDA50-specific and is necessary for anyone needing to write his own software for the UDA50:

- The address of the UDA50 IP register is 772150 (octal).
- The address of the UDA50 SA register is 772152 (octal).
- The UDA50 supports an interrupt vector that is set by the host. This value is typically 154 (octal).
- The UDA50 has a command limit value of 21. This includes 20 MSCP commands plus 1 immediate-only command.
- The UDA50 supports an NPR burst value of 1 to 32 long words. One long-word is the default condition.
- The UDA50 supports only 512 byte disk formats.
- The UDA50 supports both the MSCP and the diagnostic and utilities protocols (DUP).
- The diagnostic option capabilities available on the UDA50 are the purge and poll and the diagnostics wrap.
- The UDA50 supports maintenance read and maintenance write to and from the UDA RAM.
- The UDA50 supports last fail log packets.

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Your comments and suggestions will help us in our efforts to improve the quality and usefulness of our publications.

1. **Which of the following most closely describes your job?** 1 ⊂a⊃ ⊂b⊃ ⊂c⊃ ⊂d⊃ ⊂e⊃ ⊂f⊃ ⊂g⊃ ⊂h⊃ ⊂i⊃

   (a) Administrative support (d) Scientist/Engineer (g) Educator/Trainer
   (b) Programmer/Analyst (e) Systems Manager (h) Computer Operator
   (c) Software support (f) Sales (i) Other _____

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   (a) Less than 1 (b) 1 to 3 (c) 4 to 6 (d) 7 to 9 (e) 10 or more

3. **What did you like *most* about this manual?**

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(h) Visual Appeal	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(i) Relevance of Information	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(j) Ease of Learning	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(k) Ease of Use	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(l) YOUR OVERALL IMPRESSION	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(m) Quality Relative to Other Digital Manuals	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃
(n) Quality Relative to Other Companies' Manuals	⊂1⊃	⊂2⊃	⊂3⊃	⊂4⊃	⊂5⊃

6. **List any errors you found in the manual. (Reference page, table, or figure numbers.)**

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