IMSAI

PIO 4

FUNCTIONAL DESCRIPTION

The PIO 4 board provides for up to four input and four output ports of eight bits each parallel input and parallel output. Each input and each output port has its own latch and both input and output latches are provided with handshaking logic for conventional eight bit parallel transfers.

Connection to the input or output ports is made through board edge connectors at the top of the board on .10 inch centers and the fingers will accept the 3M flat cable edge connectors as well as most other .1 inch center-to-center board edge connectors.

The handshake logic on any input or output port will generate an interrupt. The priority level of the interrupt is selectable. The address of the four ports is four sequential addresses, and this block of four addresses may be jumper-selected to be any block of four sequential addresses in the 256 I/O address space. The board may also be addressed with memory-mapped I/O, in which case normal memory read or write instructions are used to read or write data to the Input/Output ports. When using memory-mapped I/O, board addressing is done by selectable jumpers for the lower byte of address and the upper byte of address is hex FF or octal 377.

Provision is made for each of the four output ports to drive eight LED's for a total of 32 on-board LED's.

This feature can be used to provide program-controlled output for dedicated processor applications of the IMSAI 8080 in which case this PIO board would be plugged in where the front panel would normally be mounted and a special photographic mask made to put in front of it with the appropriate labels for the specific purpose the controller is to be used. The front panel can still be used during development by plugging it into an extender card in another slot.

The board is double-sided glass-epoxy-laminate G10-type and all holes are plated through to eliminate the need for any circuit jumpers. The power regulator is provided with a heat sink and has current limiting for protection in case of an overload. The I/O ports utilize the Intel 8212 8-bit latch.

The +5 and ground pins on the input or output port connectors can be used to provide 5 volt power at up to 200 or 300 milliamperes total from the full board. In addition, approximately 100 additional milliamperes of +5 volt power would be available for each 8212 input or output port which is not installed in the PIO 4 board. For example, if four input ports were installed, but only two output ports were installed, the 5 volt power that could be drawn from the connectors would raise from 300 milliamperes to 500 milliamperes.

THEORY OF OPERATION

The board enable is the output of the 74LS30 in position C9. Input to this 8 input NAND gate is the true or complement address bits 2 through 6, according to how they are jumpered. The input and output status bits are logically ORed and the output or its complement is also jumpered to the NAND gate in position C9. These two are used for I/O reference instructions or these two inputs to the NAND gate are taken from the complement of the status input or output instruction and the high address line which comes from the 74LS30 in position C6. This NAND gate in position C6 is active when all the high order of address bits 8 through 15 are true, that is, high. Address 0 and 1 and their complements are fed into a one-of-4 decoder consisting of the 7427 in position and part of the 7402 in position C11 along with one inverter.

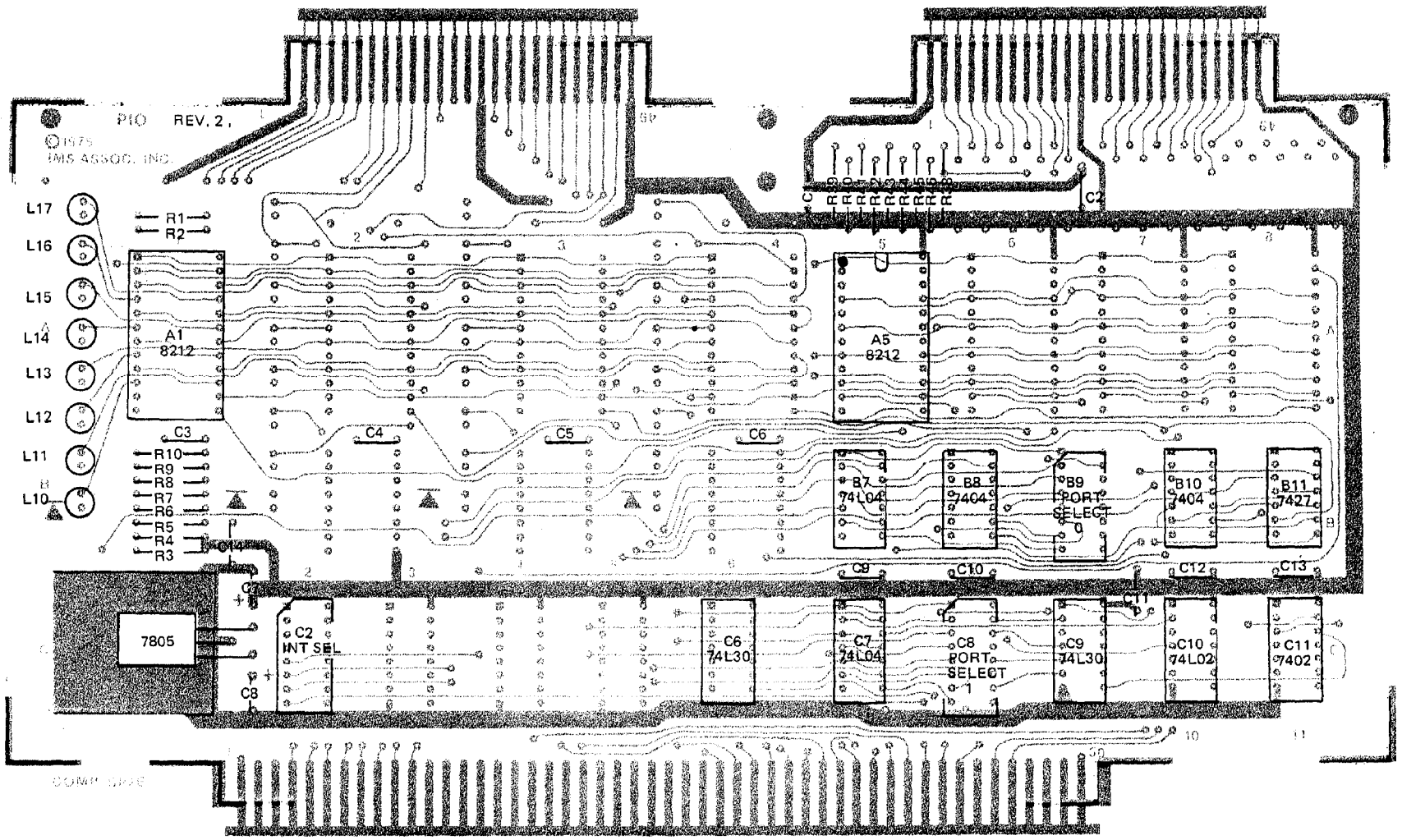
Also as a condition in this one-of-four decoder is the board enable. The outputs of this one-of-four decoder are fed directly to the enable pins on the respective 8212 input or output ports. The DATAIN bus on the IMSAI 8080 system is driven directly from the output of the four input latches. This is a tri-state output and is enabled only when the chip is selected by the one-of-four decoder.

The DATA OUTPUT bus in the IMSAI 8080 goes directly to the four 8212 output ports. The second enable line on each of the input ports is connected to the PROCESSOR DATA BUS-IN signal such that the data is placed on the IMSAI 8080 bus during the time that the processor wishes to read it. The other device select line in output port 8212's is driven by the ORed condition of the PROCESSOR WRITE STROBE or FRONT PANEL WRITE STROBE, these coming from pins 77 and 68 on the IMSAI 8080 back plane respectively. The PROCESSOR DATA BUS-IN signal appears on pin 78 of the IMSAI 8080 back plane.

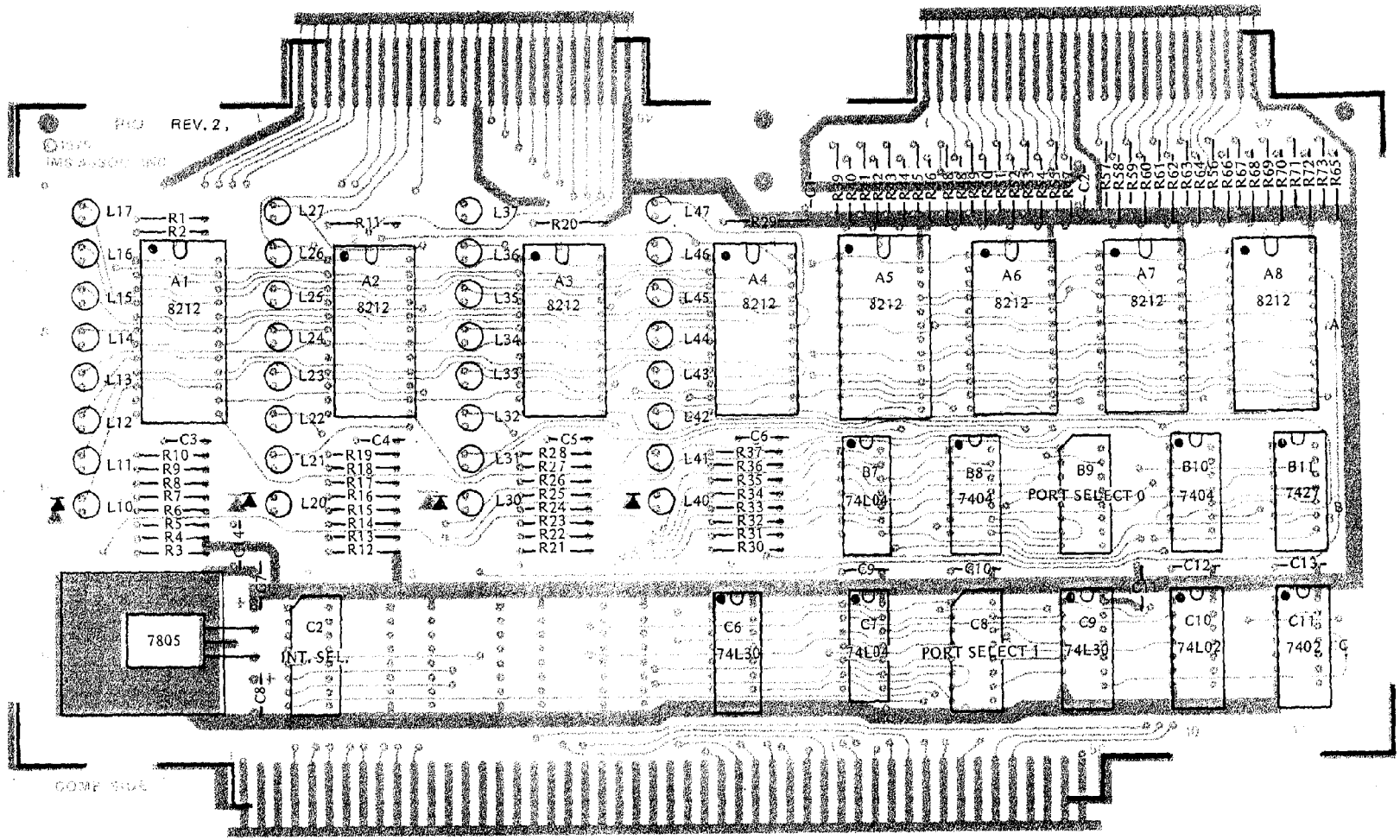
Handling the interrupt levels from the four input and four output ports requires only the interrupt select jumper socket in position 2 so that the appropriate interrupt levels which are already originated by the 8212 chips can be connected as desired to the proper priority interrupt line on the IMSAI 8080 back plane. The remainder of the interrupt function is affected by the PIC-8 board, the Priority Interrupt/Clock board.

The LED's on the output ports are driven through the current-limiting resistor to +5 volts, so that when the output bit is low the LED is on. This orientation was chosen because the 8212's have a greater ability to sink current than they do to source current.

The strobe line into each 8212 input or output port is tied through a 1K resistor to +5 volts so that if the strobe line is not used, it will remain high and noise will not trigger signals on the input or output ports or the interrupt lines. All of the input lines have a 1K resistor to +5 volts, so that when the lines are not connected they exist in a defined state.



IMS ASSOCIATES INC.
ASSEMBLY DIAGRAM
PIO 4–1 REV. 2 5/76

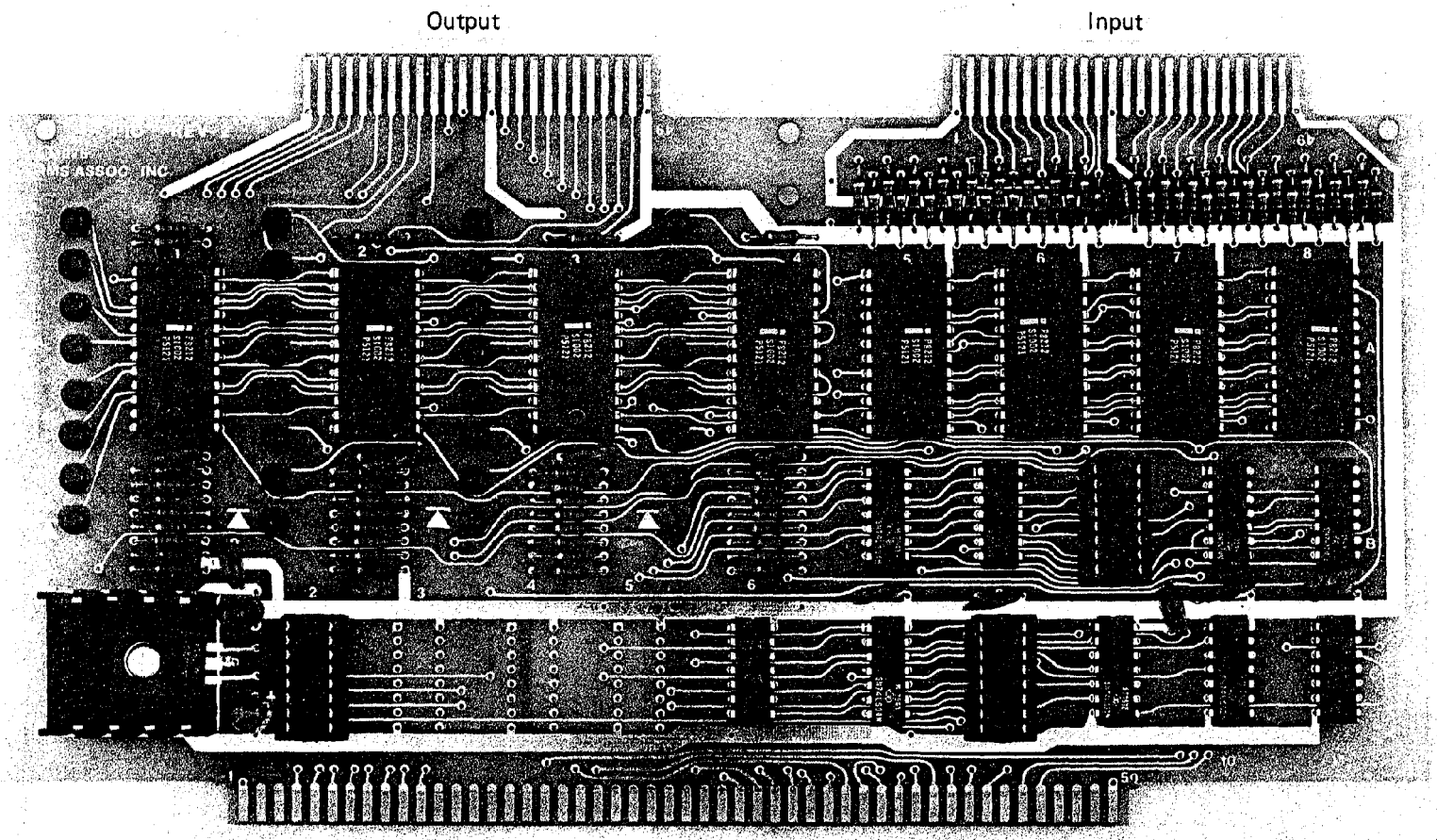


IMS ASSOCIATES INC.

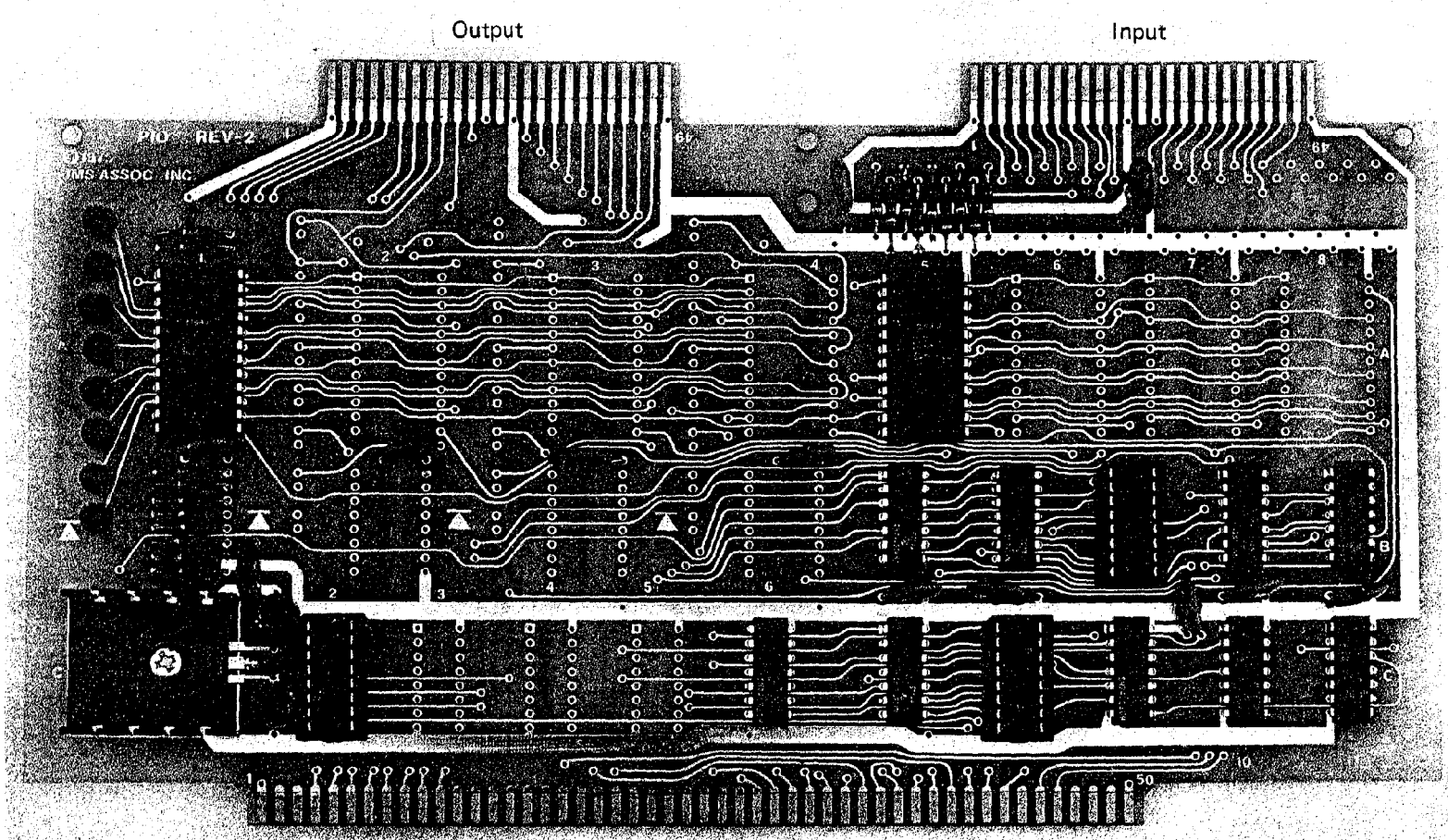
ASSEMBLY DIAGRAM

PIO 4–4 REV 2 1/76

3/4/76



PIO 4 REV 2



PIO 4-1 REV 2

PIO 4, Rev. 2
Parts List

BOARD: PIO 4

ITEM	IMSAI PART #	QUANTITY	DESCRIPTION/IDENTIFYING MARKS
Solder	15-0000001	10'	
Heat Sink	16-0100002	1	Thermalloy Heat Sink/6106B-14
Screw	20-3303001	1	6-32x3/8" Phillips Pan Head Machine
Nut	21-3120001	1	6-32 Hex Nut
Lockwasher	21-3350001	1	#6 Internal Star Lockwasher
Header	23-0400001	3	16 Pin IC Header
Socket	23-0800001	3	16 Pin Solder Tail Socket
Resistor	30-3220362	8 32	(For PIO 4-1) 220 Ohm, ¼ Watt/ (For PIO 4-4) Red, red, brown
Resistor	30-4100362	41	1K Ohm, ¼ Watt/brown, black, red
Capacitor	32-2010010	12	.1uF Disk Ceramic
Capacitor	32-2233070	2	33-25 Tantalum
LED	35-3000001	8 32	(For PIO 4-1) Red Light Emitting Diode (For PIO 4-4)
7402	36-0740201	1	Quad 2 Input NOR/SN7402N
74LS02	36-0740202	1	Quad 2 Input NOR (Low Power Schottky)/ SN74LS02N
7404	36-0740401	2	Hex Inverter/SN7404N
74LS04	36-0740402	2	Hex Inverter (LPS)/SN74LS04N
7427	36-0742701	1	Triple 3 Input NOR/SN7427N
74LS30	36-0743002	2	8 Input NAND (LPS)/SN74LS30N
7805	36-0780501	1	5 Volt Positive Voltage Regulator/ MC7805CP
8212	36-0821201	2 8	(For PIO 4-1) 8 Bit I/O Port/D8212 (For PIO 4-4)
PC Board	92-0000013	1	PIO 4, Rev. 2

ASSEMBLY INSTRUCTIONS

( ) 1. Unpack your board and check all parts against the parts lists enclosed in the package.

( ) 2. If gold contacts on the edge connector appear to be corroded, use pencil eraser to remove any oxidation. NOTE: Do not use Scotchbright or any abrasive material as it will remove the gold plating.

RESISTOR INSTALLATION

( ) 3. Insert and solder the thirty-six 1K ohm, ¼ watt resistors (brown, black, red) at locations R38 through R73 in the upper right hand corner of the board as shown on the Assembly Diagram for PIO 4-4 and the 9 1K, ¼ watt resistors at locations R38 through R46 for PIO 4-1.

( ) 4. Insert and solder the other five 1K ohm, ¼ watt resistors at locations R1, R2, R11, R20 and R29 above the output port locations as shown on the Assembly Diagram for PIO 4-4; and the other two 1K ohm, ¼ watt resistors at locations R1 and R2 at output port location as shown on the PIO 4-1 Assembly Diagram.

IC INSTALLATION

NOTE: All Pin 1's are toward the upper left hand edge and away from the 100 pin connector.

( ) 5. Insert and solder the one 7402 at location C11.

( ) 6. Insert and solder the one 74LS02 at location C10.

( ) 7. Insert and solder the two 7404's at locations B8 and B10.

( ) 8. Insert and solder the two 74LS04's at locations B7 and C7.

( ) 9. Insert and solder the one 7426 at location B11.

( ) 10. Insert and solder the two 74LS20's at locations C6 and C9.

( ) 11. Insert and solder the eight 8212's at locations A1 through A8 for PIO 4-4; the two 8212's at locations A1 and A5 for PIO 4-1. NOTE: If fewer than

4 output or 4 input ports are being installed, they would normally be installed from left to right as the address of the output ports; for instance: address 0 for position A3 and address 3 for position A4. The input port chips are arranged in a similar fashion from low to high address left to right, starting with position A5 and going to position A8. The choice of positions to be filled first can be made according to which addresses desired on the input or output ports.

( ) 12. Insert and solder the twelve .1uF capacitors at locations C1 through C6 and C9 through C14 as shown on the Assembly Diagram. Be sure the capacitors are pulled in close to the board. In applications where the PIO board will be used in place of a front panel for programmed output in dedicated processor uses, care should be taken to lay the .1 disk ceramic bypass capacitors below the lowest LED position. This is to insure that nothing in the upper half of the board extends higher off the board than the LED's. If LED's are to be mounted, they can be mounted at this time.

( ) 13. Insert and solder the two 33uF tantalum capacitors at locations C7 and C8 as shown on the Assembly Diagram. NOTE: Observe polarity (+ to +) as shown on the board.

( ) 14. Insert and solder the 32 LED's at locations L10 through L17, L20 through L27, L30 through L37, and L40 through L47 as shown on the Assembly Diagram for PIO 4-4; the 7 LED's at locations L10 through L17 for PIO 4-1 as shown on the Assembly Diagram. Take a piece of cardboard, plastic or aluminum and cut it to approximately 3/8" wide for a strip about 3/4 inches long and then cut up the center. Don't cut all the way, so that the center saw cut can be placed on either side of the LED's leads, and the LED's can then be pushed into the holes and against the 1/8 inch spacer and soldered. The tool is then removed, and the LED should have a uniform spacing of 1/8 inch above the board. The 220 ohm or 230 ohm LED resistors should also be installed at this time if the LED's are installed. These are user supplied resistors and are not provided by IMSAI.

( ) 15. Insert and solder the 3 16 pin solder tail sockets at locations B9 and C8, to provide for addressing jumpers, and at location C2 to provide for priority interrupt jumpers.

REGULATOR AND HEAT SINK INSTALLATION

( ) 16. Before installing the regulator and heat sink, bend the 7805 regulator leads at 90 degree angles to facilitate mounting on the heat sink.

( ) 17. Insert the #6 screw through the regulator and heat sink on the component side of the board and attach through the lockwasher and nut on the circuit side. Tighten the screw carefully to insure proper alignment of the heat sink. Solder the 7805 leads.

USER GUIDE

The PIO 4 Board has four input ports and four output ports. Each port has an eight bit latch associated with it. These ports may be addressed in one of two different ways: First, addressed as an input/output port with input or output instructions; second, they may be addressed with memory reference instructions. The type of addressing is selectable by jumpers and the board cannot have both types of addressing at the same time. The four input ports form a block of addresses that are four sequential addresses and the four output ports form a block of four sequential addresses which are the same four addresses as the input port. In other words, the same address used with an input instruction to input on port number 0 is the same address used to output on port number 0.

When the board is being used with memory-mapped I/O, any 8080 instruction which either reads or writes a byte from memory can be used to either read or write respectively a byte from an input or output port on the I/O board. That is, a load accumulator, from the address that this board is jumper-selected to respond to, will load the accumulator with the data from the input port addressed. Each of the four input and each of the four output latches are equipped with data strobe lines. Each port has both an interrupt line and a strobe line which can be used as hand-shake signals for conventional parallel data transfers. In the case of the output ports, a low pulse on the strobe line will set the interrupt line low. The interrupt line changes on the falling edge of the strobe line and the strobe line would normally be kept high.

The interrupt line is made high again upon the trailing edge of the WRITE strobe of the processor which is writing a new eight bits of data into the output port. Thus, the strobe line would be the input hand-shaking line and the interrupt line would be the output hand-shaking line. The interrupt line may also be jumpered to one of the IMSAI 8080 priority interrupt lines on the back plane to effect an interrupt to the processor when it goes low, that is, when the strobe line has been pulsed low to indicate it has been taken by the peripheral device.

If it is not desired to use hand-shaking lines, it is not necessary to jumper them or take any other action. Successive bits may be put out to the output ports with no further action by any other device. In this case, the strobe line would remain high from the on-board pull-up resistor and

the interrupt line would remain high for lack of any strobe signal to affect it.

The input ports also have one strobe line and one interrupt line each. Each of the strobe lines for the input ports also has an on-board pull-up resistor. If the strobe line is not connected or if it is driven high, the data in the latch will follow the input lines. The program can read input from the input lines. The program can read input from the input lines and it will read the data that is present at the instant that the input instruction is executed. When the strobe line is made low the data that is present on the input lines at the falling edge of the strobe lines is latched into the input latch and remains there as long as the strobe line is held low. As soon as the strobe line is raised, the data in the latch will again follow the input lines. On the falling edge of the strobe lines the interrupt line will change from high to low.

This can be jumpered to the IMSAI 8080 priority interrupt lines to create an interrupt to the processor, and/or it may be used as an indication that the processor has not yet read the latched data. If, while the strobe line is being held low, the processor reads data from the input port, then the interrupt line will return high at the trailing edge of the read strobe, thus indicating to the peripheral device that the processor has read that data and the latch is available for latching the next data byte into it. Each input and each output port has its own strobe and interrupt line. They may be driven together or separately.

All four of the output port strobe, interrupt and data lines appear on the 50 pin connector on the upper left edge of the board, and all four of the input port strobe, interrupt and data lines appear on the 50 pin connector on the upper right hand edge of the board.

Also appearing on these connectors is ground and +5 volts. See the schematic diagram for pin numbers.

Both the input and the output connectors are designed to accept 3M-type flat cable board edge connectors. The flat cable may be run directly from the peripheral in through the flat cable clamp at the top back of the IMSAI 8080 Cabinet and directly to the edge connector which slips onto the top of the PIO 4 board.

Each of the data input lines on the input ports is tied to +5 volts through a 1K resistor so that unused lines will be read as high data level or true data level.

As an alternative, two EIA type connectors, 25 pins each, may be connected by way of flat cable and the 3M flat cable system to the board, so that the board connections can be taken to the EIA connectors with no hand wiring. This is true of the input port connector and the output port connector.

The connectors are arranged so that if the EIA 25 pin connectors are used, either two output ports or two input ports appear on the pins of the EIA connector along with both ground and +5 volts. If there are two devices, each needing only one output port, they may be connected without hand wiring both to the EIA 25 pin connectors by passing the flat cable through the first connector into a second so that two 25 pin connectors can be connected to the same flat cable; then only one port would be used in the first connector and the other port would be used in the other connector. This would permit separate plugs from separate peripheral devices without requiring any hand wiring of cables. The same, of course, is true for the input ports.

If desired for custom program display front panel-type use or just debugging use, the user can assemble the output ports with 8 LED's and current limiting resistors of either 220 or 330 ohms, so that the user has a visual indication fo the status of the output bits.

If the PIO 4 board is to be used in place of the front panel for custom program output, care should be taken during assembly to make sure that the disk ceramic bypass capacitors are not stood up but rather are laid over on top of the resistors they are next to so that they do not extend higher than the LED's.

The LED's on the output ports are turned on when the data bit is written as a 0. This was done because it was felt it was a more cost-effective solution for the user to put a complement instruction in his/her firmware than it was for IMSAI to put inverters in the hardware.

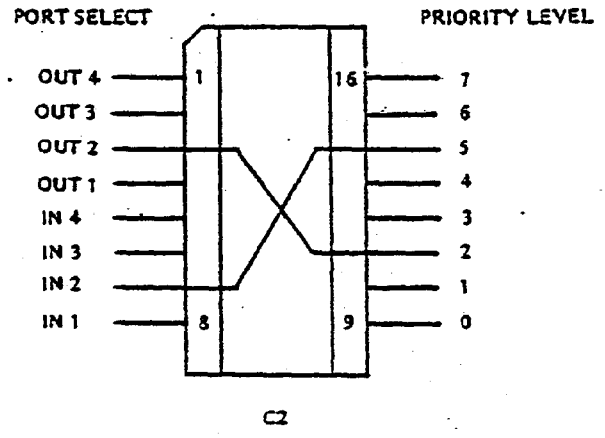
The +5 and ground pins on the input and output port connectors can be used to provide 5 volt power at up to 200 or 300 milliamperes total from the full board. In addition, approximately 100 additional milliamperes of +5 volt power would be available for each 8212 input or output port

which is not installed in the PIO 4 board. For example, if four input ports were installed, the 5 volt power that could be drawn from the connectors would raise from 300 to 500 milliamperes.

INTERRUPT SELECT JUMPER SOCKET

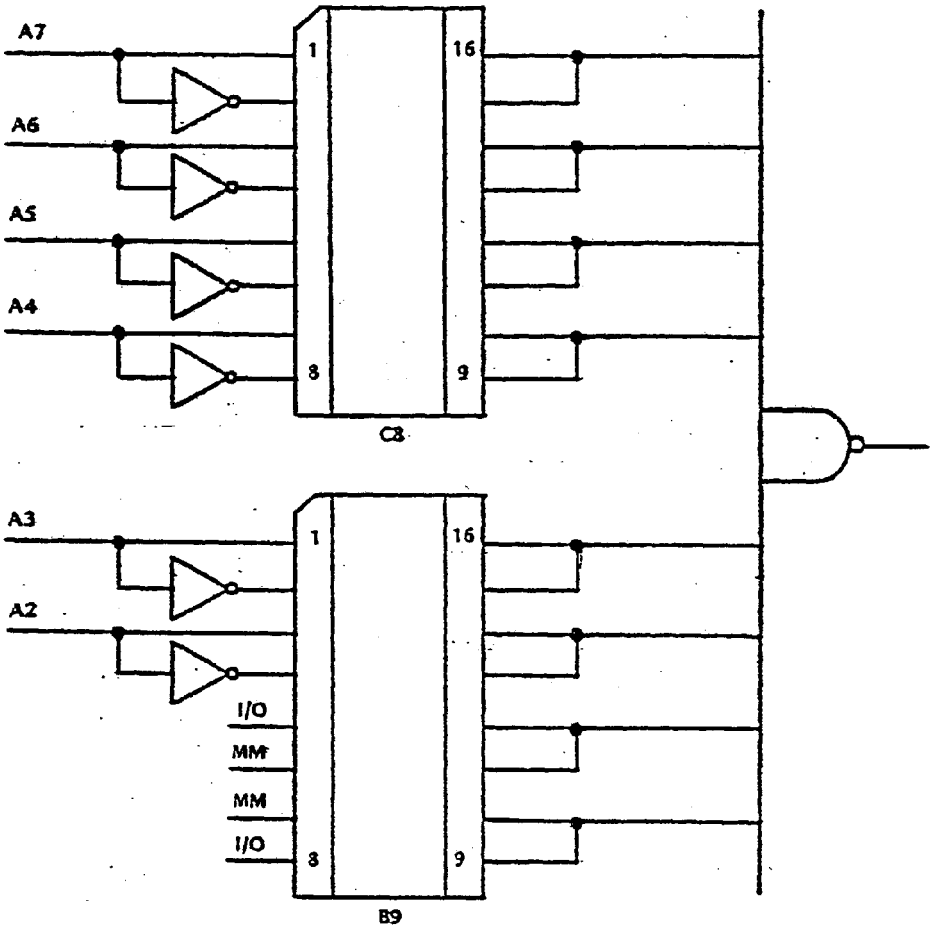
Position C2 on the PIO 4 board is the interrupt select jumper socket. Appearing at the pins of this socket are all eight of the priority interrupt lines for the IMSAI 8080, the four input interrupt lines and the four output interrupt lines of the PIO 4 board. Thus, any interrupt line desired to be used may be jumpered from the appropriate pin as noted on the diagram below.

If an interrupt is desired to be used, the jumper may be put between the interrupt line from the desired input or output port to the desired priority interrupt on the IMSAI 8080 back plane. The IMSAI PIC-8 board must be used to monitor these interrupt lines and originate the interrupt to the processor according to which line is requesting an interrupt. If more than one line is requesting an interrupt at the same time, the higher priority line rules. An example is shown below for connecting the interrupt line from input port 2 to level 5 priority and the interrupt line from output port 2 to level 2 priority interrupt.



C2

BOARD ADDRESS SELECTION JUMPER SOCKETS



The board address is selected by jumpers or a DIP switch in locations C8 and B9. There are two cases for which this board may be jumpered: 1) to respond to input/output instructions and 2) to respond to memory access instructions. The case of input/output instructions will be treated first.

In selection location B9, pins 8 and 9 must be jumpered together and pins 5 and 12 must be jumpered together. Address bits 0 and 1 determine which of the four input or output ports will be addressed. Port address bits 2 and 3

are also selected on location B9 with jumpers. If, for instance, address bit 2 is desired to be a 0 when the board responds, then pins 4 and 13 would be jumpered together. If address bit A2 was desired to be a 1, then either pins 3 or 13 may be jumperd together, since 13 and 14 are tied to the common address selection input.

It is suggested, however, that when jumpers are being used, pins 3 and 13 be connected together to provide an easy visual indication of whether the address bit is a 1 or a 0 since that will correspond to whether the jumpers are slanted or straight across the jumper socket. Pins 13 and 14 were tied together so that an 8 position DIP switch can be inserted in this location and used to select the address.

Address bits 3, 4, 5, 6 and 7 are jumpered in a similar manner. Address bit 3 is also on location B9; address 4, 5, 6 and 7 are jumpered on position C8. See the diagram on the previous page for pin numbers for each address bit.

If it is desired to use the board in a memory-mapped I/O capacity, then in position B9 the jumpers between pins 8 and 9 and 5 and 12 must be removed and two jumpers inserted between pins 7 and 10 and between 6 and 11. The remaining jumpers for bits 2 through 7 function exactly the same and affect the lower eight bits of the memory address. The upper eight bits of the address will always be all ones, that is hex FF or octal 377.

When used as a memory-mapped I/O board, all instructions that normally affect the memory will operate on the I/O ports. For example, an increment memory instruction would read the data from the addressed input port, increment that data by one and output it on the same address output port.

IMSAI

PIO 6

FUNCTIONAL DESCRIPTION

The PIO6 Board provides the IMSAI 8080 Microcomputer System with two sets of 24 parallel programmable I/O lines and the capability of extending its own standard I/O bus to peripheral devices. Each set of 24 parallel I/O lines is derived from Intel's 8255 programmable peripheral interface integrated circuit. The function of the PIO6 Board is that of a general purpose I/O component to interface peripheral equipment to the IMSAI 8080 Microcomputer System bus.

The functional configuration of the PIO6 Board is controlled by the microprocessor software. The twenty-four 8255 I/O pins are programmable in two groups of 12 each and used in three basic modes of operation:

Mode 0 - Each group of 12 I/O pins may be programmed in sets of four to be input or output.

Mode 1 - Each group of 12 may be programmed to have eight lines of input or output. The four remaining lines in each group are left for "handshaking" and interrupt control signals.

Mode 2 - Bidirectional bus mode which uses eight lines for a bidirectional bus, and five lines, borrowing one from the other group, for "handshaking".

The control lines of the 8255 chips are also brought to PIO6 connector pins (in J2 and J3) for additional control by the peripheral device.

Enough microprocessor control and bus signals are brought through the PIO6 Board connectors J2 and J3 so that the "Isolated I/O" technique directly from the processor can be implemented in the peripheral device. With the addition of J4 to the PIO6 Board, the "Memory Mapped I/O" technique directly from the microprocessor can be implemented in the peripheral device. J4 also provides interrupt lines from the microprocessor. Pads are provided on the PIO6 board so that interrupt lines from the 8255's can be directly jumpered to the processor's vectored interrupts.

Connection to the input or output ports is made through board edge connectors at the top of the board on 0.10 inch centers, and the fingers will accept 3M flat cable edge connectors as well as most other 0.1 inch center to center board edge connectors.

The board uses a 7805 integrated circuit regulator for the +5 volt power and tantalum capacitors before and after the regulator with ample ceramic disk capacitor bypassing throughout the board.

The board size is 4.7 inches by 10 inches with a 100 pin edge connector on the bottom, dual 50's on 0.125 inch centers. On the top of the board are two 50 pin edge connectors, dual 25's on 0.10 inch centers and a 26 pin edge connector, dual 13's also on 0.10 inch centers.

Connector fingers on all edge connectors are gold plated over nickel for reliable contact and long life. The remainder of the board circuitry is tin-lead plated for appearance and reliable solder connections.

The board is double sided glass-epoxy-laminate G10-type, and all holes are plated through to eliminate the need for any circuit jumpers. The power regulator is provided with a heat sink and has current limiting for protection in case of an overload.

The +8, +18, and -18 volt lines provided at the PIO6 Board top edge connectors are bussed directly from the microprocessor motherboard and are unregulated. Before using these voltages, the user should regulate these lines with, for example, a 7805 integrated circuit regulator to obtain +5 volts.

THEORY OF OPERATION

The PIO6 Board is enabled by having its address (as jumpered in the Address Jumper Sockets) appear on the microprocessor address lines during an input or output instruction. When this occurs, the outputs of the Address Jumper Socket will all be high, causing the output of the 74LS30 at location C7 to be low which is the true state of the board enable signal "/BDENA". This signal is buffered by an 8T97 and passed on to connectors J2 and J3 as "/HIADD". Also, AND'ed into the board enable signal is the OR of the microprocessor status bits "SINP" and "SOUT" which are the strobes used to indicate input instruction and output instruction respectively.

The board enable signal is further AND'ed with address lines 2 and 3 to create the 8255 chip selects "/CSO" and "/CS1". This is done in three section of the 74LS32 in location C8. To get either of the chip selects true, address line 3 must be low. Address line 2 low allows /CSO to be true while address line 2 high allows /CS1 to be true.

Once an 8255 is selected, it becomes responsive to the I/O command to transfer data to it or from it. The various functions of which the 8255's are capable are selected by the appropriate combination of address bits 0 and 1 which are bussed to 8255 port address inputs A0 and A1 (pins 9 and 8).

After buffering through 8T97's, the processor's read (PDBIN) and write (/PWR) strobes are wired to the read and write lines of the 8255's. The read signal is inverted before reaching the 8255 to create the proper polarity read signal.

External clear (/EXT CLR) from the processor front panel switch and power on clear (/POC) from the processor are OR'ed together to provide the reset signal to the 8255's and the J2 and J3 connectors.

Four 8216's are utilized to provide two levels of buffering for the data bus. The first pair buffer between the microprocessor and the 8255's. The second pair buffer between the 8255's and the J2 and J3 connectors. The board enable signal (/BDENA) allows the microprocessor data bus to be connected to the 8255's data bus. In addition, if address line 3 (A3) is high, the 8255 bus is connected to the J2 and J3 connectors. The external board enable signal available to the J2 and J3 connectors (/BDEN) enables both pairs of 8216's which allow the microprocessor data bus to be bussed to the J2 and J3 connectors.

All other processor signals brought to the J2, J3 and J4 connectors are buffered by 8T97's. The processor voltages +8, +18 and -18 volts and GROUND are bussed directly from the J1 connector (which plugs into the processor motherboard) to the J2 and J3 connectors.

Traces from the 8255 lines "PCO" and "PC3" are brought from each 8255 to the bottom of the board where they may be jumpered to inverters (to get the right polarity) and then jumpered to either the processor's "/INT" line or one of the vectored interrupts.

TABLE 1

SIGNAL DESCRIPTION J2 & J3 CONNECTORS

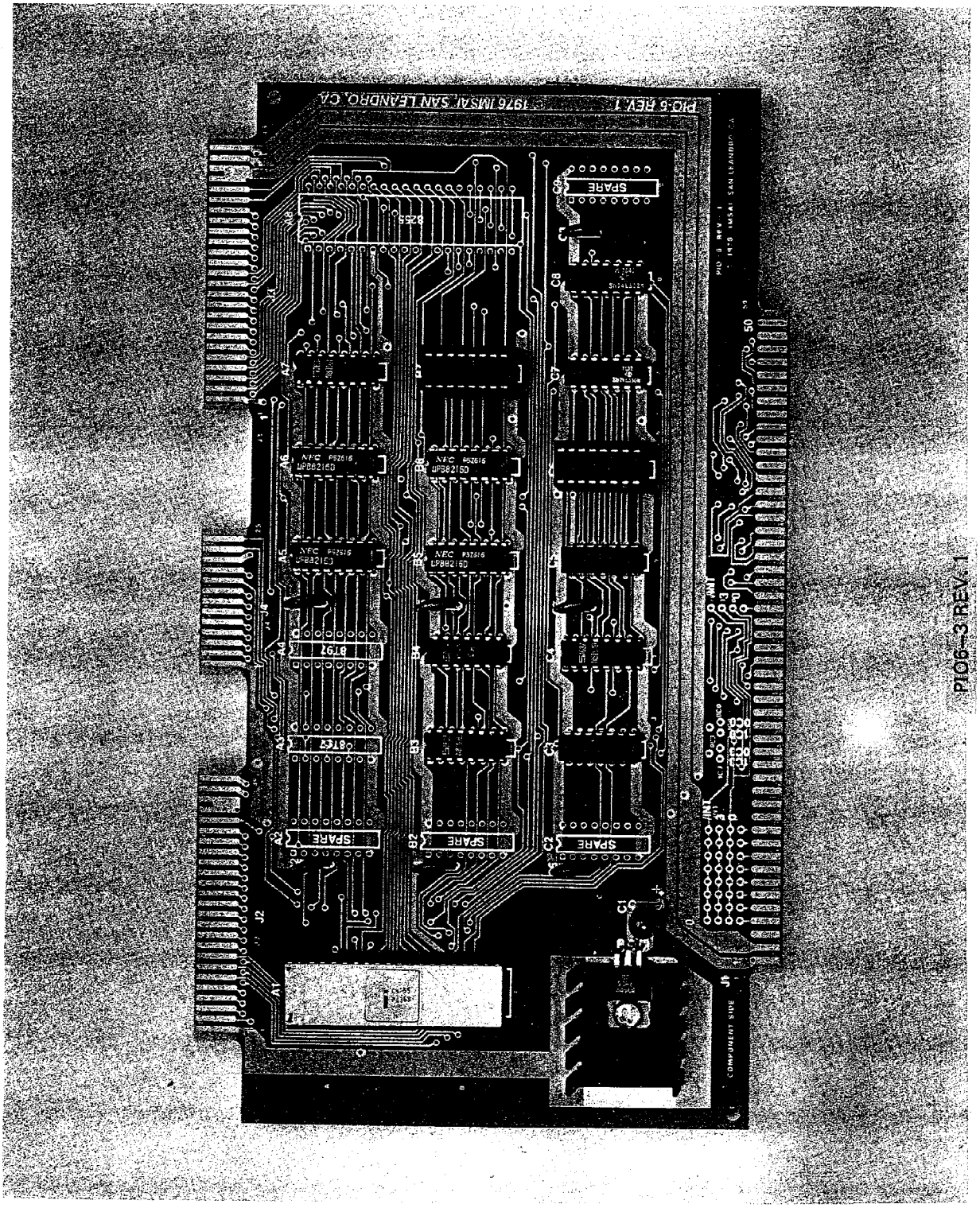
Pin #	Name	Description
1	GROUND	
2	PB0	
3	PB1	
4	PB2	
5	PB3	Port B lines brought directly from
6	PB4	8255 to connector.
7	PB5	
8	PB6	
9	PB7	
10	PC0	
11	PC1	
12	PC2	
13	PC3	Port C lines brought directly from
14	PC4	8255 to connector.
15	PC5	
16	PC6	
17	PC7	
18	PA0	
19	PA1	
20	PA2	
21	PA3	Port A lines brought directly from
22	PA4	8255 to connector.
23	PA5	
24	PA6	
25	PA7	
26	A0	Buffered low order address bits from
27	A1	microprocessor.
28	A2	
29	A3	
30	DB0	
31	DB1	
32	DB2	
33	DB3	Bidirectional data bus from micro-
34	DB4	processor buffered through two 8216's.
35	DB5	
36	DB6	
37	DB7	
38	/HIADD	High Address. Same as internal PIO-6 signal "/BDENA" except buffered through an 8T97. This signal is the decode of the PIO-6 port address. Address lines

TABLE 1

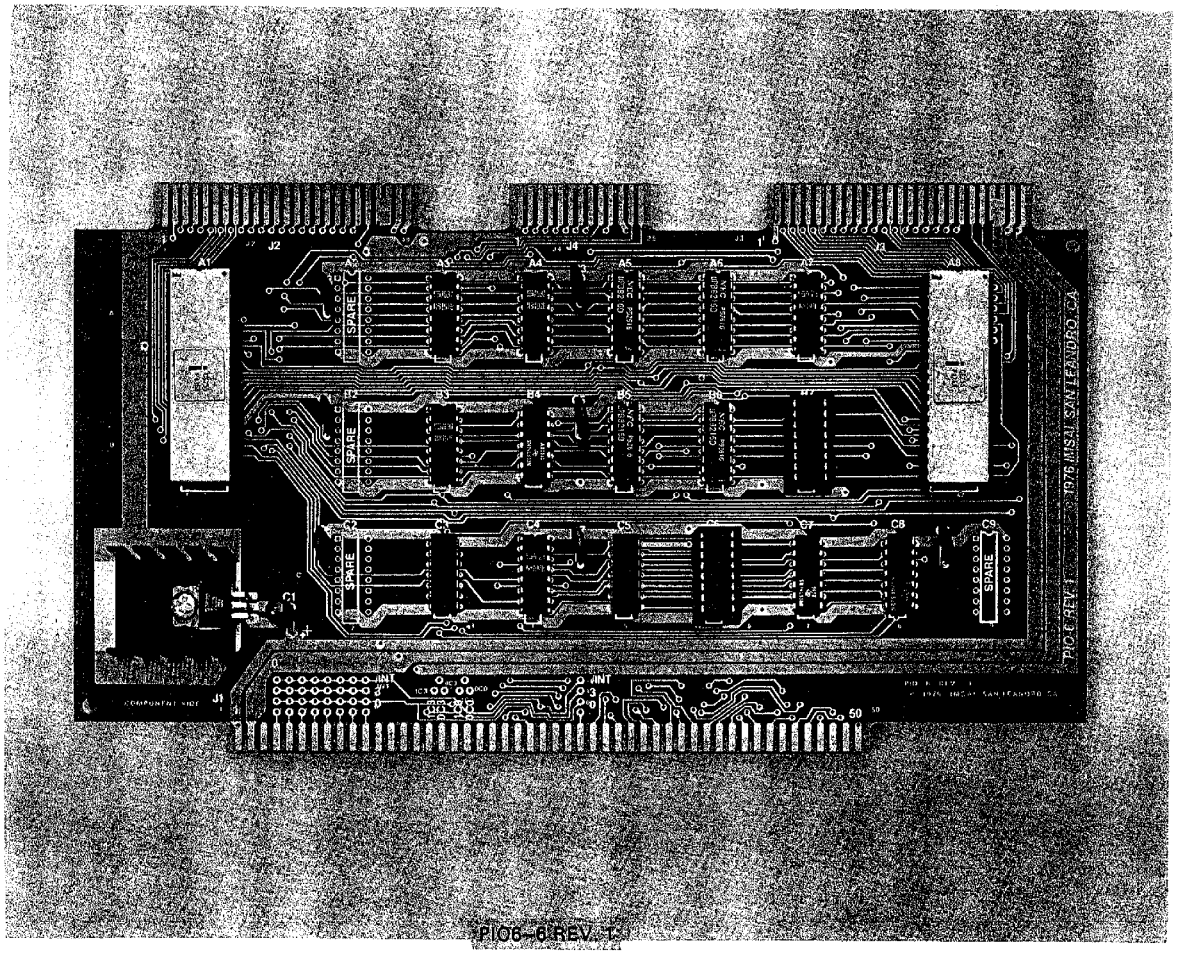
Pin #	Name	Description
38	/HIADD (Cont.)	"A2" through "A7" are decoded. "A2" and "A3" may be jumpered to "DON'T CARE".
39	/RESET	Buffered external clear signal from microprocessor front panel switch.
40	DBIN	Buffered "PDBIN" signal from microprocessor. Processor command/control output signal indicating to external circuits that the data bus is in the input mode.
41	/WR	Buffer /PWR" from microprocessor. Processor command/control output used for memory write or 1/O output control. Data on the data bus is stable while the "/PWR" is active.
42	GROUND	
43	+8V	
44	+8V	+8 volts unregulated.
45	+8V	
46	+18V	+18 volts unregulated.
47	+18V	
48	-18V	
49	-18V	-18 volts unregulated.
50	GROUND	

TABLE 2

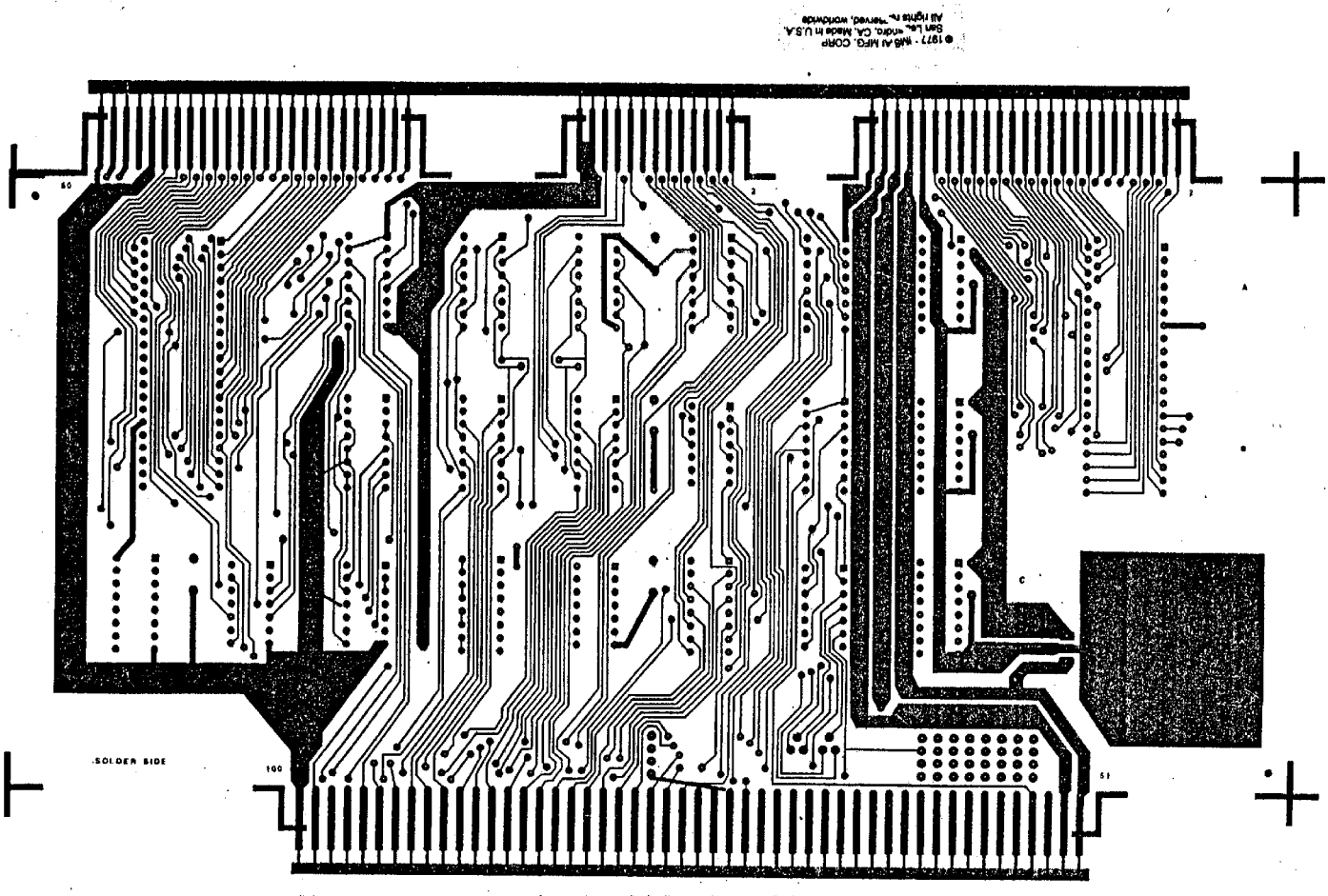
Pin #	Name	Description
20	INP	Buffered status output signal from the microprocessor which indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when "PDBIN" is active.
21	GROUND	
22	READY	Buffered "PRDY" signal to the microprocessor. Processor command/control input that controls the RUN state of the processor. If the line is pulled low, the processor will enter a WAIT state until the line is released.
23	SYNC	Buffered "PSYNC" from the microprocessor. Processor command/control output indicating the beginning of each machine cycle.
24	GROUND	
25	Ø2	Buffered phase 2 clock from the microprocessor.
26	GROUND	


PIO-6 REV 1
1976 IMSAI SAN LEANDRO, CA
SPARE
NEC P82216
UPB8216D
COMPONENT SIDE

PIO6-3 REV.1


SPARE
SPARE
SPARE
SPARE
PIO-6 REV 1
1976 MSI SAN LEANDRO, CA
J1
J2
J3
J4
50

PIO6-6 REV. 1



PIO8 REV. 1 (CUIT SIDE

PIO6-3
Parts List

Item	IMSAI Part #	Quantity	Description/Identifying Marks
Heat Sink	16-0100002	1	Thermalloy, 5 Prong/6106-B-14
Screw	20-3302001	1	6-32 x 5/15" Phillips Pan Head Machine
Nut	21-3120001	1	6-32 x ¼" (OD)
Lockwasher	21-3350001	1	#6 Internal Star
Wire	22-0030001	1'	Wire, Wire Wrap, 30 GA., Kynar, Blue
Header **	23-0400001	2	16 Pin
Socket **	23-0800001	2	16 Pin, Solder Tail Low-Profile IC Socket TIN C831602
Socket	23-0800004	1	40 Pin, Solder Tail Low-Profile IC Socket TIC 834002
Capacitor	32-2010010	7	.1uF Disk Ceramic Capacitor
Capacitor	32-2233070	1	33uF, 25V Tantalum Capacitor
8T97	36-0089701	3	Tri-State Buffer/N8T97B
74LS04*	36-0740402	2	Hex Inverter/DM74LS04N
74LS08*	36-0740802	1	Quad 2 Input AND/SN74LS08N
74LS30*	36-0743002	1	8 Input NAND/SN74LS30N
74LS32*	36-0743202	1	Quad 2 Input OR Gate/SN74LS32N
7805	36-0780501	1	5 Volt Positive Voltage Regulator/7805CU
P8216	36-0821601	4	Bi-directional Bus Driver/μPB8216D
8255	36-0825501	1	Programmable Peripheral Interface/C8255
PC Board	92-0000038	1	PIO6-3

* NOTE: Regulator version of all chips is OK.

** Replaceable by 2, 8-position DIP Switches.

Item	IMSAI Part #	Quantity	Description/Identifying Marks
Heat Sink	16-0100002	1	Thermalloy 5 Prong/6106-B-14
Screw	20-3302001	1	6-32 x 5/16" Phillips Pan Head Machine
Nut	21-3120001	1	6-32 x ¼" (OD)
Lockwasher	21-3350001	1	#6 Internal Star
Wire	22-0030001	1'	Wire, Wire Wrap, 30 GA., Kynar, Blue
Header **	23-0400001	2	16 Pin
Socket **	23-0800001	2	16 Pin, Solder Tail Low-Profile IC Socket TIN C831602
Socket	23-0800004	2	40 Pin, Solder Tail Low-Profile IC Socket TIC 834002
Capacitor	32-2010010	7	.1uF Disk Ceramic Capacitor
Capacitor	32-2233070	1	33uF, 25V Tantalum Capacitor
8T97	36-0089701	5	Hex Tri-State Buffer/N8T97B
74LS04*	36-0740402	2	Hex Inverter/DM74LS04N
74LS08*	36-0740802	1	Quad 2 Input AND/SN74LS08N
74LS30*	36-0743002	1	8 Input NAND/SN74LS30N
74LS32*	36-0743202	1	Quad 2 Input OR Gate/SN74LS32N
7805	36-0780501	1	5 Volt, Positive Voltage Regulator/7805CU
P8216	36-0821602	4	Bi-directional Bus Driver/μPB8216D
8255	36-0825501	2	Programmable Peripheral Interface/C8255
PC Board	92-0000038	1	PIO6-6

* NOTE: Regular version of all LS chips is OK.

** Replaceable by 2, 8-Position DIP Switches.

PIO6-M
Parts List

Item	IMSAI Part #	Quantity	Description/Identifying Marks
Socket	23-0800004	1	40 Pin, Solder Tail Low-Profile IC Socket TIC 834002
8T97	36-0089701	2	Tri-State Buffer/N8T97B
8255	36-0825501	1	Programmable Peripheral Interface/C8255

1. Unpack your board and check all parts against the parts list enclosed.

2. If gold contacts on the edge connectors appear to be tarnished, use pencil eraser to remove any oxidation.
NOTE: Do not use Scotchbright or any abrasive material as it may remove the gold plating.

IC INSTALLATION

NOTE: Pin 1's are located toward the upper left hand edge of the printed circuit board and the three edge connectors.

3. Insert and solder the two 74LS04's at locations C3 and C5 as shown on the Assembly Diagram.

4. Insert and solder the one 74LS08 at location B4 as shown on the Assembly Diagram.

5. Insert and solder the one 74LS30 at location C7 as shown on the Assembly Diagram.

6. Insert and solder the one 74LS32 at location C8 as shown on the Assembly Diagram.

7. Insert and solder the five 8T97's at locations A3, A4, A7, B3 and C4 (three for PIO6-3 at locations A7, B3 and C4) as shown on the Assembly Diagram.

8. Insert and solder the four 8216's at locations A5, A6, B5 and B6 as shown on the Assembly Diagram.

9. Insert and solder the two 40 pin sockets at locations A1 and A8 as shown on the Assembly Diagram (one for PIO6-3 at location A1).

10. Insert and solder the two 16 pin sockets at locations B7 and C6 as shown on the Assembly Diagram.

DISCRETE COMPONENT INSTALLATION

11. Insert and solder the one 33uF, 25V tantalum capacitor at location C1 as shown on the Assembly Diagram.

12. Insert and solder the seven .1uF disk ceramic capacitors at locations C2 through C8 as shown on the Assembly Diagram.

HEAT SINK AND REGULATOR INSTALLATION

13. Bend the leads of the 7805 regulator at 90 degree angles approximately ¼" from the bottom edge of the regulator to facilitate insertion.

14. Place the heat sink on the board and insert the regulator leads into the holes. Use the #6 screw and insert from the top side through the regulator and heat sink and tighten with lockwasher and nut on back

side of the board. Solder the 7805 leads. NOTE: Be sure to place in proper position to prevent shorting.

15. Insert the two 8255's at this time into their proper sockets (one for PIO6-3) at locations A1 and A8.

16. Insert the 16 pin headers at this time at locations B7 and C6.

17. On the solder side of the board, cut the trace going to pin 13 of IC-C7 (74LS30). Solder an insulated jumper between pin 11 of IC-C7 (74LS30) and pin 11 of B7 (address jumper select). This may be done most easily on the back of the board (solder side).

NOTE: Step 18 is only necessary if direct interrupt to the $\overline{\text{PINT}}$ bus is used. It is not necessary if either no interrupts from this board are used or vectored interrupts are used.

18. Cut the trace coming from pin 28 of J1 on the component side of the board. Solder an insulated jumper between the top of pin 73 of J1 and the pad with the large diameter hole immediately above pin 28 of J1. This is the pad that was cut free from pin 28. Be careful not to allow solder to flow down the edge connector at pin 73. This jumper is on the solder side of the board.

SER GUIDE

The basic purpose of the PIO6 Board is to provide the microprocessor with two programmable 24 line parallel I/O ports and to extend a fully buffered microprocessor I/O interface to a peripheral device.

The address of the PIO6 Board is jumpered using the "Address Jumper Select" headers in locations C6 and B7. These sockets are also shown in Figure One. The address byte is divided in half. Location C6 contains the four high order address bits. To make an address bit high, the odd numbered pin on the left must be jumpered to the corresponding pin on the right. For example, the dotted lines in Figure One represent an address of:

A7	A6	A5	A4
O	1	O	1

In the low order half of the address, bits 2 and 3 are selected by location B7. These bits can be jumpered as above using pins 5, 6, 7, 8, 9, 10, 11, and 12. Bits 2 and/or 3 can be jumpered as "DON't CARE" bits by jumpering pin 3 to 14 or 4 to 13 respectively.

When addressing the 8255's bit 3 must be low. Bit 2 high, addresses 8255-1 and bit 2 low addresses 8255-0. Address bits 0 and 1 are used for addressing the particular functions within a given 8255. For example, when writing to an 8255 with address bits 0 and 1 both high, this causes the 8255 to interpret the incoming data byte as a control word. A summary of the address scheme is shown in Figure Two.

The 8255's operate completely independent of one another. The functional configuration of the 8255's is under program control by the software residing in the microprocessor. A control word is output to an 8255 setting up a desired functional configuration, while other I/O commands operate on the particular configuration. Refer to the Intel 8080 Microcomputer Systems User's Manual for the details of operation of the 8255's.

Connectors J2 and J3 contain all the signals necessary for operation of and interfacing the 8255's to peripheral devices. Both J2 and J3 are 50 pin edge connectors which accept a 3M type flat cable edge connector. Table One is a list and description of the signals contained in connectors J2 and J3 (see PIO6 Theory of Operation).

By using either J2 or J3 combined with J4, the microprocessor I/O bus can be extended to a peripheral device so the user may implement I/O logic direct from the microprocessor. Both Intel's "Isolated I/O" and "Memory Mapped I/O" techniques may be utilized. The "Isolated I/O" technique utilizes input and output commands between a particular address port and the A register. "Memory Mapped I/O" allows the user to use any memory reference instruction for I/O. It treats I/O ports

as memory locations. For details on these techniques and the microprocessor I/O bus, the user is referred to Intel's user's guide again and the microprocessor user's guide.

The J4 connector has 26 pins and also accepts the 3M type flat cable edge connectors.

Signals to and from the 8255's are direct with no buffering. 8255 outputs have the ability to source 1 ma of current at 1.5 volts. This allows Darlington transistors to be directly driven for applications, such as printers and high voltage displays.

The +18, -18 and +8 volt power supplied to J2 and J3 is unregulated. The +5 volts is regulated and is output from the 7805 on the PIO6 Board. The +5 volts supplies the card and does not appear on any of the edge connectors.

The PIO6 Board plugs into one slot of the microprocessor motherboard. Cables may be run directly from the PIO6 Board or from the PIO6 Board to 25 pin EIA connectors at the rear of the microprocessor and from here to the peripheral device.

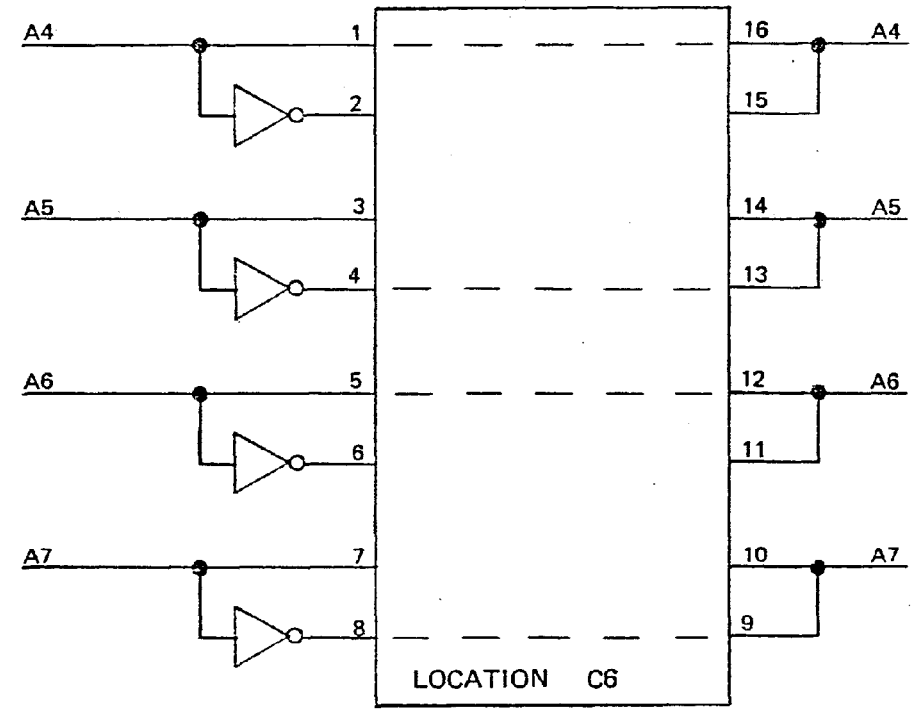
The PIO6 Board is available in two configurations: PIO6-3 and PIO6-6. The PIO6-3 contains one 8255 and the PIO6-6 utilizes two 8255's. J2, J3 and J4 cables are available separately for either configuration.

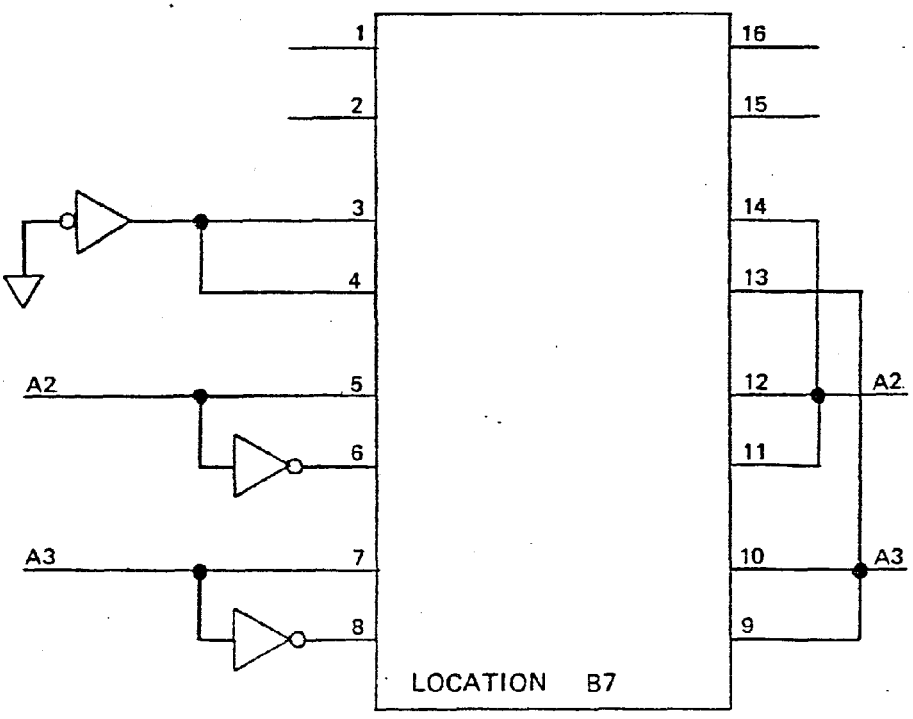
The 8255 I.C.'s can be programmed to generate a signal to be used as an interrupt request (see Intel 8080 Microcomputer Systems User's Manual for details).

These signals, PC0 and PC3 are brought down to the bottom of the board where they can be jumpered for use. They are labelled "0C0" and "0C3" from 8255-0 and "1C0" and "1C3" from 8255-1. Any two of these can be jumpered to an adjacent inverter input. The inverter outputs labelled "3" and "0" can be jumpered to "/INT" at the pad provided which connects to J1-73 or to the vectored interrupt pads connecting to J1-4 through J1-11. "/INT" is also connected to J4-2 so that an external interrupt request may be generated and brought to either the MPU "/INT" or the vectored interrupts.

A dual 25 card edge connector to the dual D connectors, Cable B, is available for providing interface connections at the back of the chassis.

FIGURE ONE ADDRESS SELECTION





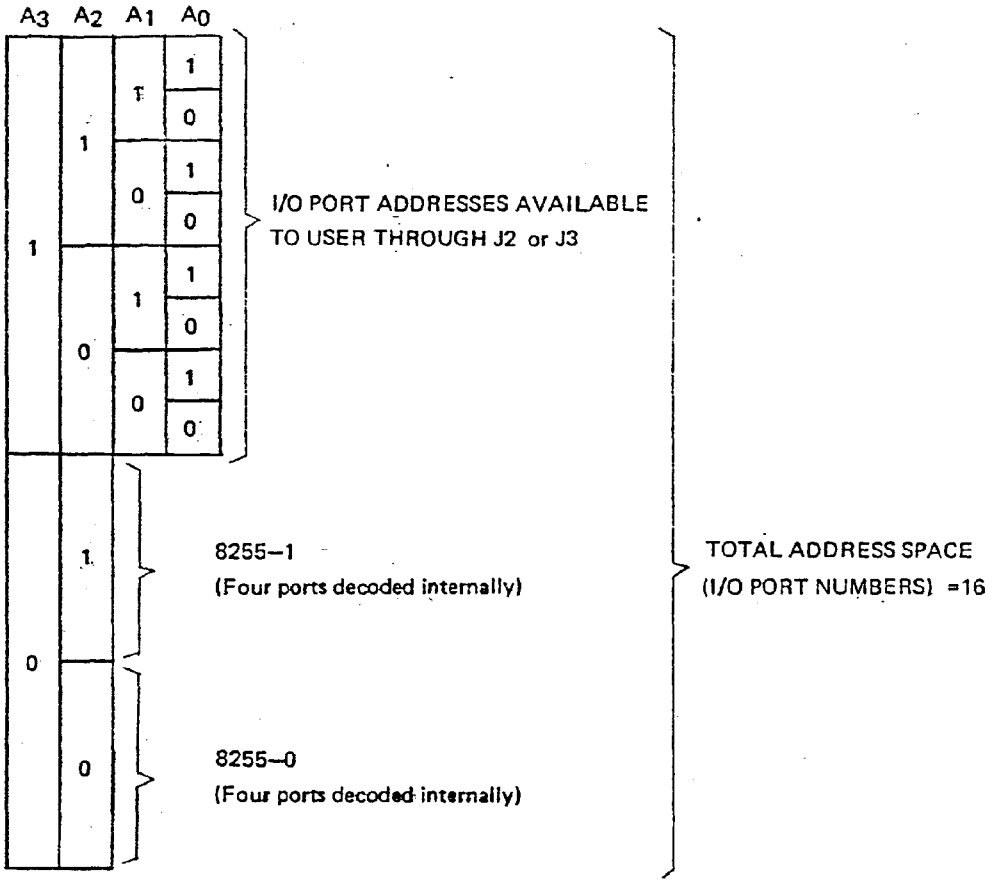


FIGURE TWO ADDRESS SPACE SUMMARY